



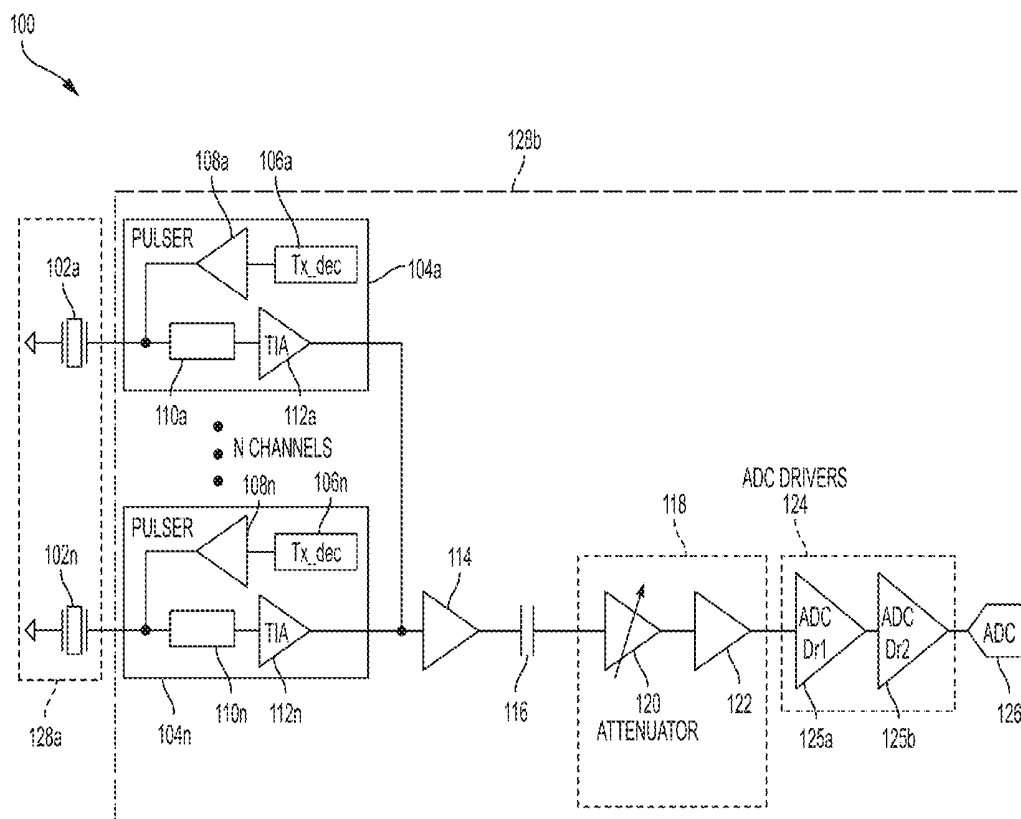
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Singh et al.(10) **Pub. No.: US 2018/0360426 A1**(43) **Pub. Date: Dec. 20, 2018**(54) **MULTI-STAGE TRANS-IMPEDANCE
AMPLIFIER (TIA) FOR AN ULTRASOUND
DEVICE****Publication Classification**

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(US)(21) Appl. No.: **16/011,715**(22) Filed: **Jun. 19, 2018****Related U.S. Application Data**(60) Provisional application No. 62/522,597, filed on Jun.
20, 2017.(57) **ABSTRACT**

An ultrasound circuit comprising a multi-stage trans-impedance amplifier (TIA) is described. The TIA is coupled to an ultrasonic transducer to amplify an electrical signal generated by the ultrasonic transducer in response to receiving an ultrasound signal. The TIA may include multiple stages, at least two of which operate with different supply voltages. The TIA may be followed by further processing circuitry configured to filter, amplify, and digitize the signal produced by the TIA.



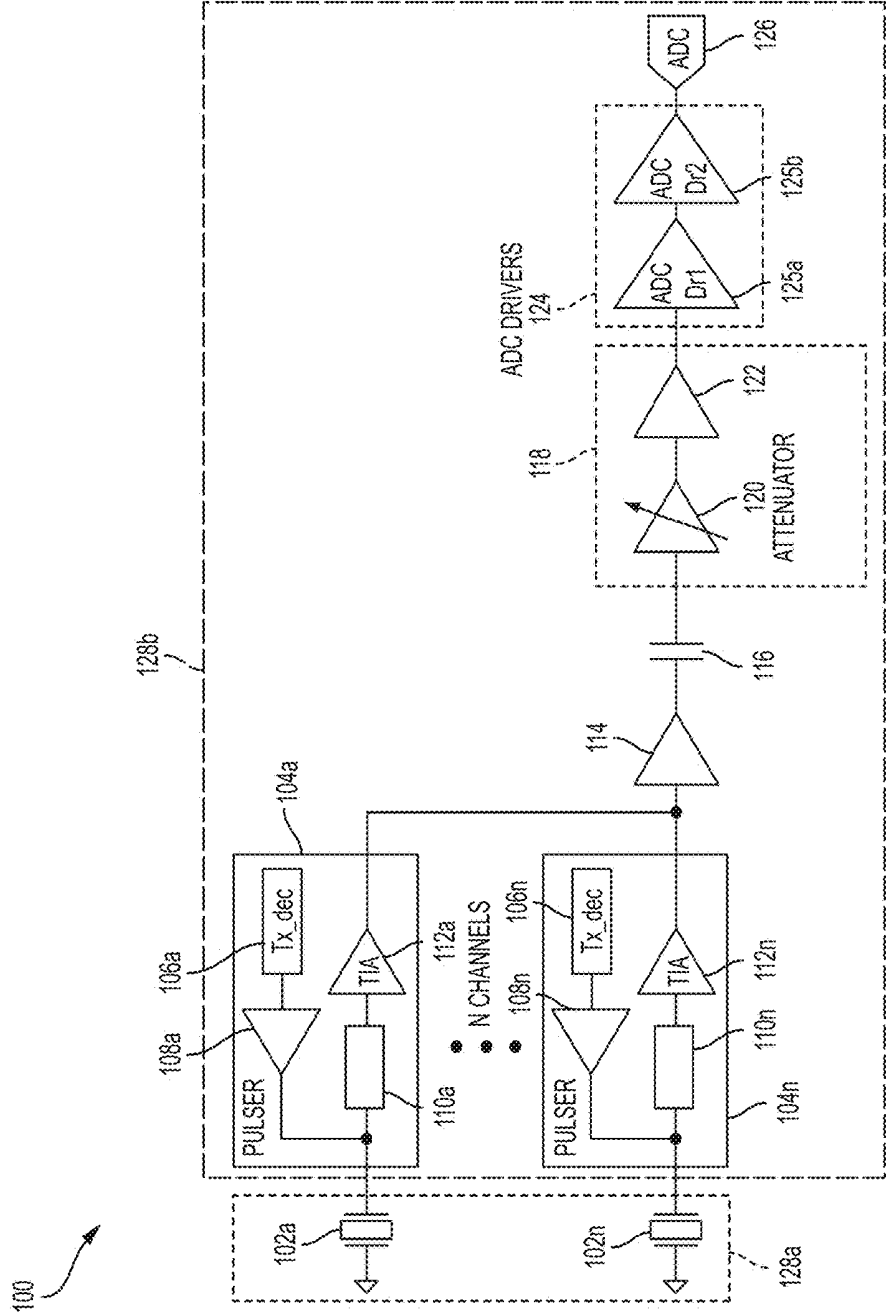


FIG. 1

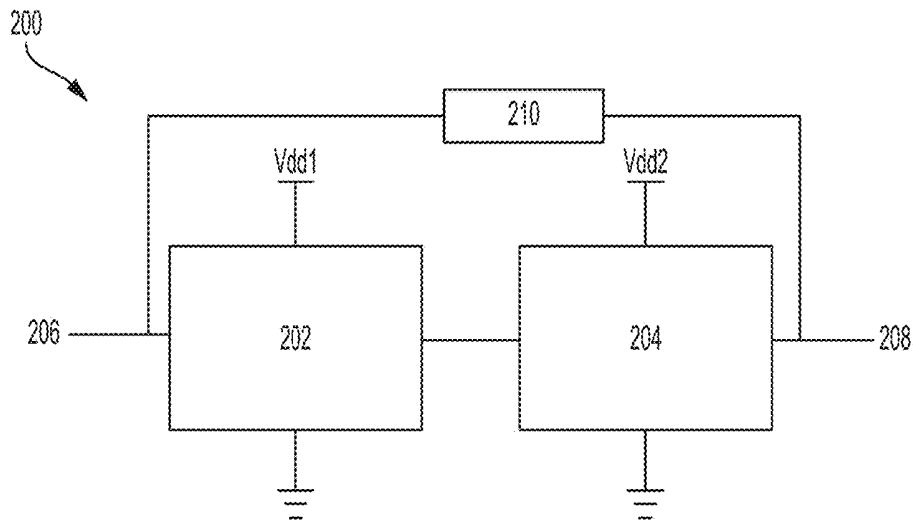


FIG. 2

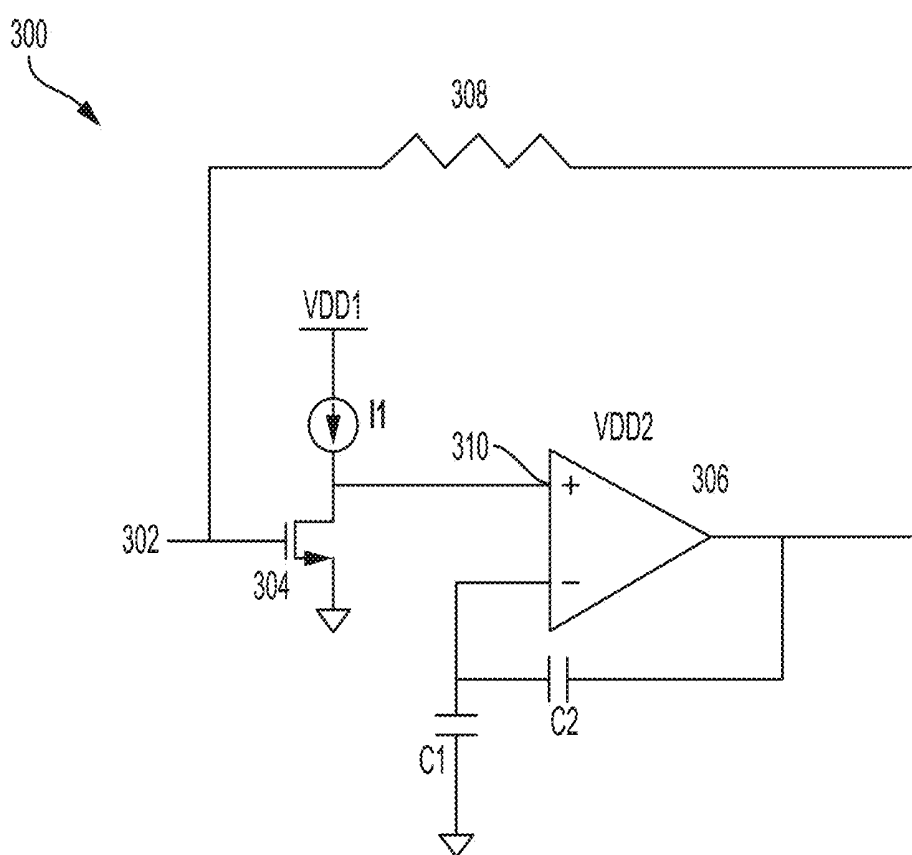


FIG. 3

MULTI-STAGE TRANS-IMPEDANCE AMPLIFIER (TIA) FOR AN ULTRASOUND DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This Application claims the benefit under 35 U.S.C. § 119(e) of U.S. Provisional Application Ser. No. 62/522,597, filed Jun. 20, 2017 under Attorney Docket No. B1348.70046US00, and entitled “MULTI-STAGE TRANS-IMPEDANCE AMPLIFIER (TIA) FOR AN ULTRASOUND DEVICE,” which is hereby incorporated herein by reference in its entirety.

BACKGROUND

Field

[0002] The present application relates to ultrasound devices having an amplifier for amplifying received ultrasound signals.

Related Art

[0003] Ultrasound probes often include one or more ultrasound sensors which sense ultrasound signals and produce corresponding electrical signals. The electrical signals are processed in the analog or digital domain. Sometimes, ultrasound images are generated from the processed electrical signals.

BRIEF SUMMARY

[0004] According to an aspect of the present application, an ultrasound apparatus is provided, comprising an ultrasound sensor and a multi-stage trans-impedance amplifier (TIA) coupled to the ultrasound sensor and configured to receive and amplify an output signal from the ultrasound sensor. The multi-stage TIA may include stages operating with different supply voltages, which may reduce power consumption in at least some situations.

[0005] According to an aspect of the present application, an ultrasound apparatus is provided, comprising an ultrasonic transducer and a multi-stage trans-impedance amplifier (TIA) having an input terminal coupled to the ultrasonic transducer. The multi-stage TIA is configured to receive and amplify an analog electrical signal from the ultrasonic transducer. The multi-stage TIA comprises a first stage configured to receive a first supply voltage and a second stage configured to receive a second supply voltage different than the first supply voltage.

[0006] According to an aspect of the present application, an ultrasound on a chip device is provided, comprising a substrate, a plurality of ultrasonic transducers integrated on the substrate, and analog processing circuitry integrated on the substrate and coupled to the plurality of ultrasonic transducers. The analog processing circuitry comprises a multi-stage trans-impedance amplifier coupled to an ultrasonic transducer of the plurality of ultrasonic transducers. The multi-stage TIA comprises multiple stages configured to receive different supply voltages.

[0007] According to an aspect of the present application, a method of operating an ultrasound circuit is provided, comprising receiving and amplifying, with a first stage of a multi-stage trans-impedance amplifier, an electrical signal output by an ultrasonic transducer, the first stage of the

multi-stage TIA operating at a first supply voltage value, and amplifying, with a second stage of the multi-stage TIA operating at a second supply voltage value different than the first supply voltage value, an output signal of the first stage.

BRIEF DESCRIPTION OF DRAWINGS

[0008] Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

[0009] FIG. 1 is a block diagram of an ultrasound device including an amplifier for amplifying an ultrasound signal, according to a non-limiting embodiment of the present application.

[0010] FIG. 2 illustrates a block diagram representation of the amplifier of FIG. 1, illustrating two stages with different supply voltages, according to a non-limiting embodiment of the present application.

[0011] FIG. 3 illustrates a non-limiting example implementation of the multi-stage amplifier of FIG. 2, according to a non-limiting embodiment of the present application.

DETAILED DESCRIPTION

[0012] Aspects of the present application relate to amplification circuitry for an ultrasound device. An ultrasound device may include one or more ultrasonic transducers configured to receive ultrasound signals and produce electrical output signals. Thus, the ultrasonic transducers may be operated as ultrasound sensors. The ultrasound device may include one or more amplifiers for amplifying the electrical output signals. In some embodiments, the amplifier(s) may be multi-stage amplifiers, with stages that operate at different supply voltage levels. In this manner, a lower supply voltage level may be used for at least one of the stages, thus facilitating lower power operation. In some embodiments, the first stage of the multi-stage amplifier may operate with a lower supply voltage than a following stage. The following stage may provide a desired output gain of the amplifier.

[0013] According to an aspect of the present application, a method of operating an ultrasound circuit is provided, comprising producing an electrical signal with an ultrasonic transducer and amplifying the electrical signal with a multi-stage TIA. The multi-stage TIA may include a first stage configured to operate at a lower supply voltage level than a following stage, and thus may provide power savings.

[0014] The aspects and embodiments described above, as well as additional aspects and embodiments, are described further below. These aspects and/or embodiments may be used individually, all together, or in any combination of two or more, as the application is not limited in this respect.

[0015] FIG. 1 illustrates a circuit for processing received ultrasound signals, according to a non-limiting embodiment of the present application. The circuit 100 includes N ultrasonic transducers 102a . . . 102n, wherein N is an integer. The ultrasonic transducers are sensors in some embodiments, producing electrical signals representing received ultrasound signals. The ultrasonic transducers may also transmit ultrasound signals in some embodiments. The ultrasonic transducers may be capacitive micromachined ultrasonic transducers (CMUTs) in some embodiments. The ultrasonic transducers may be piezoelectric micromachined

ultrasonic transducers (PMUTs) in some embodiments. Alternative types of ultrasonic transducers may be used in other embodiments.

[0016] The circuit 100 further comprises N circuitry channels 104a . . . 104n. The circuitry channels may correspond to a respective ultrasonic transducer 102a . . . 102n. For example, there may be eight ultrasonic transducers 102a . . . 102n and eight corresponding circuitry channels 104a . . . 104n. In some embodiments, the number of ultrasonic transducers 102a . . . 102n may be greater than the number of circuitry channels.

[0017] The circuitry channels 104a . . . 104n may include transmit circuitry, receive circuitry, or both. The transmit circuitry may include transmit decoders 106a . . . 106n coupled to respective pulsers 108a . . . 108n. The pulsers 108a . . . 108n may control the respective ultrasonic transducers 102a . . . 102n to emit ultrasound signals.

[0018] The receive circuitry of the circuitry channels 104a . . . 104n may receive the (analog) electrical signals output from respective ultrasonic transducers 102a . . . 102n. In the illustrated example, each circuitry channel 104a . . . 104n includes a respective receive circuit 110a . . . 110n and an amplifier 112a . . . 112n. The receive circuit 110a . . . 110n may be controlled to activate/deactivate readout of an electrical signal from a given ultrasonic transducer 102a . . . 102n. An example of suitable receive circuits 110a . . . 110n are switches. That is, in one embodiment the receive circuits are controllable switches which are switched during transmit mode to disconnect the ultrasonic transducers from the receive circuitry and during receive mode to connect the ultrasonic transducers to the receive circuitry. Alternatives to a switch may be employed to perform the same function.

[0019] The amplifiers 112a . . . 112n may be multi-stage TIAs in some embodiments, outputting amplified analog signals. As will be described further below, in some embodiments one or more—and in some embodiments all—of the amplifiers 112a-112n may include a first stage operating at a lower supply voltage level than a subsequent stage. The use of multi-stage TIAs with multiple supply voltages may facilitate low power operation of the circuit 100 compared to the use of alternative amplifier designs.

[0020] The circuit 100 further comprises an averaging circuit 114, which is also referred to herein as a summer or a summing amplifier. In some embodiments, the averaging circuit 114 is a buffer or an amplifier. The averaging circuit 114 may receive output signals from one or more of the amplifiers 112a . . . 112n and may provide an averaged output signal. The averaged output signal may be formed in part by adding or subtracting the signals from the various amplifiers 112a . . . 112n. The averaging circuit 114 may include a variable feedback resistance. The value of the variable feedback resistance may be adjusted dynamically based upon the number of amplifiers 112a . . . 112n from which the averaging circuit receives signals. In some embodiments, the variable resistance may include N resistance settings. That is, the variable resistance may have a number of resistance settings corresponding to the number of circuitry channels 104a . . . 104n. Thus, the average output signal may also be formed in part by application of the selected resistance to the combined signal received at the input(s) of the averaging circuit 114.

[0021] The averaging circuit 114 is coupled to an auto-zero block 116, also referred to herein as a “DC block.” The auto-zero block 116 may filter the averaged signal provided

by the averaging circuit 114, and thus may be considered a filter in at least some embodiments.

[0022] The auto-zero block 116 is coupled to a programmable gain amplifier 118 which includes an attenuator 120 and a fixed gain amplifier 122. The programmable gain amplifier 118 may perform time gain compensation (TGC), and thus may alternatively be referred to as a TGC stage or circuit. In performing TGC, the programmable gain amplifier 118 may increase the amplification provided during reception of an ultrasound signal by an ultrasonic transducer, thus compensating for the natural attenuation of the signal which occurs over time.

[0023] The programmable gain amplifier 118 is coupled to an ADC 126 via ADC drivers 124. In the illustrated example, the ADC drivers 124 include a first ADC driver 125a and a second ADC driver 125b. The ADC 126 digitizes the signal (s) from the averaging circuit 114.

[0024] While FIG. 1 illustrates a number of components as part of a circuit of an ultrasound device, it should be appreciated that the various aspects described herein are not limited to the exact components or configuration of components illustrated. For example, aspects of the present application relate to the amplifiers 112a . . . 112n, and the components illustrated downstream of those amplifiers in circuit 100 are optional in some embodiments.

[0025] The components of FIG. 1 may be located on a single substrate or on different substrates. For example, as illustrated, the ultrasonic transducers 102a . . . 102n may be on a first substrate 128a and the remaining illustrated components may be on a second substrate 128b. The first and/or second substrates may be semiconductor substrates, such as silicon substrates. In an alternative embodiment, the components of FIG. 1 may be on a single substrate. For example, the ultrasonic transducers 102a . . . 102n and the illustrated circuitry may be monolithically integrated on the same die (e.g., a semiconductor die, such as silicon). Such integration may be facilitated by using CMUTs as the ultrasonic transducers.

[0026] According to an embodiment, the components of FIG. 1 form part of an ultrasound probe. The ultrasound probe may be handheld. In some embodiments, the components of FIG. 1 form part of an ultrasound patch configured to be worn by a patient, or part of an ultrasound pill to be swallowed by a patient.

[0027] As previously described, aspects of the present application provide a multi-stage TIA for an ultrasound device, in which at least two stages of the multi-stage TIA operate with different supply voltages. The inventors have appreciated that the stages of a multi-stage TIA may impact noise performance, linearity, and gain differently. For example, the first stage, electrically closest to the ultrasonic transducer, may dominate noise performance of the TIA, while following (or “subsequent” or “downstream”) stages of the TIA may have a greater impact on linearity. Moreover, the reduction of noise achievable with the first stage may depend, at least in part, on the amount of current used in the first stage, with greater current resulting in greater noise reduction. However, since greater current consumption also corresponds with greater power consumption, the inventors have recognized that operating the first stage of a multi-stage TIA at a lower supply voltage may be desirable to reduce the power consumption of that stage. Meanwhile, later stages of the TIA with a greater impact on the linearity of the TIA may be operated at a higher supply voltage level. By using

distinct supply voltage levels for the multi-stage TIA, power consumption may be reduced compared to a scenario in which all stages of the multi-stage TIA operate with the same supply voltage level. The closed loop gain may be primarily controlled by the feedback resistance, so long as the open-loop gain bandwidth (the unity gain bandwidth) of the TIA is sufficient.

[0028] FIG. 2 illustrates a non-limiting example of a multi-stage TIA having stages which operate at different supply voltage levels, according to a non-limiting embodiment of the present application. The illustrated TIA may represent one non-limiting implementation of the TIAs 112a . . . 112n of FIG. 1.

[0029] As shown, the multi-stage TIA 200 in this non-limiting example includes a first stage 202 and a second stage 204. The first stage 202 may have an input terminal 206 configured to receive an output signal of an ultrasonic transducer. For example, the input terminal 206 may be coupled directly to an ultrasonic transducer or coupled through one or more additional components, such as a receive switch.

[0030] The output of the first stage 202 may couple to the input of the second stage 204, and an output signal of the TIA 200 may be provided at the output terminal 208 of the second stage 204.

[0031] The multi-stage TIA 200 of FIG. 2 may further comprise a feedback impedance 210. The feedback impedance may be formed by a resistor, capacitor, or combination of impedance elements in some embodiments. The feedback impedance may have any suitable value to provide a target gain of the TIA.

[0032] As shown, the first stage 202 and second stage 204 may have respective supply voltages, Vdd1 and Vdd2. The supply voltages Vdd1 and Vdd2 may differ, with Vdd2 greater than Vdd1 in at least some embodiments. As described above, the first stage of the TIA, that is stage 202, may have a greater impact on noise performance of the TIA than the second stage 204, while the second stage 204 may have a greater impact on the linearity of the TIA. Thus, operating the first stage 202 at a lower supply voltage Vdd1 may not negatively impact the linearity of the TIA, but may allow for the first stage 202, and thus the TIA 200, to consume less power for a given level of noise performance.

[0033] As should be appreciated from FIG. 2, aspects of the present application provide a multi-stage TIA for an ultrasound device, in which an upstream stage of the multi-stage TIA operates with a lower supply voltage than a downstream stage of the multi-stage TIA. Aspects of the present application provide a multi-stage TIA for an ultrasound device, in which the first stage of the multi-stage TIA operates with a lower supply voltage than a subsequent stage (e.g., a last stage) of the multi-stage TIA.

[0034] FIG. 3 illustrates a non-limiting example of an implementation of the multi-stage TIA 200 of FIG. 2. The multi-stage TIA 300 of FIG. 3 comprises an input terminal 302, a first stage comprising a current source I1 and a transistor 304, a second stage comprising an amplifier 306 (e.g., an operational amplifier) and capacitors C1 and C2, and a feedback resistor 308.

[0035] As shown, the first stage of the multi-stage TIA 300 may receive a first supply voltage Vdd1, while the second stage may receive a second supply voltage Vdd2. In at least some embodiments, Vdd1 may be less than Vdd2, and in some embodiments is significantly less than Vdd2. For

example, Vdd1 may be less than three-quarters of the value of Vdd2, less than half of Vdd2, less than one-quarter of Vdd2, between 25% and 90% of Vdd2, or any other suitable value.

[0036] The second stage of the multi-stage TIA 300 may be the dominant factor in controlling the linearity of the TIA. In at least some embodiments, it may be desirable for the TIA to provide a high degree of linearity. The voltage Vdd2 may be selected at least in part to provide a desired degree of linearity.

[0037] Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the technology described in the application. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described.

[0038] As described, some aspects may be embodied as one or more methods. The acts performed as part of the method(s) may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0039] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0040] The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, i.e., elements that are conjunctively present in some cases and disjunctively present in other cases.

[0041] As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements.

[0042] As used herein, the term “between” used in a numerical context is to be inclusive unless indicated otherwise. For example, “between A and B” includes A and B unless indicated otherwise.

[0043] In the claims, as well as in the specification above, all transitional phrases such as “comprising,” “including,” “carrying,” “having,” “containing,” “involving,” “holding,” “composed of,” and the like are to be understood to be open-ended, i.e., to mean including but not limited to. Only the transitional phrases “consisting of” and “consisting essentially of” shall be closed or semi-closed transitional phrases, respectively.

What is claimed is:

1. An ultrasound apparatus, comprising:
an ultrasonic transducer; and
a multi-stage trans-impedance amplifier (TIA) having an input terminal coupled to the ultrasonic transducer and configured to receive and amplify an analog electrical

- signal from the ultrasonic transducer, the multi-stage TIA comprising a first stage configured to receive a first supply voltage and a second stage configured to receive a second supply voltage different than the first supply voltage.
2. The ultrasound apparatus of claim 1, wherein the second supply voltage is greater than the first supply voltage.
3. The ultrasound apparatus of claim 1, wherein the ultrasonic transducer and the multi-stage TIA are integrated on a same substrate.
4. The ultrasound apparatus of claim 1, further comprising a switch coupling the multi-stage TIA with the ultrasonic transducer.
5. The ultrasound apparatus of claim 1, further comprising a feedback impedance coupling the second stage with the first stage.
6. An ultrasound on a chip device, comprising:
a substrate;
a plurality of ultrasonic transducers integrated on the substrate; and
analog processing circuitry integrated on the substrate and coupled to the plurality of ultrasonic transducers, the analog processing circuitry comprising a multi-stage trans-impedance amplifier coupled to an ultrasonic transducer of the plurality of ultrasonic transducers, the multi-stage TIA comprising multiple stages configured to receive different supply voltages.
7. The ultrasound on a chip device of claim 6, wherein the multiple stages of the multi-stage TIA include an upstream stage and a downstream stage, the upstream stage being configured to operate at a lower supply voltage than the downstream stage.

8. The ultrasound on a chip device of claim 6, wherein the multiple stages of the multi-stage TIA include a first stage and a last stage, the last stage coupled to a larger supply voltage than the first stage.

9. The ultrasound on a chip device of claim 6, further comprising filtering and time gain compensation circuitry coupled to the multi-stage TIA.

10. The ultrasound on a chip device of claim 6, further comprising an averaging circuit having an input coupled to outputs of multiple TIAs of the ultrasound on a chip device.

11. A method of operating an ultrasound circuit, comprising:

receiving and amplifying, with a first stage of a multi-stage trans-impedance amplifier, an electrical signal output by a an ultrasonic transducer, the first stage of the multi-stage TIA operating at a first supply voltage value; and

amplifying, with a second stage of the multi-stage TIA operating at a second supply voltage value different than the first supply voltage value, an output signal of the first stage.

12. The method of claim 11, wherein the second supply voltage is greater than the first supply voltage.

13. The method of claim 12, wherein the first supply voltage is less than half the second supply voltage.

14. The method of claim 11, further comprising providing a feedback signal from the second stage to the first stage.

15. The method of claim 11, further filtering and time gain compensating an output signal of the multi-stage TIA.

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专利名称(译)	用于超声设备的多级跨阻放大器 (TIA)		
公开(公告)号	US20180360426A1	公开(公告)日	2018-12-20
申请号	US16/011715	申请日	2018-06-19
[标]申请(专利权)人(译)	爱玛·辛格 RALSTON TYLER小号		
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IPC分类号	A61B8/08 H03F3/50 A61B8/00		
CPC分类号	A61B8/5207 H03F3/50 A61B8/4483 A61B8/54 A61B8/56 H03F3/45475 H03F2200/411 H03F2200/516 H03F2203/45512		
优先权	62/522597 2017-06-20 US		
外部链接	Espacenet USPTO		

摘要(译)

描述了包括多级跨阻放大器 (TIA) 的超声电路。TIA耦合到超声换能器，以响应于接收超声信号而放大由超声换能器产生的电信号。TIA可以包括多个级，其中至少两个级以不同的电源电压工作。TIA之后可以是进一步的处理电路，其被配置为对由TIA产生的信号进行滤波，放大和数字化。

