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(54) **ULTRASONIC MEASUREMENT APPARATUS, ULTRASONIC HEAD UNIT, ULTRASONIC PROBE, AND ULTRASONIC IMAGING APPARATUS**

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*A61B 8/13* (2013.01)  
USPC ..... **367/7; 367/138**

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(57) **ABSTRACT**

An ultrasonic measuring apparatus includes an ultrasonic transducer device having a substrate and an ultrasonic transducer element array that has a first channel group and a second channel group that are arranged on the substrate, a first integrated circuit apparatus that is mounted on the substrate, at one edge portion of the ultrasonic transducer element array in a first direction, such that a long-side direction coincides with a second direction that intersects the first direction, and performs at least one of signal transmission to the first channel group and signal reception from the first channel group, and a second integrated circuit apparatus that is mounted on the substrate, at the other edge portion of the ultrasonic transducer element array in the first direction, such that the long-side direction coincides with the second direction, and performs at least one of signal transmission to the second channel group and signal reception from the second channel group. In the ultrasonic transducer element array, the first group of channels and the second group of channels are arranged alternately every channel in the second direction.

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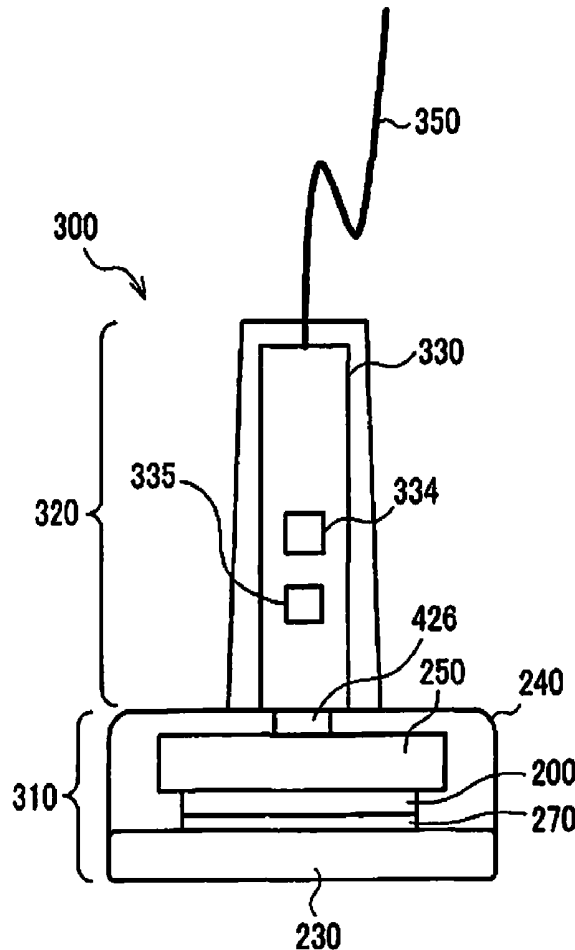
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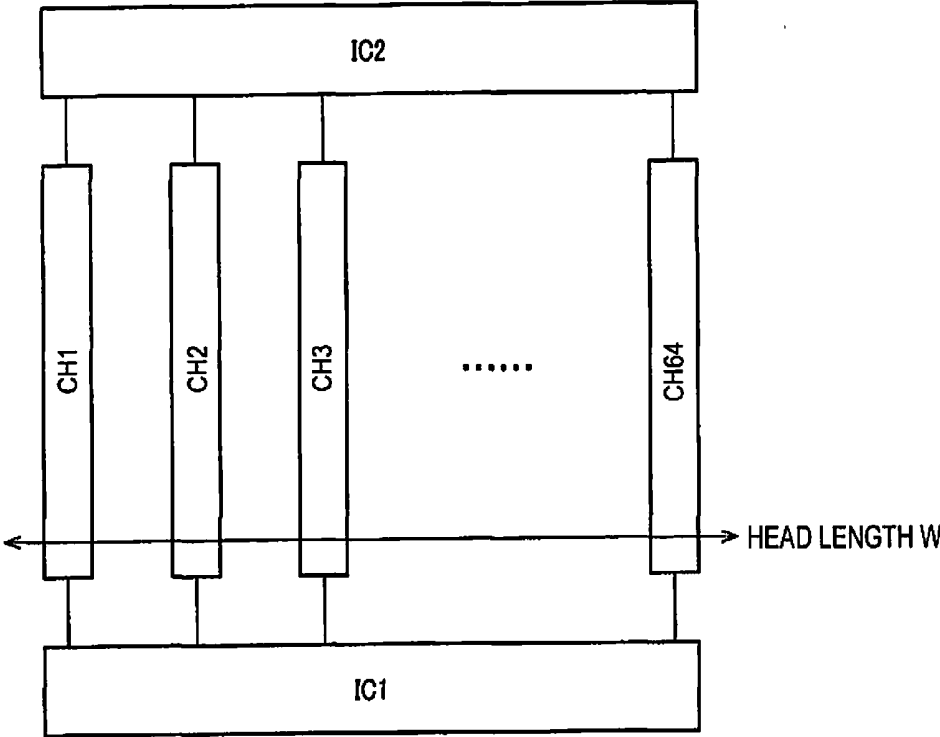


FIG. 1A

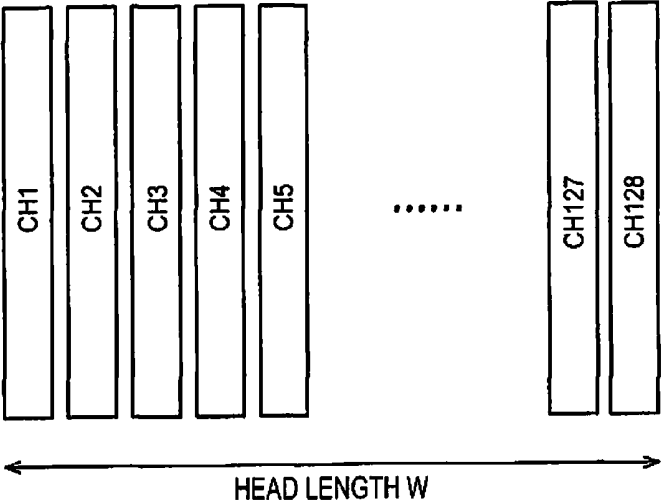


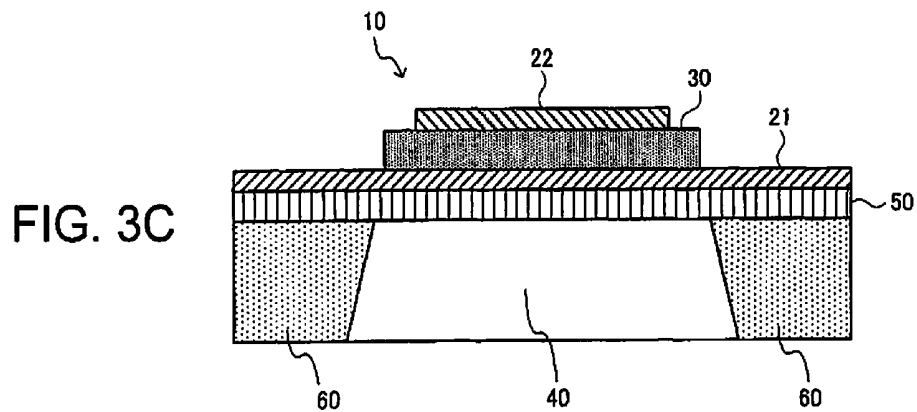
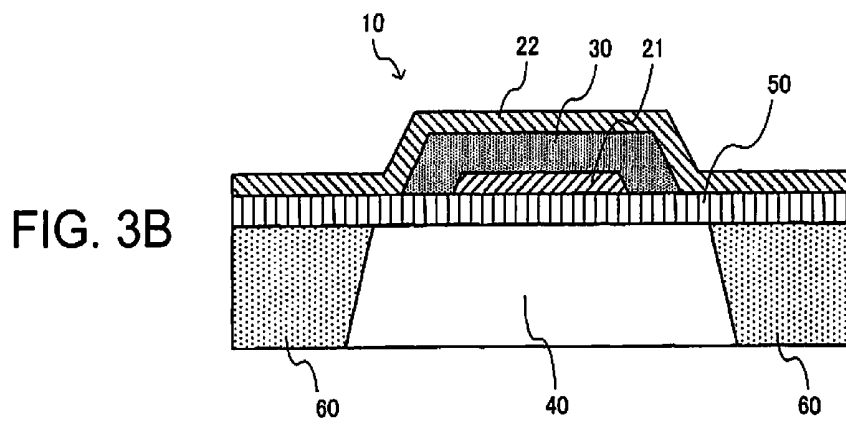
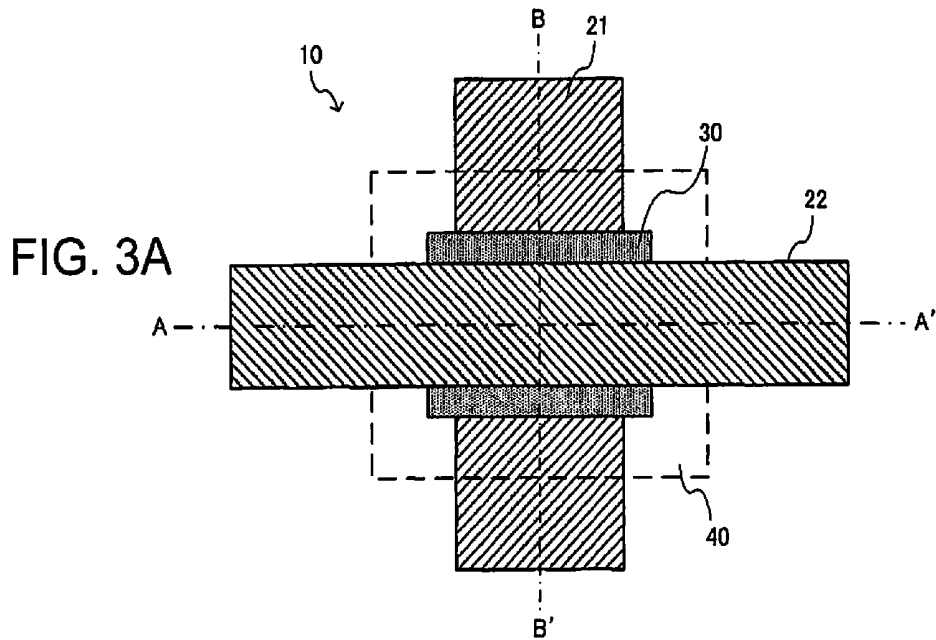
FIG. 1B

	LYPHHEDEMA	DECUBITUS	SKIN	MUSCLE / TENDON
MAIN APPLICATION	EDEMA PROGNOSIS, etc.	CONTROL	COLLAGEN FIBERS	TREATMENT EVALUATION
DEPTH	~80mm	~50mm	~30mm	~80mm
HEAD LENGTH	40mm	40mm	40mm	40mm
FREQUENCY	5MHz	7MHz	20MHz	5MHz~

FIG. 2A

FREQUENCY	3. 5MHz	7. 5MHz	7. 5MHz
HEAD LENGTH	38~40mm	25~26mm	38~40mm
NO. OF CHANNELS	64	64	128
NO. OF TRANSMISSION / RECEPTION CHs	8	8	16
HORIZONTAL RESOLUTION	3mm	2mm	0. 5mm

FIG. 2B



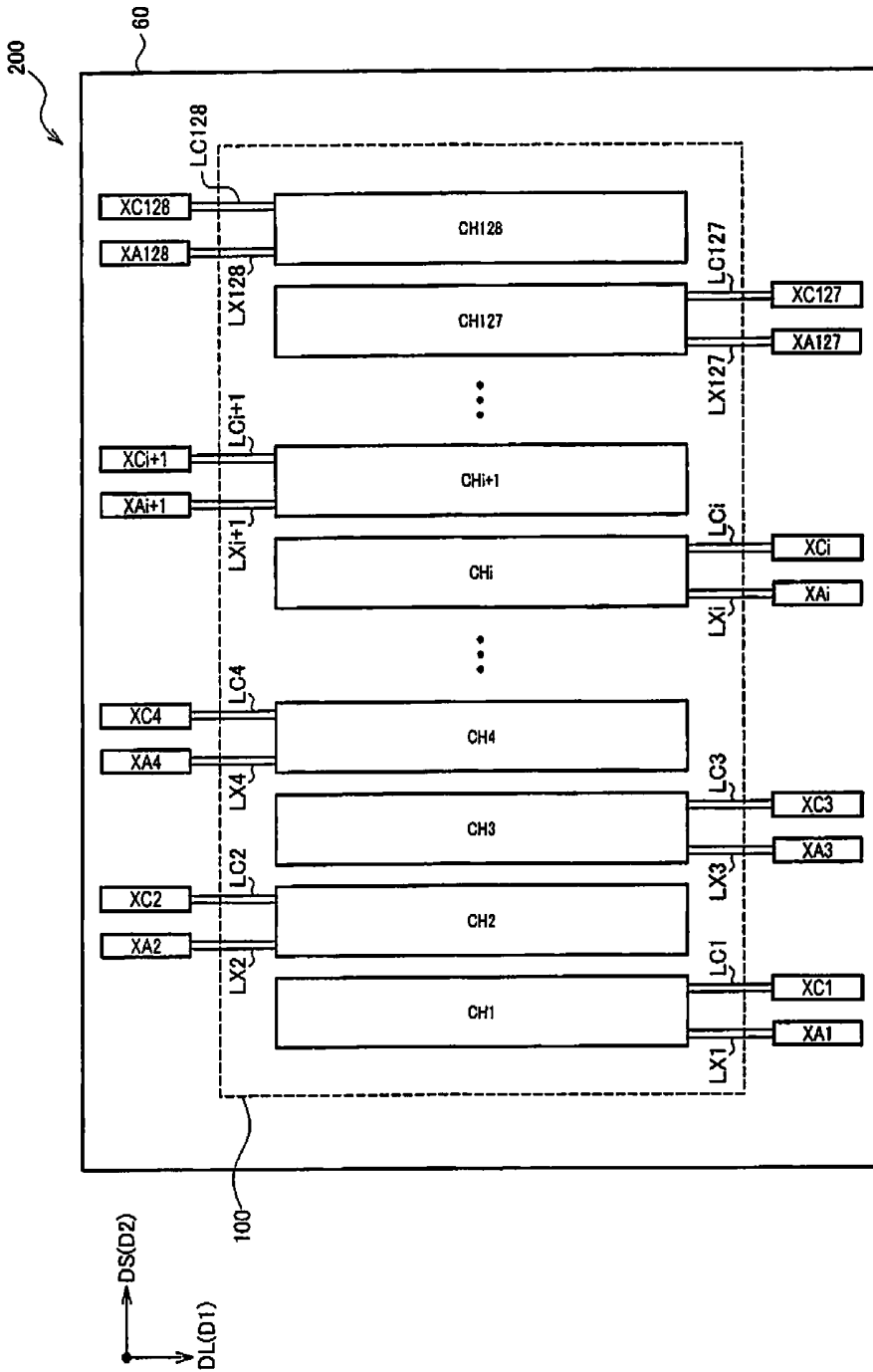


FIG. 4

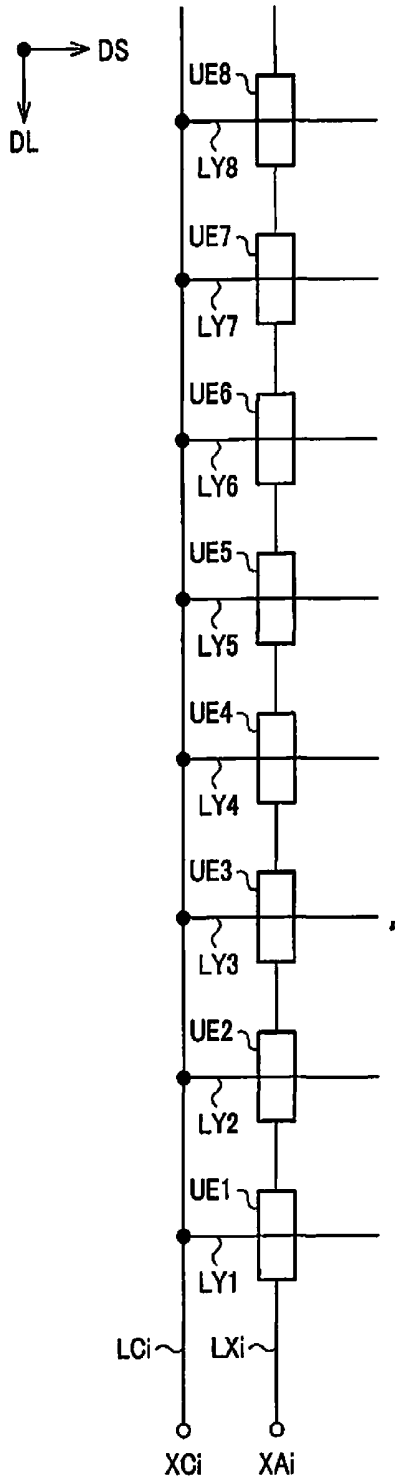


FIG. 5A

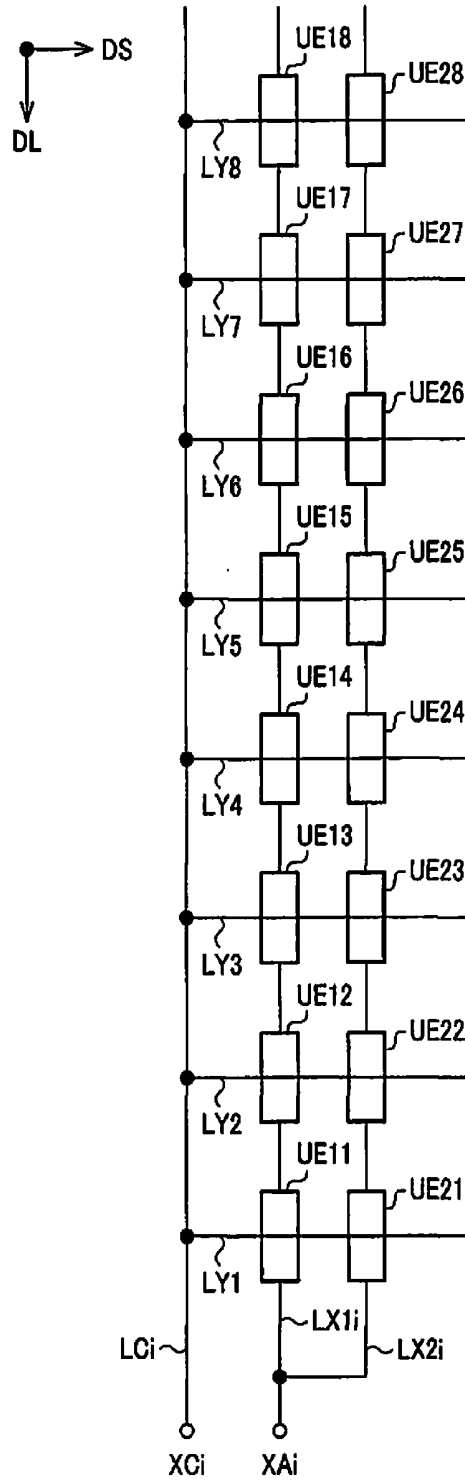


FIG. 5B

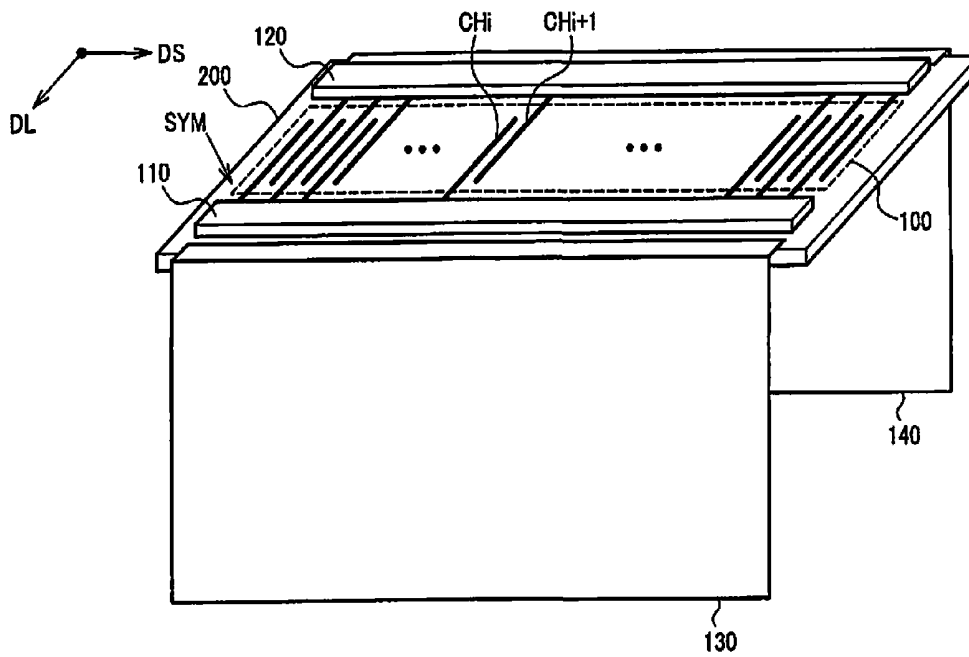


FIG. 6

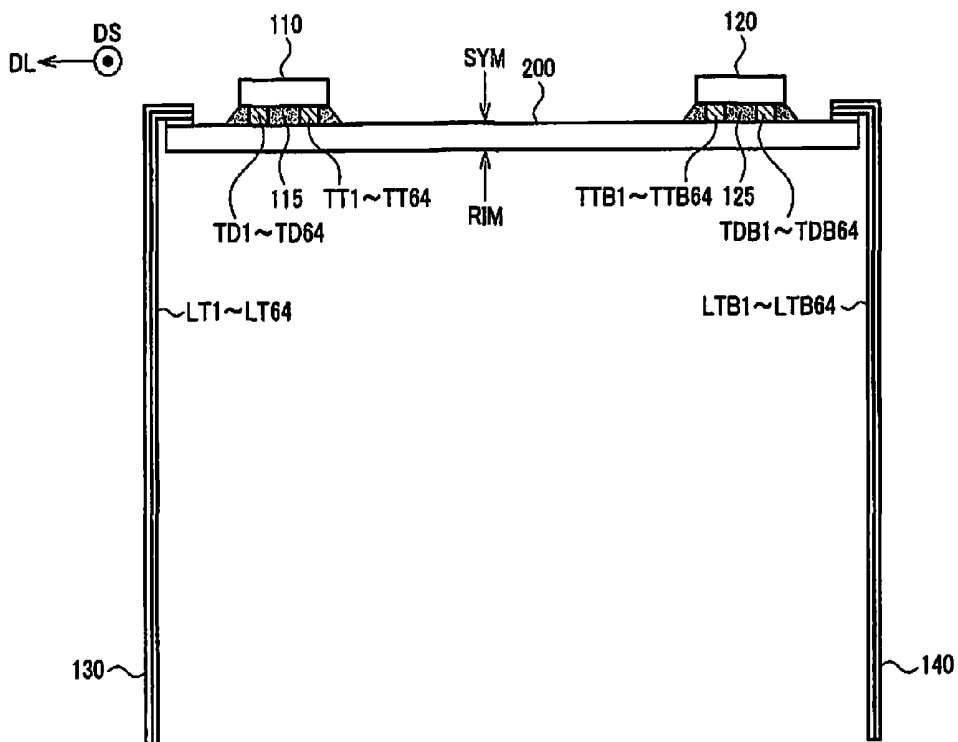


FIG. 7

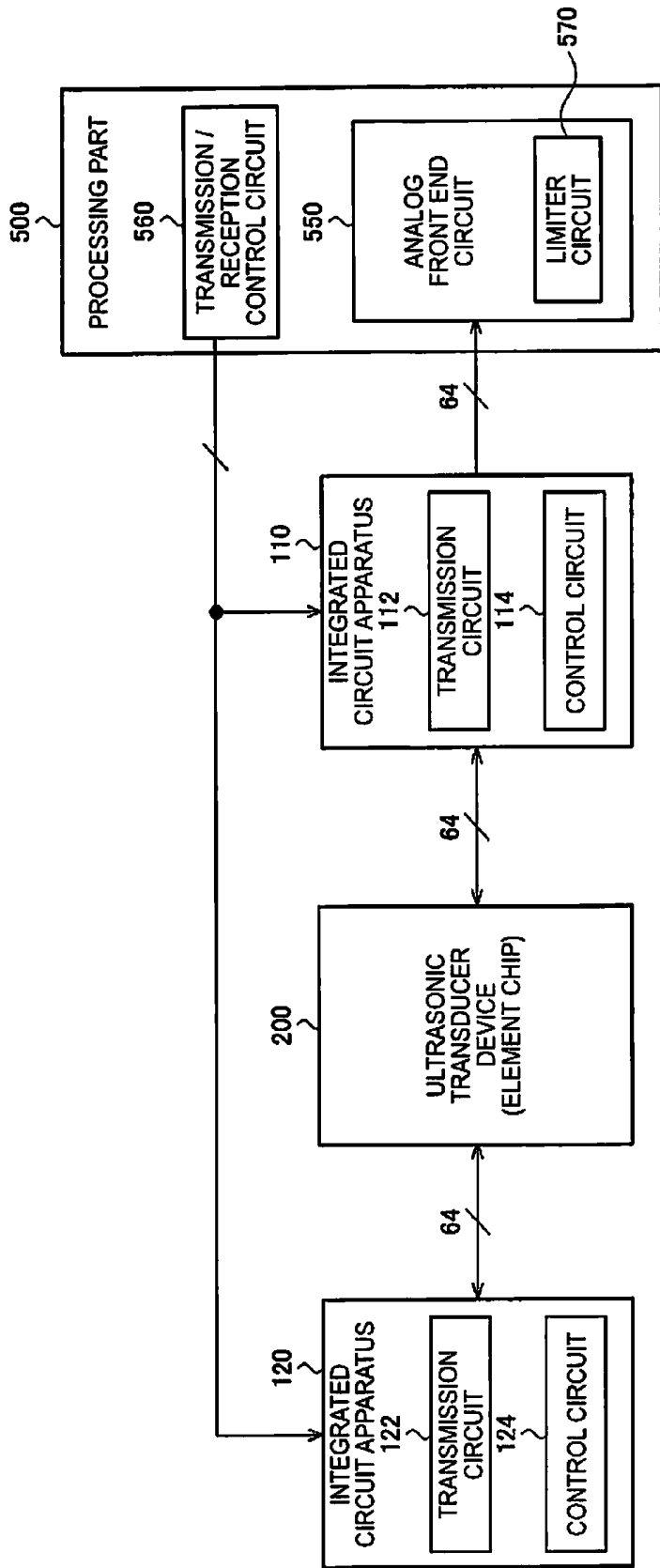


FIG. 8

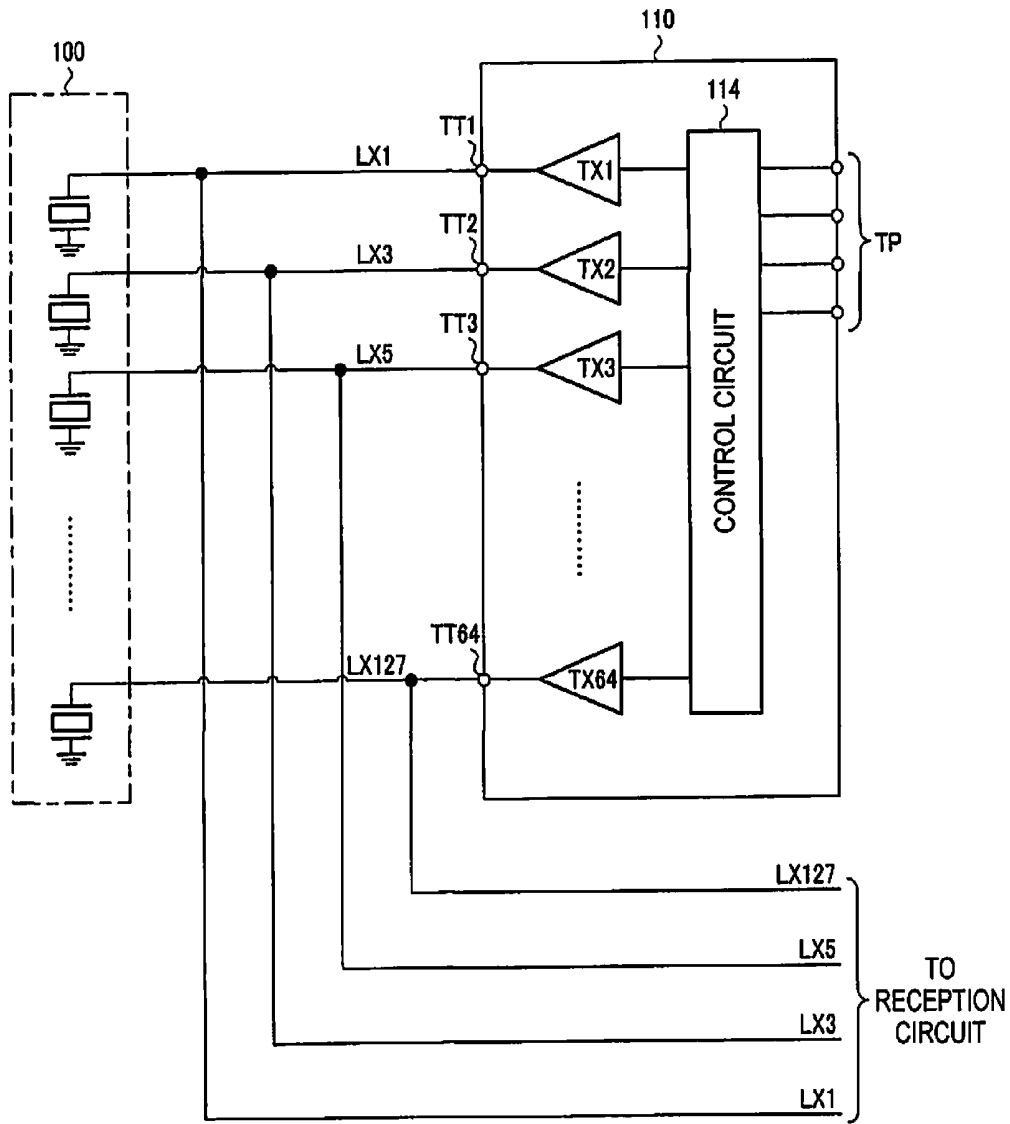


FIG. 9



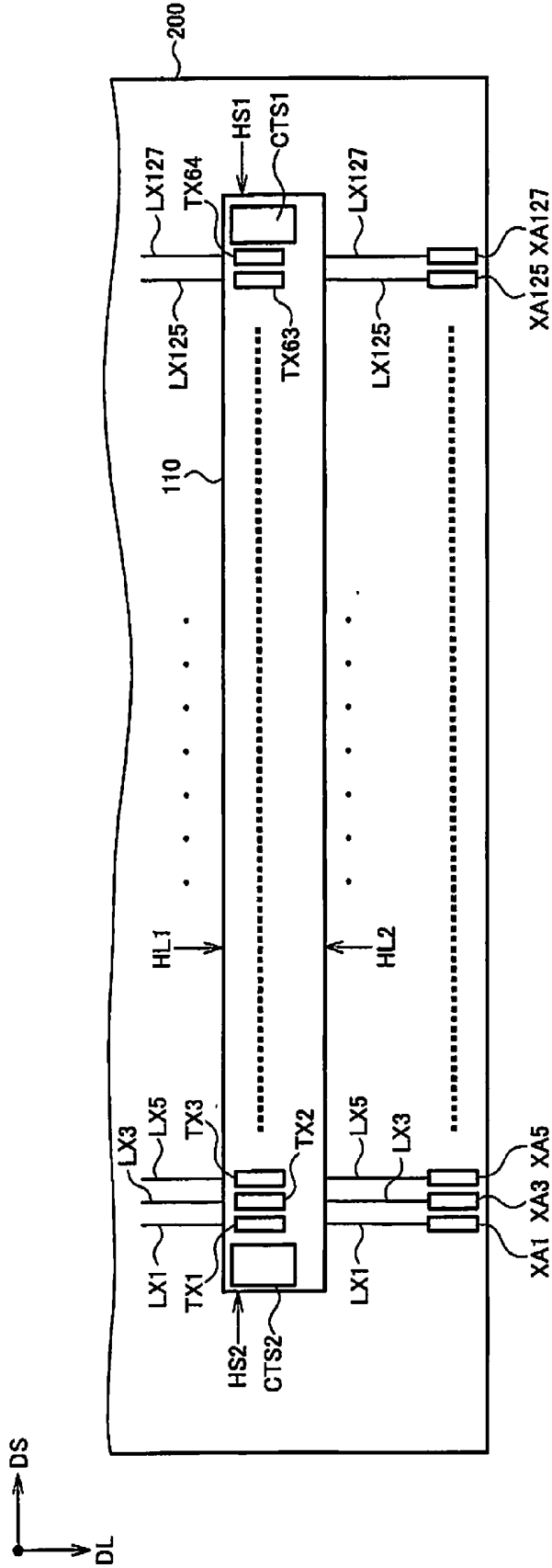


FIG.11

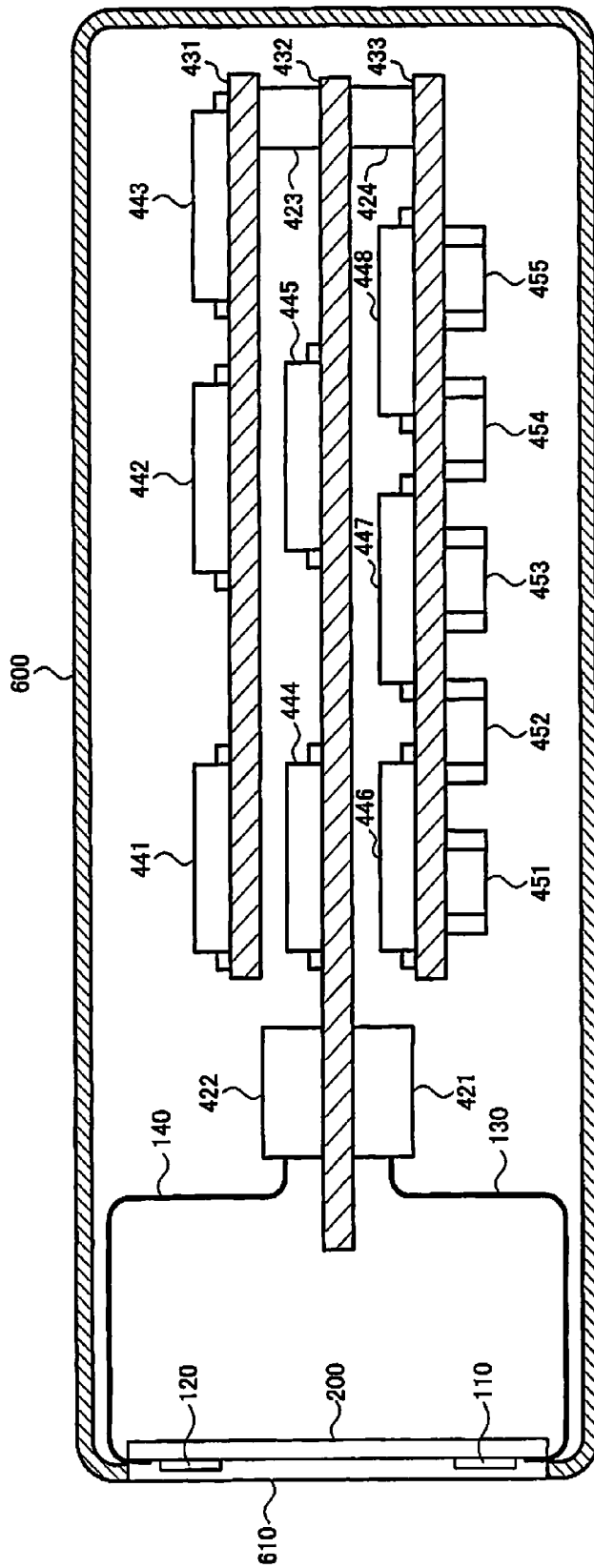


FIG.12

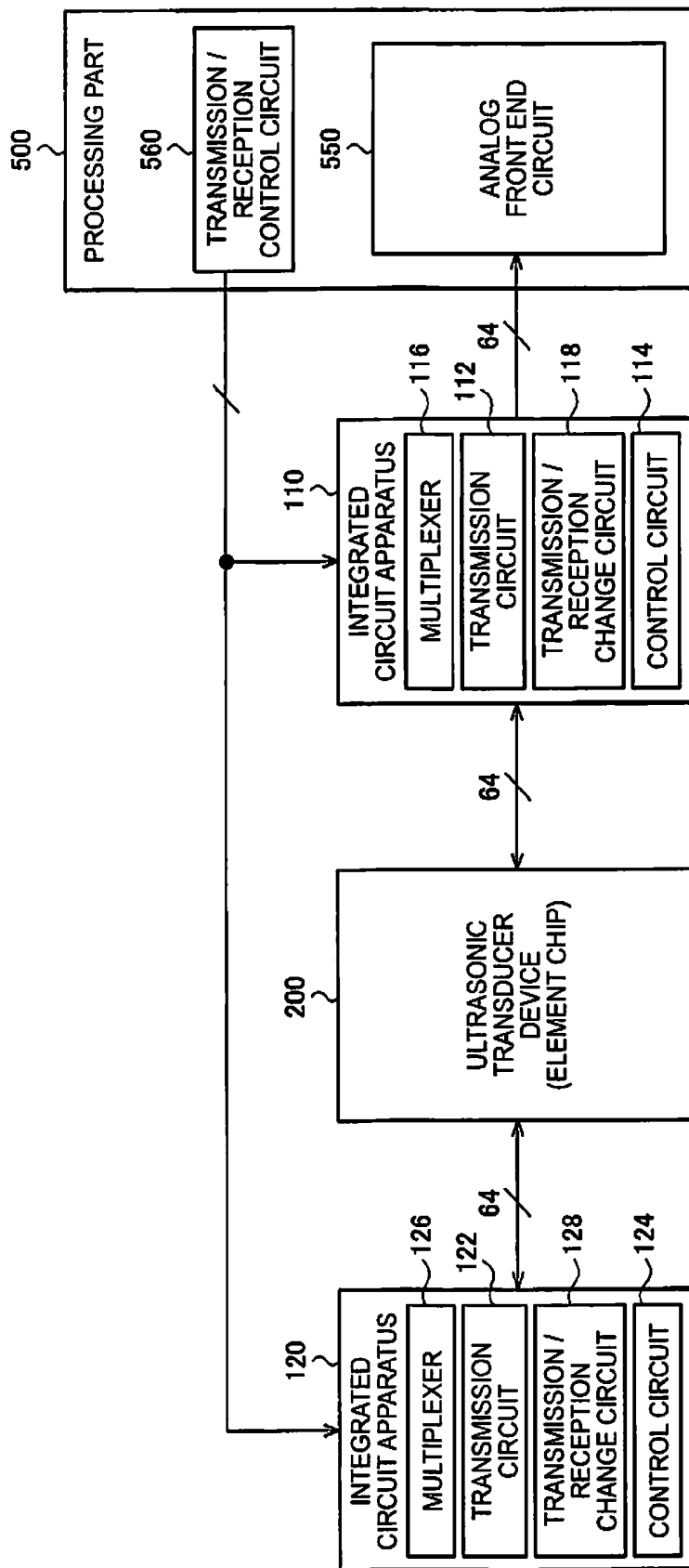


FIG. 13

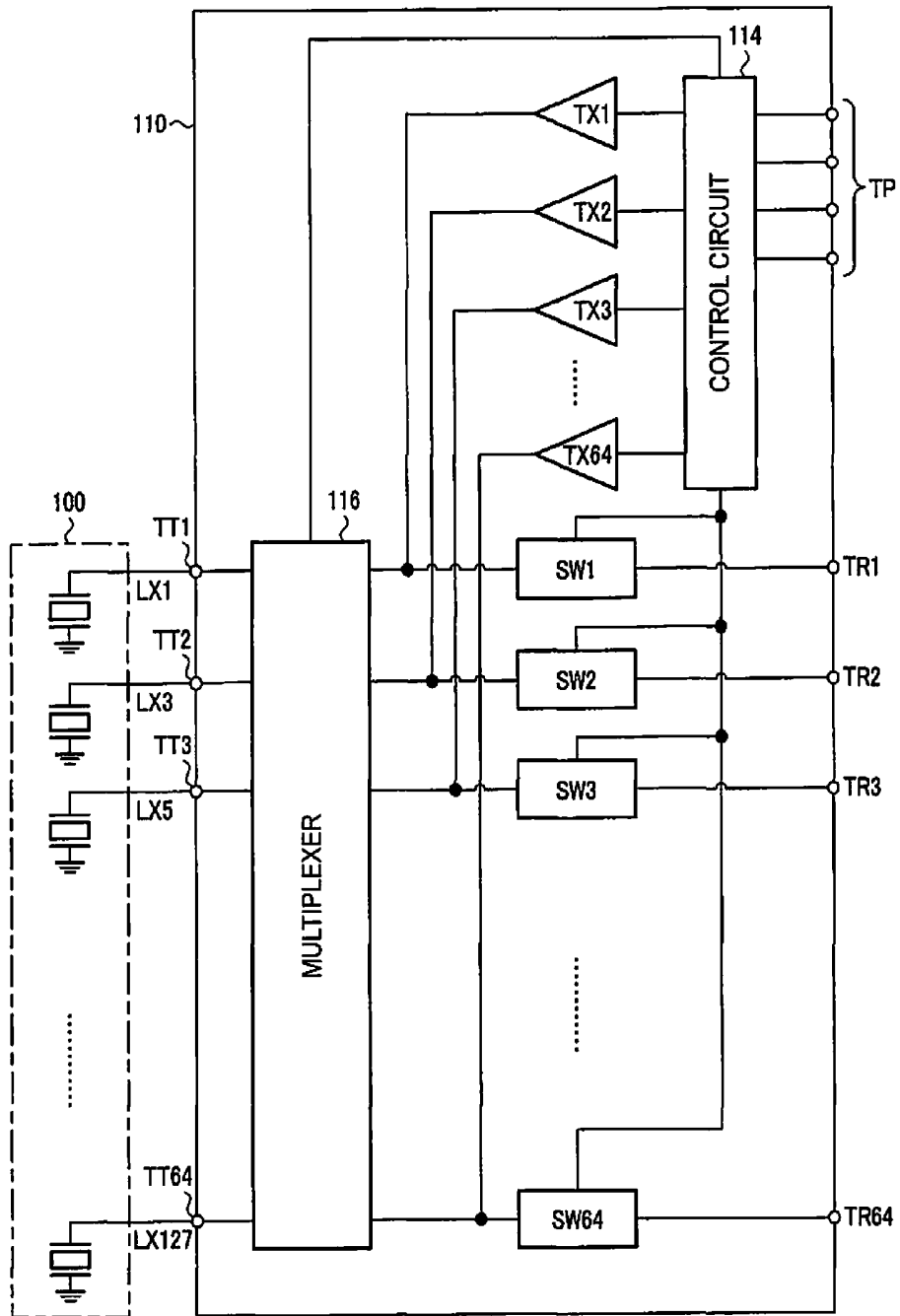


FIG. 14



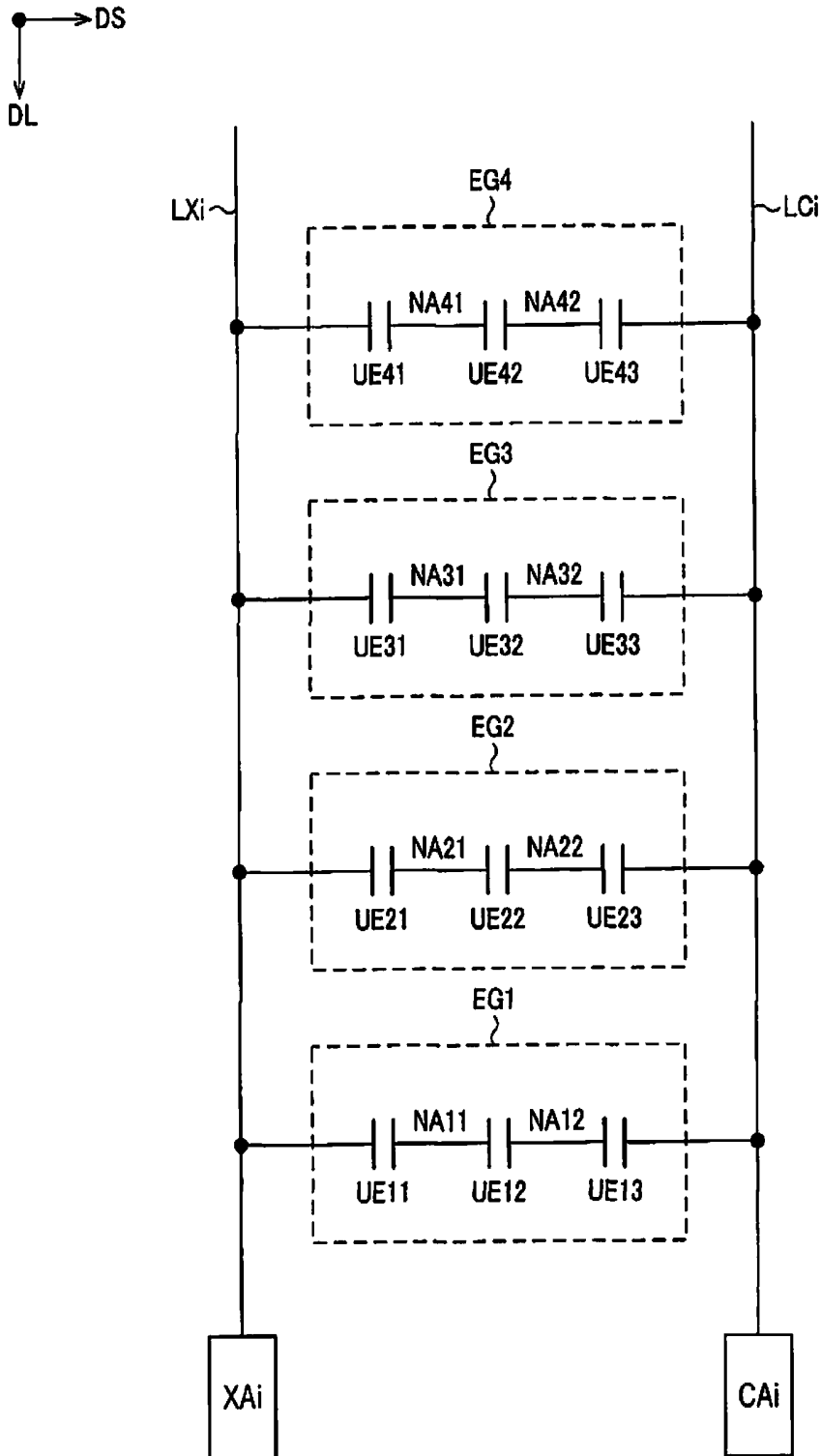


FIG.16

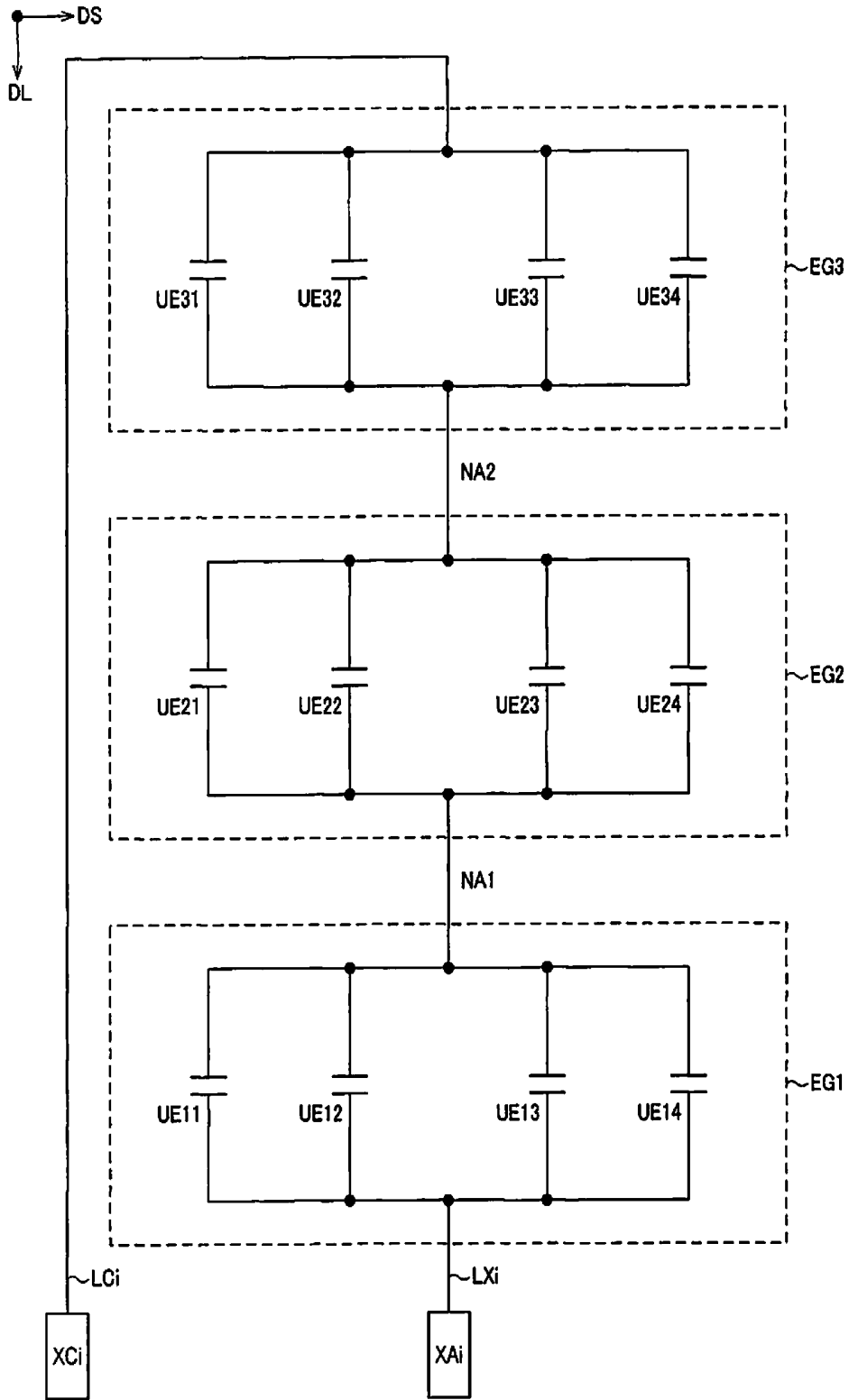


FIG.17

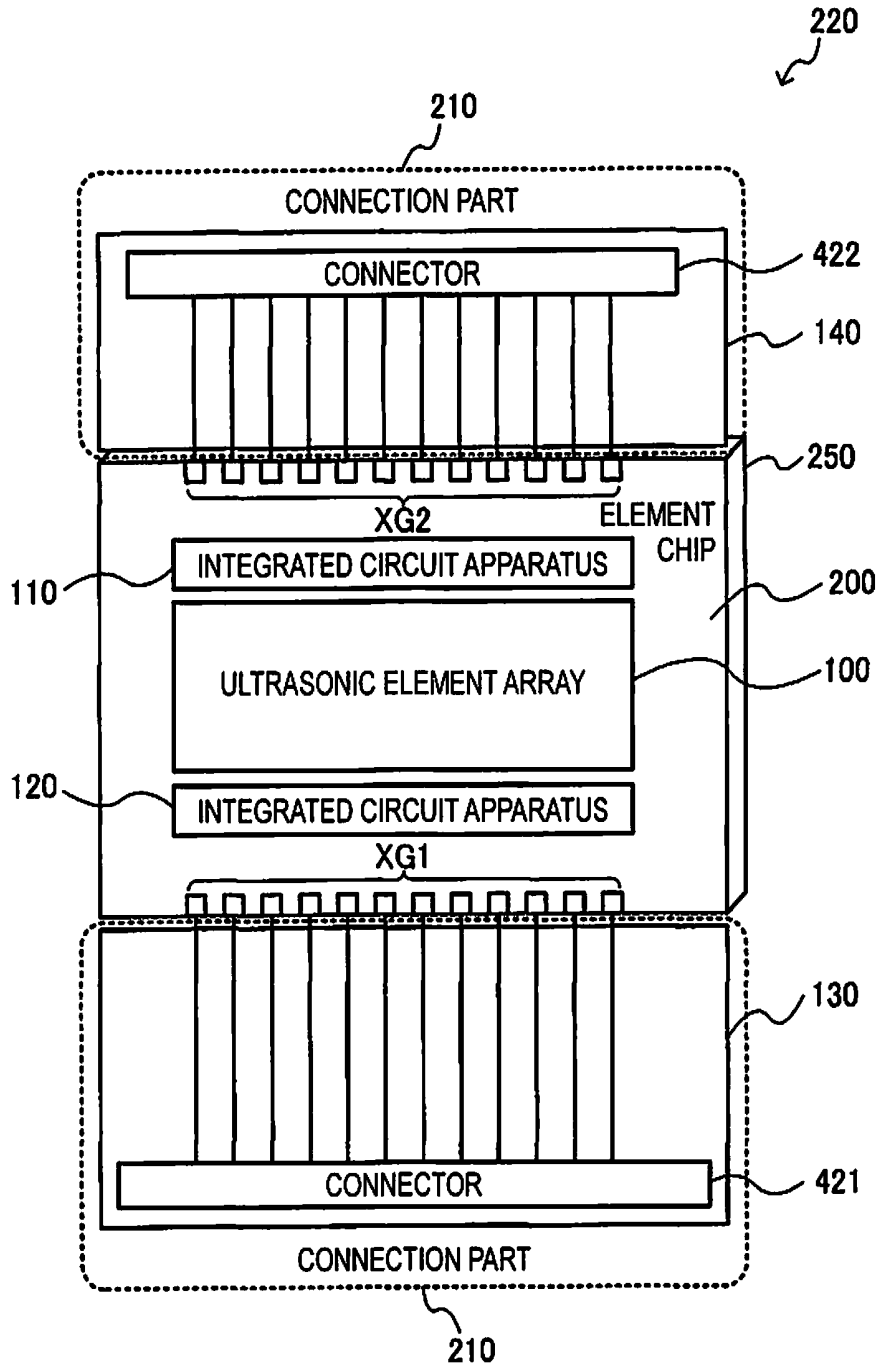


FIG.18

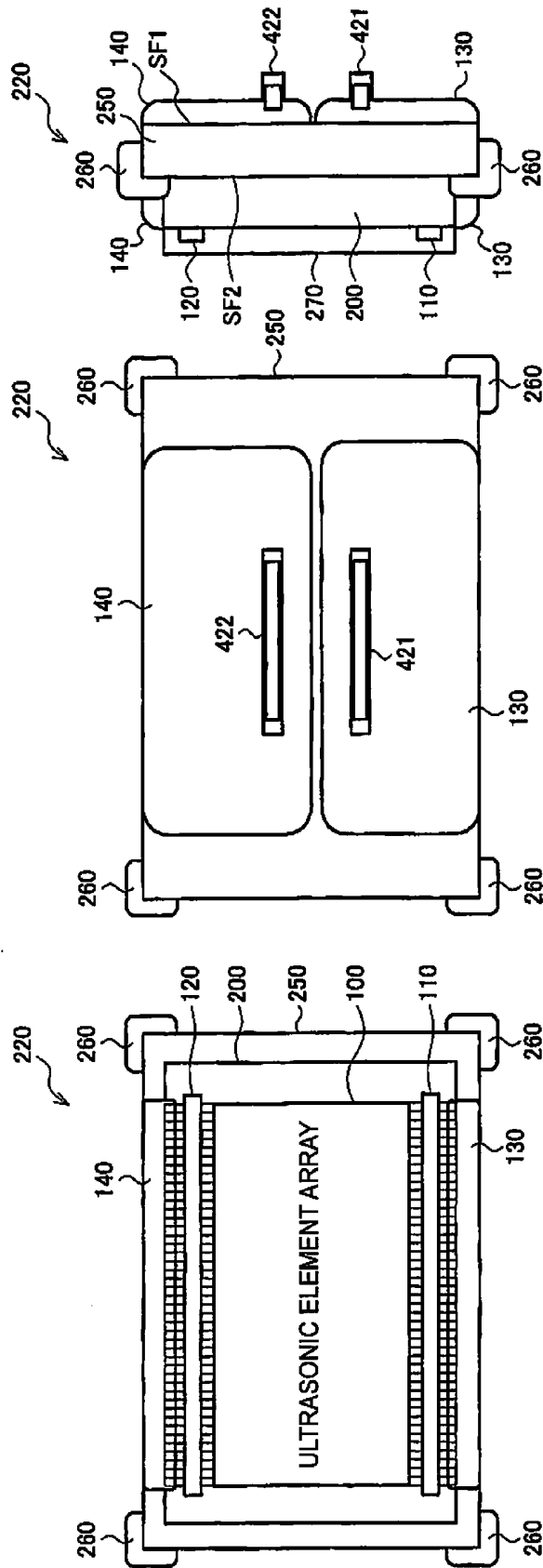


FIG. 19A

FIG. 19B

FIG. 19C

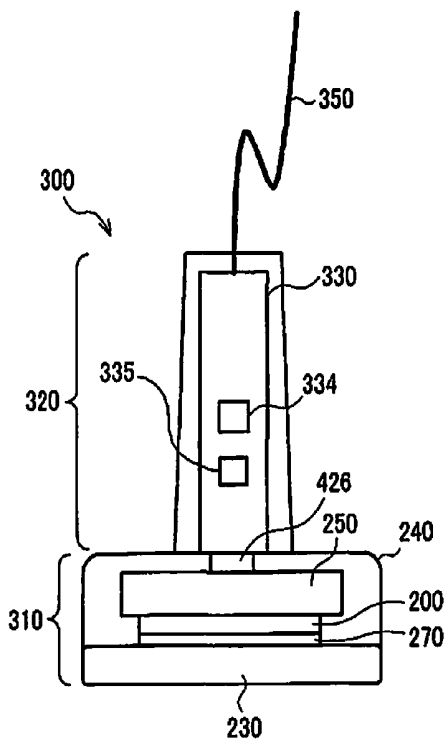


FIG. 20A

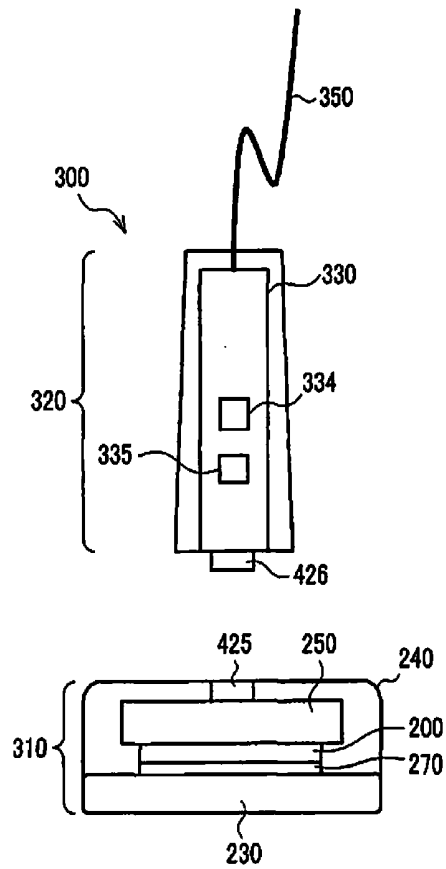


FIG. 20B

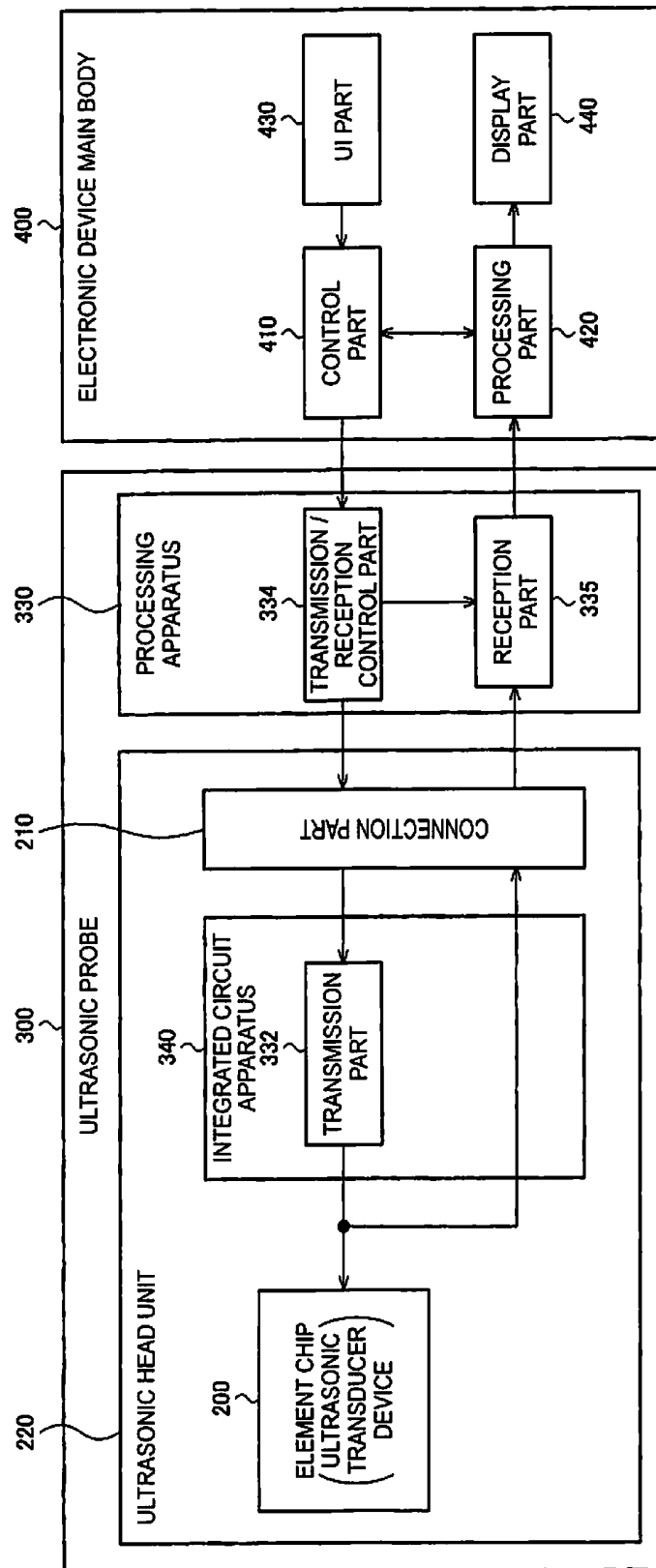


FIG.21

**ULTRASONIC MEASUREMENT APPARATUS,  
ULTRASONIC HEAD UNIT, ULTRASONIC  
PROBE, AND ULTRASONIC IMAGING  
APPARATUS**

**BACKGROUND**

[0001] 1. Technical Field

[0002] The present invention relates to an ultrasonic measurement apparatus, an ultrasonic head unit, an ultrasonic probe, an ultrasonic imaging apparatus, and the like.

[0003] 2. Related Art

[0004] Heretofore, bulk piezoelectric members have been used as ultrasonic transducer elements that transmit and receive ultrasonic waves. For example, JP-A-2005-341085 discloses an ultrasonic probe in which an insulator layer is provided from a portion of a back surface electrode of a bulk piezoelectric member to a lateral surface of the piezoelectric member, a conductor layer is provided continuously with a front surface electrode of the piezoelectric member so as to wrap around to the back surface electrode side, and wiring formed in a flexible substrate is connected to the conductor layer and the back surface electrode on the back surface side of the piezoelectric member.

[0005] A high voltage of around 100 V, for example, is needed in order to drive a bulk piezoelectric member, thus requiring the use of ICs having a high breakdown voltage. There is a problem in that ICs having a high breakdown voltage typically take up a large mounting area and the number of ICs increases, thus making it difficult to miniaturize an apparatus equipped with such ICs.

**SUMMARY**

[0006] An advantage of some aspects of the invention is to provide an ultrasonic measurement apparatus, an ultrasonic head unit, an ultrasonic probe, ultrasonic imaging apparatus and the like that enable device miniaturization to be realized.

[0007] An aspect of the invention relates to an ultrasonic measuring apparatus that includes an ultrasonic transducer device having a substrate and an ultrasonic transducer element array that has a first channel group and a second channel group that are arranged on the substrate, a first integrated circuit apparatus that is mounted on the substrate, at one edge portion of the ultrasonic transducer element array in a first direction, such that a long-side direction coincides with a second direction that intersects the first direction, and performs at least one of signal transmission to the first channel group and signal reception from the first channel group, and a second integrated circuit apparatus that is mounted on the substrate, at the other edge portion of the ultrasonic transducer element array in the first direction, such that the long-side direction coincides with the second direction, and performs at least one of signal transmission to the second channel group and signal reception from the second channel group. In the ultrasonic transducer element array, the first group of channels and the second group of channels are arranged alternately every channel in the second direction.

[0008] According to an aspect of the invention, a first integrated circuit apparatus is arranged at one end of an ultrasonic transducer element array in a first direction, a second integrated circuit apparatus is arranged at the other end, and a first channel group with respect to which the first integrated circuit apparatus performs at least one of signal transmission and reception and a second channel group with respect to which

the second integrated circuit apparatus performs at least one of signal transmission and reception are arranged alternately in the second direction. It thereby becomes possible to miniaturize the apparatus.

[0009] Also, in an aspect of the invention, in a first scanning period, the first integrated circuit apparatus may output odd-numbered pulse signals, among 1st to kth pulse signals (where k is a natural number of 2 or more) to channels belonging to the first channel group, among 1st to kth channels, and the second integrated circuit apparatus may output even-numbered pulse signals, among the 1st to kth pulse signals, to channels belonging to the second channel group, among the 1st to kth channels, and in a second scanning period subsequent to the first scanning period, the second integrated circuit apparatus may output the odd-numbered pulse signals to channels belonging to the second channel group, among 2nd to k+1th channels, and the first integrated circuit apparatus may output the even-numbered pulse signals to channels belonging to the first channel group, among the 2nd to k+1th channels.

[0010] According to this configuration, a scanning operation can be performed in an aspect of the invention in which the first group of channels and the second group of channels are arranged alternately every channel.

[0011] Also, in an aspect of the invention, the ultrasonic measurement apparatus may include a processing part that outputs a control command for controlling transmission in the first scanning period and the second scanning period to the first integrated circuit apparatus and the second integrated circuit apparatus, and the first integrated circuit apparatus and the second integrated circuit apparatus may each include a plurality of transmission circuits that transmit pulse signals; and a control circuit that controls the plurality of transmission circuits based on the control command.

[0012] According to this configuration, a plurality of transmission circuits are able to transmit pulse signals in the first scanning period and the second scanning period, as a result of the processing part outputting a control command, and each integrated circuit apparatus controlling the plurality of transmission circuits based on the control command.

[0013] Also, in an aspect of the invention, the ultrasonic measurement apparatus may include a processing part that performs reception processing of reception signals, and the processing part may perform the reception processing, based on the reception signals from the first channel group and the reception signals from the second channel group obtained by the first integrated circuit apparatus and the second integrated circuit apparatus transmitting signals.

[0014] According to this configuration, reception processing of reception signals from the first channel group and reception signals from the second channel group is performed by the processing part, thus enabling the reception signals of a plurality of channels to be combined in the reception processing which includes reception focusing and the like, for example.

[0015] Also, in an aspect of the invention, in the ultrasonic transducer element array, 1st to Nth channels (where N is a natural number of 2 or more) may be arranged in the second direction, the first channel group may consist of odd-numbered channels, among the 1st to Nth channels, and the second channel group may consist of even-numbered channels, among the 1st to Nth channels.

[0016] According to this configuration, the first channel group with respect to which the first integrated circuit appa-

ratus performs at least one of transmission and reception and the second channel group with respect to which the second integrated circuit apparatus performs at least one of transmission and reception can be arranged alternately every channel.

**[0017]** Also, in an aspect of the invention, the first integrated circuit apparatus may have a plurality of transmission circuits that are arranged in the second direction and transmit a signal to the first channel group, and the second integrated circuit apparatus may have a plurality of transmission circuits that are arranged in the second direction and transmit a signal to the second channel group.

**[0018]** According to this configuration, the first integrated circuit apparatus is able to output a transmission signal to odd-numbered channels, and the second integrated circuit apparatus is able to output a transmission signal to even-numbered channels. The arrangement pitch of the channels is thereby smaller than the arrangement pitch of the transmission circuits, enabling an ultrasonic transducer element array having a smaller element pitch to be realized.

**[0019]** Also, in an aspect of the invention, the first integrated circuit apparatus and second integrated circuit apparatus may be flip chip mounted on the substrate.

**[0020]** According to this configuration, rather than mounting integrated circuit apparatuses on a rigid board using a flat package or the like, the integrated circuit apparatuses can be mounted on the ultrasonic transducer device, thus enabling the ultrasonic measurement apparatus to be miniaturized.

**[0021]** Also, in an aspect of the invention, each channel of the first channel group and the second channel group may have 1st to mth element groups (where m is a natural number of 2 or more), the plurality of ultrasonic transducer elements included in each of the 1st to mth element groups may be electrically connected in parallel within the element group, and the 1st to mth element groups may be electrically connected in series.

**[0022]** According to this configuration, because the 1st to mth element groups are connected in series, the amplitudes of the reception voltages of the 1st to mth element groups are added together, enabling reception sensitivity to be improved. Also, transmission sound pressure can be increased as a result of the ultrasonic transducer elements included in each element group being connected in parallel. This enables an increase in transmission sound pressure to be achieved together with an improvement in reception sensitivity.

**[0023]** Also, in an aspect of the invention, each channel of the first channel group and the second channel group may have 1st to mth element groups (where m is a natural number of 2 or more), the plurality of ultrasonic transducer elements included in each of the 1st to mth element groups may be electrically connected in series within the element group, and the 1st to mth element groups may be electrically connected in parallel.

**[0024]** According to this configuration, because the plurality of ultrasonic transducer elements in each element group are connected in series, the amplitudes of the reception voltages of the plurality of ultrasonic transducer elements are added together, enabling the reception sensitivity to be improved. Also, transmission sound pressure can be increased as a result of the 1st to mth element groups being connected in parallel. This enables an increase in transmission sound pressure to be achieved together with an improvement in reception sensitivity.

**[0025]** Also, in an aspect of the invention, the substrate may have a plurality of openings arranged in an array, the ultra-

sonic transducer element array may have an ultrasonic transducer element for each of the plurality of openings, the ultrasonic transducer elements may each include a vibration film that closes a corresponding opening among the plurality of openings, and a piezoelectric element part that is provided on the vibration film, and the piezoelectric element part may include a lower electrode that is provided on the vibration film, a piezoelectric layer that is provided so as to cover at least a portion of the lower electrode, and an upper electrode that is provided so as to cover at least a portion of the piezoelectric layer.

**[0026]** According to this configuration, an ultrasonic transducer element array can be configured by ultrasonic transducer elements that use a piezoelectric layer to vibrate a vibration film which closes an opening. This enables the ultrasonic transducer elements to be driven with a drive signal of a lower voltage compared with the case where bulk piezoelectric elements are used, and an integrated circuit apparatus can be manufactured with a process having a low breakdown voltage, thus enabling the integrated circuit apparatus to be formed compactly.

**[0027]** A further aspect of the invention relates to an ultrasonic head unit including the ultrasonic measurement apparatus according to any of the above.

**[0028]** A still further aspect of the invention relates to an ultrasonic probe including the ultrasonic measurement apparatus according to any of the above.

**[0029]** A still further aspect of the invention relates to an ultrasonic imaging apparatus including the ultrasonic probe described above and a display part that displays image data for display.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0030]** The invention will be described with reference to the accompanying drawings, wherein like numbers reference like elements.

**[0031]** FIGS. 1A and 1B show illustrative diagrams regarding a comparative example of an embodiment of the invention.

**[0032]** FIG. 2A shows exemplary specifications of an ultrasonic probe and devices, and FIG. 2B shows exemplary specifications of a typical commercial probe.

**[0033]** FIGS. 3A to 3C show an exemplary configuration of an ultrasonic transducer element.

**[0034]** FIG. 4 shows an exemplary configuration of an ultrasonic transducer element.

**[0035]** FIGS. 5A and 5B show exemplary configurations of a channel.

**[0036]** FIG. 6 shows an exemplary basic configuration of an ultrasonic measurement apparatus.

**[0037]** FIG. 7 shows an exemplary basic configuration of an ultrasonic measurement apparatus.

**[0038]** FIG. 8 shows a circuit block diagram of an exemplary configuration of an ultrasonic measurement apparatus.

**[0039]** FIG. 9 shows a detailed exemplary configuration of an integrated circuit apparatus.

**[0040]** FIG. 10 shows an illustrative diagram regarding transmission/reception control.

**[0041]** FIG. 11 shows an exemplary layout configuration of an integrated circuit apparatus.

**[0042]** FIG. 12 shows an exemplary configuration of an ultrasonic probe.

**[0043]** FIG. 13 shows a circuit block diagram of a second exemplary configuration of an ultrasonic measurement apparatus.

**[0044]** FIG. 14 shows a second detailed exemplary configuration of an integrated circuit apparatus.

**[0045]** FIG. 15 shows a second exemplary layout configuration of an integrated circuit apparatus.

**[0046]** FIG. 16 shows a first exemplary modified configuration of a channel.

**[0047]** FIG. 17 shows a second exemplary modified configuration of a channel.

**[0048]** FIG. 18 shows an exemplary configuration of a head unit.

**[0049]** FIGS. 19A to 19C show a detailed exemplary configuration of an ultrasonic head unit.

**[0050]** FIGS. 20A and 20B show an exemplary configuration of an ultrasonic probe.

**[0051]** FIG. 21 shows an exemplary configuration of an ultrasonic imaging apparatus.

#### DESCRIPTION OF EXEMPLARY EMBODIMENTS

**[0052]** Hereinafter, preferred embodiments of the invention will be described in detail. Note that the embodiments described below are not intended to unduly limit the scope of the invention as defined in the claims, and not all combinations of the features described in the embodiments are essential to means for solving the problems addressed by the invention.

##### 1. Comparative Example of the Present Embodiment

**[0053]** As described above, since an IC having a high breakdown voltage is needed when bulk ultrasonic transducer elements are used, there is a problem in that device miniaturization is not readily achieved. For example, although there is a demand, with portable ultrasonic imaging apparatuses, to miniaturize the probe and the device body, miniaturization is hindered when ICs having a high breakdown voltage are mounted.

**[0054]** Also, in JP-A-2005-341085 discussed above, the electrodes of bulk piezoelectric members, which are ultrasonic transducer elements, are connected to a transmission/reception part via a flexible substrate. Since only the wiring that connects the transmission/reception part to the electrodes is formed in the flexible substrate, there is a problem in that the number of components and costs increase.

**[0055]** Also, since almost all ICs (integrated circuit apparatuses) that drive ultrasonic transducer elements are mounted on the main substrate, which consists of a rigid board, ICs are assumed to be constituted by a flat package, and the ICs thus occupy a large area on the main substrate. Also, since a semiconductor process that can withstand a high voltage of around 100 V needs to be used in order to drive a bulk piezoelectric member, a large IC mounting area is required. Thus, with the technique disclosed in JP-A-2005-341085, there is a problem in that device miniaturization is difficult to achieve in the case where this technique is applied to a portable ultrasonic imaging apparatus or the like.

**[0056]** Also, since the area and number of drive ICs will be reduced by reducing the number of drive channels in order to achieve device miniaturization using ICs having a large mounting area such as described above, there is a problem in that the number of channels of the ultrasonic transducer ele-

ment array decreases. Since the convergence of the ultrasonic beam drops when the number of channels decreases, resolution, which is an important characteristic of an ultrasonic imaging apparatus, will be reduced.

**[0057]** In view of this, in the present embodiment, the ultrasonic transducer elements are constituted using thin film piezoelectric elements (piezoelectric layer 30), as will be discussed later with FIG. 3A and the like. With this configuration, the drive ICs can be miniaturized because of being able to drive the ultrasonic transducer elements with 10 to 30 V. For example, an exemplary comparative configuration of the present embodiment is shown in FIG. 1A.

**[0058]** This exemplary comparative configuration includes channels CH1 to CH64 and integrated circuit apparatuses IC1 and IC2 that drive the channels CH1 to CH64 from both ends. The channels CH1 to CH64 are constituted by a plurality of ultrasonic transducer elements, and are, for example, element columns such as will be discussed later with FIG. 5A. The ultrasonic transducer element array is constituted by the channels CH1 to CH64, and the length thereof in the scan direction is given as head length W. Integrated circuit apparatuses IC1 and IC2 are arranged so that the long-side direction thereof coincides with the direction of the head length W, and output terminals for the 64 channels are aligned along the long side thereof. In the present embodiment, since the drive voltage is lower than a bulk piezoelectric member, it is possible to miniaturize the integrated circuit apparatuses IC1 and IC2 to achieve a configuration such as shown in FIG. 1A.

**[0059]** FIG. 2A shows exemplary specifications and diseases given in the present embodiment, and FIG. 2B shows exemplary specifications of a common commercial probe. The suitable depth for observation varies according to the type of disease being diagnosed, and the ultrasonic wave frequency and the number of channels are set according to the depth. For example, the suitable depth for observation and the ultrasonic wave frequency are defined for lymphedema, decubitus and the like shown in FIG. 2A. As shown in FIG. 2B, the head length, number of channels and the like are automatically decided in correspondence to the ultrasonic wave frequency that is determined. Generally, a higher frequency and larger number of channels is required the shallower the depth.

**[0060]** On the other hand, as shown in FIGS. 2A and 2B, the head length is the same (or substantially the same) irrespective of the disease, the number of channels, or the like. That is, an increase in the number of channels is required in order to correspond to a disease having a shallow observation depth, but the head length will remain unchanged. For example, as shown in FIG. 1B, 128 channels are constituted with the same head length W as in the case of 64 channels. In this case, the integrated circuit apparatuses IC1 and IC2 need to be set to 128 channels, although the use of a process having a breakdown voltage of 10 to 30 V makes it difficult to increase the number of channels while maintaining the length in the long-side direction. Thus, there is a problem in that the length in the long-side direction will be greater than the head length W, making compact arrangement and wiring difficult.

##### 2. Ultrasonic Transducer Element

**[0061]** Hereinafter, an ultrasonic measurement apparatus of the present embodiment that can solve such problems will be described. First, the ultrasonic transducer element that is applied to the ultrasonic measurement apparatus of the present embodiment will be described.

[0062] FIGS. 3A to 3C show an exemplary configuration of an ultrasonic transducer element 10 that is applied to an ultrasonic transducer device of the present embodiment. This ultrasonic transducer element 10 includes a vibration film 50 (membrane, supporting member), a first electrode layer 21 (lower electrode layer), a piezoelectric layer 30 (piezoelectric film), and a second electrode layer 22 (upper electrode layer).

[0063] The ultrasonic transducer element 10 is formed on a substrate 60. The substrate 60 is a silicon substrate, for example. FIG. 3A is a plan view of the ultrasonic transducer element 10 looking from a direction perpendicular to the element formation side of the substrate 60. FIG. 3B is a cross-sectional view showing a cross-section along AA' in FIG. 3A. FIG. 3C is a cross-sectional view showing a cross-section along BB' of FIG. 3A.

[0064] The first electrode layer 21 is formed on an upper layer of the vibration film 50 with a metal thin film, for example. This first electrode layer 21 may be wiring that extends to outside the element formation area as shown in FIG. 3A, and is connected to an adjacent ultrasonic transducer element 10.

[0065] The piezoelectric layer 30 is formed using a PZT (lead zirconate titanate) thin film, for example, and is provided so as to cover at least a portion of the first electrode layer 21. Note that the material of the piezoelectric layer 30 is not limited to PZT, and materials such as lead titanate ( $\text{PbTiO}_3$ ), lead zirconate ( $\text{PbZrO}_3$ ) and lead lanthanum titanate ( $(\text{Pb,Lu})\text{TiO}_3$ ), for example, may be used.

[0066] The second electrode layer 22 is formed with a metal thin film, for example, and is provided so as to cover at least a portion of piezoelectric layer 30. This second electrode layer 22 may be wiring that extends to outside the element formation area as shown in FIG. 3A, and is connected to an adjacent ultrasonic transducer element 10.

[0067] One of the portion of the first electrode layer 21 covered by the piezoelectric layer 30 and the portion of the second electrode layer 22 covering the piezoelectric layer 30 constitutes a first electrode and the other thereof constitutes a second electrode. The piezoelectric layer 30 is provided so as to be sandwiched by the first electrode and second electrode. The first electrode, the second electrode and the piezoelectric layer 30 are also called piezoelectric element parts.

[0068] The vibration film 50 is provided so as to close an opening 40 using a two layer structure consisting of an  $\text{SiO}_2$  thin film and an  $\text{ZrO}_2$  thin film, for example. This vibration film 50 supports the piezoelectric layer 30, the first electrode layer 21 and the second electrode layer 22, and is able to produce ultrasonic waves by vibrating in accordance with the expansion and contraction of the piezoelectric layer 30.

[0069] The opening 40 (cavity area) is formed by etching using reactive ion etching (RIE) or the like from the bottom surface of the substrate 60 (surface on which the element is not provided). The resonance frequency of the ultrasonic waves is determined by the size of the vibration film 50 which can vibrate due to formation of the opening 40, and the ultrasonic waves are irradiated to the piezoelectric layer 30 side (in a direction from far to near on the page in FIG. 3A).

[0070] The piezoelectric layer 30 expands and contracts in an in-plane direction as a result of a voltage being applied between the first electrode and the second electrode, that is, between the first electrode layer 21 and the second electrode layer 22. The ultrasonic transducer element 10 uses a monomorph (unimorph) structure in which a thin piezoelectric element (piezoelectric layer 30) and a metal plate (vibration

film 50) are stuck together, and warping occurs because the dimensions of the vibration film 50 remain the same when the piezoelectric layer 30 stuck thereto expands and contracts in-plane. The vibration film 50 vibrates in the film thickness direction as a result of an AC voltage being applied to the piezoelectric layer 30, and ultrasonic waves are irradiated due to the vibrations of the vibration film 50. The voltage applied to the piezoelectric layer 30 is 10 to 30 V, for example, and the frequency is 1 to 10 MHz, for example.

[0071] By constituting the ultrasonic transducer element as described above, the element can be miniaturized compared with a bulk ultrasonic transducer element, enabling the element pitch to be reduced. The occurrence of grating lobes can thereby be suppressed. Also, since the element can be driven with a small voltage amplitude compared with a bulk ultrasonic transducer element, the drive circuit can be constituted by circuit elements having a low breakdown voltage.

### 3. Ultrasonic Transducer Device

[0072] FIG. 4 shows an exemplary configuration of an ultrasonic transducer device 200 that is included in the ultrasonic measurement apparatus of the present embodiment.

[0073] Note that although a case in which a type of transducer that uses a piezoelectric element (thin film piezoelectric element) such as described above as the ultrasonic transducer device 200 is employed will be described below as an example, the present embodiment is not limited thereto. For example, a type of transducer that uses a capacitive element such as a c-MUT (Capacitive Micro-machined Ultrasonic Transducers) may be employed.

[0074] Also, although a case in which the transmission/reception channels are constituted by channels 1 to 128 will be described hereinafter as an example, the present embodiment is not limited thereto, and the transmission/reception channels may be constituted by channels 1 to N other than  $N=128$ . Also, although a case in which an element group is connected between a channel terminal (signal terminal) and a common terminal will be described hereinafter as an example, the present embodiment is not limited thereto. That is, the element group may be connected between two signal terminals, and anti-phase signals, for example, may be supplied to these two signal terminals.

[0075] The ultrasonic transducer device 200 includes the substrate 60, an ultrasonic transducer element array 100 formed on the substrate 60, channel terminals XA1 to XA128 (signal terminals) formed on the substrate 60, common terminals XC1 to XC128 (broadly speaking, signal terminals) formed on the substrate 60, signal electrode lines LX1 to LX128 formed on the substrate 60, and common electrode lines LC1 to LC128 (broadly speaking, signal electrode lines) formed on the substrate 60.

[0076] Channel terminals XAi (where i is an odd number) and common terminals XCi are arranged on one edge portion of the ultrasonic transducer element array 100 in a slice direction DL. The channel terminals XAi are connected to one end of signal electrode lines LXi, and the common terminals XCi are connected to one end of common electrode lines LCi. Channel terminals XAi+1 (where i+1 is an even number) and common terminals XCi+1 are arranged on the other edge portion of the ultrasonic transducer element array 100 in the slice direction DL. The channel terminals XAi+1 are connected to one end of signal electrode lines LXi+1, and the common terminals XCi+1 are connected to one end of common electrode lines LCi+1. For example, the substrate 60 is a

rectangle whose long-side direction coincides with a scan direction DS, the odd-numbered channel terminals X<sub>Ai</sub> and common terminals X<sub>CI</sub> are arranged along one long side of the rectangle, and the even-numbered channel terminals X<sub>Ai+1</sub> and common terminals X<sub>CI+1</sub> are arranged along the other long side of the rectangle.

[0077] Here, the slice direction DL (first direction) and the scan direction DS (second direction) represent the directions of the plane of the substrate 60. The scan direction DS corresponds to a direction in which an ultrasonic beam is scanned in a scanning operation such as linear scanning or sector scanning, for example. The slice direction DL is a direction intersecting (for example, orthogonal to) the scan direction DS, and, in the case where, for example, a tomographic image is obtained by scanning an ultrasonic beam, corresponds to a direction orthogonal to the image.

[0078] The ultrasonic transducer element array 100 includes channels CH<sub>1</sub> to CH<sub>128</sub> that are arranged in the scan direction DS. Channels CH<sub>i</sub> and CH<sub>i+1</sub> are each constituted by a plurality of ultrasonic transducer elements 10 that are electrically connected, and are respectively connected to the other end of the signal electrode lines LX<sub>i</sub> and LX<sub>i+1</sub> and the other end of the common electrode lines LC<sub>i</sub> and LC<sub>i+1</sub>. The configuration of the channels CH<sub>i</sub> and CH<sub>i+1</sub> will be discussed in detail later.

[0079] Transmission and reception of ultrasonic waves are performed as follows. Taking the odd-numbered channels as an example, upon a transmission signal (for example, a voltage pulse) being supplied to the channel terminals X<sub>Ai</sub>, the ultrasonic transducer elements 10 of the channels CH<sub>i</sub> convert the transmission signal into an ultrasonic wave, and the ultrasonic wave is emitted. The ultrasonic transducer elements 10 then convert an ultrasonic echo reflected by the subject into a reception signal (for example, a voltage signal), and the reception signal is output from the channel terminals X<sub>Ai</sub>. Note that a common voltage (for example, a fixed voltage) is supplied to the common terminals X<sub>CI</sub>.

#### 4. Channels

[0080] A detailed exemplary configuration of the channel CH<sub>i</sub> (channel element group) is shown in FIG. 5A. Note that the channel CH<sub>i+1</sub> can also be similarly constituted.

[0081] The channel CH<sub>i</sub> includes the ultrasonic transducer elements UE<sub>1</sub> to UE<sub>8</sub> that are arranged in the slice direction DL. One of the electrodes (for example, the first electrode layer 21 in FIG. 3A) of the ultrasonic transducer elements UE<sub>1</sub> to UE<sub>8</sub> is connected to the signal electrode line LX<sub>i</sub>. The other electrode (for example, the second electrode layer 22 in FIG. 3A) is connected to common electrode lines LY<sub>1</sub> to LY<sub>8</sub>. The common electrode lines LY<sub>1</sub> to LY<sub>8</sub> are laid out in the scan direction DS, and are connected to the common electrode line LC<sub>i</sub>.

[0082] In the case where the channel CH<sub>i</sub> in FIG. 5A is applied to FIG. 4, the ultrasonic transducer elements 10 will be arranged in the ultrasonic transducer element array 100 in a matrix consisting of 8 rows and 128 columns.

[0083] Note that although the case where eight ultrasonic transducer elements are arranged in the slice direction DL was described above as an example, the present embodiment is not limited thereto, and M ultrasonic transducer elements (where M is a natural number of 2 or more) other than M=8 may be arranged. That is, the ultrasonic transducer element array 100 may be a matrix consisting of M rows and N columns. Also, the ultrasonic transducer element array 100 is

not limited to arrangement in matrix form. For example, channels having different numbers of elements in the slice direction DL may be provided together, or elements may be arranged so as to not be in a straight line in the scan direction DS or the slice direction DL (for example, arranged in a staggered pattern).

[0084] Also, although the case where one channel is constituted by one element column was described above as an example, the present embodiment is not limited thereto, and one channel may be constituted by a plurality of element columns. For example, as shown in FIG. 5B, the channel CH<sub>i</sub> has ultrasonic transducer elements UE<sub>11</sub> to UE<sub>18</sub> and UE<sub>21</sub> to UE<sub>28</sub> arranged in the slice direction DL. The ultrasonic transducer elements UE<sub>11</sub> to UE<sub>18</sub> and UE<sub>21</sub> to UE<sub>28</sub> are connected to signal electrode lines LX<sub>1i</sub> and LX<sub>2i</sub>. The signal electrode lines LX<sub>1i</sub> and LX<sub>2i</sub> are connected to the channel terminal X<sub>Ai</sub>.

[0085] Also, although the case where a common terminal is connected to each channel and the common electrode lines are divided one to each channel was described above as an example, the present embodiment is not limited thereto. For example, the channels CH<sub>1</sub> to CH<sub>128</sub> may be connected to shared common electrode lines and common terminals.

#### 5. Basic Configuration of Ultrasonic Measurement Apparatus

[0086] FIGS. 6 and 7 show an exemplary basic configuration of the ultrasonic measurement apparatus of the present embodiment. This ultrasonic measurement apparatus includes the ultrasonic transducer device 200, a first flexible substrate 130, a second flexible substrate 140, and a first integrated circuit apparatus 110 and a second integrated circuit apparatus 120 that are mounted on the substrate 60 of the ultrasonic transducer device 200. Note that, hereinafter, the ultrasonic transducer device 200 is also called an element chip as appropriate.

[0087] On a surface SYM on the ultrasonic wave emission direction side of the substrate 60 of the element chip 200 (that is, on the side on which the piezoelectric layer 30 is formed), the signal electrode lines LX<sub>1</sub> to LX<sub>128</sub> are formed in the slice direction DL, and the integrated circuit apparatuses 110 and 120 are mounted. In a state where the integrated circuit apparatuses 110 and 120 are mounted, transmission terminals TT<sub>1</sub> to TT<sub>64</sub> and dummy terminals TD<sub>1</sub> to TD<sub>64</sub> of the integrated circuit apparatus 110 are connected to the odd-numbered signal electrode lines LX<sub>1</sub>, LX<sub>3</sub>, . . . , LX<sub>127</sub>, and transmission terminals TTB<sub>1</sub> to TTB<sub>64</sub> and dummy terminals TDB<sub>1</sub> to TDB<sub>64</sub> of the integrated circuit apparatus 120 are connected to even-numbered signal electrode lines LX<sub>2</sub>, LX<sub>4</sub>, . . . , LX<sub>128</sub>.

[0088] The transmission terminals TT<sub>1</sub> to TT<sub>64</sub> are arrayed along a first long side (HL1 of FIG. 11) of the integrated circuit apparatus 110. The dummy terminals TD<sub>1</sub> to TD<sub>64</sub> are arrayed along a second long side (HL2) of the integrated circuit apparatus 110. The integrated circuit apparatus 110 is mounted on the substrate 60 such that the long sides lay in the scan direction DS, and the long side on which the transmission terminal TT<sub>1</sub> to TT<sub>64</sub> are arrayed faces the ultrasonic transducer element array 100 side. In plan view looking at the substrate 60 from the side on which the integrated circuit apparatus 110 is mounted, the signal electrode lines LX<sub>1</sub>, LX<sub>3</sub>, . . . , LX<sub>127</sub> pass under the integrated circuit apparatus 110.

[0089] Here, a “dummy terminal” is a terminal that does not input or output signals such as transmission signals, reception signals and control signals, for example, and is, for example, formed from a bump terminal, without a circuit being connected to the bump terminal. Note that the dummy terminals may also include test terminals that input and output signals in a test step of the manufacturing process. Also, an electrostatic protection circuit may be connected to the dummy terminals.

[0090] Note that control terminals (TP in FIG. 9) may be arranged along a first short side (HS1 in FIG. 11) and a second short side (HS2) of the integrated circuit apparatus 110. The control terminals are connected to control signal lines formed on the substrate 60 of the element chip 200. These control signal lines are formed in the same interconnect layer (conductive layer) as the first electrode layer 21 and the second electrode layer 22 that were described with FIG. 3A and the like, for example. Transmission pulse signals and transmission/reception control signals are supplied to the control terminals from the transmission/reception control circuit 560 in FIG. 8, for example, and the integrated circuit apparatus 110 generates transmission signals based on these transmission pulse signals and transmission/reception control signals. Also, although not illustrated, common output terminals may be provided in the integrated circuit apparatus 110. The common output terminals supply a common voltage to the common electrode lines LC1, LC3, . . . , LC127 of the element chip 200.

[0091] The terminals of the integrated circuit apparatus 110 are bump terminals, and are formed by metal plating pad terminals of the integrated circuit apparatus 110, for example. Alternatively, a resin layer serving as an insulating layer, metal wiring, and bump terminals that are connected to the metal wiring may be formed on the element formation surface of the integrated circuit apparatus 110.

[0092] The terminals of the integrated circuit apparatus 120 can be constituted similarly to the terminals of the integrated circuit apparatus 110. In plan view, the signal electrode lines LX2, LX4, . . . , LX128 pass under the integrated circuit apparatus 120.

[0093] Signal lines LT1 to LT64 are formed on the flexible substrate 130. These signal lines LT1 to LT64 are formed on the inner side of the flexible substrate 130 (on the right side when facing the page in FIG. 7), and are connected to the odd-numbered channel terminals XA1, XA3, . . . , XA127 of the element chip 200. The other end of the signal lines LT1 to LT64 extends to the other end of the flexible substrate 130, and are connected to connector terminals for connecting to a downstream circuit board or the like, for example.

[0094] The flexible substrate 140 can constitute similarly to the flexible substrate 130. Signal lines LTB1 to LTB64 of the flexible substrate 140 are connected to the even-numbered channel terminals XA2, XA4, . . . , XA128 of the element chip 200.

[0095] The operations of above ultrasonic measurement apparatus will now be described. Transmission signals from the integrated circuit apparatuses 110 and 120 are input to the ultrasonic transducer element array 100 via the transmission terminals TT1 to TT64 and TTB1 to TTB64 and the signal electrode lines LX1 to LX128. The ultrasonic transducer element array 100 emits ultrasonic waves using these transmission signals, the ultrasonic waves are reflected by the observation object, and the reflected waves are received by the ultrasonic transducer element array 100. When these ultrasonic waves are received, a reception signal from the

ultrasonic transducer element array 100 is output to the signal lines LT1 to LT64 and LTB1 to LTB64 of the flexible substrates 130 and 140, via the signal electrode lines LX1 to LX128 and the channel terminals XA1 to XA128. The reception signal is output to a downstream reception circuit (for example, analog front end circuit 550 in FIG. 8). The circuit configuration and operations of the integrated circuit apparatuses 110 and 120 will be discussed in detail later.

## 6. Flip Chip Mounting

[0096] Hereinafter, flip chip mounting will be described taking the integrated circuit apparatus 110 as an example. Note that the integrated circuit apparatus 120 is also mounted using a similar technique.

[0097] Mounting of the integrated circuit apparatus 110 is realized by flip chip mounting (bare chip mounting) using an anisotropic conductive film 115 (ACF), as shown in FIG. 7. The anisotropic conductive film 115 is a resin film containing conductive particles such as metal particulates. When the integrated circuit apparatus 110 has been adhered to the substrate 60 with this anisotropic conductive film 115 interposed therebetween and the anisotropic conductive film 115 has been thermoset, the anisotropic conductive film 115 shrinks on hardening, and the integrated circuit apparatus 110 and the substrate 60 are drawn to each other as a result of the shrinkage. Electrical continuity is then established with the wiring of the substrate 60 by projecting terminals (bumps) of the integrated circuit apparatus 110 crushing the conductive particles, and the integrated circuit apparatus 110 is supported by these projecting terminals countering the shrinkage force due to hardening. In the portions of the film that are not compressed by the terminals, the conductive particles are maintained in an insulated state by the resin, and short-circuiting of the terminals is thereby prevented.

[0098] By thus performing flip chip mounting on the substrate 60 using the anisotropic conductive film 115, the mounting area can be reduced compared with the case where the integrated circuit apparatuses of a flat package are mounted to a downstream printed circuit board (rigid board). Also, since the element chip 200 of the present embodiment can be driven at around 10 to 30 V as described above, the integrated circuit apparatus 110 can be miniaturized. Thus, miniaturization by flip chip mounting, which is difficult with bulk piezoelectric elements that required integrated circuit apparatuses having a high breakdown voltage, can be easily realized. Also, the substrate 60 is constituted by a silicon substrate, the same as the integrated circuit apparatus 110. That is, since substrates having the same coefficient of thermal expansion are bonded, mounting having high bonding reliability can be realized, compared with bonding different materials having different coefficients of thermal expansion.

[0099] Note that the flip chip mounting is, for example, face-down mounting in which mounting is performed with the element formation surface on the substrate 60 side. Alternatively, the flip chip mounting may be face-up mounting in which mounting is performed with the opposite surface to the element formation surface on the substrate 60 side.

[0100] In the present embodiment, the dummy terminals TD1 to TD64 are provided on the integrated circuit apparatus 110. Hypothetically, in the case where the dummy terminals TD1 to TD64 are not provided, only the transmission terminals TT1 to TT64 exist on one long side of the integrated circuit apparatus 110, and the shrinkage force due to hardening of the anisotropic conductive film 115 causes an imbal-

ance between the side with terminals and the side without terminals. Due to this imbalance, a force that draws the integrated circuit apparatus 110 and the substrate 60 together occurs on the side without terminals. On the other hand, a force that lifts up the terminals occurs on the side with terminals due to this drawing force, possibly causing the transmission terminals TT1 to TT64 to rise away from the signal electrode lines LX1, LX3, . . . , LX127.

[0101] Regarding this point, in the present embodiment, the dummy terminals TD1 to TD64 are provided on the second long side of the integrated circuit apparatus 110. Since the countering force of the transmission terminals TT1 to TT64 and the countering force of the dummy terminals TD1 to TD64 with respect to the shrinkage force due to hardening of the anisotropic conductive film 115 are thereby balanced out, the forces are in equilibrium and the electrical continuity between the transmission terminals TT1 to TT64 and signal electrode lines LX1, LX3, . . . , LX127 can be maintained.

[0102] Note that the present embodiment is not limited to mounting using the anisotropic conductive film 115 (ACF), and the integrated circuit apparatus 110 may be mounted to the substrate 60 using ACP (anisotropic conductive paste), NCF (non-conductive film), NCP (non-conductive paste), or the like, for example.

[0103] The second integrated circuit apparatus 120 is also mounted similarly to the above. That is, the integrated circuit apparatus 120 is flip chip mounted on the surface SYM on the ultrasonic wave emission direction side of the element chip 200, using an anisotropic conductive film 125.

#### 7. Detailed Configuration of Ultrasonic Measurement Apparatus

[0104] FIG. 8 shows a circuit block diagram of an exemplary configuration of an ultrasonic measurement apparatus. This ultrasonic measurement apparatus includes the element chip 200, the integrated circuit apparatuses 110 and 120, and a processing part 500. The processing part 500 includes the analog front end circuit 550 and a transmission/reception control circuit 560.

[0105] The transmission/reception control circuit 560 performs ultrasonic wave transmission control and reception control on the integrated circuit apparatuses 110 and 120. The transmission/reception control circuit 560 supplies control signals thereof to the integrated circuit apparatuses 110 and 120 via the control terminals (TP in FIG. 9) of the integrated circuit apparatuses 110 and 120.

[0106] A reception signal is input to the analog front end circuit 550 from the element chip 200 via the flexible substrates 130 and 140, and the analog front end circuit 550 performs reception processing on the reception signal. Reception processing involves processing such as amplification, A/D conversion and reception focusing, for example. Also, the analog front end circuit 550 includes a limiter circuit 570 that limits the high-voltage transmission signals that are output by the integrated circuit apparatuses 110 and 120. Since the amplitude of the transmission signals is around 10 to 30 V, and the analog front end circuit 550 operates at several volts, the analog front end circuit 550 may be damaged (by electrostatic discharge) when the transmission signals are input directly to the analog front end circuit 550. Thus, the limiter circuit 570 is provided, and input of transmission signals to the analog front end circuit 550 is prevented. Note

that, rather than the limiter circuit 570, a switch element that turns off during the transmission period of ultrasonic waves may be provided.

[0107] The integrated circuit apparatus 110 includes a transmission circuit 112 that amplifies the transmission pulse signals, and a control circuit 114 that controls the transmission circuit 112 based on instructions from the transmission/reception control circuit 560. The integrated circuit apparatus 120 includes a transmission circuit 122 that amplifies the transmission pulse signals, and a control circuit 124 that controls the transmission circuit 122 based on instructions from the transmission/reception control circuit 560.

[0108] An detailed exemplary configuration of the integrated circuit apparatus 110 is shown in FIG. 9. Note that although the integrated circuit apparatus 110 is given as an example, the integrated circuit apparatus 120 can be constituted similarly. The integrated circuit apparatus 110 includes transmission circuits TX1 to TX64 (for example, pulsers) and the control circuit 114. The transmission circuits TX1 to TX64 correspond to the transmission circuit 112 in FIG. 8.

[0109] During the transmission period of ultrasonic waves, the transmission/reception control circuit 560 inputs transmission control commands to the control circuit 114 via the terminal group TP (control terminals). The transmission control commands are written in a register which is not illustrated, for example. The control circuit 114 performs scanning control and transmission focusing control based on the transmission control commands, and supplies transmission pulse signals to the transmission circuits TX1 to TX64. The transmission circuits TX1 to TX64 amplify the supplied transmission pulse signals, and output the amplified transmission pulse signals to the ultrasonic transducer element array 100 via the transmission terminals TT1 to TT64.

[0110] During the reception period of ultrasonic waves, the ultrasonic transducer element array 100 receives the reflected waves of ultrasonic waves reflected from the observation object, and the reception signals thereof are input to the analog front end circuit 550 via signal electrode lines LX1, LX3, . . . , LX127. The reception signals, being weak (voltage swing is small) compared with the transmission signals, are pass through without being limited by the limiter circuit 570, and are input to the reception circuit (for example, low noise amplifier or A/D conversion circuit) of the analog front end circuit 550, or the like.

#### 8. Transmission/reception Control

[0111] Transmission/reception control will be described in detail, taking the case where linear scanning is performed as an example. FIG. 10 shows an illustrative diagram of transmission/reception control. Although the case where one ultrasonic beam is output with eight channels will hereinafter be described as an example, the present embodiment is not limited thereto.

[0112] Scanning periods T1, T2, . . . , shown in FIG. 10 are each a period during which one ultrasonic beam is transmitted and received in a linear scanning. The pulse signals P1 to P8 are the signals of pulse waveforms constituting one ultrasonic beam. A delay is provided in the pulse signals P1 to P8 by transmission focusing control. For example, in the case of emitting an ultrasonic beam in the frontal direction (perpendicular to substrate 60), the outer pulse signals P1 and P8 are emitted first, and the delay increases towards the middle pulse signals P4 and P5.

[0113] In the scanning period T1, transmission and reception are performed using the channels CH1 to CH8. That is, the transmission circuits TX1 to TX4 of the integrated circuit apparatus 110 output the odd-numbered pulse signals P1, P3, P5 and P7 to the odd-numbered channels CH1, CH3, CH5 and CH7, and the transmission circuits TX1 to TX4 of the integrated circuit apparatus 120 output the even-numbered pulse signals P2, P4, P6 and P8 to the even-numbered channels CH2, CH4, CH6 and CH8. At the time of reception, the analog front end circuit 550 receives the reception signals of the channels CH1 to CH8, performs delay adjustment according to the delay at the time of transmission, and acquires one reception signal (signal for one line in the depth direction) by adding together the reception signals after delay adjustment.

[0114] In the next scanning period T2, the ultrasonic beam is shifted one channel, and transmission and reception are performed using the channels CH2 to CH9. That is, the transmission circuits TX1 to TX4 of the integrated circuit apparatus 120 output the odd-numbered pulse signals P1, P3, P5 and P7 to the even-numbered channels CH2, CH4, CH6 and CH8, and the transmission circuits TX2 to TX5 of the integrated circuit apparatus 110 output the even-numbered pulse signals P2, P4, P6 and P8 to the odd-numbered channels CH3, CH5, CH7 and CH9. The analog front end circuit 550 obtains one reception signal from the reception signals of the channels CH2 to CH9.

[0115] In the subsequent scanning periods T3, T4, . . . , the ultrasonic beam is shifted one channel, and similar transmission/reception control is performed.

[0116] Note that the pulse signals P1 to P8 are not limited to emission of an ultrasonic beam to the front, and may be waveforms having a delay for emitting an ultrasonic beam in a direction diagonal to the front, for example. Also, the pulse signals P1 to P8 do not need to be the same in each scanning period, and may be pulse signals having a different delay in each scanning period, for example. For example, the pulse signals may have a delay that changes the emission direction sequentially in the scanning periods T1, T2, T3, . . . .

[0117] Also, in the present embodiment, the scanning operation is not limited to linear scanning, and sector scanning (phase scanning) may be performed, for example. In the case of performing sector scanning, the beam direction is scanned by phase control of the channels CH1 to CH128. At this time, the phase difference (delay) of the channels CH1 to CH128 is controlled by appropriately controlling the delay of the odd-numbered channels that are assigned to the integrated circuit apparatus 110 and the even-numbered channels that are assigned to the integrated circuit apparatus 120.

#### 9. Layout Configuration of Integrated Circuit Apparatus

[0118] FIG. 11 shows an exemplary layout configuration of the integrated circuit apparatus 110. Note that although the integrated circuit apparatus 110 will be given as an example, the integrated circuit apparatus 120 can also be constituted similarly. The integrated circuit apparatus 110 includes the transmission circuits TX1 to TX64, and the control circuits CTS1 and CTS2.

[0119] The transmission circuits TX1 to TX64 are arrayed in the long-side direction of the integrated circuit apparatus 110. Since the integrated circuit apparatus 110 is constituted in a long thin rectangular shape in the long-side direction as a result of adopting such an arrangement, the transmission terminals TT1 to TT64 of the integrated circuit apparatus 110

can be provided opposing the ultrasonic transducer element array 100. The interconnect on the element chip 200 is thereby simplified, making it possible for the ultrasonic transducer device 200 to be configured compactly. Note that the long sides of the integrated circuit apparatus 110 are the first long side HL1 and the second long side HL2. The first long side HL1 opposes the ultrasonic transducer element array 100 at the time of mounting, and is the side on which the transmission terminals TT1 to TT64 are arrayed. The second long side HL2 opposes the channel terminals XA1, XA3, . . . , XA127 at the time of mounting, and is the side on which the dummy terminals TD1 to TD64 are arrayed.

[0120] The control circuit CTS1 is arranged on the first short side HS1 side of the integrated circuit apparatus 110, and the control circuit CTS2 is arranged on the second short side HS2 side of the integrated circuit apparatus 110. The control circuits CTS1 and CTS2 correspond to the control circuit 114 in FIG. 8. By arranging control circuits CTS1 and CTS2 on the short sides in this way, the control terminals can be arranged on the short side, and the short side can be utilized effectively while maintaining the long narrow shape in the long-side direction.

#### 10. Ultrasonic Probe

[0121] FIG. 12 shows an exemplary configuration of a ultrasonic probe that includes the ultrasonic measurement apparatus of the present embodiment. This ultrasonic probe includes a case 600, an acoustic member 610, the element chip 200, the integrated circuit apparatuses 110 and 120, flexible substrates 130 and 140, the connectors 421 to 424, rigid boards 431 to 433, integrated circuit apparatuses 441 to 448, and circuit elements 451 to 455.

[0122] The acoustic member 610 is constituted by an acoustic matching layer, an acoustic lens and the like, for example, and performs acoustic impedance matching between the element chip 200 and the observation object, convergence of the ultrasonic beam, and the like. For example, the silicon substrates of the integrated circuit apparatuses 110 and 120 have been ground down, and these thinly ground integrated circuit apparatuses 110 and 120 are mounted on the substrate 60 of the ultrasonic transducer device 200. The acoustic member 610 is formed with a silicon resin (silicon rubber) layer, for example, and covers the emission surface of the ultrasonic transducer device 200 including the integrated circuit apparatuses 110 and 120. In this way, by including the integrated circuit apparatuses 110 and 120 within the acoustic member 610, the thinly ground integrated circuit apparatuses 110 and 120 can be protected and the probe head can be miniaturized.

[0123] The flexible substrates 130 and 140 connected to the ultrasonic transducer device 200 are connected to the rigid board 432 by the connectors 421 and 422. The rigid boards 431 to 433 are connected by the connectors 423 and 424, and the integrated circuit apparatuses 441 to 448 and the circuit elements 451 to 455 are mounted on the rigid boards 431 to 433.

[0124] The analog front end circuit 550 and the transmission/reception control circuit 560 that were described in FIG. 8 and the like are included in the integrated circuit apparatuses 441 to 448. Also, the integrated circuit apparatuses 441 to 448 can include, for example, a communication processing circuit that performs communication processing with the main body of the ultrasonic imaging apparatus that connects the ultrasonic probe, an image processing circuit that per-

forms image processing, and the like. Various types of circuit elements such as resistive elements, capacitors, coils, electronic buttons and switches, for example, can be used for the circuit elements **451** to **455**.

[**0125**] As described above, a bulk ultrasonic transducer element needs a drive voltage of around 100 V, thus requiring an IC having a high breakdown voltage, and making device miniaturization (for example, miniaturization of the probe) difficult to achieve. In view of this, in the present embodiment, as described with FIG. 1A and the like, thin-film piezoelectric elements are used as ultrasonic transducer elements to reduce the drive voltage to 10 to 30 V, enabling miniaturization to be realized using a drive IC having a low breakdown voltage.

[**0126**] However, there are cases where the arrangement pitch of the channels needs to be reduced, as described with FIG. 1B and the like, and because the size of the drive IC increases with the increase in the number of channels, compact arrangement may not be possible. For example, with the layout of FIG. 11 and the like, the arrangement pitch of the transmission circuits TX1 to TX64 cannot be reduced below a prescribed pitch due to the breakdown voltages, and thus the size of the drive IC may be much greater than the head length W in FIG. 1B.

[**0127**] In view of this, the ultrasonic measurement apparatus of the present embodiment includes the ultrasonic transducer device **200**, the first integrated circuit apparatus **110**, and the second integrated circuit apparatus **120** (FIG. 4, FIG. 6, etc.).

[**0128**] The ultrasonic transducer device **200** has the substrate **60** and the ultrasonic transducer element array **100** which is arranged on the substrate **60**. The ultrasonic transducer element array **100** has the first channel group (CH1, CH3, . . . , CH127) and the second channel group (CH2, CH4, . . . , CH128). The first integrated circuit apparatus **110** is mounted on the substrate **60**, at one end of the ultrasonic transducer element array **100** in the first direction (slice direction DL), such that the long-side direction coincides with the second direction (scan direction DS) which is orthogonal to the first direction, and performs at least one of transmission of signals to the first channel group and reception of signals from the first channel group. The second integrated circuit apparatus **120** is mounted on the substrate **60**, at the other end of the ultrasonic transducer element array **100** in the first direction, such that the long-side direction coincides with the second direction, and performs at least one of transmission of signals to the second channel group and reception of signals from the second channel group.

[**0129**] In the ultrasonic transducer element array **100**, the first group of channels (CH1, CH3, . . . , CH127) and the second group of channels (CH2, CH4, . . . , CH128) are arranged alternately every channel in the second direction.

[**0130**] According to this configuration, the integrated circuit apparatuses **110** and **120** each need only supply a transmission signal every other channel, thus enabling the arrangement pitch of the channels of the ultrasonic transducer element array **100** to be reduced, even without changing the size of the integrated circuit apparatus **110**. This configuration thereby realizes a compact arrangement, and can handle various applications such as described with FIG. 2A and the like. Also, since more ultrasonic transducer elements can be mounted in the same area, a higher resolution can be achieved.

[**0131**] Here, a channel is an element group that is constituted by ultrasonic transducer elements that are connected to the same signal electrode line (i.e., that are supplied with the same transmission signal), among the ultrasonic transducer elements arranged in the ultrasonic transducer element array **100**. For example, in the example in FIG. 5A, the ultrasonic transducer elements UE1 to UE8 constitute a channel, whereas in the example in FIG. 16 discussed below, the ultrasonic transducer elements UE11 to UE43 constitute a channel.

[**0132**] Also, in the present embodiment, in a first scanning period T1, the first integrated circuit apparatus **110** outputs the odd-numbered pulse signals P1, P3, P5 and P7, among the 1st to kth pulse signals P1 to P8 (where k=8; k can be a natural number of 2 or more), to the channels CH1, CH3, CH5 and CH7 belonging to the first channel group, among first to kth channels CH1 to CH8, and the second integrated circuit apparatus **120** outputs the even-numbered pulse signals P2, P4, P6 and P8, among the 1st to kth pulse signals P1 to P8, to the channels CH2, CH4, CH6 and CH8 belonging to the second channel group, among the 1st to kth channels CH1 to CH8. In a second scanning period T2 after the first scanning period T1, the second integrated circuit apparatus **120** outputs the odd-numbered pulse signals P1, P3, P5, and P7 to the channels CH2, CH4, CH6 and CH8 belonging to the second channel group, among the 2nd to k+1th channels CH2 to CH9, and the first integrated circuit apparatus **110** outputs the even-numbered pulse signals P2, P4, P6, and P8 to the channels CH3, CH5, CH7 and CH9 belonging to the first channel group, among the 2nd to k+1th channels CH2 to CH9 (FIG. 10, etc.).

[**0133**] According to this configuration, scanning operations can be realized in the present embodiment in which the first group of channels (CH1, CH3, . . . , CH127) and the second group of channels (CH2, CH4, . . . , CH128) are arranged alternately every channel. That is, linear scanning in which the ultrasonic beam is shifted one channel every scanning period can be realized by the integrated circuit apparatuses **110** and **120** outputting even-numbered and odd-numbered pulse signals alternately every scanning period.

[**0134**] Also, in the present embodiment, the ultrasonic measurement apparatus includes the processing part **500** which outputs control commands for controlling transmission in the first scanning period T1 and the second scanning period T2 to the first integrated circuit apparatus **110** and the second integrated circuit apparatus **120** (FIG. 8, etc.). The first integrated circuit apparatus **110** and the second integrated circuit apparatus **120** each have a plurality of transmission circuits TX1 to TX64 that transmit the pulse signals P1 to P8, and a control circuit **114** or **124** that controls the plurality of transmission circuits based on the control commands (FIG. 9, etc.).

[**0135**] Providing such control commands enables the integrated circuit apparatuses **110** and **120** to be instructed to perform scanning operations such as described above. That is, the transmission circuits TX1 to TX64 are able to transmit appropriate pulse signals P1 to P8 as a result of the processing part **500** outputting control commands, and the control circuits **114** and **124** interpreting the control commands and setting the pulse signal delay and the output channels.

[**0136**] Also, in the present embodiment, the processing part **500** performs reception processing of reception signals. That is, the processing part **500** performs reception processing based on the reception signals from the first channel group (CH1, CH3, . . . , CH127) and the reception signals from the

second channel group (CH2, CH4, . . . , CH128) obtained by the first integrated circuit apparatus 110 and the second integrated circuit apparatus 120 transmitting signals (FIG. 8, etc.).

[0137] In the reception processing, it is necessary to combine the reception signals of a plurality of channels by processing such as reception focusing, and obtain a final reception signal. Regarding this point, in the present embodiment, the integrated circuit apparatuses 110 and 120 respectively transmit signals to odd-numbered and even-numbered channels, and a final reception signal can be acquired by the processing part 500 performing reception processing on the reception signals of the odd-numbered and even-numbered channels in reception.

[0138] Also, in the present embodiment, the 1st to Nth channels CH1 to CH128 (where  $N=128$ ;  $N$  can be a natural number of 2 or more) are arranged in the ultrasonic transducer element array 100 in the second direction (scan direction DS). The first channel group consists of the odd-numbered channels CH1, CH3, . . . , CH127 among the 1st to Nth channels. The second channel group consists of the even-numbered channel CH2, CH4, . . . , CH128 among the 1st to Nth channels.

[0139] According to this configuration, the first channel group with respect to which the first integrated circuit apparatus 110 performs at least one of signal transmission and reception, and the second channel group with respect to which the second integrated circuit apparatus 120 performs at least one of signal transmission and reception can be arranged alternately.

[0140] Also, in the present embodiment, the plurality of transmission circuits TX1 to TX64 of the first integrated circuit apparatus 110 are arranged in the second direction (scan direction DS) (FIG. 11, etc.), and transmit signals to the first channel group (CH1, CH3, . . . , CH127). The plurality of transmission circuits TX1 to TX64 of the second integrated circuit apparatus 120 are arranged in the second direction, and transmit signals to the second channel group (CH2, CH4, . . . , CH128).

[0141] According to this configuration, the first integrated circuit apparatus 110 is able to output transmission signals to odd-numbered channels, and the second integrated circuit apparatus 120 is able to output transmission signals to even-numbered channels. The number of the transmission circuits aligned in the scan direction DS can thereby be reduced to half the number of channels, enabling an ultrasonic transducer element array 100 having half the element pitch to be realized with the integrated circuit apparatuses 110 and 120 of the same size.

[0142] Also, in the present embodiment, the first integrated circuit apparatus 110 and the second integrated circuit apparatus 120 are flip chip mounted on the substrate 60.

[0143] According to this configuration, rather than the integrated circuit apparatuses being mounted on a rigid board using a flat package or the like, for example, the integrated circuit apparatuses 110 and 120 can be mounted on the ultrasonic transducer device 200, thus enabling the ultrasonic measurement apparatus to be miniaturized.

#### 11. Second Detailed Configuration of Ultrasonic Measurement Apparatus

[0144] In the abovementioned embodiment, the case where the integrated circuit apparatus 110 includes only the transmission circuits TX1 to TX64 and the control circuit 114 was

described as an example, but the present embodiment is not limited thereto, and the integrated circuit apparatus 110 may also further include switch elements, multiplexers and the like. Hereinafter, an exemplary configuration of an ultrasonic measurement apparatus in this case will be described.

[0145] FIG. 13 shows a circuit block diagram of an exemplary configuration of an ultrasonic measurement apparatus. This ultrasonic measurement apparatus includes the element chip 200, the integrated circuit apparatuses 110 and 120, and the processing part 500. The processing part 500 includes the analog front end circuit 550 and the transmission/reception control circuit 560. Note that the same reference signs are given to constituent elements that are the same as constituent elements described with FIG. 8 and the like, and description thereof will be omitted as appropriate.

[0146] The integrated circuit apparatus 110 includes a transmission circuit 112 that amplifies transmission pulse signals, a multiplexer 116 that performs transmission control of transmission signals from the transmission circuit 112 and reception control of reception signals from the element chip 200, a transmission/reception change circuit 118 that outputs reception signals from the multiplexer 116 to the analog front end circuit 550, and a control circuit 114 that controls the transmission circuit 112, the multiplexer 116 and the transmission/reception change circuit 118 based on the instructions from the transmission/reception control circuit 560. Similarly, the integrated circuit apparatus 120 includes a transmission circuit 122, a multiplexer 126, a transmission/reception change circuit 128, and a control circuit 124.

[0147] FIG. 14 shows a detailed exemplary configuration of the integrated circuit apparatus 110. Note that although the integrated circuit apparatus 110 will be given as an example, the integrated circuit apparatus 120 can also be constituted similarly. The integrated circuit apparatus 110 includes the transmission circuits TX1 to TX64 (pulsars), the control circuit 114, the multiplexer 116, and switch elements SW1 to SW64 (transmission/reception changeover switches). The transmission circuits TX1 to TX64 correspond to the transmission circuit 112 in FIG. 13, and the switch elements SW1 to SW64 correspond to the transmission/reception change circuit 118 in FIG. 13.

[0148] In the transmission period of ultrasonic waves, the transmission/reception control circuit 560 inputs a transmission control command to the control circuit 114 via the terminal group TP (control terminals). The control circuit 114 supplies a transmission pulse signal to the transmission circuits TX1 to TX64 based on the transmission control command. The transmission circuits TX1 to TX64 amplify the supplied transmission pulse signal, and output the amplified transmission pulse signal to the multiplexer 116. The multiplexer 116 outputs the amplified transmission pulse signal to the ultrasonic transducer element array 100 via the transmission terminals TT1 to TT64.

[0149] In the transmission period, the switch elements SW1 to SW64 are turned off based on an instruction from the control circuit 114, and the transmission pulse signals from the transmission circuits TX1 to TX64 are not output to the analog front end circuit 550. The analog front end circuit 550 generally operates with a voltage of several volts, and the transmission pulse signals are blocked so that the analog front end circuit 550 is not damaged by the transmission pulse signals which have an amplitude of around 10 to 30 V.

[0150] In the reception period of ultrasonic waves, the ultrasonic transducer element array 100 receives the reflected

waves of ultrasonic waves reflected from the observation object, and reception signals are input to the multiplexer **116** via the transmission/reception terminals TT1 to TT64. The multiplexer **116** outputs the reception signals to the switch elements SW1 to SW64. The switch elements SW1 to SW64 are ON during the ultrasonic wave reception period of the ultrasonic transducer element array **100**, and output reception signals to the analog front end circuit **550** via the reception signal output terminals TR1 to TR64.

## 12. Transmission/reception Control in Second Detailed Configuration

[0151] Transmission/reception control will be described in detail, taking the linear scanning described with FIG. 10 as an example. In the linear scanning, the transmission circuits TX5 to TX64 are set to a non-operational mode (for example, power saving mode or power down mode), and the switch elements SW5 to SW64 are turned off. The multiplexer **116** performs switching control on transmission signals and reception signals based on instructions from the control circuit **114**.

[0152] Specifically, in the scanning period T1, the transmission circuits TX1 to TX4 of the integrated circuit apparatus **110** output the odd-numbered pulse signals P1, P3, P5 and P7. The multiplexer **116** outputs the pulse signals P1, P3, P5 and P7 to the channels CH1, CH3, CH5 and CH7. The transmission circuits TX1 to TX4 of the integrated circuit apparatus **120** output the even-numbered pulse signals P2, P4, P6 and P8, and the multiplexer **126** outputs the pulse signals P2, P4, P6 and P8 to the channels CH2, CH4, CH6 and CH8.

[0153] At the time of reception, the multiplexer **116** of the integrated circuit apparatus **110** outputs the reception signals of the channels CH1, CH3, CH5 and CH7 to the analog front end circuit **550** via the switch elements SW1 to SW4 of the integrated circuit apparatus **110**. The multiplexer **126** of the integrated circuit apparatus **120** outputs the reception signals of the channels CH2, CH4, CH6 and CH8 to the analog front end circuit **550** via the switch elements SW1 to SW4 of the integrated circuit apparatus **120**.

[0154] In the next scanning period T2, the ultrasonic beam is shifted one channel, and transmission and reception are performed using the channels CH2 to CH9. That is, the transmission circuits TX1 to TX4 of the integrated circuit apparatus **120** output the odd-numbered pulse signals P1, P3, P5 and P7, and the multiplexer **126** outputs the pulse signals P1, P3, P5 and P7 to the channels CH2, CH4, CH6 and CH8. Also, the transmission circuits TX1 to TX4 of the integrated circuit apparatus **110** output the even-numbered pulse signals P2, P4, P6 and P8, and the multiplexer **116** outputs the pulse signals P2, P4, P6 and P8 to the channels CH3, CH5, CH7 and CH9.

[0155] At the time of reception, the multiplexer **126** of the integrated circuit apparatus **120** outputs the reception signals of the channels CH2, CH4, CH6 and CH8 to the analog front end circuit **550** via the switch elements SW1 to SW4 of the integrated circuit apparatus **120**. The multiplexer **116** of the integrated circuit apparatus **110** outputs the reception signals of the channels CH3, CH5, CH7 and CH9 to the analog front end circuit **550** via the switch elements SW1 to SW4 of the integrated circuit apparatus **110**.

[0156] In the subsequent scanning periods T3, T4, . . . , multiplexer **116** shifts the ultrasonic beam one channel at a time, and performs similar transmission/reception control.

[0157] Note that, in the present embodiment, the scanning operation is not limited to linear scanning, and sector scan-

ning (phase scanning) may be performed, for example. In the case of performing sector scanning, the transmission circuits TX1 to TX64 output pulse signals at the time of transmission, and the switch elements SW1 to SW64 are turned ON at the time of reception.

[0158] Also, although a configuration having transmission circuits and switch elements for 64 channels (half of the 128 channels of the element chip **200**) has been described as an example with FIG. 14, the present embodiment is not limited thereto. For example, in the case of performing linear scanning, a configuration having transmission circuits and switch elements for 4 channels (half of the 8 channels that output one ultrasonic beam) may be adopted.

[0159] In this way, with the ultrasonic measurement apparatus of the present embodiment, the number of transmission circuits and switch elements (and the number of terminals corresponding thereto) can be constituted in various combinations, according to the scanning mode, the number of drive channels, the number of reception channels, and the like.

[0160] Also, in the present embodiment, a configuration in which the multiplexers **116** and **126** are omitted may be adopted. In this case, when performing linear scanning, the transmission circuit that outputs a transmission signal is changed over sequentially every scanning period, similarly to the transmission operation described with FIG. 9. At the time of reception, the switch elements SW1 to SW4 of the integrated circuit apparatus **110** and the switch elements SW1 to SW4 of the integrated circuit apparatus **120** allow the reception signals of the channels CH1 to CH8 to pass in the scanning period T1. In the next scanning period T2, the switch elements SW1 to SW4 of the integrated circuit apparatus **120** and the switch elements SW2 to SW5 of the integrated circuit apparatus **110** allow the reception signals of the channels CH2 to CH9 to pass. In this way, the switch element that is ON is changed over sequentially.

## 13. Second Layout Configuration of Integrated Circuit Apparatus

[0161] FIG. 15 shows a second exemplary layout configuration of the integrated circuit apparatus **110**. Although the integrated circuit apparatus **110** will be given hereinafter as an example, the integrated circuit apparatus **120** can also be constituted similarly. The integrated circuit apparatus **110** includes multiplexers MUX1 to MUX64, transmission circuits TX1 to TX64, switch elements SW1 to SW64, and control circuits CTS1 and CTS2. Note that the multiplexers MUX1 to MUX64 correspond to the multiplexer **116** in FIG. 14, and the control circuits CTS1 and CTS2 correspond to the control circuit **114** in FIG. 14.

[0162] The multiplexers MUX1 to MUX64 are arrayed along the first long side HL1 of the integrated circuit apparatus **110**. The multiplexers MUX may be arranged in cells as shown in FIG. 15, or may be formed as one circuit block. The multiplexers MUX, in the case of being formed as one circuit block, are arranged such that the long side of the circuit block lies along the first long side HL1. By arranging the multiplexers in this way, the multiplexers MUX1 to MUX64 can be arranged in close proximity corresponding to the transmission/reception terminals TT1 to TT64, enabling an efficient layout to be realized.

[0163] The switch elements SW1 to SW64 are arrayed along the second long side HL2 of the integrated circuit apparatus **110**. The reception signal output terminals TR1 to TR64 are arrayed along the second long side HL2. The switch

elements SW1 to SW64 are arranged in cells as shown in FIG. 15. Since the switch elements SW1 to SW64 can be arranged in close proximity corresponding to the reception signal output terminals TR1 to TR64, an efficient layout can be realized.

[0164] One end of the reception signal lines LR1, LR3, . . . , LR127 is connected to the reception signal output terminals TR1 to TR64. The other end of reception signal lines LR1, LR3, . . . , LR127 is connected to the channel terminals XA1, XA3, . . . , XA127. The reception signals from the switch elements SW1 to SW64 are output to the analog front end circuit 550 from the channel terminals XA1, XA3, . . . , XA127 via reception signal lines LR1, LR3, . . . , LR127. The reception signal lines LR1, LR3, . . . , LR127 are wired in the slice direction DL.

[0165] The transmission circuits TX1 to TX64 are arranged in the long-side direction, between the multiplexers MUX1 to MUX64 and the switch elements SW1 to SW64. The transmission circuits TX1 to TX64 are arranged in cells as shown in FIG. 15.

[0166] The control circuit CTS1 is arranged on the first short side HS1 side of the integrated circuit apparatus 110, and the control circuit CTS2 is arranged on the second short side HS2 side of the integrated circuit apparatus 110. By arranging the control circuits CTS1 and CTS2 on the short sides in this way, the control terminals can be arranged on the short side, and the short sides can be utilized effectively while maintaining the long narrow form in the long-side direction.

[0167] Note that although, in the above embodiment, the cases where the integrated circuit apparatuses 110 and 120 perform only transmission and perform both transmission and reception were described as examples, the present embodiment is not limited thereto, and the integrated circuit apparatuses 110 and 120 need only perform at least one of transmission and reception. For example, the integrated circuit apparatus 110 may perform only transmission and the integrated circuit apparatus 120 may perform only reception. In this case, transmission is performed with the 64 odd-numbered channels, and reception is performed with the 64 even-numbered channels. Analog front end circuits such as reception signal amplification circuits, A/D conversion circuits or the like, for example, are envisaged as the reception circuits that are integrated in the integrated circuit apparatus 120.

#### 14. Exemplary Modified Configurations of the Channels

[0168] Although, in FIGS. 5A and 5B, the case where ultrasonic transducer elements are connected in parallel between the channel terminals XAi and the common terminals XCi was described as an example, the present embodiment is not limited thereto.

[0169] A first exemplary modified configuration of the channels CHi is shown in FIG. 16. Each channel CHi includes element groups EG1 to EGm (where m is a natural number such that  $m \geq 2$ ) that are connected in parallel between the signal electrode line LXi and the common electrode line LCi. Note that although the case where  $m=4$  will be described hereinafter as an example, the present embodiment is not limited thereto.

[0170] Each element group of the element groups EG1 to EG4 has j ultrasonic transducer elements 10 (where j is a natural number such that  $j \geq 2$ ) connected in series. Note that although the case where  $j=3$  will be described hereinafter as an example, the present embodiment is not limited thereto.

Specifically, an element group EGt (where t is a natural number such that  $t \leq m$ ) has an ultrasonic transducer element UEt1 that is provided between the signal electrode line LXi and a node NAT1, an ultrasonic transducer element UEt2 that is provided between the node NAT1 and a node NAT2, and an ultrasonic transducer element UEt3 that is provided between the node NAT2 and the common electrode line LCi.

[0171] The ultrasonic transducer elements UEt1 to UEt3 of each element group EGt are arranged in the scan direction DS, and the element groups EG1 to EG4 are arranged in the slice direction DL. Specifically, the sth ultrasonic transducer elements UE1s, UE2s, UE3s and UE4s (where s is a natural number such that  $s \leq j$ ) of the element groups EG1 to EG4 are arranged in the slice direction DL.

[0172] According to the above first modification, each channel CHi (or CHi+1) has the 1st to mth element groups EG1 to EG4 (where  $m=4$ ; m can be a natural number of 2 or more). The plurality of ultrasonic transducer elements that are included in each of the 1st to mth element groups EG1 to EG4 are electrically connected in series within the element group. The 1st to mth element groups EG1 to EG4 are electrically connected in parallel.

[0173] According to this configuration, because a plurality of ultrasonic transducer elements are connected in series between the terminals XAi and XCi in each element group, the amplitudes of the reception voltages of the plurality of ultrasonic transducer elements are added together, enabling reception sensitivity to be improved. Also, transmission sound pressure can be increased by connecting the element groups EG1 to EG4 in parallel. An increase in transmission sound pressure can thereby be achieved together with an improvement in reception sensitivity, enabling minute echoes from deep in the human body to be received with a high S/N, while suppressing the influence of transmitted ultrasonic waves on the human body.

[0174] A second exemplary modified configuration of the channels CHi is shown in FIG. 17. Each channel CHi includes the element groups EG1 to EGm (where m is a natural number such that  $m \geq 2$ ) which are connected in series between the signal electrode line LXi and the common electrode line LCi. Note that although the case where  $m=3$  will be described hereinafter as an example, the present embodiment is not limited thereto.

[0175] Each element group of the element groups EG1 to EG3 has j ultrasonic transducer elements 10 (where j is a natural number such that  $j \geq 2$ ) connected in parallel. Note that although the case where  $j=4$  will be described hereinafter as an example, the present embodiment is not limited thereto. Specifically, the element group EG1 has ultrasonic transducer elements UE11 to UE14 that are connected in parallel between the signal electrode line LXi and a node NA1, the element group EG2 has ultrasonic transducer elements UE21 to UE24 that are connected in parallel between the node NA1 and a node NA2, and the element group EG3 has ultrasonic transducer elements UE31 to UE34 that are connected in parallel between the node NA2 and the common electrode line LCi.

[0176] The ultrasonic transducer elements UE11 to UE14, UE21 to UE24, and UE31 to UE34 of the respective element groups are arranged in the scan direction DS, and the element groups EG1 to EG3 are arranged in the slice direction DL. Specifically, ultrasonic transducer elements UE1s, UE2s and UE3s (where s is a natural number such that  $s \geq 4-j$ ) are arranged in the slice direction DL.

[0177] According to the above second modification, each channel  $CHI$  (or  $CHI+1$ ) has 1st to  $m$ th element groups  $EG1$  to  $EG3$  (where  $m=3$ ;  $m$  can be a natural number of 2 or more). The plurality of ultrasonic transducer elements included in each of the 1st to  $m$ th element groups  $EG1$  to  $EG3$  are electrically connected in parallel within the element group. The 1st to  $m$ th element groups  $EG1$  to  $EG3$  are electrically connected in series.

[0178] According to this configuration, because the element groups  $EG1$  to  $EG3$  are connected in series between the terminals  $XAi$  and  $XCi$ , the amplitudes of the reception voltages of the element groups  $EG1$  to  $EG3$  are added together, enabling reception sensitivity to be improved. Also, transmission sound pressure can be increased by connecting the ultrasonic transducer elements of each element group in parallel. An increase in transmission sound pressure can thereby be achieved together with an improvement in reception sensitivity, enabling minute echoes from deep in the human body to be received with a high S/N, while suppressing the influence of transmitted ultrasonic waves on the human body.

#### 15. Head Unit

[0179] FIG. 18 shows an exemplary configuration of a head unit 220 in which the ultrasonic measurement apparatus of the present embodiment is installed. The head unit 220 shown in FIG. 18 includes the element chip 200, a connection part 210, and a supporting member 250.

[0180] The element chip 200 corresponds to the ultrasonic transducer device described with FIG. 4. The element chip 200 includes the ultrasonic transducer element array 100, a first chip terminal group  $XG1$  (odd-numbered channel terminals  $XAi$ , common terminals  $XCi$ ), and a second chip terminal group  $XG2$  (even-numbered channel terminals  $XAi+1$ , common terminals  $XCi+1$ ). The integrated circuit apparatuses 110 and 120 are flip chip mounted on the element chip 200. The element chip 200 is electrically connected to a processing apparatus (for example, processing apparatus 330 in FIG. 21) that is included in the probe body via the connection part 210.

[0181] The connection part 210 electrically connects the probe body and the head unit 220, and has connectors 421 and 422 having a plurality of connection terminals, and flexible substrates 130 and 140 on which the connectors 421 and 422 are provided. A first wiring group that connects the first chip terminal group  $XG1$  and the terminal group of the connector 421 that are provided on a first side of the element chip 200 is formed on the flexible substrate 130. A second wiring group that connects the second chip terminal group  $XG2$  and the terminal group of the connector 422 that are provided on a second side of the element chip 200 is formed on the flexible substrate 140.

[0182] Note that the connection part 210 is not limited to the configuration shown in FIG. 18. For example, a first connection terminal group may be provided on the flexible substrate 130, instead of the connector 421. Also, a second connection terminal group may be provided on the flexible substrate 140, instead of the connector 422.

[0183] By providing the connection part 210, the probe body and the head unit 220 can be electrically connected, and the head unit 220 can be configured to be detachable from the probe body.

[0184] The supporting member 250 is a member that supports the element chip 200, and, as will be discussed later, a plurality of connection terminals are provided on a first sur-

face side of the supporting member 250, and the element chip 200 is supported at a second surface side that is the opposite surface to the first surface of the supporting member 250. Note that specific structures of the element chip 200, the connection part 210, and the supporting member 250 will be discussed later.

[0185] A detailed exemplary configuration of the head unit 220 is shown in FIGS. 19A to 19C. FIG. 19A shows a second surface  $SF2$  side of the supporting member 250, FIG. 19B shows a first surface  $SF1$  side of the supporting member 250, and FIG. 19C shows the lateral surface side of the supporting member 250.

[0186] The connectors 421 and 422 are provided on the first surface  $SF1$  side of the supporting member 250. Connectors 421 and 422 can be detachably attached to corresponding connectors on the probe body.

[0187] The element chip 200 is supported on the second surface  $SF2$  side, which is the opposite surface to the first surface  $SF1$  of the supporting member 250. The other end of the flexible substrates 130 and 140 is connected to the terminals of the element chip 200. Fixing members 260 are provided on each corner portion of the supporting member 250, and are used for fixing the head unit 220 to the probe casing.

[0188] As shown in FIG. 19C, a protective member 270 (protective film) that protects the element chip 200 is provided on the surface of the element chip 200 (surface on which the piezoelectric layer 30 is formed in FIG. 3B). The integrated circuit apparatuses 110 and 120, along with the surface of the element chip 200, are covered by the protective member 270.

#### 16. Ultrasonic Probe

[0189] An exemplary configuration of an ultrasonic probe 300 to which the above head unit 220 is applied is shown in FIGS. 20A and 20B. FIG. 20A shows the case where a probe body 320 is mounted on a probe head 310, and FIG. 20B shows the case where the probe head 310 is removed from the probe body 320.

[0190] The probe head 310 includes a head unit 220 and a probe casing 240 storing the head unit 220 and a contact member 230 that contacts the sample. The element chip 200 is provided between the contact member 230 and the supporting member 250.

[0191] The probe body 320 includes a processing apparatus 330 and a connector 426 on the probe body side. The processing apparatus 330 includes a reception part 335 (analog front end part) and a transmission/reception control part 334. The reception part 335 performs reception processing of ultrasonic echo signals (reception signals) from the ultrasonic transducer elements. The transmission/reception control part 334 performs control of the integrated circuit apparatuses 110 and 120 and the reception part 335. The connector 426 on the probe body side is connected to a connector 425 on the head unit side. The probe body 320 is connected to the main body of an electronic device (for example, ultrasonic imaging apparatus) by a cable 350.

[0192] Although the head unit 220 is stored in the probe casing 240, the head unit 220 can be removed from the probe casing 240. This enables only the head unit 220 to be replaced. Alternatively, the head unit 220 can also be replaced in a state of being stored in the probe casing 240, that is, along with the probe head 310.

## 17. Ultrasonic imaging Apparatus

[0193] FIG. 21 shows an exemplary configuration of an ultrasonic imaging apparatus. The ultrasonic imaging apparatus includes the ultrasonic probe 300 and an electronic device main body 400. The ultrasonic probe 300 includes the ultrasonic head unit 220 and the processing apparatus 330. The electronic device main body 400 includes a control part 410, a processing part 420, a user interface part 430, and a display part 440.

[0194] The processing apparatus 330 includes the transmission/reception control part 334 and the reception part 335 (analog front end part). The ultrasonic head unit 220 includes the element chip 200 (ultrasonic transducer element), an integrated circuit apparatus 340 mounted on the element chip 200, and the connection part 210 (connector part) which connects the element chip 200 to a circuit board (for example, rigid board). The transmission/reception control part 334 and the reception part 335 are mounted on the circuit board. The integrated circuit apparatus 340 includes a transmission part 332. Note that the integrated circuit apparatus 340 corresponds to the integrated circuit apparatuses 110 and 120.

[0195] In the case of transmitting ultrasonic waves, the transmission/reception control part 334 issues a transmission instruction to the transmission part 332, and the transmission part 332 amplifies a drive signal to the high voltage after receiving the transmission instruction, and outputs a drive voltage. The reception part 335 has a limiter circuit which is not illustrated, and the limiter circuit blocks the drive voltage. In the case of receiving a reflected wave of ultrasonic waves, the reception part 335 receives the signal of the reflected wave detected by the element chip 200. The reception part 335 performs processing on the signal of the reflected waves (for example, amplification, A/D conversion, etc.), based on a reception instruction from the transmission/reception control part 334, and transmits the processed signal to the processing part 420. The processing part 420 converts the signal into a video signal, and displays the video signal on the display part 440.

[0196] Note that the ultrasonic measurement apparatus of the present embodiment is applicable not only to an ultrasonic imaging apparatus for medical use such as described above but to various electronic devices. For example, devices such as diagnostic devices that perform non-destructive examination of the inside of buildings or the like, and user interface devices that detect the motion of a user's finger through reflection of ultrasonic waves are envisaged as electronic devices to which the ultrasonic transducer device can be applied.

[0197] Note that although the present embodiment has been described in detail above, a person skilled in the art will appreciate that numerous modifications can be made without substantially departing from the novel matter and effects of the invention. Accordingly, all such modifications are within the scope of the invention. For example, terms that appear in the description or drawings at least once together with other broader or synonymous terms can be replaced by those other terms at any place within the description or drawings. All combinations of the present embodiment and the modifications are also within the scope of the invention. Also, the configurations and operations of the integrated circuit apparatus, the ultrasonic transducer element, the ultrasonic transducer device, the ultrasonic head unit, the ultrasonic probe and the ultrasonic imaging apparatus, the method of mounting the integrated circuit apparatus, the method of scanning

an ultrasonic beam, and the like are not limited to those described in this embodiment, and various modifications can be made.

[0198] The entire disclosure of Japanese Patent Application No. 2013-155346, filed Jul. 26, 2013 is expressly incorporated by reference herein.

What is claimed is:

1. An ultrasonic measuring apparatus comprising:
  - a first integrated circuit apparatus that is mounted on the substrate, at one edge portion of the ultrasonic transducer element array in a first direction, such that a long-side direction coincides with a second direction that intersects the first direction, and performs at least one of signal transmission to the first channel group and signal reception from the first channel group; and
  - a second integrated circuit apparatus that is mounted on the substrate, at the other edge portion of the ultrasonic transducer element array in the first direction, such that the long-side direction coincides with the second direction, and performs at least one of signal transmission to the second channel group and signal reception from the second channel group,
 wherein, in the ultrasonic transducer element array, the first group of channels and the second group of channels are arranged alternately every channel in the second direction.
2. The ultrasonic measurement apparatus according to claim 1,
  - wherein, in a first scanning period, the first integrated circuit apparatus outputs odd-numbered pulse signals, among 1st to kth pulse signals (where k is a natural number of 2 or more) to channels belonging to the first channel group, among 1st to kth channels, and the second integrated circuit apparatus outputs even-numbered pulse signals, among the 1st to kth pulse signals, to channels belonging to the second channel group, among the 1st to kth channels, and
  - in a second scanning period subsequent to the first scanning period, the second integrated circuit apparatus outputs the odd-numbered pulse signals to channels belonging to the second channel group, among 2nd to k+1th channels, and the first integrated circuit apparatus outputs the even-numbered pulse signals to channels belonging to the first channel group, among the 2nd to k+1th channels.
3. The ultrasonic measurement apparatus according to claim 2, comprising:
  - a processing part that outputs a control command for controlling transmission in the first scanning period and the second scanning period to the first integrated circuit apparatus and the second integrated circuit apparatus, wherein the first integrated circuit apparatus and the second integrated circuit apparatus each include:
    - a plurality of transmission circuits that transmit pulse signals; and
    - a control circuit that controls the plurality of transmission circuits based on the control command.
4. The ultrasonic measurement apparatus according to claim 1, comprising:

- a processing part that performs reception processing of reception signals,
- wherein the processing part performs the reception processing, based on the reception signals from the first channel group and the reception signals from the second channel group obtained by the first integrated circuit apparatus and the second integrated circuit apparatus transmitting signals.
5. The ultrasonic measurement apparatus according to claim 1,
- wherein, in the ultrasonic transducer element array, 1st to Nth channels (where N is a natural number of 2 or more) are arranged in the second direction,
- the first channel group consists of odd-numbered channels, among the 1st to Nth channels, and
- the second channel group consists of even-numbered channels, among the 1st to Nth channels.
6. The ultrasonic measurement apparatus according to claim 1,
- wherein the first integrated circuit apparatus has a plurality of transmission circuits that are arranged in the second direction and transmit a signal to the first channel group, and
- the second integrated circuit apparatus has a plurality of transmission circuits that are arranged in the second direction and transmit a signal to the second channel group.
7. The ultrasonic measurement apparatus according to claim 1,
- wherein the first integrated circuit apparatus and second integrated circuit apparatus are flip chip mounted on the substrate.
8. The ultrasonic measurement apparatus according to claim 1,
- wherein each channel of the first channel group and the second channel group has 1st to mth element groups (where m is a natural number of 2 or more),
- the plurality of ultrasonic transducer elements included in each of the 1st to mth element groups are electrically connected in parallel within the element group, and
- the 1st to mth element groups are electrically connected in series.
9. The ultrasonic measurement apparatus according to claim 1,
- wherein each channel of the first channel group and the second channel group has 1st to mth element groups (where m is a natural number of 2 or more),
- the plurality of ultrasonic transducer elements included in each of the 1st to mth element groups are electrically connected in series within the element group, and
- the 1st to mth element groups are electrically connected in parallel.
10. The ultrasonic measurement apparatus according to claim 1,
- wherein the substrate has a plurality of openings arranged in an array,
- the ultrasonic transducer element array has an ultrasonic transducer element for each of the plurality of openings,
- the ultrasonic transducer elements each include:
- a vibration film that closes a corresponding opening among the plurality of openings; and
- a piezoelectric element part that is provided on the vibration film, and
- the piezoelectric element part includes:
- a lower electrode that is provided on the vibration film;
- a piezoelectric layer that is provided so as to cover at least a portion of the lower electrode; and
- an upper electrode that is provided so as to cover at least a portion of the piezoelectric layer.
11. An ultrasonic head unit comprising the ultrasonic measurement apparatus according to claim 1.
12. An ultrasonic probe comprising the ultrasonic measurement apparatus according to claim 1.
13. An ultrasonic imaging apparatus comprising:
- the ultrasonic probe according to claim 12; and
- a display part that displays image data for display.

\* \* \* \* \*

专利名称(译)	超声波测量装置，超声波头单元，超声波探头和超声波成像装置		
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摘要(译)

一种超声波测量装置，包括：超声波换能器装置，具有基板；超声波换能器元件阵列，具有设置在基板上的第一通道组和第二通道组；第一集成电路装置，安装在基板上，一个超声换能器元件阵列的边缘部分在第一方向上，使得长边方向与与第一方向交叉的第二方向一致，并且执行到第一通道组的信号传输和从第一通道组的信号接收中的至少一个。通道组，以及安装在基板上的第二集成电路装置，在第一方向上的超声换能器元件阵列的另一边缘部分处，使得长边方向与第二方向一致，并执行至少一个信号传输到第二信道组和从第二信道组接收信号。在超声换能器元件阵列中，第一组通道和第二组通道在第二方向上每个通道交替排列。

