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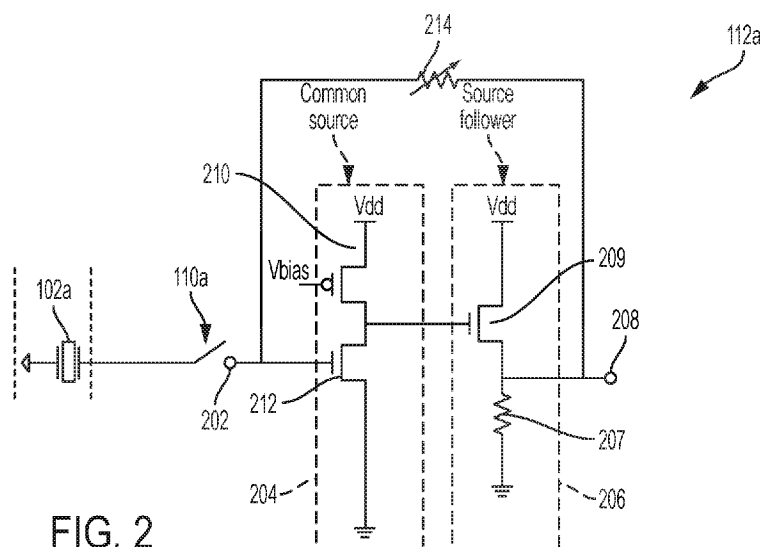


FIG. 2

(57) Abstract: An ultrasound circuit comprising a single-ended trans-impedance amplifier (TIA) is described. The TIA is coupled to an ultrasonic transducer to amplify an electrical signal generated by the ultrasonic transducer in response to receiving an ultrasound signal. The TIA is followed by further processing circuitry configured to filter, amplify, and digitize the signal produced by the TIA.



SINGLE-ENDED TRANS-IMPEDANCE AMPLIFIER (TIA) FOR ULTRASOUND DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This Application claims the benefit under 35 USC §119(e) of U.S. Provisional Patent Application Serial No. 62/522,606, filed June 20, 2017 under Attorney Docket No. B1348.70047US00, and entitled "SINGLE-ENDED TRANS-IMPEDANCE AMPLIFIER (TIA) FOR ULTRASOUND DEVICE," which is hereby incorporated herein by reference in its entirety.

BACKGROUND

Field

[0002] The present application relates to ultrasound devices having an amplifier for amplifying received ultrasound signals.

Related Art

[0003] Ultrasound probes often include one or more ultrasound sensors which sense ultrasound signals and produce corresponding electrical signals. The electrical signals are processed in the analog or digital domain. Sometimes, ultrasound images are generated from the processed electrical signals.

BRIEF SUMMARY

[0004] According to an aspect of the present application, an ultrasound apparatus is provided, comprising an ultrasound sensor and a single-ended trans-impedance amplifier (TIA) coupled to the ultrasound sensor and configured to receive and amplify an output signal from the ultrasound sensor.

[0005] According to an aspect of the present application, an ultrasound apparatus is provided, comprising an ultrasonic transducer, and a single-ended trans-impedance amplifier (TIA) having an input terminal coupled to the ultrasonic transducer and configured to receive and amplify an analog electrical signal from the ultrasonic transducer.

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[0006] According to an aspect of the present application, an ultrasound circuit is provided, comprising an ultrasonic transducer, and a plurality of analog processing stages coupled to an output of the ultrasonic transducer. The plurality of analog processing stages includes one analog processing stage configured to exhibit a greater voltage swing than other analog processing stages of the plurality of analog processing stages.

[0007] According to an aspect of the present application, an ultrasound circuit is provided, comprising an ultrasonic transducer, an amplifier having an input terminal coupled to the ultrasonic transducer, and a time gain compensation (TGC) circuit. The amplifier is electrically coupled between the ultrasonic transducer and the TGC circuit. The amplifier is configured to exhibit a first voltage swing and the TGC circuit is configured to exhibit a second voltage swing greater than the first voltage swing.

BRIEF DESCRIPTION OF DRAWINGS

[0008] Various aspects and embodiments of the application will be described with reference to the following figures. It should be appreciated that the figures are not necessarily drawn to scale. Items appearing in multiple figures are indicated by the same reference number in all the figures in which they appear.

[0009] FIG. 1 is a block diagram of an ultrasound device including an amplifier for amplifying an ultrasound signal, according to a non-limiting embodiment of the present application.

[0010] FIG. 2 illustrates the amplifier of FIG. 1 in greater detail, coupled to the ultrasonic transducer of FIG. 1, according to a non-limiting embodiment of the present application.

[0011] FIG. 3 illustrates an ultrasound signal receive circuitry chain including a single-ended TIA and a plurality of analog signal processing stages following the TIA, with voltage swings of the various stages illustrated, according to a non-limiting embodiment of the present application.

[0012] FIG. 4 illustrates an analog-to-digital converter (ADC) driver having a super source follower configuration, according to a non-limiting embodiment of the present application.

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[0013] FIG. 5 illustrates a non-limiting example of a single-ended TIA with alternating current (AC) coupling between a common source input stage and a source follower.

[0014] FIG. 6 illustrates a non-limiting example of a single-ended TIA with a bleeder circuit coupling a common source input stage to a source.

[0015] FIG. 7 illustrates a non-limiting example of a single-ended TIA having backgate voltage control of an input transistor.

DETAILED DESCRIPTION

[0016] Aspects of the present application relate to amplification circuitry for an ultrasound device. An ultrasound device may include one or more ultrasonic transducers configured to receive ultrasound signals and produce electrical output signals. Thus, the ultrasonic transducers may be operated as ultrasound sensors. The ultrasound device may include one or more amplifiers for amplifying the electrical output signals. In some embodiments, the amplifier(s) may be a single-ended trans-impedance amplifier (TIA).

[0017] According to an aspect of the present application, analog processing stages (alternatively referred to herein as “blocks” or “components”) may follow a single-ended TIA of an ultrasound device. The analog processing stages may perform various analog processing functions, such as filtering an electrical signal produced by the single-ended TIA. In some embodiments, the TIA and all but one of the analog processing stages have a first voltage swing, and a time gain compensation stage representing the last analog processing stage has a second voltage swing greater than the first voltage swing. Such a configuration may facilitate use of a single-ended TIA in the signal chain, which may therefore provide for lower power operation than if a differential or pseudo-differential TIA was implemented. Also, the power of the signal processing chain may be reduced because less power is consumed to maintain linearity through the signal chain.

[0018] According to an aspect of the present application, an ultrasound circuit is provided, comprising an ultrasonic transducer, a multi-stage analog processing circuit, and an analog-to-digital converter (ADC). In some embodiments, the multi-stage analog processing circuit includes a plurality of processing stages operating at a first voltage swing and a time gain compensation (TGC) stage operating at a larger voltage swing. The plurality of processing stages operating at the first voltage swing may include a single-ended TIA.

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[0019] According to an aspect of the present application, a method of processing ultrasound signals is provided. The method comprises generating an electrical signal using an ultrasonic transducer, and amplifying the electrical signal with a single-ended TIA. In some embodiments, multiple single-ended TIAs are provided, and further processing comprises averaging the signals provided by multiple single-ended TIAs and filtering the averaged signal. Amplifying the electrical signal from the ultrasonic transducer, and averaging and filtering the signal(s) from the single-ended TIA may be performed using components providing a first voltage swing. In some embodiments, the method further comprises performing time gain compensation (TGC) on the signals after averaging and filtering, and prior to converting the analog signals to digital signals with an ADC. The TGC may be performed using a TGC stage providing a second voltage swing greater than the voltage swing provided by preceding analog stages.

[0020] According to an aspect of the present application, a circuit is provided for processing ultrasound signals. The circuit may include an ultrasonic transducer which produces analog electrical signals in response to receiving an ultrasound signal, analog processing circuitry to process (e.g., amplify, filter, and compensate) the analog signals, and an ADC to convert the analog electrical signals into digital signals. An ADC driver for the ADC may include a super source follower in at least some embodiments.

[0021] The aspects and embodiments described above, as well as additional aspects and embodiments, are described further below. These aspects and/or embodiments may be used individually, all together, or in any combination of two or more, as the application is not limited in this respect.

[0022] FIG. 1 illustrates a circuit for processing received ultrasound signals, according to a non-limiting embodiment of the present application. The circuit 100 includes N ultrasonic transducers 102a...102n, wherein N is an integer. The ultrasonic transducers are sensors in some embodiments, producing electrical signals representing received ultrasound signals. The ultrasonic transducers may also transmit ultrasound signals in some embodiments. The ultrasonic transducers may be capacitive micromachined ultrasonic transducers (CMUTs) in some embodiments. The ultrasonic transducers may be piezoelectric micromachined ultrasonic transducers (PMUTs) in some embodiments. Alternative types of ultrasonic transducers may be used in other embodiments.

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[0023] The circuit 100 further comprises N circuitry channels 104a...104n. The circuitry channels may correspond to a respective ultrasonic transducer 102a...102n. For example, there may be eight ultrasonic transducers 102a...102n and eight corresponding circuitry channels 104a...104n. In some embodiments, the number of ultrasonic transducers 102a...102n may be greater than the number of circuitry channels.

[0024] The circuitry channels 104a...104n may include transmit circuitry, receive circuitry, or both. The transmit circuitry may include transmit decoders 106a...106n coupled to respective pulsers 108a...108n. The pulsers 108a...108n may control the respective ultrasonic transducers 102a...102n to emit ultrasound signals.

[0025] The receive circuitry of the circuitry channels 104a...104n may receive the (analog) electrical signals output from respective ultrasonic transducers 102a...102n. In the illustrated example, each circuitry channel 104a...104n includes a respective receive circuit 110a...110n and an amplifier 112a...112n. The receive circuit 110a...110n may be controlled to activate/deactivate readout of an electrical signal from a given ultrasonic transducer 102a...102n. An example of suitable receive circuits 110a...110n are switches. That is, in one embodiment the receive circuits are controllable switches which are switched during transmit mode to disconnect the ultrasonic transducers from the receive circuitry and during receive mode to connect the ultrasonic transducers to the receive circuitry. Alternatives to a switch may be employed to perform the same function.

[0026] The amplifiers 112a...112n may be single-ended TIAs in some embodiments, outputting amplified analog signals. As will be described further below, in some embodiments one or more—and in some embodiments all—of the amplifiers 112a-112n may include a common source subcircuit and a source follower. The use of single-ended TIAs may facilitate low power operation of the circuit 100 compared to the use of alternative amplifier designs.

[0027] The circuit 100 further comprises an averaging circuit 114, which is also referred to herein as a summer or a summing amplifier. In some embodiments, the averaging circuit 114 is a buffer or an amplifier. The averaging circuit 114 may receive output signals from one or more of the amplifiers 112a...112n and may provide an averaged output signal. The averaged output signal may be formed in part by adding or subtracting the signals from the various amplifiers 112a...112n. The averaging circuit 114 may include a variable feedback resistance. The value of the variable feedback resistance may be adjusted dynamically based upon the number of amplifiers 112a...112n from which the averaging circuit receives signals. In some

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embodiments, the variable resistance may include N resistance settings. That is, the variable resistance may have a number of resistance settings corresponding to the number of circuitry channels 104a...104n. Thus, the average output signal may also be formed in part by application of the selected resistance to the combined signal received at the input(s) of the averaging circuit 114.

[0028] The averaging circuit 114 is coupled to an auto-zero block 116, also referred to herein as a “DC block.” The auto-zero block 116 may filter the averaged signal provided by the averaging circuit 114, and thus may be considered a filter in at least some embodiments.

[0029] The auto-zero block 116 is coupled to a programmable gain amplifier 118 which includes an attenuator 120 and a fixed gain amplifier 122. The programmable gain amplifier 118 may perform time gain compensation (TGC), and thus may alternatively be referred to as a TGC stage or circuit. In performing TGC, the programmable gain amplifier 118 may increase the amplification provided during reception of an ultrasound signal by an ultrasonic transducer, thus compensating for the natural attenuation of the signal which occurs over time.

[0030] The programmable gain amplifier 118 is coupled to an ADC 126 via ADC drivers 124. In the illustrated example, the ADC drivers 124 include a first ADC driver 125a and a second ADC driver 125b. The ADC 126 digitizes the signal(s) from the averaging circuit 114.

[0031] While FIG. 1 illustrates a number of components as part of a circuit of an ultrasound device, it should be appreciated that the various aspects described herein are not limited to the exact components or configuration of components illustrated. For example, aspects of the present application relate to the amplifiers 112a...112n, and the components illustrated downstream of those amplifiers in circuit 100 are optional in some embodiments.

[0032] The components of FIG. 1 may be located on a single substrate or on different substrates. For example, as illustrated, the ultrasonic transducers 102a...102n may be on a first substrate 128a and the remaining illustrated components may be on a second substrate 128b. The first and/or second substrates may be semiconductor substrates, such as silicon substrates. In an alternative embodiment, the components of FIG. 1 may be on a single substrate. For example, the ultrasonic transducers 102a...102n and the illustrated circuitry may be monolithically integrated on the same die (e.g., a semiconductor die, such as silicon). Such integration may be facilitated by using CMUTs as the ultrasonic transducers.

[0033] According to an embodiment, the components of FIG. 1 form part of an ultrasound probe. The ultrasound probe may be handheld. In some embodiments, the

components of FIG. 1 form part of an ultrasound patch configured to be worn by a patient, or part of an ultrasound pill to be swallowed by a patient.

[0034] As previously described, aspects of the present application provide a single-ended TIA for an ultrasound device. FIG. 2 illustrates a non-limiting example of the amplifier 112a of FIG. 1 in greater detail, illustrating a single-ended configuration. The same configuration may be used for the other TIAs 112n of FIG. 1.

[0035] The amplifier 112a includes an input terminal 202 coupled to the receive circuit 110a, which is illustrated as a switch in this non-limiting embodiment. The input terminal 202 is therefore coupled to the ultrasonic transducer 102a to receive electrical signals output by the ultrasonic transducer.

[0036] The amplifier 112a further comprises a common source subcircuit 204 (referred to herein simply as a “common source”), source follower 206, feedback impedance 214, and output terminal 208. The common source 204 in turn includes a PMOS transistor 210 and NMOS transistor 212 between a power supply rail, Vdd, and ground (GND). The PMOS transistor 210 represents a non-limiting example of a current sourced, with its gate biased by a suitable bias voltage Vbias. Other forms of current sources may alternatively be implemented. The gate of the NMOS transistor 212 may correspond to the input terminal 202, configured to receive the electrical signal output by the ultrasonic transducer 102a. The source follower 206 includes a resistor 207 and NMOS transistor 209, the gate of which is coupled to the drain of NMOS transistor 212 of the common source 204. The resistor 207 is used in the illustrated non-limiting embodiments, but other forms of current sources could alternatively be implemented.

[0037] The amplifier 112a also includes a programmable feedback impedance 214, shown in this non-limiting example as a resistor. In some embodiments, the feedback impedance may comprise a resistor in parallel with a capacitor, one or both of which may be variable. The feedback impedance determines the transimpedance gain of the transimpedance amplifier, such that the input current signal may be converted into an output voltage of varying amplitude. The feedback impedance 214 may be programmed before operation, and remains static during operation. Thus, in at least some embodiments the feedback impedance may be considered a programmable static feedback impedance.

[0038] The amount of power savings realized from use of a single-ended TIA in an ultrasound signal chain like that illustrated in FIG. 1 may be significant. For example, in the circuit 100, the amplifiers 112a...112n may consume a relatively significant amount of power.

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In some embodiments, the amplifiers 112a...112n may consume more power than any other components of the circuit 100. Accordingly, reducing the power consumption of the amplifiers 112a...112n may provide a significant reduction in power of the circuit 100. The use of a single-ended TIA may reduce power consumption of the TIA stage by half or more, for a single TIA. Thus, multiplying such power savings by N TIAs may be significant compared to TIA designs which are not single-ended.

[0039] While FIG. 2 illustrates an example of a single-ended TIA in accordance with various aspects of the present application, it should be appreciated that alternative implementations are possible. For example, while FIG. 2 illustrates the use of NMOS and PMOS transistors, different transistor technology may be used (e.g., bipolar junction transistor technology). Moreover, while FIG. 2 illustrates an NMOS common source and NMOS source follower, a PMOS common source and PMOS source follower could alternatively be implemented. Also, different circuit configurations may be used other than a common source followed by a source follower. FIGs. 5-7 illustrate various non-limiting alternative configurations.

[0040] FIG. 5 illustrates a non-limiting example of a single-ended TIA with alternating current (AC) coupling between a common source input stage and a source follower. The TIA 500 is connected to the ultrasonic transducer 102a, and includes transistors 502, 504, 506, 508, 510, and 512, switches SW1, SW2, SW3, and SW4, capacitor C1, and variable feedback impedance 514.

[0041] The TIA 500 includes a common source input stage. The common source input stage comprises transistors 502, 504, 506, and 508. Transistors 504 and 506 are configured in cascode, and receive cascode bias signals V_{casN} and V_{casP} , respectively. Transistor 508 is a bias transistor configured to receive a bias voltage V_{bias1} .

[0042] The TIA 500 further comprises a source follower represented by transistor 510. A bias transistor 512 is coupled to the source follower and receives bias voltage V_{bias2} .

[0043] The TIA 500 includes AC coupling between the common source input stage and the source follower. The AC coupling is provided by switches SW2 and SW3, coupled to opposite plates of the capacitor C1. In some embodiments, the switches SW1, SW2, SW3, and SW4 are operated as follows. The switch SW1 may be a receive switch which is closed for the duration of a receive event, and opened when the ultrasound device is operating in a transmit mode. Prior to the beginning of a receive event, SW2 and SW4 are ON to pre-charge or reset the

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voltage across capacitor C1. During the receive period, and in at least some embodiments during the entire receive period encompassing the duration to receive at all target imaging depths, SW2 and SW4 are OFF and SW3 is ON, and capacitor C1 statically holds the charge from the pre-charge phase. The capacitor C1 is floating during this period and the voltage across the capacitor C1 during this period is such that $V_x = V_{dd}/2$.

[0044] The variable feedback impedance 514 may be of the same type as variable feedback impedance 214, described earlier, or any other suitable feedback impedance.

[0045] The TIA 500 may provide various benefits. For example, the source follower gate node (the node at the gate of transistor 510) does not limit the swing of the TIA. The capacitor C1 allows the gate node of the source follower to swing above V_{dd} . TIA 500 may also exhibit less noise than other two-stage operational amplifier designs.

[0046] FIG. 6 illustrates a variation on the single-ended TIA 500 of FIG. 5, lacking the AC coupling capacitor C1. The TIA 600 of FIG. 6 comprises the common source input stage and the source follower of FIG. 5, but lacks the capacitor C1 and instead includes a current bleeding circuit (also referred to herein as a “bleeder circuit”) including transistors 606 and 608, which may be considered current bleeding transistors. A feedback circuit 604 is provided to control the bleeder circuit. The feedback circuit 604 receives V_x and $V_{dd}/2$ as inputs and provides control signals V_P and V_N to the bleeder circuit to control transistors 606 and 608 as shown. In the configuration illustrated, the voltage V_x may be substantially centered at $V_{dd}/2$. It should be appreciated from FIG. 6 that an embodiment of the present application provides an ultrasound device including a signal receive circuitry chain comprising a single-ended TIA having a common source input stage coupled to a source follower by a bleeder circuit. Moreover, while FIG. 6 illustrates a bleeder circuit including two current bleeding transistors, an alternative is to use only one such transistor, 606 or 608. When only a positive or negative side current bleeding transistor is provided, the feedback circuit 604 may be simplified to provide only one of V_P or V_N .

[0047] FIG. 7 illustrates a further non-limiting example of a single-ended TIA as may be used in an ultrasound device. In the example of FIG. 7, the single-ended TIA 700 exhibits backgate control of transistor 502. The TIA 700 does not use an AC coupling capacitor or a bleeder circuit. The TIA 700 includes the common source input stage and source follower of TIAs 500 and 600. Backgate control of the input common source NMOS transistor 502 is provided.

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[0048] The backgate voltage of transistor 502 may be controlled by a positive programmable voltage to substantially maintain the backgate voltage V_{back} at a positive voltage between the supply rails, but not to exceed one diode turn-on voltage above 0V. The TIA 700 also includes a feedback circuit 702 configured to receive V_x and $V_{dd}/2$ and provide the voltage V_{back} . The construction of the backgate feedback control circuit 702 depends on whether positive or negative backgate control is being provided. When the TIA 700 is configured to provide positive backgate voltage, V_{back} may be maintained substantially above 0V in some embodiments. By contrast, when the TIA 700 is configured to provide negative backgate voltage, the circuit may include a negative power supply to provide the negative voltage or the feedback circuit 702 may include a charge pump to facilitate maintaining V_{back} below 0V. In such a situation, any suitable charge pump may be implemented. In some embodiments, an optional floating capacitor may be included to provide a voltage to the backgate, and in such embodiments the feedback circuit 702 may be disconnected during the receive period, with the backgate voltage V_{back} being provided by the floating capacitor.

[0049] It should be appreciated from FIG. 7 that an embodiment of the present application provides an ultrasound device including a signal receive circuitry chain comprising a single-ended TIA having backgate voltage control of an input transistor of the TIA.

[0050] In some embodiments, a signal receive circuitry chain of an ultrasound device may include a single-ended TIA followed by differential circuitry, such as a differential amplifier, averaging circuit, filter, or other circuitry. In such situations, the single-ended TIA may be combined with a replica circuit configured to generate a pseudo-differential input signal for downstream stages of the signal receive circuitry chain. In at least some such embodiments, the replica circuit may be substantially the same as the respective single-ended TIA but lacking a variable feedback impedance 514 and configured to produce a direct current (DC) output signal. In this manner, the TIA may produce a variable output signal corresponding to an output of the ultrasonic transducer and the replica circuit may generate a DC output, with those two outputs forming the pseudo-differential input signals to downstream differential circuitry in the signal receive circuitry chain. An exception is the circuit configuration having a bleeder circuit, for which the replica circuit still comprises the same variable feedback impedance as the single-ended TIA.

[0051] According to an aspect of the present application, an ultrasound signal receive chain includes a plurality of analog signal processing stages, in which at least two of the stages

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differ in the voltage swing they provide. In some embodiments, the stage prior to an ADC provides a different voltage swing than upstream (or preceding) analog processing stages. In some embodiments, the stage prior to the ADC provides a larger voltage swing than upstream (or preceding) stages. In this manner, power of the signal chain may be reduced, by providing a desired output voltage swing from the last stage prior to the conversion of the analog signal to a digital signal.

[0052] FIG. 3 illustrates an ultrasound signal receive circuitry chain including a single-ended TIA and a plurality of analog signal processing stages following the TIA, and may represent a generalized version of the corresponding signal processing stages of FIG. 1. The illustrated ultrasound signal receive circuitry chain includes eight TIAs 312, an averaging circuit 314, a DC block (or filter) stage 316, a time gain compensation stage 318, and an ADC driver and ADC stage 320. While eight TIAs 312 are shown, any suitable number may be included.

[0053] In the non-limiting example of FIG. 3, the illustrated analog signal processing stages provide the illustrated voltage swings. In particular, the TIAs 312, averaging circuit 314, and DC block stage 316 each provide an output voltage swing of V_1 , as indicated by the vertically indicated double-ended arrows. By contrast, the TGC stage 318 provides an output voltage swing of V_2 . In at least some embodiments, V_2 may be greater than V_1 . For example, V_2 may be between 1.5 and five times greater than V_1 , including any value and range within that range. As a non-limiting example, V_1 may be between 0.2 Volts and 0.7 Volts (e.g., 0.5 Volts), while V_2 may be between 1.5 and five times (e.g., two times, three times, or four times) greater than V_1 .

[0054] Operating the TIAs 312, averaging circuit 314, and DC block stage 316 with lower voltage swings V_1 may reduce the power consumed by those stages. Low-swing operational amplifiers (op-amps) typically consume less power than operational amplifiers with larger swings. The desired output voltage swing for the signal chain may correspond to V_2 , and thus may be provided by the TGC stage 318, which in at least some embodiments is the analog signal processing stage immediately prior to the ADC driver and ADC. Thus, in some embodiments, all but the last stage of the analog signal processing chain have a lower output voltage swing than does the last stage, allowing for power savings in the stages having the lower output voltage swing.

[0055] In some embodiments, providing a larger voltage swing V_2 with the TGC stage 318 may allow for providing lower gain from the TIAs 312, and thus conserving power with the

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TIAs 312. For example, the gain of the TIAs may be less than 100dB in some embodiments, and the gain of the TGC may be between 5dB and 30dB in some embodiments. Other gains may be implemented, as those listed are non-limiting examples.

[0056] While FIG. 3 illustrates multiple stages providing an output voltage swing V_1 , alternative embodiments provide configurations in which the stages preceding the TGC stage have non-uniform output voltage swings. For example, the TIAs 312, averaging circuit 314, and DC block stage 316 may provide different voltage swings than each other, but in at least some embodiments may all provide a lower output voltage swing than the TGC stage 318. Thus, in some embodiments, at least one analog processing stage preceding a time gain compensation stage provides a lower output voltage swing than the TGC stage.

[0057] According to an aspect of the present application, an ultrasound signal receive circuitry chain includes an ADC and an ADC driver, and the ADC driver includes a super source follower. FIG. 4 illustrates an ADC driver having a folded cascode super source follower configuration, according to a non-limiting embodiment of the present application. The ADC driver 400 may be used as the ADC driver in the circuits of FIGs. 1 and 3, among other possible implementations.

[0058] The ADC driver 400 includes an input terminal 402 configured to receive an input signal, such as the output produced by a TGC stage, such as TGC stage 318 of FIG. 3. The input terminal 402 may correspond to the gate (or control terminal) of NMOS transistor 404. The output of the ADC driver 400 may be taken from the source of transistor 404. Transistor 404 is coupled to transistor 406.

[0059] The ADC driver 400 further comprises current sources I_1 and I_2 , resistor R , capacitor C , and transistor 408. The resistor R and capacitor C may provide compensation to ensure sufficient phase margin for the loop and may have any suitable values for doing so. The cascode may be biased with a voltage V_B . The illustrated ADC driver structure may provide a relatively low output impedance by using feedback, while the folded cascode structure may allow for high output voltage swing. In this manner, the same output resistance associated with a source follower may be achieved with a relatively small bias current, while maintaining output voltage swing. Accordingly, the ADC driver may consume relatively little power compared to other configurations.

[0060] Using a super source follower as the ADC driver helps reduce the ADC driver power considerably in at least some embodiments. A super source follower reduces the output

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impedance by negative feedback rather than by increasing the current, but does so at the expense of supporting a smaller swing. The folded cascode super source follower according to the embodiments described herein exhibits the advantage of a super source follower in terms of lowering the power consumption needed to achieve a given output impedance, but also allows for a larger swing compared to a super source follower not having a folded cascade structure.

[0061] The ADC driver of FIG. 4 may be used with various types of ADCs. As an example, the illustrated ADC driver may be used with a successive approximation register (SAR) ADC. The combination of the illustrated ADC driver with a SAR ADC may provide low power operation coupled with high output voltage swing.

[0062] Having thus described several aspects and embodiments of the technology of this application, it is to be appreciated that various alterations, modifications, and improvements will readily occur to those of ordinary skill in the art. Such alterations, modifications, and improvements are intended to be within the spirit and scope of the technology described in the application. It is, therefore, to be understood that the foregoing embodiments are presented by way of example only and that, within the scope of the appended claims and equivalents thereto, inventive embodiments may be practiced otherwise than as specifically described.

[0063] As described, some aspects may be embodied as one or more methods. The acts performed as part of the method(s) may be ordered in any suitable way. Accordingly, embodiments may be constructed in which acts are performed in an order different than illustrated, which may include performing some acts simultaneously, even though shown as sequential acts in illustrative embodiments.

[0064] All definitions, as defined and used herein, should be understood to control over dictionary definitions, definitions in documents incorporated by reference, and/or ordinary meanings of the defined terms.

[0065] The phrase “and/or,” as used herein in the specification and in the claims, should be understood to mean “either or both” of the elements so conjoined, *i.e.*, elements that are conjunctively present in some cases and disjunctively present in other cases.

[0066] As used herein in the specification and in the claims, the phrase “at least one,” in reference to a list of one or more elements, should be understood to mean at least one element selected from any one or more of the elements in the list of elements, but not necessarily including at least one of each and every element specifically listed within the list of elements and not excluding any combinations of elements in the list of elements.

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[0067] As used herein, the term “between” used in a numerical context is to be inclusive unless indicated otherwise. For example, “between A and B” includes A and B unless indicated otherwise.

[0068] In the claims, as well as in the specification above, all transitional phrases such as “comprising,” “including,” “carrying,” “having,” “containing,” “involving,” “holding,” “composed of,” and the like are to be understood to be open-ended, *i.e.*, to mean including but not limited to. Only the transitional phrases “consisting of” and “consisting essentially of” shall be closed or semi-closed transitional phrases, respectively.

CLAIMS

1. An ultrasound apparatus, comprising:
an ultrasonic transducer;
a single-ended trans-impedance amplifier (TIA) having an input terminal coupled to the ultrasonic transducer and configured to receive and amplify an analog electrical signal from the ultrasonic transducer.
2. The ultrasound apparatus of claim 1, further comprising a switch coupled between the ultrasonic transducer and the input terminal of the single-ended TIA.
3. The ultrasound apparatus of claim 1, wherein the ultrasonic transducer is a first ultrasonic transducer and the single-ended TIA is a first single-ended TIA, and wherein the ultrasound apparatus comprises a plurality of ultrasonic transducers including the first ultrasonic transducer and a plurality of respective single-ended TIAs coupled to the respective ultrasonic transducers, the plurality of respective single-ended TIAs including the first single-ended TIA, wherein the ultrasound apparatus further comprises an averaging circuit having an input coupled to the plurality of respective single-ended TIAs.
4. The ultrasound apparatus of claim 3, further comprising a filter and a time gain compensation (TGC) circuit, the filter being coupled electrically between the averaging circuit and the TGC circuit.
5. The ultrasound apparatus of claim 4, further comprising an analog-to-digital converter (ADC) coupled to an output terminal of the TGC circuit.
6. The ultrasound apparatus of claim 5, further comprising an ADC driver coupled to the ADC and configured to drive the ADC, the ADC driver comprising a folded cascode super source follower.

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7. The ultrasound apparatus of claim 5, wherein the plurality of respective single-ended TIAs are configured to exhibit a first voltage swing, and wherein the TGC circuit is configured to exhibit a second voltage swing greater than the first voltage swing.
8. The ultrasound apparatus of claim 7, wherein the second voltage is between 1.5 and five times greater than the first voltage swing.
9. The ultrasound apparatus of claim 7, wherein the averaging circuit and filter are configured to exhibit a voltage swing less than the second voltage swing.
10. The ultrasound apparatus of claim 9, wherein the averaging circuit and filter are configured to exhibit the first voltage swing.
11. The ultrasound apparatus of claim 7, wherein the plurality of ultrasonic transducers, plurality of respective single-ended TIAs, filter, and TGC circuit are formed on a single substrate.
12. The ultrasound apparatus of claim 11, wherein the plurality of ultrasonic transducers are capacitive micromachined ultrasonic transducers (CMUTs).
13. The ultrasound apparatus of claim 1, wherein the single-ended TIA comprises a common source circuit coupled to a source follower.
14. An ultrasound circuit, comprising:
 - an ultrasonic transducer; and
 - a plurality of analog processing stages coupled to an output of the ultrasonic transducer and including one analog processing stage configured to exhibit a greater voltage swing than other analog processing stages of the plurality of analog processing stages.
15. The ultrasound circuit of claim 14, wherein the one analog processing stage configured to exhibit a greater voltage swing is a time gain compensation (TGC) circuit.

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16. The ultrasound circuit of claim 15, wherein the TGC circuit is the last analog processing stage before an analog-to-digital converter (ADC).
17. The ultrasound circuit of claim 14, wherein the one analog processing stage configured to exhibit a greater voltage swing is the last analog processing stage before an analog-to-digital converter (ADC).
18. The ultrasound circuit of claim 14, wherein the plurality of analog processing stages comprises a single-ended trans-impedance amplifier.
19. The ultrasound circuit of claim 14, further comprising an analog-to-digital converter (ADC) and an ADC driver coupled to a last analog processing stage of the plurality of analog processing stages, the ADC driver comprising a folded cascode super source follower.
20. An ultrasound circuit, comprising:
 - an ultrasonic transducer;
 - an amplifier having an input terminal coupled to the ultrasonic transducer; and
 - a time gain compensation (TGC) circuit, wherein the amplifier is electrically coupled between the ultrasonic transducer and the TGC circuit, and
 - wherein the amplifier is configured to exhibit a first voltage swing and the TGC circuit is configured to exhibit a second voltage swing greater than the first voltage swing.
21. The ultrasound circuit of claim 20, wherein the amplifier is a single-ended trans-impedance amplifier (TIA).
22. The ultrasound circuit of claim 21, wherein the single-ended TIA comprises a common source circuit coupled to a source follower.
23. The ultrasound circuit of claim 20, further comprising an analog-to-digital converter (ADC) driver coupled electrically downstream of the TGC, the ADC driver comprising a folded cascode super source follower.

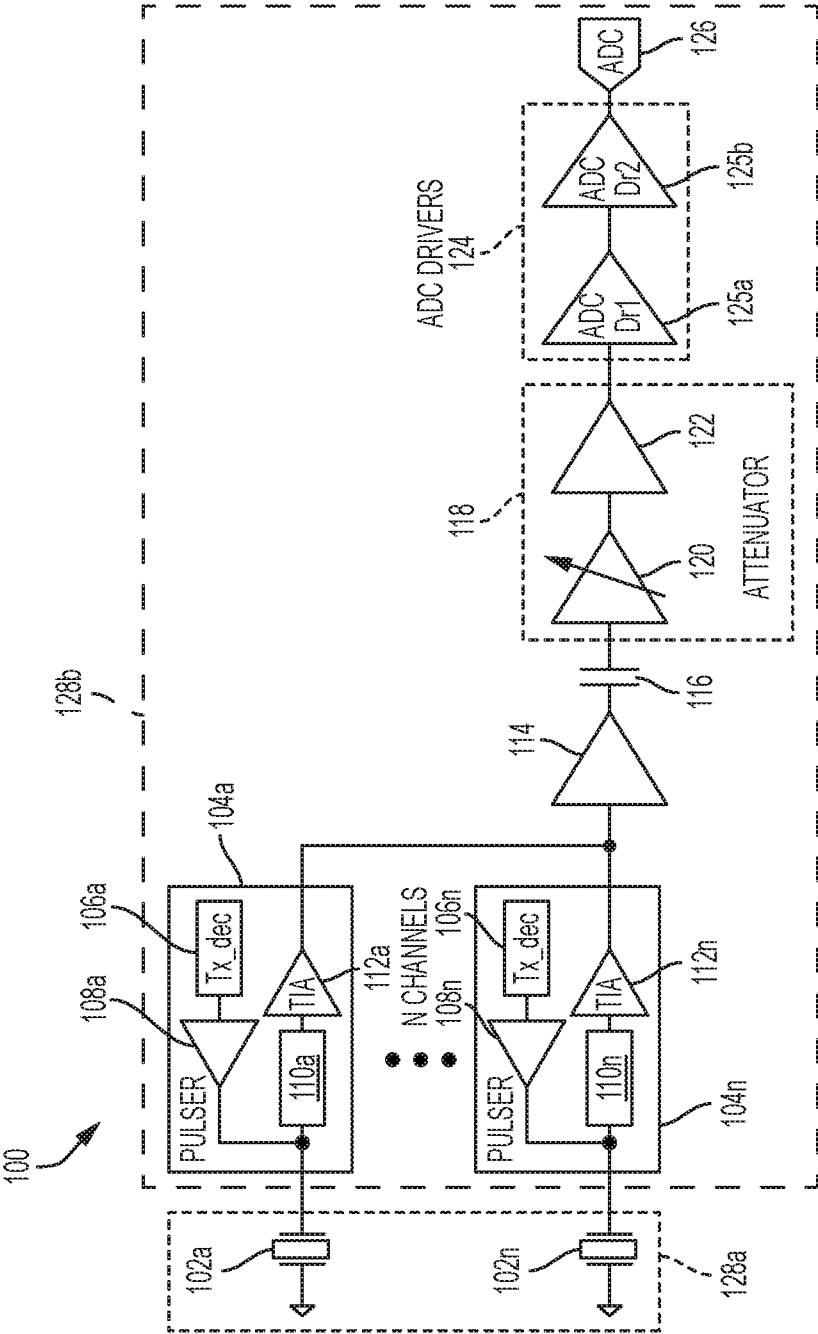


FIG. 1

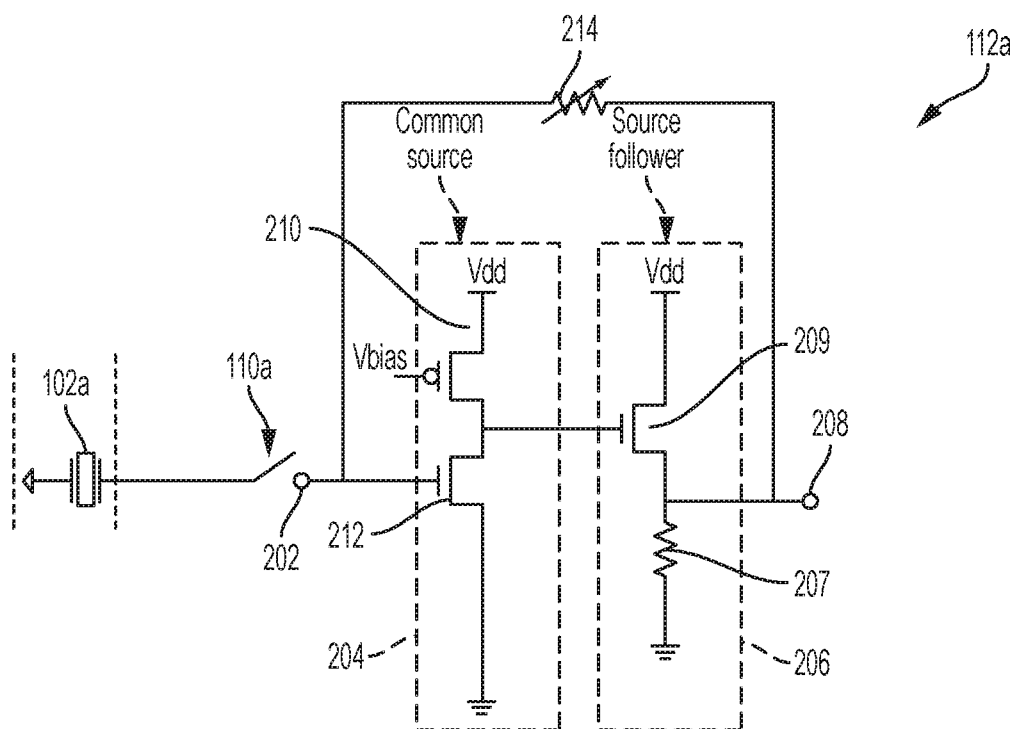


FIG. 2

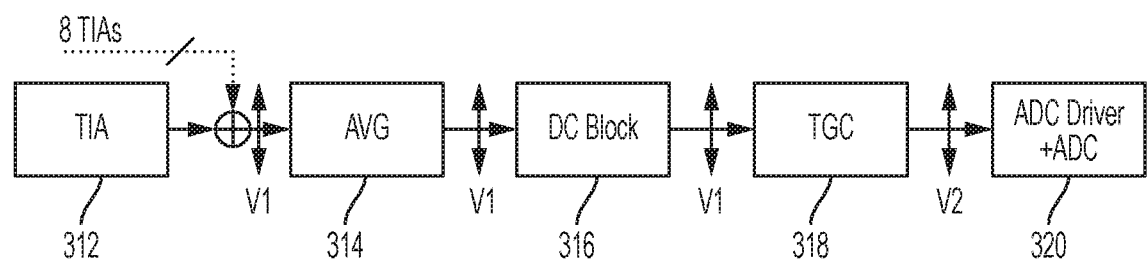


FIG. 3

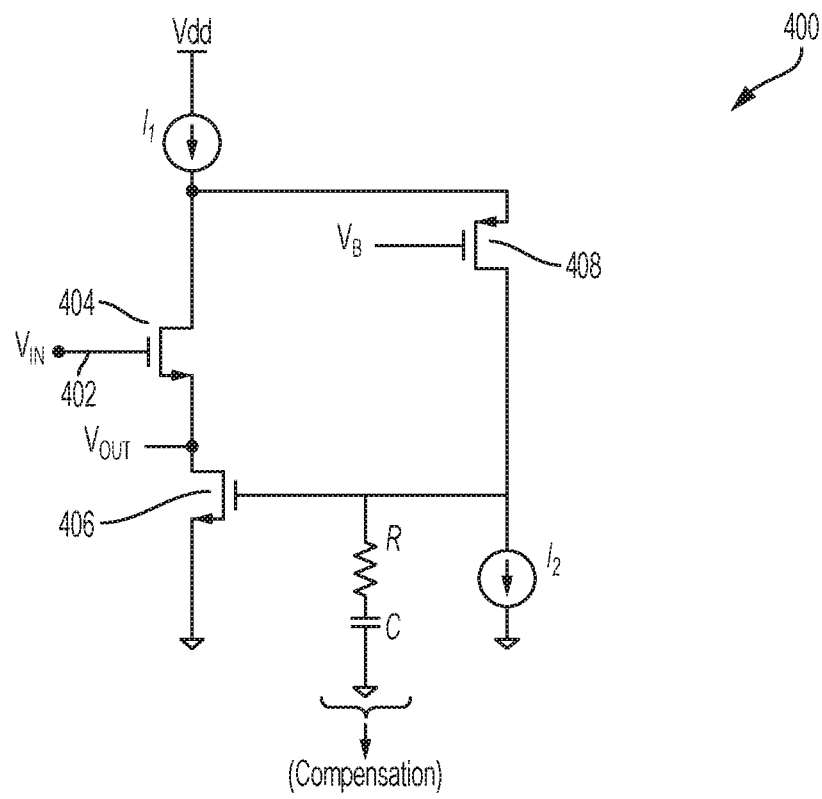


FIG. 4

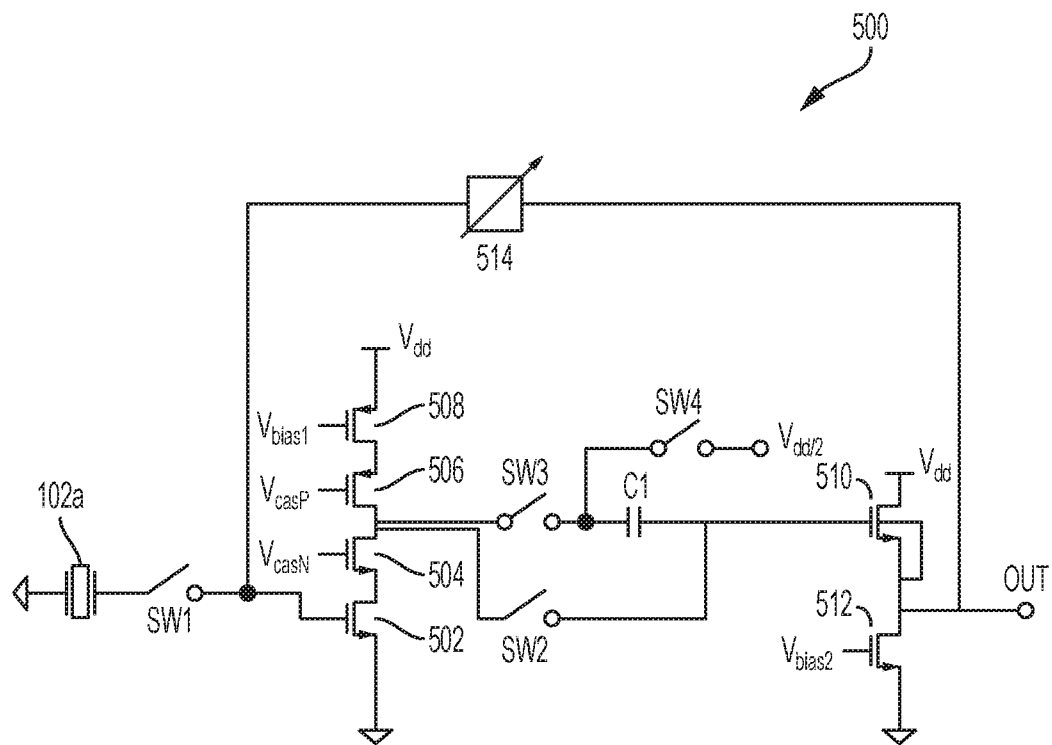


FIG. 5

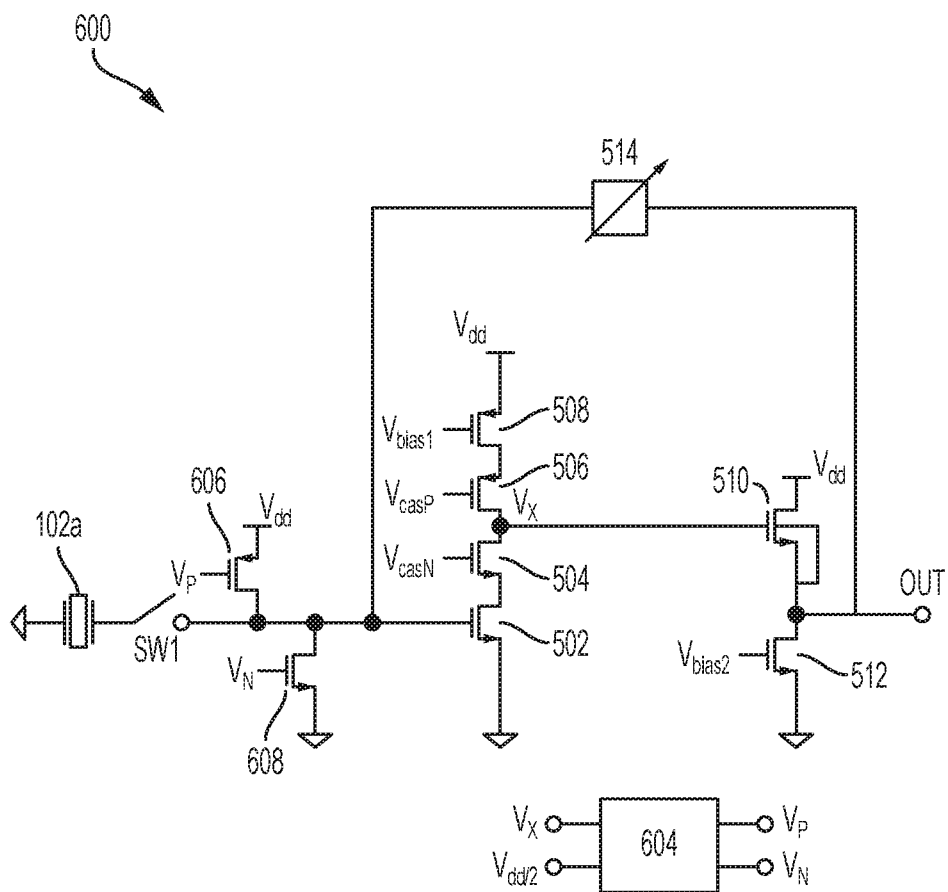


FIG. 6

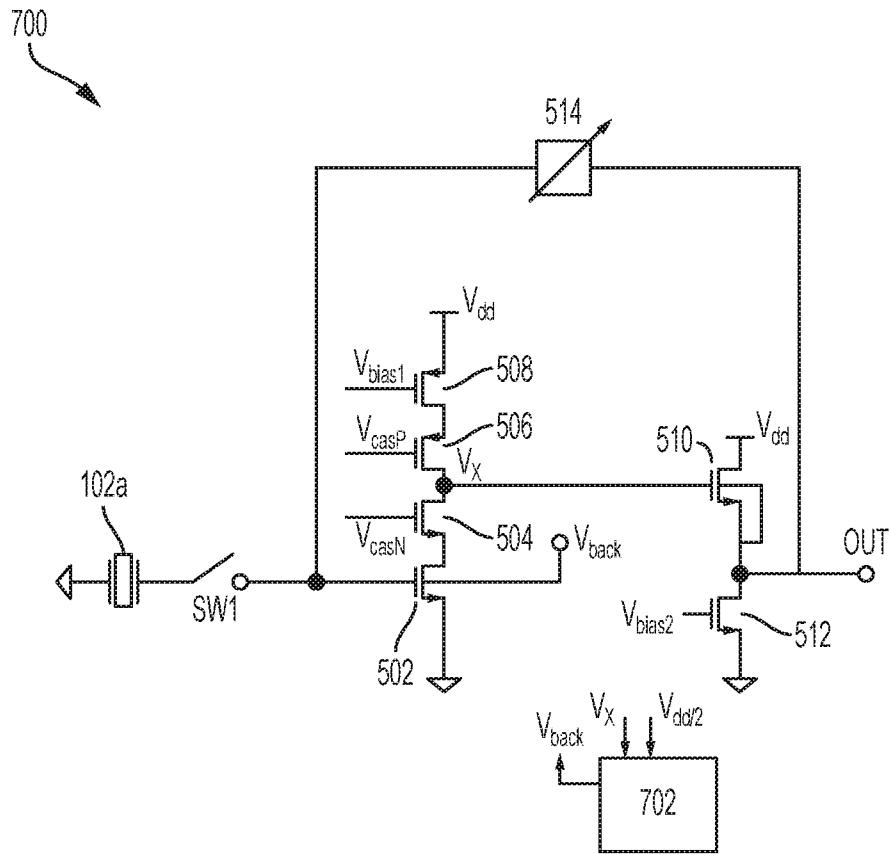


FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US18/38180

A. CLASSIFICATION OF SUBJECT MATTER

IPC - A61N 7/00; A61B 8/00; G01S 7/282 (2018.01)

CPC - G01S 7/52033, 7/282, 7/52095; A61B 8/46, 8/5215; H03F 3/45206, 3/45094

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y -- A	US 2017/0160239 A1 (BUTTERFLY NETWORK, INC.) June 8, 2017; abstract, figure 1, paragraphs [0021], [0024]-[0027]	1-3 -- 4, 5, 13, 14, 18 -- 6-12, 15-17, 19-23
Y	US 2016/0228099 A1 (KONINKLIJKE PHILIPS N.V.) August 11, 2016; figure 3, paragraphs [0014], [0015]	4, 5
Y	US 2011/0130109 A1 (OGASAWARA, Y) June 2, 2011; paragraph [0009]	13
Y -- A	US 2015/0374335 A1 (SHARP KABUSHIKI KAISHA) December 31, 2015; figure 2b, paragraph [0066]	14, 18 -- 6-12, 15-17, 19-23
A	US 6,356,152 B1 (JEZDIC, A et al.) March 12, 2002; the entire document	1-23
A	US 4,829,491 A (SAUGEON, U et al.) May 9, 1989; the entire document	1-23



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

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"O" document referring to an oral disclosure, use, exhibition or other means

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"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

09 August 2018 (09.08.2018)

Date of mailing of the international search report

06 SEP 2018

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申请号	EP2018820732	申请日	2018-06-19
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申请(专利权)人(译)	蝶形网络，INC.		
当前申请(专利权)人(译)	蝶形网络，INC.		
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发明人	SINGH, AMANDEEP CHEN, KAILIANG RALSTON, TYLER S.		
IPC分类号	A61N7/00 A61B8/00 G01S7/282		
CPC分类号	G01N29/2406 G01N29/44 G01N29/4463 G01N29/449 H03F3/345 H03F2200/129 H03M1/124 H03M1/38 H03F3/45179 H03F2203/45116 H03F2203/45524		
优先权	62/522606 2017-06-20 US		
外部链接	Espacenet		

摘要(译)

描述了一种包括单端跨阻放大器 (TIA) 的超声电路。 TIA耦合到超声换能器，以响应于接收到超声信号而放大由超声换能器产生的电信号。 在 TIA之后是进一步的处理电路，该处理电路配置为对TIA产生的信号进行滤波，放大和数字化。