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(54) Title: ULTRASOUND IMAGING WITH ANALOG PROCESSING

(57) Abstract: An approach to signal processing in an imaging system, for instance an ultrasound medical imaging system, makes use of analog signal processing prior to conversion to digital form, which may be performed in a portable probe of the system. In some examples, the system includes multiple controllable input processing blocks, each implementing a discrete time analog signal processing stage such as time domain filtering for fractional time delay, anti-alias filtering, or matched filtering. The processing blocks may be implemented using a passive charge sharing approach in which charge is transferred between capacitive elements in successive phases using controlled switches.

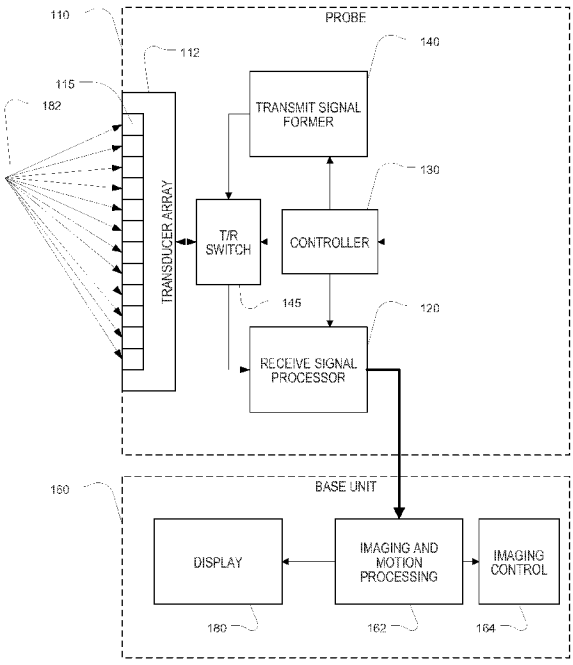

FIG. 1

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ULTRASOUND IMAGING WITH ANALOG PROCESSING

Cross-Reference to Related Applications

This application claims the benefit of U.S. Provisional Application No. 61/357,819, filed June 23, 2010, titled "Imaging System with Analog Processing," and U.S. Provisional Application No. 61/374,946, filed August 18, 2010, titled "Ultrasound Imaging with Probe-Based Analog Processing," which are incorporated herein by reference.

This application is also related to U.S. Patent Application Serial No. 12/545,590, titled "ANALOG COMPUTATION," published as US2010/0207644A1 on August 19, 2010, and to U.S. Provisional Application Serial No. 61/374,915, filed August 18, 2010, titled "CHARGE SHARING ANALOG COMPUTATION," U.S. Provisional Application Serial No. 61/374,931, filed August 18, 2010, titled "ANALOG FOURIER TRANSFORM DEVICE," U.S. Provisional Application Serial No. 61/374,954, filed August 18, 2010, titled "SIGNAL ACQUISITION SYSTEM," and U.S. Provisional Application Serial No. 61/493,893, filed June 6, 2011, titled "CHARGE SHARING IIR FILTER." The contents of the above-referenced applications are incorporated herein by reference.

Background

This document relates to ultrasound imaging with analog processing.

Imaging systems, for instance medical ultrasound imaging systems, often perform signal processing of acquired signals for purposes such as beam forming. In some examples, initial processing may be performed in a probe in which sensor signals are digitized and then processed using digital signal processing techniques before being passed to another component of the system in which images are formed from the processed signals.

In a ultrasound system in which the transducers in a probe form an array, one approach to sending excitation ultrasound signals and reconstructing images of tissue within the body from received ultrasound signals is to transmit excitation signals for each of the transducers from a main processing unit to the probe and then to transmit the received signals from the transducers back to the main processing unit. In some examples, each transducer has a separate electrical conductor for passing a signal to and/or from the main unit. In some examples, various forms of multiplexing or

modulation are used to reduce the number of conductors required to pass the signals between the main unit and the probe. Processing the signals includes introducing desired delays on signals associated with different transducers to focus the delivery of transmitted ultrasonic signals or to focus the reception of signals on selected locations within the body.

In some ultrasound systems, some degree of processing is performed in the probe, thereby reducing the number of conductors needed for communication between the probe and a main unit or to reduce the amount of information passed between the probe and the mail unit. One form of processing is to introduce delays for input or output signals for different transducers to vary the focus of signals within the body. In some examples, a memory and a clocked system is used to sample signal to introduce delays that are an integral number of sampling periods by storing input or output values in the memory and retrieving them at the desired delay. In some examples, delay is introduced using a configurable analog phase delay element. In some examples, subsets of transducers form "micro-arrays" and suitably delayed received signals are added together to form a combined signal such that each microarray has a single conductor or channel linking the probe and the main unit.

There is a need to perform more processing of the transmitted and/or received signals in an ultrasound probe in order to reduce the communication requirements between the probe and a main unit, or to completely eliminate the main unit entirely to form a portable imaging system, for example, with an integrated display.

There is also a need to perform processing using reduced power in a wireless probe, thereby permitting longer operating duration between battery charges or to reduce the power delivery requirements from a main unit to the probe or to reduce the power dissipation requirements of the probe. Also, in a two part system with a probe and a main unit, there is a need to reduce the amount of information passing from the probe to the main unit, thereby reducing the bandwidth requirement (e.g., over a wireless link) and/or transmission power requirement of the probe.

Summary

In one aspect, in general, an approach to signal processing in an imaging system, for instance an ultrasound medical imaging system, makes use of analog signal processing prior to conversion to digital signals. In some examples, the outputs of ultrasound signals are acquired in analog form and processed in a discrete time analog circuit, for example, using techniques described in the co-pending application titled "ANALOG COMPUTATION," referenced above.

In another aspect, in general, an ultrasound processing system comprising a plurality of controllable input processing blocks, each implementing a discrete time analog signal processing stage for processing one or more corresponding input signals representing ultrasound signals.

Aspects can include one or more of the following features.

Each input processing block is controllable, for instance, being controllable to introduce relative delays between signals that are a fraction of the sampling period of the signal processing stage, for instance, as part of a beamforming operation.

The ultrasound processing system further comprises a plurality of ultrasound elements, each coupled to provide a signal representing an ultrasound signal received at the ultrasound element to a corresponding input processing block.

The ultrasound processing system further comprises a plurality of amplifiers, each coupled to an input of a corresponding input processing block. In some examples, at least some of the processing blocks are passive (i.e., without signal amplification elements).

Each input processing block comprises a passive charge sharing processing section including a plurality of capacitive elements and a plurality of switches (e.g., transistors) for controlling transfer of charge between the capacitive elements, wherein characteristics of the processing section are controllable according to sequencing of operation of the switches.

A controller is coupled to the input processing blocks for controlling operation of one or more of the input processing blocks.

Each input processing block is controllable to implement a discrete time analog finite impulse response (FIR) filter.

Each input processing block further comprises a coarse delay stage controllable to introduce a delay that is a multiple of the sampling period.

The ultrasound processing system further comprises an analog-to-digital converter (ADC) coupled to an output of each of (or at least some of) the processing stages.

The ultrasound processing system further comprises combination circuitry for combining multiple outputs of the input processing blocks to form a combined signal.

The ultrasound processing system further comprises an analog-to-digital converter (ADC) coupled to an output of the combination circuitry.

The probe is linked to a base unit by a communication link suitable for passing the combined signals to the base unit.

The input processing blocks and the combination circuitry are within a portable probe of the system.

The ultrasound processing system further comprises a controller coupled to the input processing blocks for repeatedly reconfiguring the input processing blocks.

The controller is responsive to the combined signals to adapt to signal acquisition characteristics of the input signals.

Each input processing block comprises a plurality of a passive signal scaling circuits each for accepting an analog input signal value and a digital scaling control value representing a scaling factor and storing an analog representation of a scaled signal value equal to a product of the accepted signal value and the scaling factor in an output stage for the scaling circuit.

Each signal scaling circuit comprises a plurality of switchably interconnected capacitive elements

In operation of the scaling circuit, the scaled signal value is formed in a succession phases, each phase being associated with a configuration of the switchable interconnection of capacitive elements permitting charge sharing among interconnected capacitors, at least one of the capacitive elements being configured according to the digital scaling control value.

The ultrasound processing system further comprises a plurality of controllable output processing blocks for generating a corresponding signal for emission as an ultrasound signal, each block implementing a discrete time analog signal processing stage, and controllable to introduce relative delay between signals that are a fraction of the sampling period of the signal processing stage.

In another aspect, in general, a signal processing unit for processing ultrasound generated signals comprises: inputs for a plurality of ultrasound generated signals; one or more controllable passive signal processing blocks, each implementing a discrete time analog signal processing stage for processing signals received or determined from the inputs of the unit; at least one analog-to-digital converter (ADC) for converting an analog signal output from one of the processing blocks to a digital signal; an output for providing the digital signal from the at least on ADC; a controller coupled to the one or more processing for controlling operation of one or more of the input processing blocks; and a controller input coupled to the controller for providing control information to the controller for controlling operation of the unit and effecting signal processing functions performed by at least some of the signal processing blocks.

In another aspect, in general, a method for processing ultrasound generated signals comprises: accepting a plurality of a plurality of ultrasound generated signals; processing the signals in a plurality of controllable input processing blocks, including performing a discrete time analog signal processing of the signals; controlling the input processing blocks, including introducing relative delays between signals that are a fraction of the sampling period of the signal processing. In some examples, erforming the discrete time analog signal processing of the signals includes controlling operation of a passive charge sharing circuit to implement a desired signal transformation.

Advantages of one or more aspects of the system can include reduced power requirements for the processing in a probe, which may enable wireless battery-powered operation and which may reduce the size, complexity, or component costs of the probe.

Increased processing in the probe can reduce communication capacity required between a probe and a base unit, thereby reducing cost and complexity of a two-part ultrasound system.

Other advantages can include improved imaging performance by enabling more complex processing (e.g., in the probe) than is feasible using purely digital signal processing techniques.

Other aspects, features, and advantages are apparent from the following description and from the claims.

Description of Drawings

FIG. 1 is a block diagram of an ultrasound imaging system;

FIG. 2 is a block diagram showing signal processing blocks; and

FIG. 3 is a block diagram of a signal processing unit for use in an ultrasound imaging system.

Description

Referring to FIG. 1, an example of an ultrasound system 100 includes a probe 110 and a base unit 160 coupled to the probe via a communication link. In other examples, the system is portable, and some or all of the elements of the base unit are hosted within the probe itself.

The ultrasound system makes use of an array 112 with a set of ultrasonic elements 115, for example 256 or 1024 or more arranged in a linear or grid pattern. These elements are used to emit and sense ultrasonic signals. These emitted signals are reflected within the patient's body and the reflected signals are sensed at the ultrasonic elements. A transmit signal former 140 generates the signals for transmission from the elements, and a receive signal processor 120 processes the sensed signals. A transmit/receive switch circuit 145 is used to alternate between transmission and receiving phases of operation.

In some embodiments of the system, a beamforming approach is used in which the ultrasonic signals emitted from the elements are formed to create a focused signal at one or more desired locations within the body being sensed. Similarly, the signals received at the ultrasonic elements are processed in order to selectively acquire reflections originating at desired locations within the body.

Generally, the receive signal processor 120 performs some or all of its processing in an analog domain prior to performing analog-to-digital conversion (ADC) of the received signals at the probe or base unit. In some examples, some of this analog processing is performed prior to amplification and reduces the performance requirements of such amplifiers. Various embodiments of the system may perform one or more of the following analog domain signal processing steps prior to digitization:

- Time delay
- Anti-alias filtering
- Matched filtering (e.g., for processing of coded excitation signals)
- Gain control
- Transform (e.g., Fourier, compressing sensing) analysis
- Matrix operations

Similarly, the formation of the excitation signals in the transmit signal former 140 may make use of analog processing techniques, for example, to introduce delays suitable for focusing the emitted signals on desired parts of the body.

Generally, the processing performed by the receive signal processor 120 and/or the transmit signal former 140 varies as an image is acquired, for example, to perform a scanning operation in which a focus of the emitted signals is scanned through a three-dimensional body volume and the acquired signal is similarly focused to different locations in the body volume. A controller 130 sends control signals to the processor 120 and former 140. For example, control signal may encode desired delays to introduce in the various output or input signal paths, or may provide more specific processing characteristics, for example, parameters of filters.

In some embodiments, the analog processing implemented in the transmit signal former 140 and/or the receive signal processor 120 make use of discrete time analog domain processing in which capacitors are coupled by controlled switches in order to accomplish desired signal processing functions by successive transfers of charge between the capacitors. A number of signal processing techniques using such charge sharing approaches are described in one or more of the following applications:

- U.S. Patent Application Serial No. 12/545,590, titled "ANALOG COMPUTATION," published as US2010/0207644A1 on August 19, 2010

- U.S. Provisional Application Serial No. 61/374,915, filed August 18, 2010, titled "CHARGE SHARING ANALOG COMPUTATION."

- U.S. Provisional Application Serial No. 61/374,931, filed August 18, 2010, titled "ANALOG FOURIER TRANSFORM DEVICE."

- U.S. Provisional Application Serial No. 61/374,954, filed August 18, 2010, titled "SIGNAL ACQUISITION SYSTEM."

- U.S. Provisional Application Serial No. 61/493,893, filed June 6, 2011, titled "CHARGE SHARING IIR FILTER."

Referring to FIG. 2, in one example, each ultrasound element 115 provides an analog signal that is sampled at a rate that is sufficiently high to avoid aliasing, for example, based on a band-limit of the sensors and/or an anti-aliasing filter between the sensor and the sampling unit (not shown). Each signal is processed to introduce a delay controlled by the controller 130 in order to focus the acquired signal from a desired point 182 in the body. In some embodiments, each signal passes through two delay stages. A coarse delay stage 121 introduces a delay that is an integral number of sampling periods, for example using a capacitor array provides the temporary storage of the analog signal values. A second stage 122 provides a fine time delay, which is less than a full sampling period. In some implementations, this second stage 122 is implemented using a time domain filter that provides an appropriate interpolation of sample values in order to effect the desired delay.

Fractional delay can be implemented using a Finite Impulse Response (FIR) filter, which can be expressed as

$$y(n) = \sum_{k=0}^{K-1} h_k \, x(n-k).$$

The coefficients h_k are chosen, for example, using a windowed fractionally offset sinc function. In one implementation, each fractional delay stage 122 includes K^2 capacitors (doubly indexed (0,0) through $(K-1, K-1)$). An input $x(i)$ output from the coarse delay at time i is coupled to multiple capacitors $(i \bmod K, 0) \ldots, (i \bmod K, K-1)$ such that they are all charged based on the same input. Then, an output $y(i)$ is formed by coupling capacitors $(i \bmod K, 0), (i-1 \bmod K, 1), \ldots, (i-K+1 \bmod K, K-1)$, optionally with an output

capacitor or a capacitor in another storage section. In order to accommodate different fractional delays, different sets of filter tap values may be achieved my making the (j,k)th capacitor value $c_{(j,k)}$ have a selectable value value that is proportional to h_k. For example, if a fixed number of fractional delay values can be selected by the controller, a different set of K^2 capacitors can be selected for each different fractional delay.

Rather than having K^2 fixed capacitors for each possible delay, the capacitor values may be controllable, for example, according to a binary control value to selects a parallel combination of power-of-2 sized capacitors.

Other approaches to FIR filter implementations that have many preferable characteristics is described in copending application No. 61/374,915, "CHARGE SHARING ANALOG COMPUTATION," in which the effective capacitance that is used to implement the filter tap values that have multiple controlled capacitors and/or use multiple phases of charge sharing. An advantage of such configurations is that a relatively large range of capacitance and therefore coefficient values can be achieved with a relatively small total capacitance (which can reduce circuit area), while providing relatively high precision in the selectable values. In one example of an FIR filter that uses this approach, K^2 fixed sampling capacitors are used as described above (e.g., each having the same value), and each FIR output is formed in a number sharing phases, for example, in a one or more phases in which each of K sampling capacitors is coupled to a digitally controlled capacitor or capacitor network to transfer a selectable amount of charge from the sampling capacitor, and a last phase in which a subset of the capacitors are coupled together effectively computing a weighted average, to form the filter output value represented as a voltage or as a charge on an output capacitor.

The controller 130 configures the filters according to the desired delays, for example, by specifying the filter coefficients for the finite impulse response filters, in order to focus the input signals on successive points 182. Note that as the body is scanned, the controller successively reconfigures the filters in order to scan various locations in the body.

After introducing the delay into the input signals, multiple signals are combined in a combiner 123, for example, by summing or averaging (e.g., by charge sharing) the signals. In some examples, a controllable gain is introduced to account for sensitivity variations of the different ultrasonic elements and/or to account for different attenuation along the paths to each of the elements through the body. In some

examples, the combiner 123 also performs an envelope detection function on the combined signal.

In some examples, as shown in FIG. 2, the array of ultrasonic sensors is divided into a set of groups. Each group is processed as described above introducing controlled delays and optionally gains. A further processing stage 125 is optionally applied to multiple of the groups, for example, to all of the groups in the array. In some examples this processing is performed in the (discrete time) analog domain, while in other embodiments, an analog-to-digital conversion is performed prior to the further processing stages, which is implemented using digital signal processing. In some embodiments, the further processing can include one or more of spatial domain and transform domain processing.

Turning back to FIG. 1, the transmission of signal information from the receive signal processor to the image and motion processing module 162 at the base unit may be analog or digital. For example, the analog signal may comprise a beamformed and spatially subsampled analog signal, which requires substantially fewer analog signal paths (e.g., micro-coaxial cables) between the probe and the base unit than conventional approaches. In other examples, signals are digitized after processing at the probe and are transmitted to the base unit in digital form, for example, time multiplexed on a serial communication link, for example, over a wireless communication domain.

Note that an analog-to-digital converter (ADC) can sample the envelope at a slower rate than that used in the filtering stages, and the filtering stages can implement an anti-aliasing filter to prevent aliasing by using the lower sampling rate.

The base unit processes the received digitized signals in an imaging and motion processing module 162, which provides the synthesized image on a display 180 to a user of the system. An image controller also receives the signals, can controls aspects including overall control of the raster process in the probe.

In some versions of the system, an imaging control 164 performs more complex adaptations, for example, to account for various signal propagation factors that may degrade the signal. For example, the required delays, pulse waveforms, etc. introduced on the transmit and receive paths may be adjusted to account for propagation rate, dispersion, etc. of the signals before reaching the sensors.

In some examples, the analog filters described above in the context of providing fractional delay also (or instead) perform a matched filter function to improve detection of the reflected pulses, or for pulse compression and/or use of coded or pseudo-random excitation waveforms.

In some examples, the processing for each group of sensors, as well as the ADC for that block are integrated into a single electronic circuit or package (referred to below as a unit), as illustrated in FIG. 3. In an example of such a unit, a set of sensor inputs is provided as analog signals, illustrated as four separate inputs in the figure, understanding that other examples, may have different numbers of inputs (e.g., 8, 14 for a 4x4 patch, etc.). The unit optionally includes analog signal amplification elements 310, whose gain is optionally controllable by a controller 330 in the unit. The unit includes a number signal processing blocks 320, 323. In some examples, a separate signal processing block 320 is associated with each input, and another signal processing block 323 is used for combination of the signals. It should be understood that some versions of such a unit may have only the signal specific blocks 320 or only a combined processing block 323. In some versions of the unit, each signal processing block 320 performs a discrete (sampled) time analog signal domain processing of the signal, for example, using switched capacitor techniques as described above. The controller 330 is coupled to the processing blocks 320 to coordinate operation of the switches in the block in order to cause the desired sequence of charge sharing to implement desired signal processing functions, such as fractional sampling period delay, matched filtering, etc. In some versions of the system, the entire processing block 320 is passive in that gain is not introduced into the signal path through the block (recognizing that the switches in the block may be implemented using transistors, which are active devices, but the block nevertheless is passive with respect to the signal path). In some versions of the unit, further signal amplification may be introduced in the signal path, for example, between the signal blocks 320 and the combination signal block 323. In some versions of the system, the combination block is controllable to perform a sum or average of the ouputs of the processing blocks 320, and an envelope detection (e.g., rectification and smoothing). In some versions of the unit, analog outputs are provided from the unit, while in units as illustrated in FIG. 3, one or more analog-to-digital converters 340 process output of the processing block 323. Note that as illustrated the combination block 323 has the same number of inputs as outputs, but it should be understood that in some versions, the block performs a reduction in the number of signals. For example, there may be four inputs and only one output, which can be configured to provide a beamformed combination of the inputs. In some implementations, multiple of such units are

integrated together in one circuit or package to process all the signals provided by the ultrasonic elements 115 of a probe array.

Note that the description above focuses on receiving ultrasound signals. The transmit portion of the probe (e.g., the transmit signal former 140) can be similarly configured, with each of multiple transducer outputs being driven by a corresponding signal that is appropriately delayed a fractional amount in a discrete time analog processing stage in order to focus the transmitted signals on the point in the body being images.

It should be understood that although the description above may focus on use of the analog signal processing to implement delay-based beamforming, other embodiments may perform other types of signal processing in the analog domain. For example, the signal processing blocks may perform joint processing, effectively implementing a multidimensional signal processing approach using the discrete time analog signal processing techniques referred to above.

As one example a transform approach may be used. For example, an analog implementation of a Discrete Cosine Transform (DCT) can be used to encode segments of the sensor grid (e.g., prior to or after performing delay based processing). In some implementations, a DCT or other transform may be used to compress the signal to reduce the amount of information that needs to be transmitted from or stored at the probe.

More generally, it should be recognized that the analog processing approaches described above and in the co-pending applications can be used to implement matrix multiplication operations. In some embodiments, the probe is configurable to perform such operations at the command of the controller at the probe and/or at the command of the base unit. Examples of functions that may be implemented in such a matrix form include transforms (e.g., effectively using square matrices) and projections (e.g., using rectangular matrices). As an example, a compressive sensing approach may be used in which a high number of sensor values are projected into a lower dimensional signal that is processed or transmitted for further processing. In some examples, the matrix operations are performed in stages, for example, combining subsets (e.g., patches) of sensors in a first matrix operation, and then combining the outputs across multiple subsets in successive stages. In some examples, a configurable probe can provide conventional beamforming functions are well as more complex multidimensional operations on the sensed signals.

In some examples, the processing in the main section provides control and/or feedback signals to configure or control the analog processing in the probe. For instance, the feedback may provide updated projection matrices for compressive sensing applications, gain control, and beam forming pattern. This feedback may be based, for example, on predicted characteristics of the sensed signals, which may be based on estimates of motion of the probe or body being sensed.

In some examples, the analog processing may include probabilistic computation, for instance, using model based or Bayesian approaches. The processing (e.g., at the base unit of the system) may include optimization-based reconstruction of an image, and output of signals suitable to driving an image presentation to a user of the system.

As introduced above, the analog processing may all be performed in a probe, and optionally digitized before being transmitted using a wired or wireless link to a main section of the system. The analog and/or digital processing may be controlled by software stored in a computer-readable for controlling a processor, such as a digital signal processor or general purpose computer. In some examples, software controlling the probe, including controlling the operation of the analog domain filters and transformation stages, is uploaded to the probe from the base unit, and stored in a tangible storage medium at the probe.

It is to be understood that the foregoing description is intended to illustrate and not to limit the scope of the invention, which is defined by the scope of the appended claims. Other embodiments are within the scope of the following claims

Claims

What is claimed is:

1. An ultrasound processing system comprising:

a plurality of controllable input processing blocks, each implementing a discrete time analog signal processing stage for processing one or more corresponding input signals representing ultrasound signals;

wherein each input processing block is controllable, including being controllable to introduce relative delays between signals that are a fraction of the sampling period of the signal processing stage.

2. The ultrasound processing system of claim 1 further comprising a plurality of ultrasound elements, each coupled to provide a signal representing an ultrasound signal received at the ultrasound element to a corresponding input processing block.

3. The ultrasound processing system of claim 1 further comprising a plurality of amplifiers, each coupled to an input of a corresponding input processing block.

4. The ultrasound processing system of claim 1 wherein each input processing block comprises a passive charge sharing processing section including a plurality of capacitive elements and a plurality of switches for controlling transfer of charge between the capacitive elements, wherein characteristics of the processing section are controllable according to sequencing of operation of the switches.

5. The ultrasound processing system of claim 4 further comprising a controller coupled to the input processing blocks for controlling operation of one or more of the input processing blocks.

6. The ultrasound processing system of claim 1 wherein each input processing block is controllable to implement a discrete time analog finite impulse response filter.

7. The ultrasound processing system of claim 6 wherein each input processing block further comprises a coarse delay stage controllable to introduce a delay that is a multiple of the sampling period.

8. The ultrasound processing system of claim 1 further comprising an analog-to-digital converter (ADC) coupled to an output of each of the processing stages.

9. The ultrasound processing system of claim 1 further comprising:

combination circuitry for combining multiple outputs of the input processing blocks to form a combined signal.

10. The ultrasound processing system of claim 9 further comprising an analog-to-digital converter (ADC) coupled to an output of the combination circuitry.

11. The ultrasound processing system of claim 9 where the probe is linked to a base unit by a communication link suitable for passing the combined signals to the base unit.

12. The ultrasound system of claim 1 wherein the input processing blocks and the combination circuitry are within a portable probe of the system.

13. The ultrasound system of claim 1 further comprising a controller coupled to the input processing blocks for repeatedly reconfiguring the input processing blocks.

14. The ultrasound system of claim 13 wherein the controller is responsive to the combined signals to adapt to signal acquisition characteristics of the input signals.

15. The ultrasound system of claim 1, wherein each input processing block comprises:

a plurality of a passive signal scaling circuits each for accepting an analog input signal value and a digital scaling control value representing a scaling factor and storing an analog representation of a scaled signal value equal to a product of the accepted signal value and the scaling factor in an output stage for the scaling circuit.

16. The ultrasound system of claim 15, wherein each signal scaling circuit comprises a plurality of switchably interconnected capacitive elements

17. The ultrasound system of claim 16, wherein in operation of the scaling circuit, the scaled signal value is formed in a succession phases, each phase being associated with a configuration of the switchable interconnection of capacitive elements permitting charge sharing among interconnected capacitors, at least one of the capacitive elements being configured according to the digital scaling control value.

18. The ultrasound system of claim 1 further comprising:

a plurality of controllable output processing blocks for generating a corresponding signal for emission as an ultrasound signal, each block implementing a discrete time analog signal processing stage, and controllable to introduce relative delay between signals that are a fraction of the sampling period of the signal processing stage.

19. A signal processing unit for processing ultrasound generated signals comprising:

inputs for a plurality of ultrasound generated signals;

one or more controllable passive signal processing blocks, each implementing a discrete time analog signal processing stage for processing signals received or determined from the inputs of the unit;

at least one analog-to-digital converter (ADC) for converting an analog signal output from one of the processing blocks to a digital signal;

an output for providing the digital signal from the at least on ADC;

a controller coupled to the one or more processing for controlling operation of one or more of the input processing blocks; and

a controller input coupled to the controller for providing control information to the controller for controlling operation of the unit and effecting signal processing functions performed by at least some of the signal processing blocks.

20. A method for processing ultrasound generated signals comprising:

accepting a plurality of a plurality of ultrasound generated signals;

processing the signals in a plurality of controllable input processing blocks, including performing a discrete time analog signal processing of the signals;

controlling the input processing blocks, including introducing relative delays between signals that are a fraction of the sampling period of the signal processing.

21. The method of claim 20 wherein performing the discrete time analog signal processing of the signals includes controlling operation of a passive charge sharing circuit to implement a desired signal transformation.

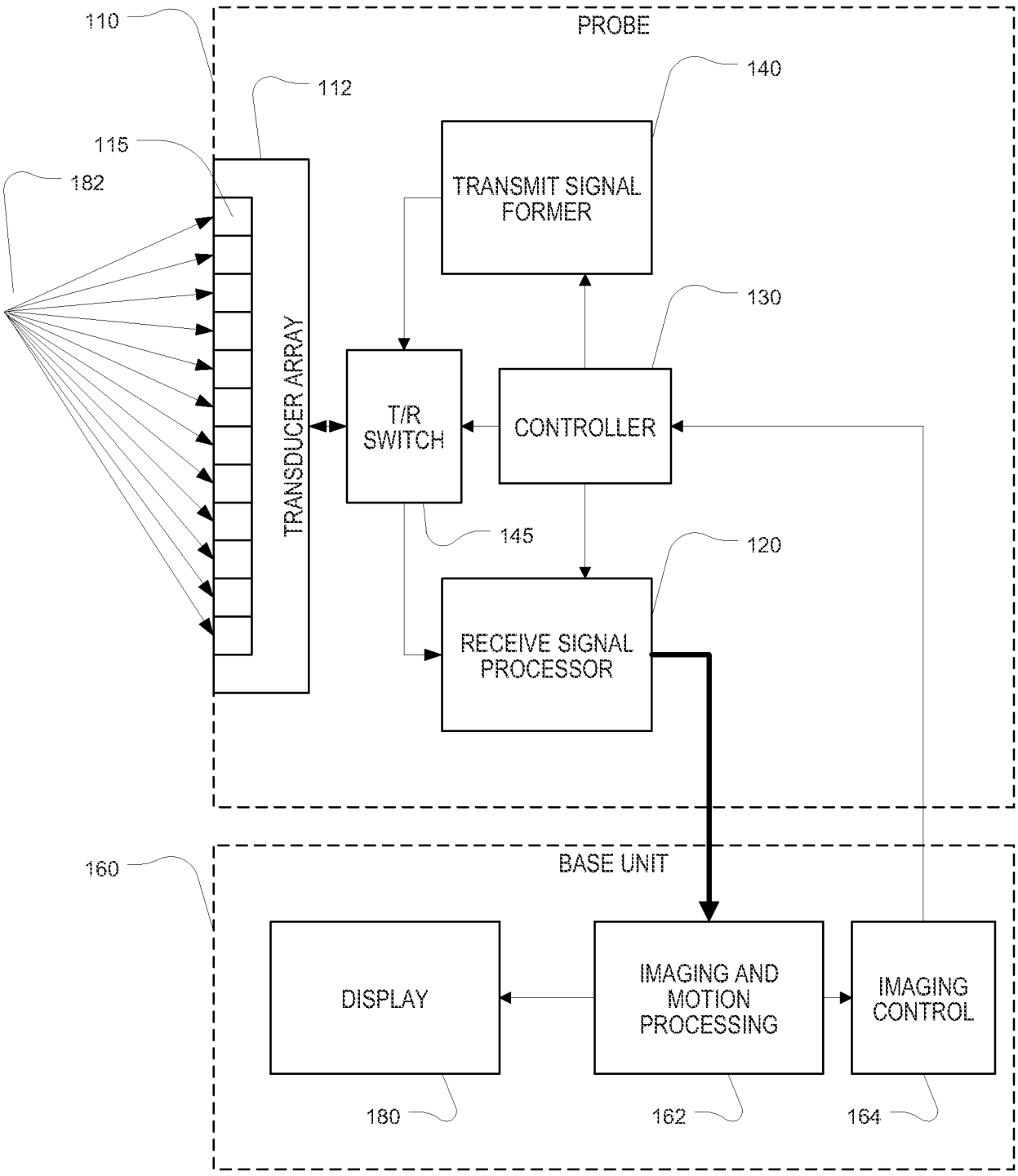
110
PROBE
112
140
115
182
TRANSMIT SIGNAL FORMER
130
TRANSDUCER ARRAY
T/R SWITCH
CONTROLLER
145
120
RECEIVE SIGNAL PROCESSOR
160
BASE UNIT
DISPLAY
IMAGING AND MOTION PROCESSING
IMAGING CONTROL
180
162
164

FIG. 1

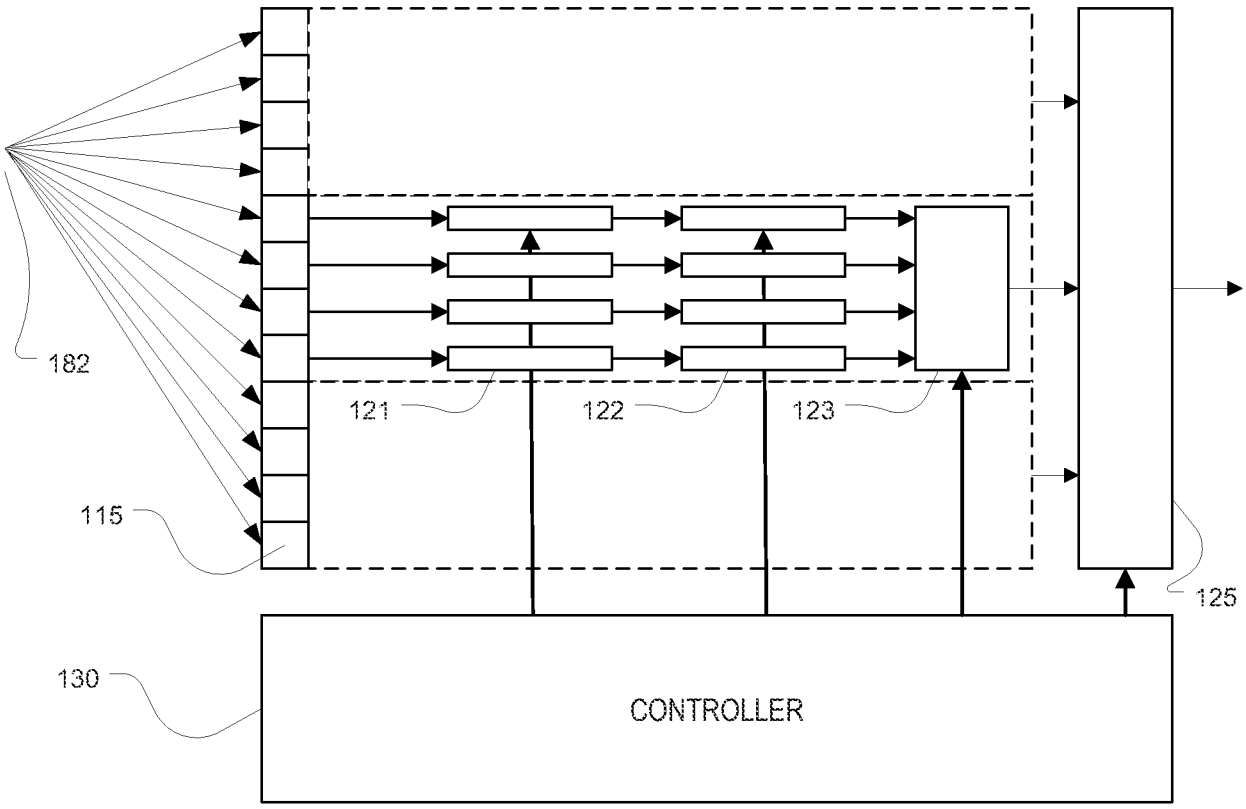
182
121
122
123
115
125
130
CONTROLLER

FIG. 2

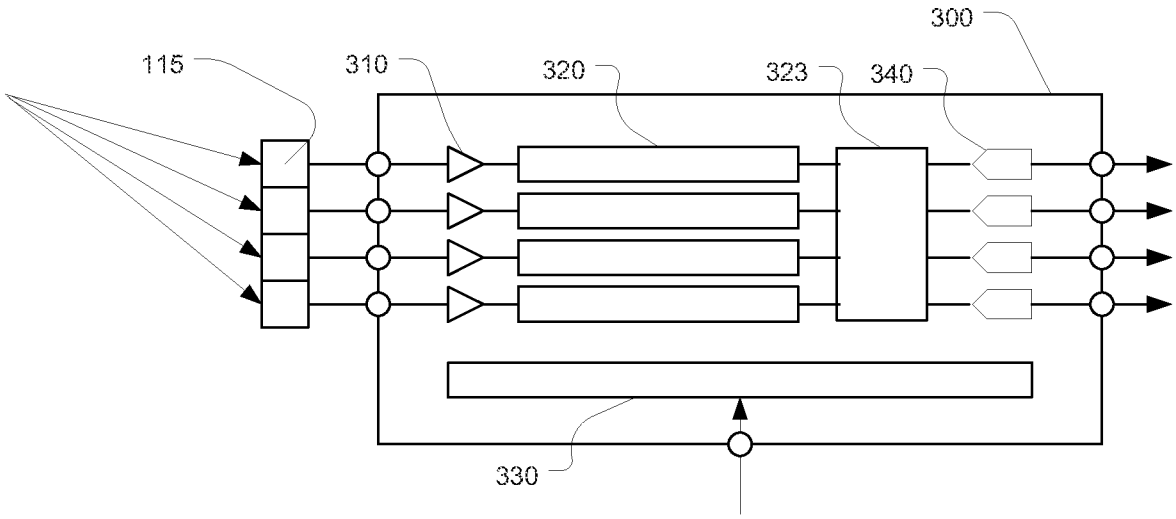
300
115
310
320
323
340
330

FIG. 3

INTERNATIONAL SEARCH REPORT

PCT/US 11/41625

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - A61B 8/00 (2011.01)
USPC - 600/437
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 600/437; IPC: A61B 8/00 (2011.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
600/300, 407, 437, 459; 382/128; A61B8/00, A61B$, search term limited, see keywords below

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWest (PGPG, USPT, EPAB, JPAB); Google Patents
Search terms: ultrasound, analog, time, temporal, delay, hindrance, stay, fraction, fractional, portion, sample, sampling, representation, amplifier, passive, capacitive, capacitor, adc, digital, finite, coarse, delay,

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 6,193,659 B1 (Ramamurthy et al.) 27 February 2001 (27.02.2011), entire document, especially title, abstract, Fig 24-26, col 6, ln 25 to col 18, ln 42, claim 8	1-3, 12, 18, 20 ---------- 4-11, 13-17, 19, 21
Y	US 2007/0239001 A1 (Mehi et al.) 11 October 2007 (11.10.2007), entire document, especially abstract and para [0172]-[0228]	5-8, 10, 13, 14, 19
Y	US 2005/0261596 A1 (Smith) 24 November 2005 (24.11.2005), entire document, especially abstract and para [0016]	4, 5, 16, 17, 21
Y	US 7,110,556 B2 (Aarts et al.) 19 September 2006 (19.09.2006), entire document, especially abstract and col 3,ln 15	9-11
Y	US 7,164,768 B2 (Aylward et al.) 16 January 2007 (16.01.2007), entire document, especially abstract and col 2, ln 13-31	15-17

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 November 2011 (01.11.2011)	03 NOV 2011
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

专利名称(译)	超声成像与模拟处理		
公开(公告)号	EP2584971A1	公开(公告)日	2013-05-01
申请号	EP2011798920	申请日	2011-06-23
[标]申请(专利权)人(译)	美国亚德诺半导体公司		
申请(专利权)人(译)	ANALOG DEVICES，INC.		
当前申请(专利权)人(译)	ANALOG DEVICES，INC.		
[标]发明人	VIGODA BENJAMIN BERNSTEIN JEFFREY NESTLER ERIC		
发明人	VIGODA, BENJAMIN BERNSTEIN, JEFFREY NESTLER, ERIC		
IPC分类号	A61B8/00 G01S7/52		
CPC分类号	A61B8/4444 A61B8/4472 A61B8/4488 A61B8/54 G01S7/5202 G01S7/5208 G01S7/52082 G01S7/52096 G01S15/8909 G01S15/8915 G01S15/8927 G10K11/346		
优先权	61/357819 2010-06-23 US 61/374946 2010-08-18 US		
其他公开文献	EP2584971A4		
外部链接	Espacenet		

摘要(译)

成像系统中的信号处理方法，例如超声医学成像系统，在转换成数字形式之前利用模拟信号处理，这可以在系统的便携式探头中执行。在一些示例中，该系统包括多个可控输入处理块，每个可实现离散时间模拟信号处理级，例如用于分数时间延迟的时域滤波，抗混叠滤波或匹配滤波。可以使用无源电荷共享方法来实现处理块，其中使用受控开关在连续相位中的电容元件之间传输电荷。