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(71) Applicant *(for all designated States except US)*: **TERATECH CORPORATION** [US/US]; 77-79 Terrace Hall Avenue, Burlington, MA 01803 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **CHIANG, Alice** [US/US]; 4 Glenfeld East, Weston, MA 02493 (US). **HE, Xingbai** [CN/US]; 494 Lowell Street, Andover, MA 01810 (US). **WONG, William** [US/US]; 1041 Randolph Avenue, Milton, MA 02186 (US). **BERGER, Noah** [US/US]; 137 Meadow Street, Framingham, MA 01701 (US).

(74) Agents: **HOOVER, Thomas, O.** et al.; Weingarten, Schurgin, Gagnebin & Lebovici, LLP, Ten Post Office Square, Boston, MA 02109 (US).

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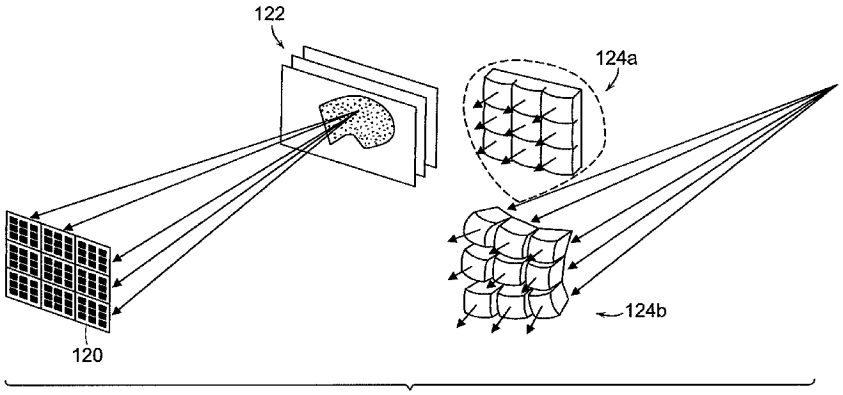

FIG.1

(57) Abstract: The present invention relates to an ultrasound imaging system in which the scan head either includes a beamformer circuit that performs far field subarray beamforming or includes a sparse array selecting circuit that actuates selected elements. When used with second stage beamforming system, three dimensional ultrasound images can be generated.

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TITLE OF THE INVENTION

ULTRASOUND 3D IMAGING SYSTEM

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of U.S. Application No. 12/286,555 filed on September 30, 2008 and claims priority to U.S. Application No. 61/192,063 filed on September 15, 2008 by Chiang et al., entitled: "Ultrasound 3D Imaging System." This application also claims priority to U.S. Application No. 11/474,098 filed June 23, 2006 and of International Application No. PCT/US2007/014526 filed June 22, 2007. The entire contents of the above applications are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Medical ultrasound imaging has become an industry standard for many medical imaging applications. Techniques have been developed to provide three dimensional (3D) images of internal organs and processes using a two dimensional (2D) transducer array. These systems require thousands of beamforming channels. The power required to operate such systems has resulted in the use of an analog phase shift technique with a digital delay beamformer that results in a compromise of image quality.

There is a continuing need for further improvements in ultrasound imaging technologies enabling improved real-time three dimensional imaging capability. In addition, this improved capability should support continuous real-time display for a fourth dimensional 4D function.

SUMMARY OF THE INVENTION

The present invention relates to a system for ultrasound medical imaging that provides three dimensional (3D) imaging using a two dimensional (2D) array of transducer elements in a probe housing. Embodiments of the invention provide systems and methods

for medical imaging having high resolution and numerous imaging modalities.

In a preferred embodiment, the probe housing contains a first beamforming circuit that transmits beamformed data to a second housing having a second beamforming circuit. The first beamforming circuit provides a far-field subarray beamforming operation. The resulting beamformed data is transmitted from the scan head to a second housing having the second beamforming circuit that provides near-field beamsteering and beamfocusing.

A preferred embodiment provides a scan head that can be connected to a conventional ultrasound system in which the scan head provides the inputs to the conventional beamforming processing function. The scan head beamformer can utilize a low power charge domain processor having at least 32 beamforming channels.

A preferred embodiment of the invention employs a sparse array where only a fraction of the transducer elements need to be activated. By selecting the four corner elements of the array to provide proper mean lobe bandwidth, minimizing average sidelobe energy and clutter, eliminating periodicity and maximizing peak to side lobe ratio, quality images are produced. To steer the beams across the volume or region of interest, different transducer elements must be actuated in proper sequence to maintain the peak to sidelobe ratio. The system processor can be programmed to provide the desired sequence for transducer actuation to direct the beam at different angles. Alternatively, a discrete controller can be used to control sparse array actuation. A preferred embodiment provides a scan head with integrated switching circuits for sequentially selecting sparse array actuation elements for sequential multiple beamforming. The scan head can be connected to a conventional ultrasound system in which the scan head provides the inputs to the conventional beamforming processing functions. In another embodiment, the transmit array elements and receive array elements can be operated independently

with the transmit elements comprising a sparse array and the receive elements being a near fully populated array. In a preferred embodiment, the multiplexer and beamformer circuits can be integrated into an interface system, or alternatively, into a host processing system, leaving a 2D transducer array mounted in the probe housing.

The present invention utilizes nondestructive sensing at each stage of the delay elements in the beamformer. So with a 65 stage delay line, for example, there are 64 usable outputs with one at each stage. The time resolution can be in the range of 1/8 λ to 1/16 λ.

Using high voltage multiplexers in the probe and the nondestructive sensing allows for time multiplexed sequential beamforming. It is now possible to sequentially change tap selection of each delay line to form multiple beams.

In addition to the three dimensional (3D) display capability, a fourth dimension or time resolved image display can be used to record and display a sequence of images recorded at 10 frames per second or higher, for example. This enables viewing of rapidly changing features such as blood or fluid flow; heart wall movement etc. at video frames rates of 30 frames per second.

Another preferred embodiment of the invention utilizes a three stage beamformer system in which a first stage performs a first beamforming operation on data received from a transducer array, which generates first beamformed data that is followed by a second stage that performs a second beamforming operation to provide second stage beamformed data that is then delivered to a third beamforming stage that performs a third beamforming operation.

The stages can be performed using charge domain processors. Data can also be converted from analog to digital form before the first stage, or the second stage, at the third stage or thereafter. One stage can utilize parallel beamforming operations and a second stage provides serial beamforming.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates the use of a two dimensional tiled array for ultrasound imaging in accordance with the invention.

Fig. 2 illustrates a steerable two dimensional array in accordance with the invention.

Fig. 3A illustrates the use of a first beamformer device for far field beamsteering and focusing and a second time delay beamformer for near field beamforming.

Fig. 3B illustrates a first analog subarray beamformer forwarding data to a digital beamformer.

Fig. 3C illustrates a scanhead for a two dimensional transducer probe.

Fig. 3D illustrates a preferred embodiment utilizing a flexible circuit board and cable assembly.

Fig. 4 illustrates a preferred embodiment of a three dimensional imaging system in accordance with the integrated Subarray scan head invention.

Fig. 5 illustrates a preferred embodiment of the integrated Subarray scan head invention using a charge domain processor for the 2^{nd} time delay beamforming.

Fig. 6A illustrates the use of the integrated subarray scan head probe of the present invention with a second stage beamforming ultrasound processor.

Fig. 6B illustrates use of the integrated Subarray scan head with a digital beamforming processor.

Fig. 7 illustrates an ultrasound system in accordance with the invention.

Fig. 8A illustrates a sparse array used in accordance with the invention.

Fig. 8B graphically illustrates the sparse array performance.

Fig. 9A illustrates the use of the integrated sparse array scan head probe of the present invention connected to a host system with charge-domain beamforming processing.

Fig. 9B illustrates the use of the integrated sparse array scan head probe of the present invention connected to a conventional digital ultrasound system with m-parallel beamforming components.

Fig. 10 illustrates a scan head connected to a portable computer in accordance with a preferred embodiment of the invention.

Fig. 11 illustrates a near fully populated receive array in which the receiving elements are independent of, and do not overlap, the transmit array.

Fig. 12 graphically illustrates the azimuth and elevation cross-sections of the receive array beampattern.

Fig. 13 is a magnified portion of the azimuthal beampattern of Fig. 12 showing the mainlobe and sidelobe structure.

Fig. 14 illustrates a near fully populated receive array beampattern.

Fig. 15 shows selected transmit locations for a sparse array in accordance with the invention.

Fig. 16 illustrates a cross-sectional view of the transmit sparse array beampattern of the embodiment in Fig. 15.

Fig. 17 illustrates a sparse transmit array beampattern.

Fig. 18 illustrates that it is possible to limit average sidelobe energy to less than -35dB relative to the central peak of the beampattern.

Fig. 19 illustrates the 2D differential delay equation.

Fig. 20 illustrates a differential display profile.

Fig. 21 illustrates differential delay errors.

Figs. 22A-22C illustrate embodiments of system processors in a four parallel beamforming system.

Figs. 23A and 23B illustrated non-coded and coded transmit waveforms for spread spectrum ultrasound transmission.

Figs. 24A-24C illustrate a process for forming a transmission signal.

Figs. 25A-25D illustrate preferred embodiments including a matched filter.

DETAILED DESCRIPTION OF THE INVENTION

The objective of the beamforming system is to focus signals received from an image point onto a transducer array. By inserting proper delays in a beamformer to wavefronts that are propagating in a particular direction, signals arriving from the direction of interest are added coherently, while those from other directions do not add coherently or cancel. For real-time three-dimensional applications, separate electronic circuitry is necessary for each transducer element. Using conventional implementations, the resulting electronics rapidly become both bulky and costly as the number of elements increases. Traditionally, the cost, size, complexity and power requirements of a high-resolution beamformer have been avoided by "work-around" system approaches. For real-time three-dimensional high-resolution ultrasound imaging applications, an electronically steerable two-dimensional beamforming processor based on a delay-and-sum computing algorithm is chosen.

The concept of an electronically-adjustable acoustic conformal lens is to divide the surface of a 2D transducer array into plane "tiles" of relatively small subarrays. As described in U.S. 6,292,433 the entire contents of which incorporated herein by reference, and illustrated in Fig. 1 the tiles/subarrays 120 are made small enough so that when an object is placed within the field-of-view of the imaging system, the incident radiation 122 from the object toward each "tile" can be treated using a far-field approximation. Additional delay elements are incorporated as second-stage processing to allow all subarrays to be coherently summed (i.e., global near-field beamforming can be achieved by

simply delaying and then summing the outputs from all subarrays.) The delay-and-sum beamformer allows each subarray to "look" for signals radiating from a particular direction. By adjusting the delays associated with each element of the array, the array's look direction can be electronically steered toward the source of radiation. Thus instead of looking in one direction as seen at 124a, the direction of tiles 120 can be steered in different direction 124b. The delay line requirement for each element in the sub-array can be less than a hundred stages. Only long delays for global summing are needed for the final near field focusing.

To scan an image plane using a steerable beamformer system a process such as that shown in Fig. 2 can be used. A raster scan 260 can be used to scan an image plane 262 using a 2D steerable transducer array 264.

A detailed diagram of an electronically-controlled beamforming system in accordance with the invention is shown in Fig. 3A. This system consists of a bank of parallel time-delay beamforming processors 330, -330N. Each processor 330 consists of two components: a 2D sub-array beamformer 332 for far-field beamsteering/focusing and an additional time delay processor 334 to allow hierarchical near-field beamforming of outputs from each corresponding subarray. The sub-arrays 332 include m-programmable delay lines 340 with tap selectors 342, multiplexers 344 and summed 346 output. As can be seen in Fig. 3A, for a system with n-sub-arrays, n-parallel programmable 2^{nd}-stage near field time delays are needed for individual delay adjustment which are converted with A/D converter 352 to allow all n-parallel outputs be summed 354 coherently, in turn, this summed output is filtered 338 and provides the 3D images of the targeted object. A processor 336 controls sub-array operation.

Use of the scan head with a second stage digital beamformer is shown in Fig. 3B. In this embodiment, a plurality of N sub-array beamformers 400, which can be near-field beamformers in a preferred embodiment, each receive signals from m transducer

elements that have separate delay lines whose outputs are summed and provided to beamformers 420 so that this beamformer can be a conventional system with conventional processor 480. A separate sub-array processor 460 controls beamformers 400.

Without using this hierarchical subarray far-field and then near-field beamforming approach, for an 80x80 element 2D array, a cable consisting of six thousand and four hundred wires is needed to connect the transducer array to a conventional beamforming system. As shown in Fig. 3A, the number of inputs to each subarray processor equals the total number of delay elements in the subarray, each sub-array only has a single output. The number of inputs to the subarray bank equals the number of 2D array elements, and the number of outputs from the subarray bank equals to the total transducer array element number divided by the subarray element number, i.e., the number of outputs from the subarray bank reference to the number of inputs is reduced by a factor equal to the size of the subarray. For example, if one selects to use a 5x5 subarray to implement this hierarchical beamforming concept, after the first stage subarray beamforming, the total number of wires needed to connect to the 2^{nd} stage near-field beamforming is reduced by a factor of 25. More specifically, as mentioned above, without using this 2D subarray beamforming, 6400 wires are needed to connect an 80x80 element 2D transducer array to a conventional back-end beamforming system. Using a 5x5 subarray processing bank first, the number of wires required to connect to the backend beamforming system is reduced to 256. Based on the current invention, a bank of 256 5x5 element subarrays Beamformer can be integrated with a 80x80 element 2D array in the scan head, so a cable consisting of 256 wires is adequate to connect the integrated scan head with the back-end near-field beamforming system. It is important to note that 5x5 subarray far-field beamforming processors can be easily integrated in a small size silicon (Si) integrated circuit, eight of such 5x5

subarray beamformers can be integrated on one chip. In this embodiment, only 32 chips or less are integrated into the scan head, thereby reducing the cable size from 6,400 wires down to 256 wires.

The beamformer processing system is a time domain processor that can simultaneously process the returns of a large 2D array providing a low-power, highly integrated beamformer system capable of real time processing of the entire array in a portable system. While a system with 192 parallel received channels supports a matrix 2D array probe for a real-time 3D/4D imaging application, the hierarchical multi-stage beamforming can be used with a low-power compact ultrasound system.

Fig. 3B demonstrates the hierarchical beamforming architecture in which the beamforming of a group of neighboring receive elements is implemented in two stages, i.e., instead of a single long delay for each of the receive elements, a common long delay is shared by all elements within the group, but each has its own shorter, programmable delay in front of the long delay. Within each group, the outputs from each of the short delays are summed together then applied to the common long delay. A small group of neighboring receiving elements having this common long delay characteristic is defined as a "subarray" of the transducer array. For example, for application using a 2D matrix array for real-time 3D imaging, the subarray can be a small array with 4x4, or 5x5 adjacent elements. The first stage programmable delays of each element within this subarray are integrated inside the transducer probe; the summed output from each subarray is then connected to the backend processor. So, for a 64x48 element 2D array (3072 or more transducer elements), if a 4x4 subarray is used for the first stage beamforming, only 192 I/O cable elements are needed to connect the front-probe to the backend processors.

In a preferred embodiment, the hierarchical beamforming can also be applied to a one dimensional (1D) array for real-time 2D

imaging application. For example, for a 128-element 1D array, a group of 8 adjacent elements can be grouped together as a subarray. Within each subarray, each of the 8 elements has its own short programmable delay and then the outputs of the eight delays are summed together and then applied to a common long delay. It is important to note that two different methods that can be used for this two-stage implementation. In the first implementation, all the beamforming circuits including both the short and long delays are placed in the back-end processor, so for a 128 element 1D array, 128 connection cables are used as I/O cables between the transducer probe and the backend processor. An alternative implementation is to integrate all the subarray processors within the transducer probe, i.e., for a 128-element array, all 16 subarray processors each with 8 programmable delays are integrated within the transducer probe, so only 16 cable elements are needed to connect the front-end integrated probe with the back-end processors. Within the back-end, only 16 long delay beamforming circuits are needed to complete the beamforming function. Similarly, for a 64-element array with integrated eight 8-element subarray processors in the probe, the back-end processor can be simplified to only 8 beamforming circuits, only 8 cable elements are needed to connect the front-end integrated probe with the back-end processor. Furthermore, low-power transmit circuit and A/D converters can be integrated into the front-end probe, so a wireless communication can be used to connect the front-end probe and the back-end processor. A wireless USB connection or a wireless FireWire connection can be used.

The construction of a 64x48 element 2D transducer probe 485 with integrated 4x4 sub-array processors is illustrated in Fig. 3C. The 64x48element 2D array 487 can include stacking 48 rows of 1D arrays each with 64 elements. Connections to the elements of each 64 element 1D transducer array are through a flex cable, so the transducer head assembly can include the 2D transducer

array and 48 flex cables 486. As shown in Fig. 3C, each sub-array can include 4x4 elements (or other rectangular or 2D geometry preferably having at least 16 elements and up to 256 elements per subarray), the 48 flex cables are grouped into 12 groups, with each adjacent four flex cables connected to a printed circuit board, i.e., flex cables corresponding to the row 1 and row 4 1D transducer array are connected to the first printed circuit board 488, the row 5 to row 8 flex cables are connected to the second printed circuit board 487 and so forth, until the row 45 to row 48 flex cables are connected to the twelfth printed circuit board. One end of each flex cables is connected to the transducer elements and the other end of the flex cable is connected to a 64-element flex connector mounted on the printed circuit board. Within each printed circuit board, there are a 16 4x4 element subarray processors 489 and a high voltage multiplexor chip 491. The subarray processor consists of 16 parallel programmable delay lines each with a low-noise pre-amplifier at its input and a separated programmable multiplier as apodizer and the outputs of the 16 multipliers are summed together to form a single outputs. Within each board, there is also a high-voltage multiplex chip, so to allow the 4x64 element transducer either operated in transmit or receive mode. A memory chip 490 is also mounted on each printed circuit board to store the programming delay for each of the delay lines. There are also power supply cables and digital inputs 492 connected through interface 495 to each printed circuit boards.

An implementation of 64 element 1D array with integrated first stage subarray processor can also be implemented using the design of Fig. 3C except that a single 64-element transducer array 491 is connected to a flex cable 497 with one end of the flex cable is connected to each of the transducer element, the other end of the cable is connected to a 64-pin flex connector. The connector is mounted on a printed circuit board. Within the

printed circuit, there are eight 8-element subarray processors. Each subarray processor consists of eight programmable delay lines, each delay line has its separated low-noise pre-amplifer and at the output of the delay line, there is an apodizer, i.e., a multiplier for beamshaping function. The outputs of the eight multipliers are summed together to form a single analog outputs. A high-voltage multiplexer circuit chip is also included on the printed circuit board, so to allow the 64 element transducer either operated in transmit or receive mode. A memory chip is also mounted on the printed circuit board to store the programming delay for each of the delay lines. There are also power supply cables and digital inputs connected to each printed circuit boards.

A preferred embodiment of a 64 element (or more, e.g. 128 or 256 elements) 1D array 496 with integrated subarray processor is shown in Fig. 3D. In this implementation, instead of using a printed circuit board, the subarray processing chip 499a, the high voltage multiplexer circuit chip 449b and the memory chip 449c are mounted on the flexible printed circuit or cable directly (497, 498). The systems described herein can be used with a catheter or probe for insertion within body cavities for cardiac imaging (4D) or other internal organs. The probe or catheter assembly can include a circuit housing with the first plurality of beamformers as described herein.

A preferred embodiment of the invention for a 2D array beamforming, each minimizing noise and cable loss with improved S/N performance, are described in Fig. 4, 5 and 6. In all three implementations, the bank of m parallel subarray beamforming processors 520 and multiplexers 528 are integrated with the 2D transducer array 525 to create a compact, low-noise, scan head 500. Fig. 4 depicts a system that the compact scan head is connected to a dedicated processing module, in which the m-parallel preamp/TGCs 522 transmit/received chips 524 and the 2nd stage time delay processing units 526 are housed. This dedicated

processing module communicates with a host computer 540 via FireWire IEEE 1394 or USB or PCI bus 542. Control and synchronization is performed by the system controller 544 located in the processing module or housing 546. Fig. 5 depicts the same architecture as stated in Fig. 4, except, inside the dedicated processing module, the 2nd stage time delay processing units are specifically implemented by using charge-domain programmable (CDP) time-delay lines 600 in housing 620 that is connected to handheld probe 660 and computer housing 648. Fig. 6B depicts a system that the compact sparse array scan head 700 is connected to a conventional, commercially available time-domain digital ultrasound imaging system 700 with n-parallel beamforming channels 760. It is easy to see that in Fig. 6A, the time-delay processor 720 can also be implemented by using CDP time-delay lines 740. In these embodiments the near-field beamforming is housed 720, 780 in the same housing with other image processing functions. These systems are described in International Application No. PCT/US2007/014526 filed June 22, 2007, designating the United States and U.S. Application No. 11/474,098 filed June 23, 2006, both applications being incorporated herein by reference in their entirety.

By systematically varying beamformer delays and shading along a viewing angle of a 2D transducer array, returned echoes along the line of sight representing the 3D radiation sources can be used to create the scanned image at the scanned angle. The system can provide continuous real-time large area scanned images throughout a large field of view at 20 frames/s or more. At this frame rate, the system can be used to display continuous 3D images vs. time, thus providing 4D information of the scanned object. As shown in Fig. 7 a CDP beamforming chip 810, a time multiplexed computing structure can be used to generate multiple beams, i.e., for each transmit pulse, the bank of 2D subarray beamformers 818 and its corresponding 2nd stage near-field time-delay line are capable of providing multiple beams sequentially. The computing

circuits sequentially generate the delays required for forming K beams. The device operates as follows. Once a set of sampled returned-echoes are loaded in the delay lines with sampling circuits 814, at time t_1, the delays required for forming beam 1 are computed 812 within each module 822 and applied in parallel to all delay lines. The sampled return-echoes with proper delays are coherently summed 802 and filtered 804 to form the first beam. At time t_2, the delays required for forming beam 2 are computed within each module and applied in parallel to all delay lines. The sampled return-echoes with proper delays are coherently summed to form the second beam. The procedure repeats until the Kth beam is coherently formed.

For example, if a computing circuit with 16-serial addressable outputs is built in with the CDP subarray and the 2^{nd} stage time delay lines, for each transmit pulse, 16 beams or scan lines each along a different scan angle can be created. For 256-pulses with a down-range depth of 15cm, the system can generate a 4096-beams with a 64x64 pixel resolution at a frame rate of 20 frames/s. The system is fully programmable; the beamforming electronics can be adjusted to zoom-in to a smaller field-of-view for high-resolution or higher frame rate images. For example, using 192-transmit pulses with the same down-range depth of 15 cm, the system can generate a 3072-beams with a 64x48 pixel resolution at a 30 frame/s frame rate.

The array described addresses ultrasound imaging applications using a two-dimensional 2cm x 2cm array at a frequency of 3 MHZ. The need for resolution on the order of less than half the wavelength dictates as large an aperture as possible that can be housed within a compact package. To interrogate a 90 degree scanning volume and also minimize the impact of grating lobes, an element pitch or separation of less than 0.25 mm is desirable, leading to a 80x80 element array. Using the subarray processing technique described above, a scan head with integrated subarray beamforming circuits followed by a 2^{nd} stage near-field

beamsteering/beamfocusing system provides a practical implementation. However, the implementation still requires at least 32 subarray chips to be integrated on a scan head. An alternative pseudo random array design approach can be used to achieve this resolution with a much less amount of processing components in the scanned head.

To make a sparse array practical, the combination of low insertion loss and wide bandwidth performance is important for realizing acceptable imaging performance with low illumination levels. Quarter-wave matching layers with low acoustic impedance, but physically solid backing results in a robust array that loses only 3-4 dB in the conversion of received signal energy to electrical energy. Array band-widths of 75% or more are typical of this design and construction process. Also, the transducer array employs element positioning and an interconnect system suitable for the beamformer circuitry. The electronics are mounted on printed-circuit boards that are attached to the transducer elements via flexible cables. In practice, a majority of the array elements are connected to outputs using the flexible cables. However, only a small fraction of the total number of elements are wired to the circuit boards. Nevertheless, the large number of array element connections are sufficient to insure a unique pattern of active-element locations in the final array.

As an example of a sparse array, assuming a 2x2 cm array with 256 active elements, the resulting filling factor is 4%. The output signal to noise ratio of the array is proportional to the number of active elements, so this filling factor corresponds to a loss in sensitivity of -13 dB when compared to a filled array of the same dimensions. To compensate for this loss, a transmitted signal of wider bandwidth is chosen to increase array sensitivity. In the approach presented here, the sensitivity is increased on the order of 10 dB. Further details regarding sparse array devices can be found in U.S. Patent No. 6,721,235, the contents of which is incorporated herein by reference.

Positioning the elements of the array follows the approach in which care must be taken to eliminate any periodicity that would produce grating lobes that compete with the main lobe. Pseudorandom or random arrays can be used (FIG. 8A). The geometry of activated element placement has been developed to maximize the efficiency of the beamformers while minimizing grating and side lobe clutter. Switching between a plurality of different array patterns is used to provide the most efficient beam pattern at different beam angles relative to the region or volume of interest being scanned. Thus, a first pattern can utilize that illustrated in Fig. 8A, which is than switched to a second pattern for a different scan angle. This can involve selecting a transducer element within a neighborhood 880 surrounding a given element to scan at a second angle.

The primary goal of the optimization method is to minimize the average side lobe energy. Specifically, this is done by interactively evaluating the optimization criterion:

$$J = \frac{1}{2u_{max}^2} \int\int_s W(u_x, u_y) B(u_x, u_y) du_x du_y, \quad (1)$$

where the weighting function, $W(u_x, u_y)$, applies more weight to regions in the array response that require side lobe reduction. The optimization method begins with no weighting (i.e., $W(u_x, u_y)=1$) and proceeds by choosing successively better weighting functions that satisfy the optimization criterion. Since the side lobes that require the greatest reduction are related to the previously computed beampattern, $B(u_x,u_y)$, the weighting is chosen such that $W(u_x,u_y)=B(u_x,u_y)$. This is done in an interactive manner until convergence.

Basically, a random array is capable of producing an imaging point spread function that has a main lobe to average side lobe ratio of N, where N is the total number of active elements in the

array. For the 256-element sparse array example, the resulting ratio is -13 dB. Using a wide bandwidth approach improves this ratio by 10 dB. Based on the preceding optimization criterion, a pseudorandom placement of the array elements was generated (FIG. 8A).

FIG. 8B is a plot of the array performance, sensitivity versus cross range, for a 256-element sparsely-sampled array at 3 MHZ. The peak to maximum side lobe level is approximately 30 dB. To improve this performance, the system is configured to achieve the maximum main lobe to clutter level ratio possible, which has been independently verified.

FIG. 9B depicts a system that the sparse array scan head 900 is connected to a conventional, commercially available time-domain digital ultrasound imaging system 940 with m-parallel beamforming channels. It is easy to see that in Fig. 9A, the time-delay processor can also be implemented by using CDP time-delay lines 920 in housing 925 that is connected to a separate computer 927. An array of m multiplexers 906 is used to switch between a sequence of scan patterns executed using a software program and system controller 940 or processor 950. The sequence of sparse array patterns is thus selected to scan at different scan angles of an object being imaged to provide 3D ultrasound imaging thereof.

A commercially available window-based 3D visualization software can be used to visualizing, manipulating, and analyzing the 3D multiple-beams volume image data generated by the electronically-adjustable acoustic conformal lens system. Traditionally, a clinician with 2D ultrasound images for diagnosis would look at the 2D scanned images slice by slice and mentally reconstruct the information into a 3D representation to judge the anatomy of the patient. This procedure requires the clinician to have well-founded experience as well as a highly sophisticated understanding of human anatomy. To create a "complete" image to the 3D structures, the clinician has to take all available slices

into account. Looking at hundreds of slices is too time-consuming, even for a single patient. 3D visualization based on 3D volume data can help overcome this problem by providing the clinician with a 3D representation of the patient's anatomy reconstructed from the set of multiple-scanned beamforming data.

A commercially available software tool such as KB-Vol3D of KB-VIS technologies, Chennai, India, provides display or viewing 3D features such as:

- Fast Volume-Rendering
- Shaded Surface Display

Shaded-Surface module allows easy visualization of surfaces in the volume. Surfaces may be created by intensity-based thresholding. Alternatively, the Seeding option allows selection of specific connected structures of interest.

- MIP (Maximum Intensity Projection) with Radials
- MPR (Multiple-Plane-Reformating) with Oblique & Double-Oblique and 3D correlation
- MRP Slabs & Multi-Cuts
- Curved MPR
- Color & Opacity Presets with Editor
- Region-Growing and Volume Measurements
- Cutaway Viewing with Slab-Volume and Interactive Real-time VOI

Volume-interiors are easily visualized using the "Cutaway-Viewing" tool. A Cut-Plane is used to slice through the volume, revealing the interior regions. The cut-plane is easily positioned and oriented using the mouse.

The VOI (Volume-of-Interest) tool allows interactive, real-time Volume-of-Interest display. The user can isolate and view sub-volumes of interest very easily and in real-time, using easy click-and-drag mouse operation.

- Image Save in Multiple Formats

Images displayed by KB-Vol3D can be captured to various image formats (including DICOM, JPEG, and BMP etc.)

- Movie Capture in AVI Format

Visualization operations can also be captured to an AVI movie .le and played on Windows Media Player, QuickTime, and Real Player etc.

The invention can be implemented using a scan head 12 connected to a portable computer 14 as shown in Fig. 10. the ultrasound system 10 can also include a cable 16 to connect the probe 12 to the processor housing 14. Certain embodiments can employ an interface unit 13 which can include a beamformer device. Scan head 12 can include a transducer array 15A (2D) and a circuit housing 15B which can house multiplexer and/or beamforming components as described in detail in U.S. Patent Nos. 6,106,472 and 6,869,401, the entire contents of these patents being incorporated herein by reference.

A 2D array configuration using sparse-array for transmission and non-overlapped fully-populated array is used for receiving. For an NxM element array, only m-elements with optimized sparse array placement are used for transmition and then the remaining NM-m elements are used as the receiving array. For example, for a 40x60-element 2D array, 256-elements are used as transmit element, the placement of the transmit elements are optimized based on selection criteria, the remaining 2144 element are used as received elements. This embodiment simplifies the multiplexer requirement needed for a 2D array, in which case the multiplexer can be mounted in the interface housing.

An example of the element locations for the near fully-populated 40 by 60 receive array 50 is shown in Fig. 11. The 2400-element array is depopulated by the 256 sparse array transmit elements to yield 2144 receive element locations. These elements are independent and do not overlap the sparse-array transmit elements. In a preferred embodiment the transmit elements

constitute less then 25% of the total number of array elements, and preferably less then 15%.

The azimuth and elevation cross-sections of the beampattern of the above mentioned receive array are shown in Fig. 12. The first sidelobe is approximately -13 dB relative to the central peak. The grating lobes are less than -30 dB relative to the peak. Given that the 2D array is wider than tall, the azimuthal beamwidth (plotted in blue (solid)) is slightly narrower than the elevation beamwidth (plotted in green (dotted)).

In Fig. 13, a magnifying view of the above mentioned azimuthal beam pattern demonstrates the detailed mainlobe and sidelobe structure. For this case, the beamwidth is approximately 1.5 degrees. The beam pattern is nearly identical to the fully populated 60x40 element beam pattern. The receive array beam pattern is shown in Fig. 14. As stated above, the received sparse array is comprised of a 2144 elements. There are no sidelobes due to depopulating the center of the array by 256 (transmit) elements.

An example of the final element locations for the 256 transmit sparse array 60 are shown in Fig. 15. The 256 element locations are confined to the central 32x32 elements of the fully populated array. These elements are independent and do not overlap the receive array elements. A cross sectional view of the transmit sparse array beampattern is shown in Fig. 16. The first sidelobe is approximately -17 dB relative to the central peak. The grating lobes are less than -27 dB relative to the peak. The sparse array optimization algorithm minimizes the sidelobe energy +/- 45 degrees in elevation and +/- 45 degrees in elevation.

Fig. 17 demonstrates the beam pattern of the sparse transmit array shown in Fig. 15. The transmit beampattern is designed to uniformly cover a 4x4 beam data pyramid. The transmit sparse array is comprised of a 256-element subset of the fully populated 2400-element array (approximately 10% fill). The placement of the transmit/receive array design algorithm required over 750

iterations to minimize the transmit and receive sidelobe energy within the +/- 45 degree azimuth, +/- 45 degree elevation region. As shown in Fig. 18, after 750 iterations, the final sparse transmit-array element locations limit the average sidelobe energy to less than -35 dB relative to the central peak of the beampattern.

A low-power ultrasound system capable of electronically scanning a two-dimensional, 2D, matrix array to generate real-time three-dimensional, 3D, volumetric images with 64 by 64, 4096, scanning beams at a greater than 20 3D images per second is described. For each transmit pulse, the system is capable of generating 16 received beams. In addition, the design is able to drive a one and one-half dimensional array and also support wide-bandwidth encoded transmit waveform for pulse compressing to improve the system sensitivity. Wide bandwidth enables the use of chirped or coded waveforms (PN sequence) that can extend the length of the low power transmit burst without a loss of axial resolution. The combination of these features results in an imaging array with electronic systems that will fit within a portable hand-carried device.

The beamformer processing system is a time domain processor that will simultaneously process the returns of a large 2D array, the low-power; highly integrated beamformer that provide a real time processing of the entire array and will thus provide a low cost unit that can be hand carried.

There is a strong need for a real-time 3D ultrasound imaging using a 2D matrix array. In this section, the minimal number of receive beamforming channels required in an ultrasound system to support a real-time 3D imaging is analyzed. It is shown that a minimum of 192 parallel received beamforming channels is required to support a reasonable sized such as 48x64-element array.

An example of a system having an electronically-adjustable acoustic conformal lens is to divide the surface of a 2D

transducer array into plane "tiles" of relatively small subarrays can be formed in U.S. Patent No. 6,292,433, the contents of which is incorporated herein by reference; beamforming of the entire array can be separated into two stages, first a small-aperture subarray beamforming followed by a second stage large-aperture coherent summing of the outputs from each of the subarrays. As depicted in the tiles/subarrays can be made small enough so that when an object is placed within the field-of-view of the imaging system, the incident radiation from the object toward each "tile" can be treated using a far-field approximation. However, near-field beamforming capability has been incorporated in the actual implementation of the subarray beamforming system to allow a broader application. Additional delay elements are incorporated as second-stage processing to allow all subarrays to be coherently summed. The delay-and-sum beamformer allows each subarray to "look" for signals radiating from a particular direction. By adjusting the delays associated with each element of the array, the array's look direction can be electronically steered toward the source of radiation. The delay line requirement for each element in the sub-array can be less than a hundred stages. Only long delays for global summing are needed for the final near field focusing. A detailed diagram of an electronically-controlled beamforming system in accordance with the invention is shown in Fig 14A of U.S. Patent No. 6,292,433. This system consists of a bank of parallel time-delay beamforming processors. Each processor consists of two components: a 2D sub-array beamformer for small-aperture beamsteering/focusing and an additional time delay processor to allow hierarchical near-field beamforming of outputs from each corresponding subarray. As can be seen in Fig. 14A referenced above for a system with m-subarrays, m-parallel programmable 2^{nd}-stage near field time delays are needed for individual delay adjustment to allow all m-parallel outputs

be summed coherently, in turn, this summed output provides the 3D images of the targeted object.

It is easy to understand that, without using this hierarchical subarray small aperture and then large aperture beamforming approach, for an 80x80 element 2D array, a cable consisting of six thousand and four hundred wires is needed to connect the transducer array to a conventional beamforming system. As shown in Fig. 14A of U.S. Patent 6,292,433 referenced above, the number of inputs to each subarray processor equals the total number of delay elements in the subarray, each subarray only has a single output. That is to say, the number of inputs to a subarray equals the number of transducer elements associated with that subarray. The number of subarray outputs equals the total transducer array element number divided by the number of subarrays. For example, if one selects to use a 5x5 subarray to implement this hierarchical beamforming system, after the first stage subarray beamforming, the total number of wires needed to connect to the 2^{nd} stage near-field beamforming is reduced by a factor of 25. More specifically, as mentioned above, without using this 2D subarray beamforming, 6400 wires are needed to connect an 80x80 2D transducer array to a conventional back-end beamforming. Using a 5x5 subarray processing bank first, the number of wires required to connect to the backend beamforming system is reduced to 256. Based on this example of the invention, a bank of 256 5x5 element subarrays beamformer can be integrated with a 80x80 element 2D array in the scan head, so a cable consisting of 256 wires is adequate to connect the integrated scan head with the back-end near-field beamforming system.

It is important to note that 5x5 subarray small-aperture beamforming processors can be easily integrated in a small size silicon integrated circuit, eight of such 5x5 subarray beamforming can be integrated on one integrated circuit. Note that subarrays have generally between 9 and 64 transducer

elements corresponding to a 3x3 subarray up to an 8x8 subarray. The preferred range is at or between 4x4 and a 6x6 array for a square array geometry. Rectangular subarrays can also be used preferably either 3x4, 4x5, or 4x6. Note that a 1/4 λ error minimum criteria is uses. Only 32 integrated circuit devices need be incorporated into the scanhead, it can reduce the cable size from 6,400 wires down to 256 wires. Similarly, for a 64x48 element 2D array, using a 4x4 subarray processing bank in the transducer housing first, the number of back-end beamforming channels is reduced to 192.

In the present invention, preferred embodiments for a 2D array beamforming, each minimizing noise and cable loss with improved signal to noise ratio performance, are described in Figs 4-6B. In these embodiments, the bank of m parallel subarray beamforming processors are integrated with the 2D transducer array to create a compact, low-noise, scan head. Fig. 4 depicts a system that the compact scan head is connected to a dedicated processing module, in which the m-parallel preamp/TGCs, transmit/received chips and the 2^{nd} stage time delay processing units are housed. This dedicated processing module communicates with a host computer 540 via FireWire, USB or PCI bus. Control and synchronization is preformed by the system controller located in the processing module. Fig. 5 depicts the same architecture as stated in Fig. 4, except, inside the dedicated processing module, the 2^{nd} stage time delay processing units are specifically implemented by using Charge-Domain programmable time-delay lines. Figs 6A and 6B depicts a system that the compact scan head is connected to a conventional, commercially available time-domain digital ultrasound imaging system with m-parallel beamforming channels. It is easy to see that in Figs 6A and 6B the time-delay processor can also be implemented by using CDP time-delay lines.

In a preferred embodiment of the system a large-aperture beamforming system is incorporated into the main processor housing

of the ultrasound imaging system as shown in connection with Figs 19-24B.

The speed of sound in tissue is about 1500cm/sec so that the round-trip propagation time for a sound wave penetrating a 15-cm depth is about 20 microseconds. For a real-time 3D imaging, at least 64x64 scanning beams at a frame rate greater than 20 3D volumetric images per second are needed to provide diagnostic quality images. For each transmit beam, the real-time 3D imaging system has to be able to form at least 16 beams for each transmit pulse to support the preferred 3D frame rate requirement. In this section, both a serial time-multiplexed beamforming and a parallel simultaneous time-domain beamforming implementation are addressed.

To achieve a 16 beam scanning requirement, a combination of serial and parallel architecture can be used, i.e., the system can use front-end time-multiplexed serial beamforming elements technique to form two beams, then followed by 8 parallel beamforms at the back-end processor, or the system can form 4 serial beams, for each serial output beam, the back-end processor then forms 4 parallel beams, and so forth.

By systematically varying beamformer delays and shading along a viewing angle of a 2D transducer array, returned echoes along the line of sight representing the 3D radiation sources can be used to create the scanned image at the scanned angle. The system can provide continuous real-time large area scanned images throughout a large field of view at 20 frames/s or more. As shown in Fig. 7, in a CDP beamforming chip, a time multiplexed computing structure can be used to generate multiple beams, i.e., for each transmit pulse, the bank of 2D subarrays and its corresponding 2^{nd} stage near-field time-delay line are capable of providing multiple beams sequentially. The computing circuits sequentially generate the delays required for forming K beams. The device operates using the following sequence: once a set of sampled returned-echoes are loaded in the delay lines, at

time t_1, the delays required for forming beam 1 are computed within each module and applied in parallel to all delay lines. The sampled return-echoes with proper delays are coherently summed to form the first beam. At time t_2, the delays required for forming beam 2 are computed within each module and applied in parallel to all delay lines. The sampled return-echoes with proper delays are coherently summed to form the second beam. The procedure repeats until the Kth beam is coherently formed.

For example, if a computing circuit with 16-serial addressable outputs is incorporated with the processor subarray and the 2^{nd} stage time delay lines, for each transmit pulse, 16 beams or scan lines each along a different scan angle can be created. For 256-pulses with a down-range depth of 15cm, the system can generate a 4096-beams with a 64x64 pixel resolution at a frame rate of 20 frames/s. The system is fully programmable; the beamforming electronics can be adjusted to zoom-in to a smaller field-of-view for high-resolution or higher frame rate images. For example, using 192-transmit pulses with the same down-range depth of 15 cm, the system can generate a 3072-beams with a 64x48 pixel resolution at a 30 frame/s frame rate.

The objective of a beamforming system is to focus signals received from an image point onto a transducer array. By inserting proper delays in a beamformer to align wavefronts that are propagating in a particular direction, signals arriving from the direction of interest are added coherently, while those from other directions do not add coherently or cancel. The time-of-flight from the radiation source to the focal point can be calculated and stored in memory for every channel from multiple directions of arrival in parallel. In a conventional implementation, separate electronic circuitry is necessary for each beam; for a multi-beam system, the resulting electronics rapidly become both bulky and costly as the number of beams increases. For example, beamforming for a linear 192 element

array requires 192 parallel delay lines each with a programmable delay length of greater than 128 λ. To form four parallel beams, for example, a total of 768 programmable long delay lines are required. To simplify the required electronics for multiple beams, a hierarchical two stage beamforming system is described.

The concept of hierarchical beamforming is to separate the time-of-flight calculation into two parts: the first part is a short delay for coarse-resolution, small aperture beamforming, followed by a long delay for fine resolution, large aperture beamforming. Shown in Fig. 19 is the 3D differential delay equation for a 2D array. This equation represents differential delay at array element (x_m, y_m) as a function of range and angles Theta and Phi (relative to the center of the 2D array). The equation can be reduced to a 1D array by setting all of the y_m (y coordinates of the element locations) to 0. The differential delay can be constrained to a single plane (instead of a volume) by setting angle Phi=0.

To exemplify operation of a two-stage delays, a differential delay profile must be generated for all elements in the 1D or 2D array. To do this, the differential delay equation is calculated and all of the differential delays as a function of angles Theta and Phi, at a given range, are tabulated. For example, as shown in Fig. 20, the differential delay profile is plotted for an element near the center of a 2D array.

In a 2 stage delay system, the tabulated data from the preceding step are broken into a coarse delay and a fine delay. To determine how to partition the coarse delay and the fine delay, the maximum differential delay error is constrained (typically set to have a maximum differential delay error less than or equal to 1 sample). The tabulated delays (from the preceding step) are also used to determine when a receive element is enabled. For example, Fig. 21 depicts the differential delay error as a function of range for a few elements. The worst case differential delay (the data plotted in blue) is for an element in the corner of a 2D

array (Theta=+45 degs, Phi=+45 degs) attempting to receive image data from the direction Theta=-45 degs, Phi=-45 degs. For this case, the maximum differential delay is greater than the constraint (> 1 sample error); therefore, the element would not be enabled to receive until a range greater than approximately 100 samples.

A block diagram of an hierarchical two-stage parallel beamforming system 958 is shown in Fig. 22A. A two dimensional transducer array 960 of a handheld probe, such as 12 in Fig. 10 weighing less than 15 lbs, can be coupled to amplifier 962 before being connected to the input of the beamforming system 964. The beamforming system can comprise a plurality of short delay lines, which are coherently summed at summing circuit 968 where the output is delivered the longer delay lines 970, which are also summed at summing circuit 972. First stage coarse beamforming includes coherently summing returned echoes from a small aperture, for example, with 8 neighboring receivers in this particular embodiment. Because of the small size of the aperture, the delay length of each short delay is only about 8 λ. So, for a 192 element inputs, 24 such small aperture, coarse beams are formed. Each of those 24 beams is then applied to its corresponding long programmable long delay line for a large aperture, fine-resolution beamforming. To form four parallel beams, four such beamforming structures are required. As can be seen in Fig. 22A, this hierarchical implementation to form 24 coarse beams, only 192 short delays are required, and then followed by 24 long delays, each one with a programmable delay length shorter than 128 λ. For four parallel beams, only 192 short delays plus 96 long delays are needed, it offers a tremendous saving in terms of electronic components and power.

Furthermore, within each small-aperture, short-delay line, a time-of-flight control circuit is used to select the tap position output from a charge-domain processing circuit that non-destructively senses the tapped-delay line output. Each

receiver has a multiplier for beam shading/apodization. Within each processor, all the multipliers share a common output. The summed charge is then applied to a matched filter to decode and to compress the returned echoes to produce an imaging pulse with a reduced signal-to-noise ration. An analog to digital (A/D) or a converter on-chip charge-domain A/D converter can be used so that hierarchical summing can be carried out digitally.

In a preferred embodiment, it is important to employ high speed digital communication connection between the beamformer output and the backend processor. As described previously, the analog returned echoes received by each transducer element is converted to a digital signal by an analog to digital converter (A/D) during signal processing. As shown in the beamformer 974 of Fig. 22B, A/D converters 976 can be used at the input of each short delay line and the time delays performed digitally. Or alternatively, as shown in the embodiment 980 of Fig. 22C, the A/D converters 982 can be used at the output of each coarse beam and the long delay can be performed digitally. The A/D conversion can be performed using available discrete components, or in a preferred embodiment, a charge domain A/D converter can be formed on the same integrated circuit with the charge domain beamformer with hierarchical summing carried out digitally.

The use of coded or spread spectrum signaling has gained tremendous favor in the communications community. It is now routinely used in satellite, cellular, and wire-line digital communications systems. Shown in Fig. 23A is an example of a 5 cycle 3 MHz sinusoid without spread spectrum coding. A coded or spread spectrum system transmits a broadband, temporally elongated excitation signal with a finite time-bandwidth product. The received signal is decoded to produce an imaging pulse with improved signal to noise ratio. The benefit of using coded signals in ultrasound imaging systems offers the use of high-resolution imaging while significantly lowering the peak acoustic power. These signals also provide signal processing

gain that improves the overall system receiving sensitivity. Direct sequence modulation is the modulation of a carrier by a code sequence. In practice, this signal can be AM (pulse), FM, amplitude, phase or angle modulation. It can also be a pseudorandom or PN sequence that can comprise a sequence of binary values that repeat after a specified period of time.

In ultrasound, the concept of using spread spectrum/coded excitation transmit waveform comprises modulating a base sequence of transmit pulses of length P with a code sequence with a code length N. A code pulse sequence of N bursts is often referred to as an N-chip code. An example of a gated 3 MHz sinusoid with a 5-Chip Barker coding [111-11] is shown in Fig. 23B. Each "chip" corresponds to 1 cycle of the gated transmit waveform. Thus, Fig. 23B appears nearly identical to that of Fig. 23A except that the 4^{th} cycle is inverted. In both Fig. 23A and Fig. 23B, the continuous line represents the continuously sampled sinusoidal waveform, whereas the cross hatched points is a sampled signal, where 10 samples are taken per cycle. The coded pulse sequence, which has a length NxP, can effectively reduce the peak power in the transmitting media by spreading the power spectrum over a longer time duration. Upon reception of the spread spectrum/coded returned echoes, a pulse compression matched filter can be used to decode the received signals to produce an imaging pulse that has improved signal to noise ration (SNR). The SNR improvement of a NxP coded pulse sequence is 10 log(NP). So, for a Barker code of length 7 and a two-cycle burst transmit waveform, a SNR of 11.4dB improvement can be achieved. However, in the present system, the transmit and received waveforms are oversampled with an oversampled rate of S. Typically an oversampled rate of S=4 has been used. It follows then, at the receiver end, a matched filter with tap length of NxPxS can be used to decode and to compress the returned echoes to produce an imaging pulse with a SNR improvement of 10log(NPS). In the above example, for N=7, P=2, S=4, a SNR of 17.5dB can be achieved.

A preferred method of forming a transmission signal is shown in Figs. 24A-24C. The base sequence is a single pulse, as can be seen in Fig. 24A. Using the 5-chip Barker code [111-11], Fig. 24B represents the convolution of the base sequence with the Barker code. Finally, the system transmits an oversampled version of the continuous waveform, as shown in Fig. 24C, a 6-times oversampled waveform is used as transmitted wave from

A 192 channel receive beamforming system capable of forming four parallel, compressed beams for each transmitted, spreaded coded excited waveform is shown in the beamformer system 985 of Fig. 25A. In this implementation, a two-stage hierarchical beamforming architecture is used, first a small aperture short delay beamformer 986 output signals that are coherently summed return echoes from 8 adjacent transducers, a pulse compression matched filter 987 is then followed to decode the received signal, this compressed signal 988 is then applied to a long delay line to complete the beamforming requirement. In system 990 of Fig. 25B, an A/D converter 992 is incorporated at each of the matched filter outputs. It follows then the long delay will be carried out digitally, using a second stage digital delay line implementation.

A matched filter implementation is shown in Fig. 25C. The filter 994 consists of a K-stage tapped delay line receiving signals from sampling circuit 995 and K programmable multipliers. The spreaded, coarse beamformed signal, f_n, is continuously applied to the input of the delay line. At each stage of the delay, the signals can be non-destructively sensed and multiplied by a tap weight 996, W_k, where k=1, 2, 3, .., K-2, K-1, K. The weighted signals are summed together with summing circuit 997 to create a compressed output g_m 998. It can be seen that, at time t=n,

$$g_n=f_{n-1}W_1+f_{n-2}W_2+f_{n-3}\,W_3+\ldots.+f_{n-K-2}W_{K-2}+f_{n-K-1}W_{k-1}+f_{n-K}W_K$$

Using the example shown in Figs. 24A-24C, if the system transmit a 6-time oversampled, 5-chip Barker code, and the weights

of the matched filter are selected as a time reversal of the transmitted 5-chip Barker code excitation waveform, the matched filter produces a cross correlation output 999 that is the compressed, decoded pulsed signal (see Fig. 25D), with a filter gain of 10log(5x6)=15dB.

The claims should not be read as limited to the recited order or elements unless stated to that effect. All embodiments that come within the scope and spirit of the following claims and equivalents thereto are claimed as the invention.

CLAIMS

What is claimed is:

1. A medical ultrasound imaging system comprising:

a two dimensional transducer array in a probe housing and a first plurality of subarray beamformers in the probe housing;

a second plurality of beamformers in a second housing, the second plurality of beamformers being in communication with the probe housing, the second beamformers receiving first image data from the first plurality of subarray beamformers having a plurality of second delay lines that receive first image data, plurality subarray beamformers operating in parallel to provide three dimensional image data.

2. The system of claim 1 further comprising a plurality of multiplexor circuits in the probe housing.

3. The system of claim 1 wherein the array of transducer elements operates as a sparse array.

4. The system of claim 1 wherein the beamformer device comprises coarse and fine delay elements.

5. The system of claim 1 wherein the second beamformer comprises a second stage beamformer.

6. The system of claim 5 further comprising a third stage beamformer.

7. The system of claim 1 wherein the system weighs less than 15 lbs.

8. The system of claim 7 wherein the system comprises a transducer array in a probe housing that is connected to a processor housing.

9. The system of claim 1 further comprising a sparse array transmission system.

10. The system of claim 1 further comprising a sparse array receiver system.

11. The system of claim 1 further comprising a matched filter.

12. The system of claim 1 further comprising a program performing a transmission waveform that is oversampled.

13. The system of claim 1 wherein the probe housing further comprises a plurality of flexible cables, each cable connecting a transducer subarray to a circuit board.

14. The system of claim 1 wherein the probe housing encloses a plurality of circuit boards, each circuit board having at least one of the first plurality of subarray beamformers, a memory that stores beamformer control data and a multiplexor circuit.

15. The system of claim 1 further comprising a flexible circuit.

16. The system of claim 15 wherein the flexible circuit comprises a flexible cable.

17. The system of claim 15 wherein the flexible circuit comprises a flexible printed circuit.

18. The system of claim 11 wherein the matched filter comprises a plurality of weights associated with stages of a delay line.

19. The system of claim 1 wherein each beam in the plurality of subarray beamformers is compressed.

20. The system of claim 1 wherein the second plurality of beamformers comprise a plurality of digital beamformers.

21. The system of claim 20 wherein the first plurality of beamformers comprise charge domain processors.

22. The system of claim 1 further comprising a program for storing a spread spectrum excitation waveform.

23. The system of claim 1 further comprising a system processor for performing scan conversion.

24. The system of claim 1 further comprising a system processor for performing Doppler processing.

25. The system of claim 1 wherein the probe housing further comprises a catheter or probe body with the transducer array mounted on a distal region.

26. The system of claim 1 wherein the system comprises a cardiac imaging system.

27. The system of claim 1 wherein the second housing comprises a processor housing, a display and a control panel weighing less than 15 lbs.

28. A medical ultrasound imaging system comprising:

an array of transducer elements in a probe housing, the probe housing including a first beamformer device;

a second beamformer device in a second housing, the second beamformer device being in communication with the probe housing, the second beamformer device receiving first beamformed image data from first subarrays, the second beamformer device having a plurality of second beamformers, the first subarrays operating in parallel to provide image data.

29. The system of claim 28 wherein the array of transducer elements comprises a single linear array.

30. The system of claim 28 wherein the array of transducer elements is connected with a flexible circuit having the first beamformer device mounted thereon.

31. The system of claim 28 wherein the beamformer device comprises coarse and fine delay elements.

32. The system of claim 28 wherein the second beamformer comprises a second stage beamformer.

33. The system of claim 32 further comprising a third stage beamformer.

34. The system of claim 28 wherein the system comprises a system processor, a display and a control panel that weighs less than 15 lbs.

35. The system of claim 28 wherein the system comprises a probe housing that is connected to a processor housing.

36. The system of claim 28 further comprising a flexible circuit board in the probe housing.

37. The system of claim 28 further comprising a flexible cable in the probe housing that connects the transducer array to a circuit board assembly.

38. The system of claim 28 further comprising a matched filter.

39. The system of claim 28 further comprising a program performing a transmission waveform that is oversampled.

40. The system of claim 34 wherein the system processor is programmed to perform scan conversion and Doppler processing.

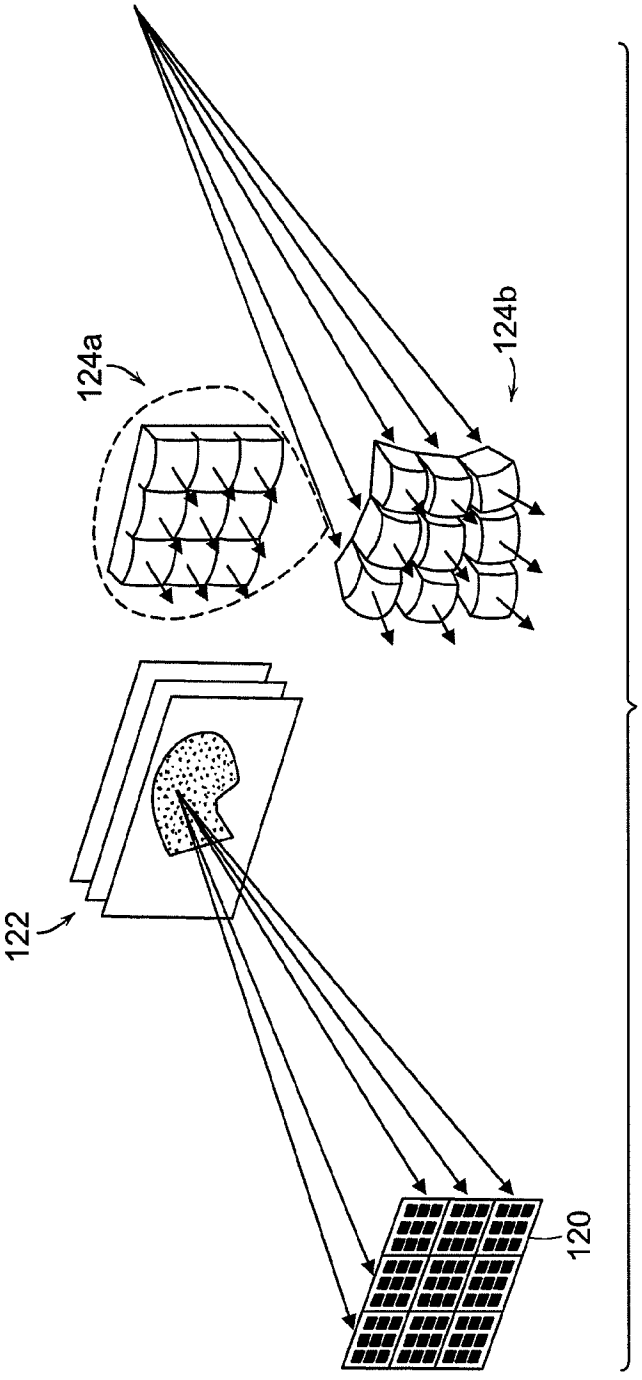


FIG.1

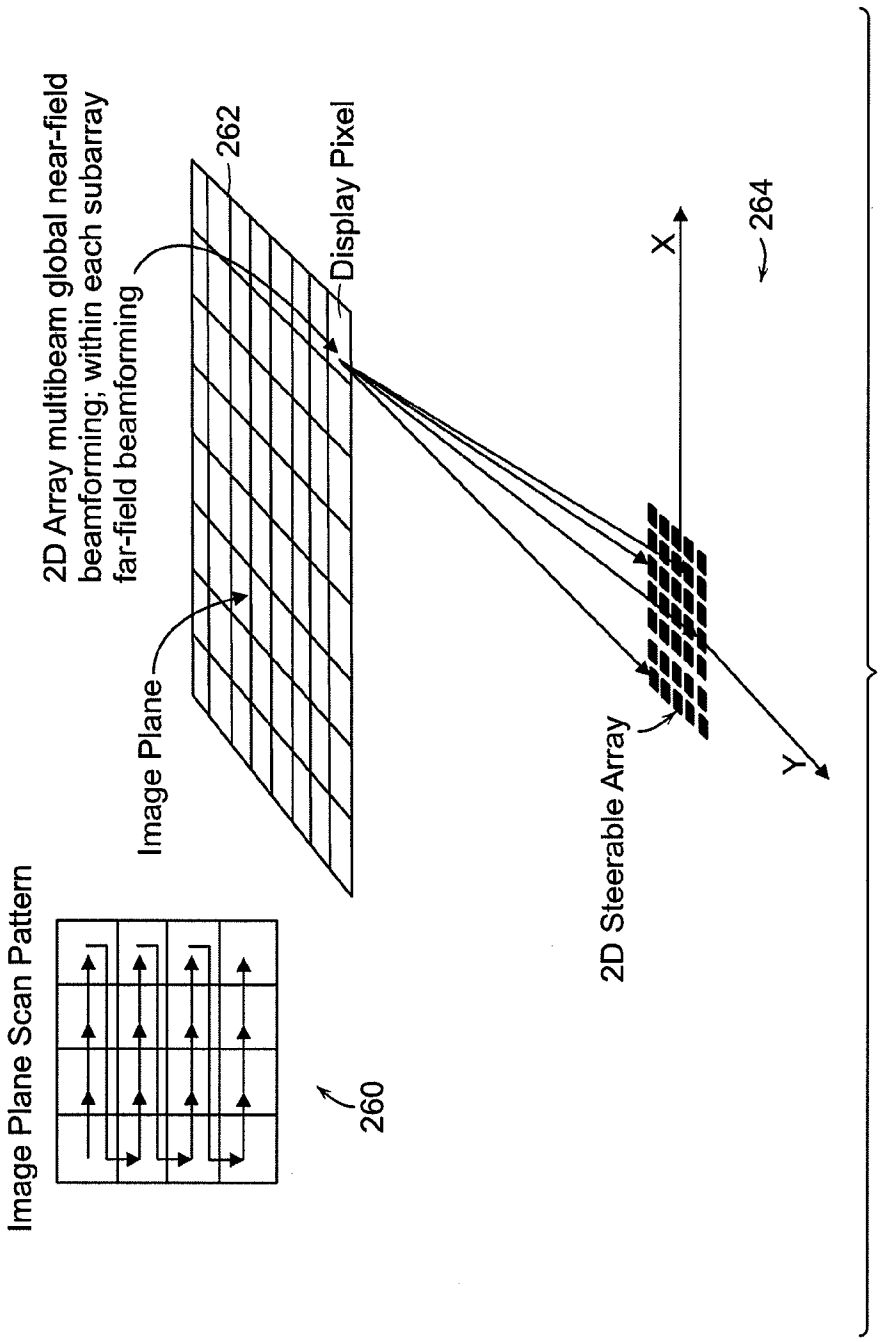


Image Plane Scan Pattern
260
Image Plane
2D Array multibeam global near-field beamforming; within each subarray far-field beamforming
262
Display Pixel
2D Steerable Array
X
Y
264

FIG. 2

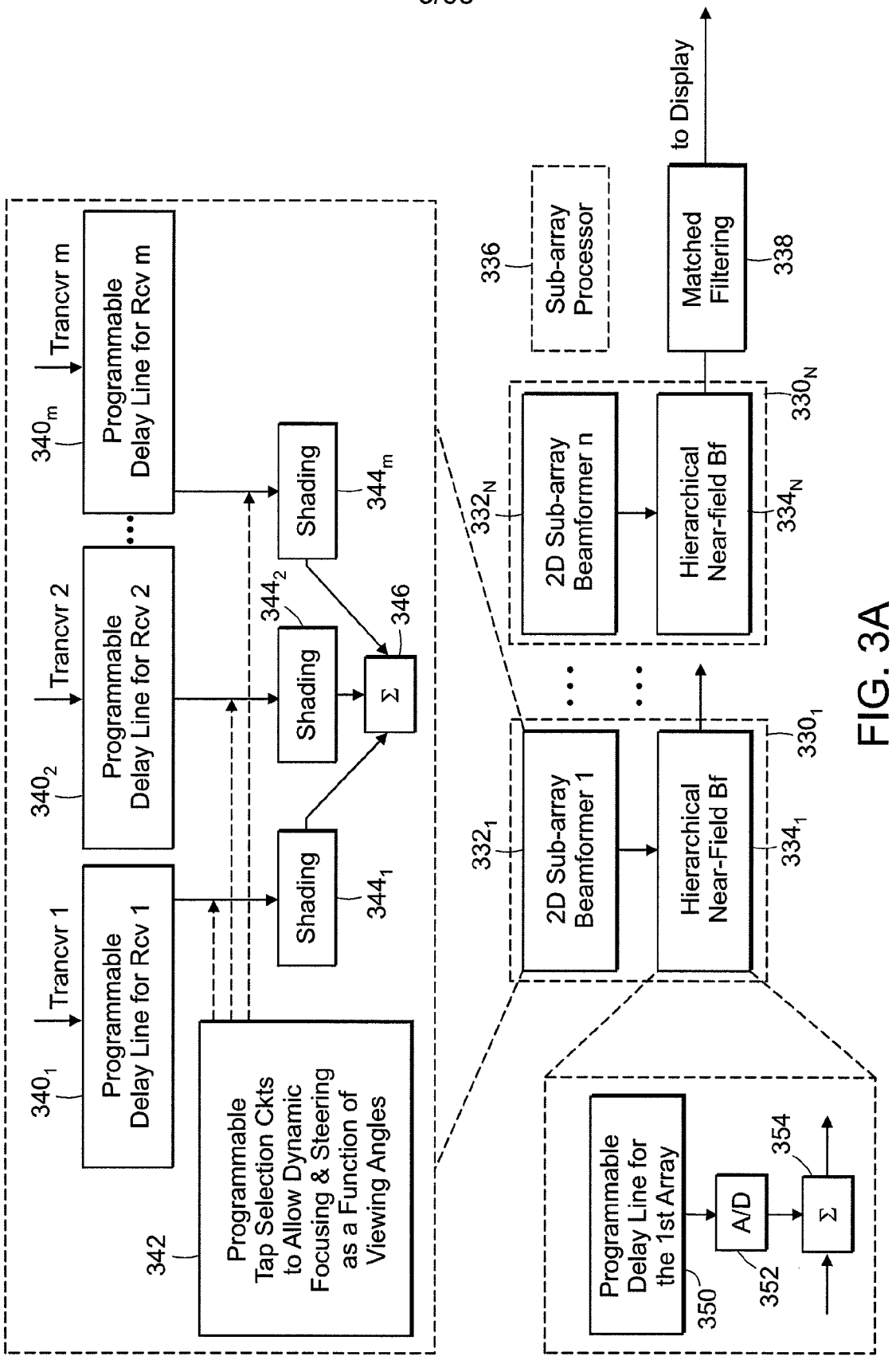

Trancvr 1
Trancvr 2
Trancvr m
Programmable Delay Line for Rcv 1
Programmable Delay Line for Rcv 2
Programmable Delay Line for Rcv m
340_1
340_2
340_m
Shading
344_1
344_2
344_m
Σ
346
Programmable Tap Selection Ckts to Allow Dynamic Focusing & Steering as a Function of Viewing Angles
342
2D Sub-array Beamformer 1
2D Sub-array Beamformer n
332_1
332_N
Hierarchical Near-Field Bf
Hierarchical Near-field Bf
334_1
334_N
330_1
330_N
Sub-array Processor
336
Matched Filtering
338
to Display
Programmable Delay Line for the 1st Array
350
A/D
352
354
Σ

FIG. 3A

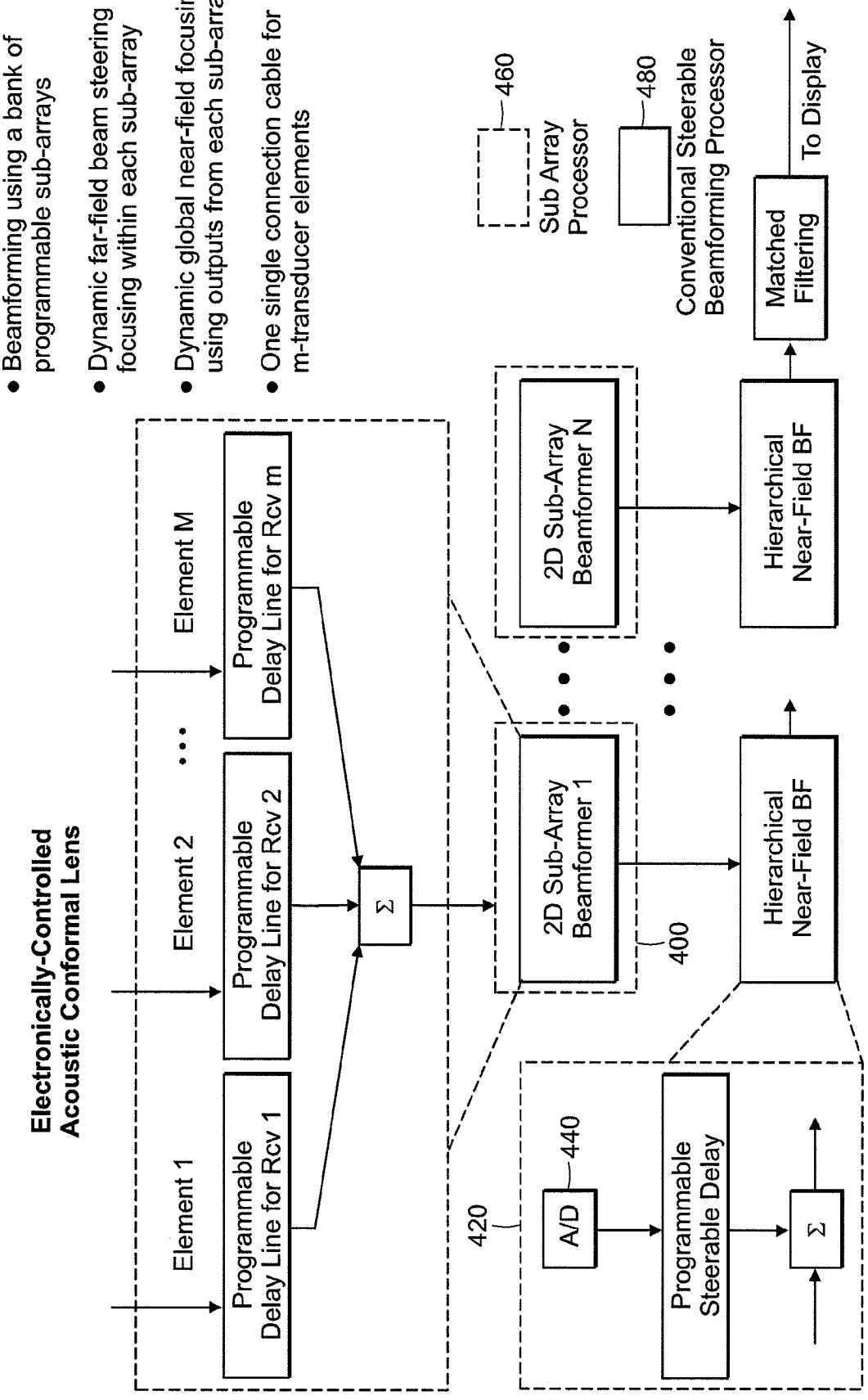

• Beamforming using a bank of programmable sub-arrays
• Dynamic far-field beam steering focusing within each sub-array
• Dynamic global near-field focusing using outputs from each sub-array
• One single connection cable for m-transducer elements
Electronically-Controlled Acoustic Conformal Lens
Element 1
Element 2
Element M
Programmable Delay Line for Rcv 1
Programmable Delay Line for Rcv 2
Programmable Delay Line for Rcv m
Σ
2D Sub-Array Beamformer 1
2D Sub-Array Beamformer N
400
420
A/D
440
Programmable Steerable Delay
Σ
Hierarchical Near-Field BF
Hierarchical Near-Field BF
460
Sub Array Processor
480
Conventional Steerable Beamforming Processor
Matched Filtering
To Display

FIG. 3B

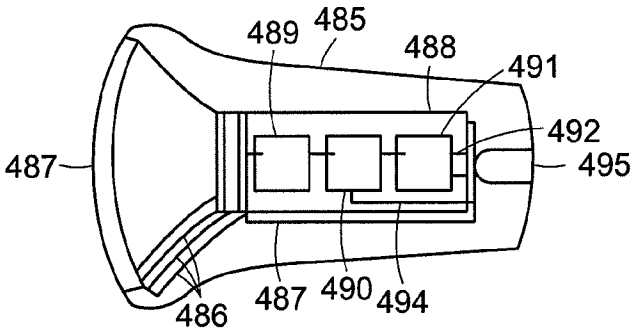

489
485
488
491
492
487
495
487
490
494
486

FIG. 3C

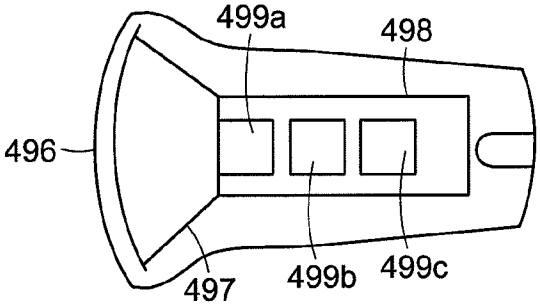

499a
498
496
497
499b
499c

FIG. 3D

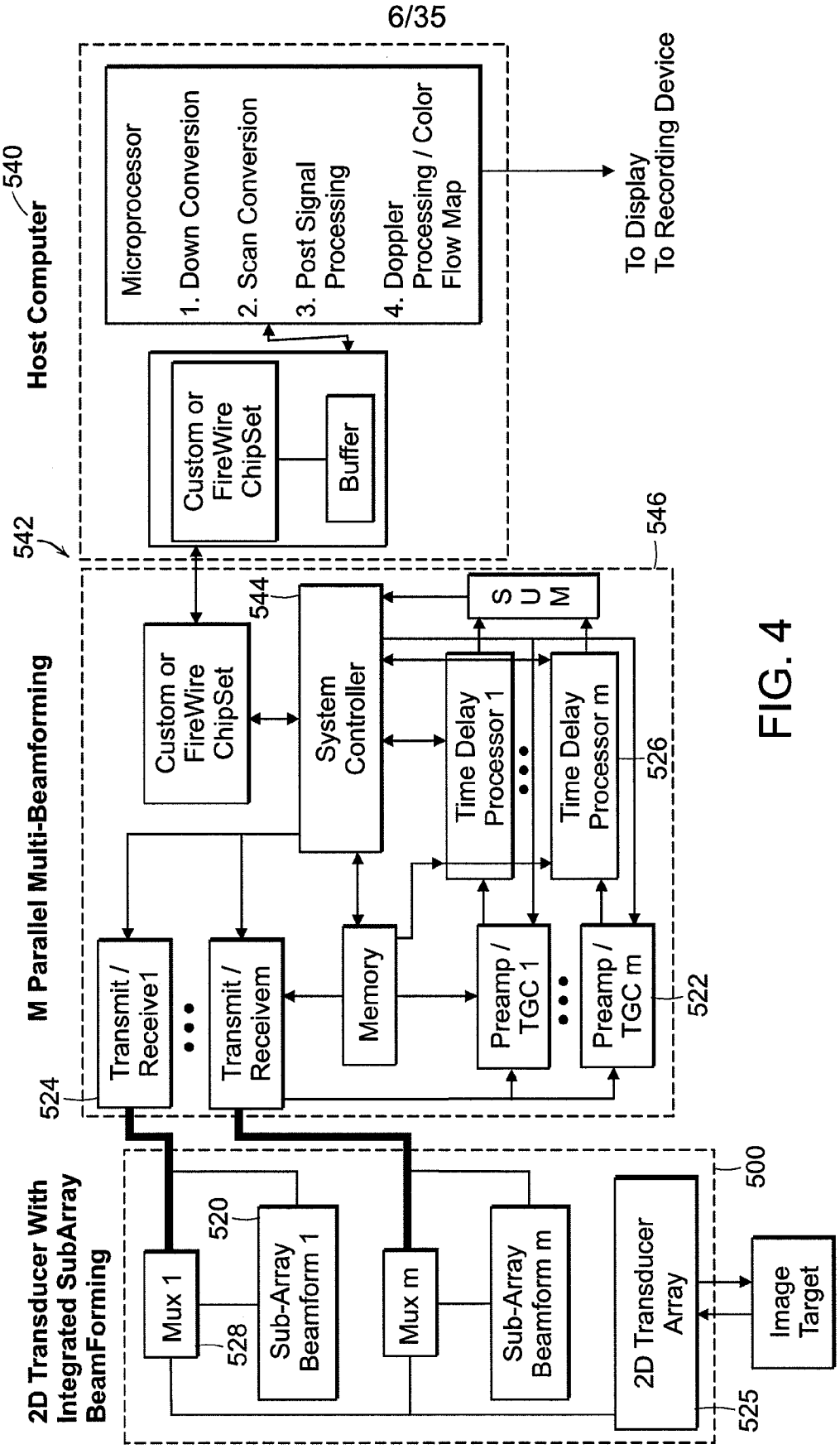

Host Computer
540
Microprocessor
1. Down Conversion
2. Scan Conversion
3. Post Signal Processing
4. Doppler Processing / Color Flow Map
To Display
To Recording Device
Custom or FireWire ChipSet
Buffer
542
546
M Parallel Multi-Beamforming
544
Custom or FireWire ChipSet
System Controller
S U M
Time Delay Processor 1
Time Delay Processor m
526
Transmit / Receive1
Transmit / Receivem
Memory
Preamp / TGC 1
Preamp / TGC m
522
524
2D Transducer With Integrated SubArray BeamForming
520
Mux 1
Sub-Array Beamform 1
528
Mux m
Sub-Array Beamform m
2D Transducer Array
500
525
Image Target

FIG. 4

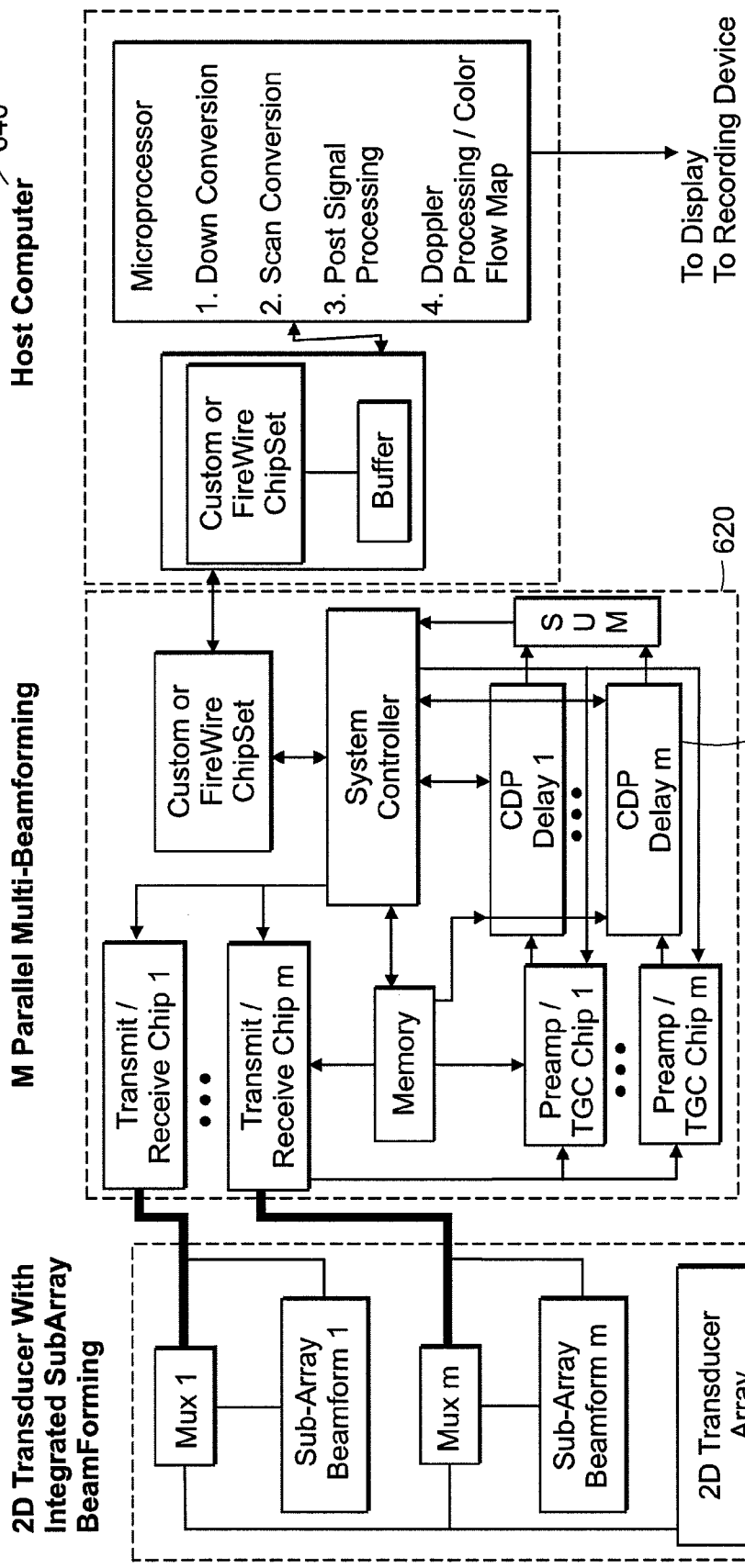

Host Computer
640
Microprocessor
1. Down Conversion
2. Scan Conversion
3. Post Signal Processing
4. Doppler Processing / Color Flow Map
To Display
To Recording Device
Custom or FireWire ChipSet
Buffer
620
M Parallel Multi-Beamforming
Custom or FireWire ChipSet
System Controller
S U M
CDP Delay 1
CDP Delay m
600
Transmit / Receive Chip 1
Transmit / Receive Chip m
Memory
Preamp / TGC Chip 1
Preamp / TGC Chip m
2D Transducer With Integrated SubArray BeamForming
660
Mux 1
Sub-Array Beamform 1
Mux m
Sub-Array Beamform m
2D Transducer Array
Image Target

FIG. 5

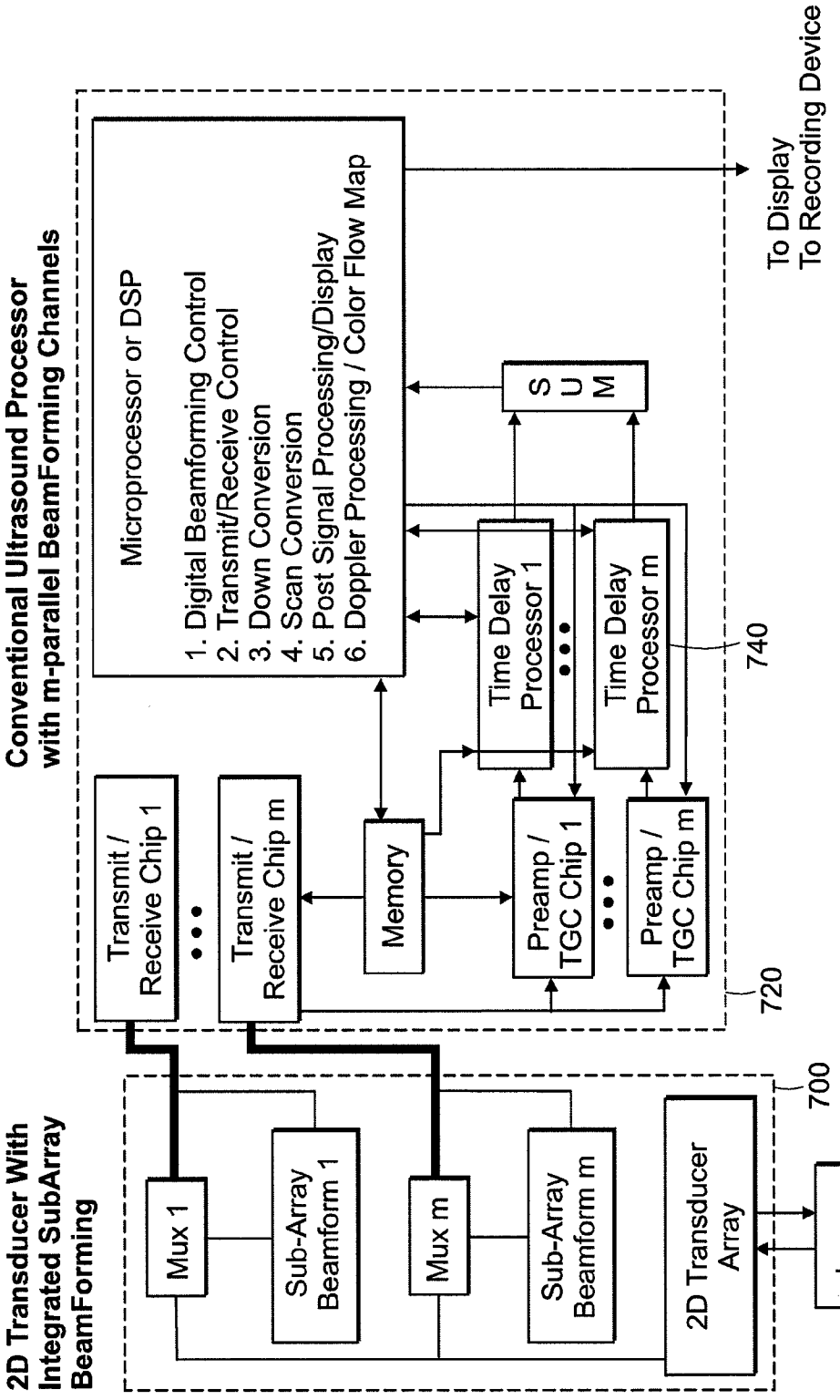

2D Transducer With Integrated SubArray BeamForming
Conventional Ultrasound Processor with m-parallel BeamForming Channels
Microprocessor or DSP
1. Digital Beamforming Control
2. Transmit/Receive Control
3. Down Conversion
4. Scan Conversion
5. Post Signal Processing/Display
6. Doppler Processing / Color Flow Map
To Display
To Recording Device
Transmit / Receive Chip 1
Transmit / Receive Chip m
Memory
Time Delay Processor 1
Time Delay Processor m
S U M
Preamp / TGC Chip 1
Preamp / TGC Chip m
Mux 1
Mux m
Sub-Array Beamform 1
Sub-Array Beamform m
2D Transducer Array
Image Target
700
720
740

FIG. 6A

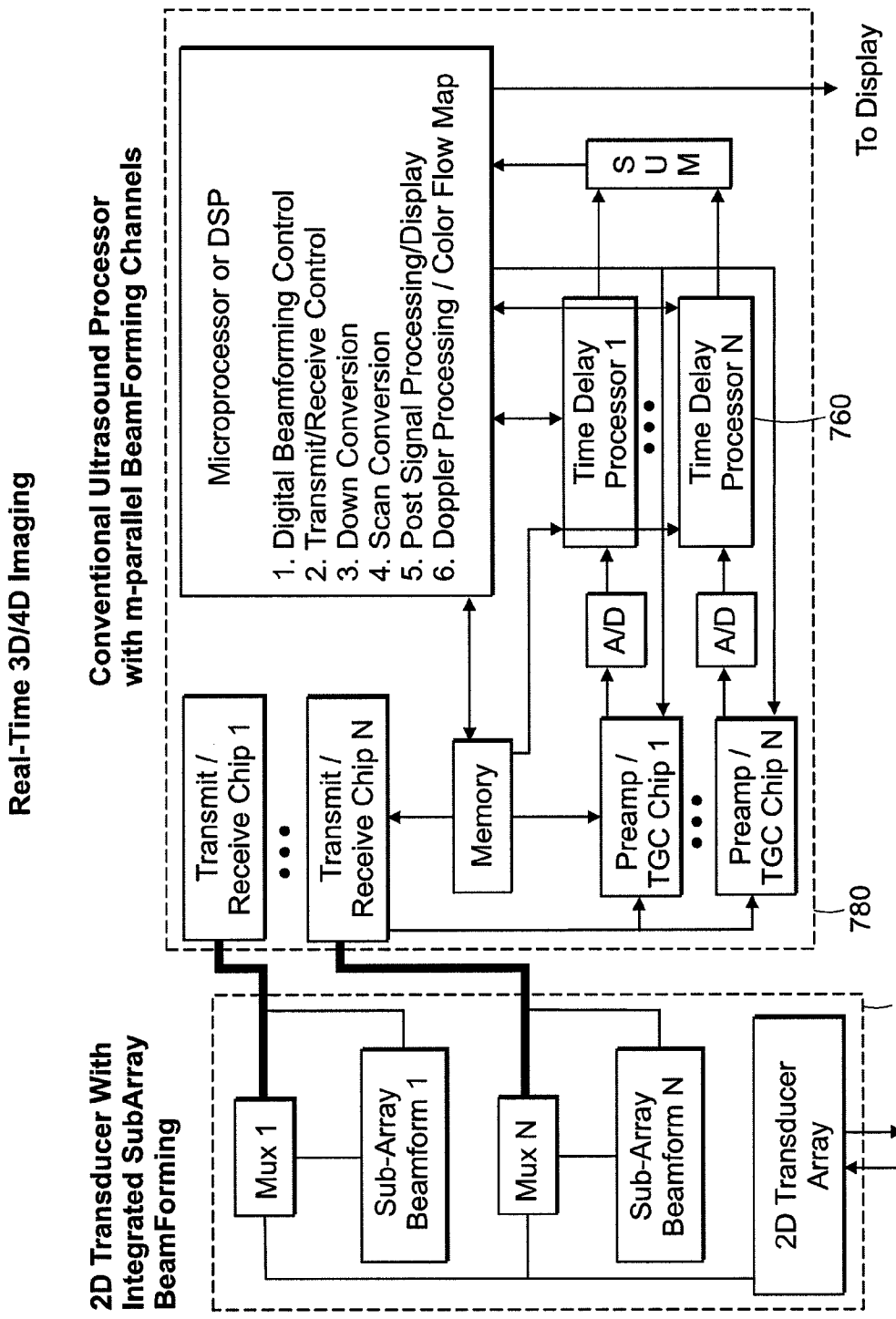

Real-Time 3D/4D Imaging
Conventional Ultrasound Processor
with m-parallel BeamForming Channels
2D Transducer With
Integrated SubArray
BeamForming
Microprocessor or DSP
1. Digital Beamforming Control
2. Transmit/Receive Control
3. Down Conversion
4. Scan Conversion
5. Post Signal Processing/Display
6. Doppler Processing / Color Flow Map
To Display
Transmit / Receive Chip 1
Transmit / Receive Chip N
Memory
Preamp / TGC Chip 1
Preamp / TGC Chip N
A/D
A/D
Time Delay Processor 1
Time Delay Processor N
S U M
760
780
Mux 1
Mux N
Sub-Array Beamform 1
Sub-Array Beamform N
2D Transducer Array
700
Image Target
N = 192

FIG. 6B

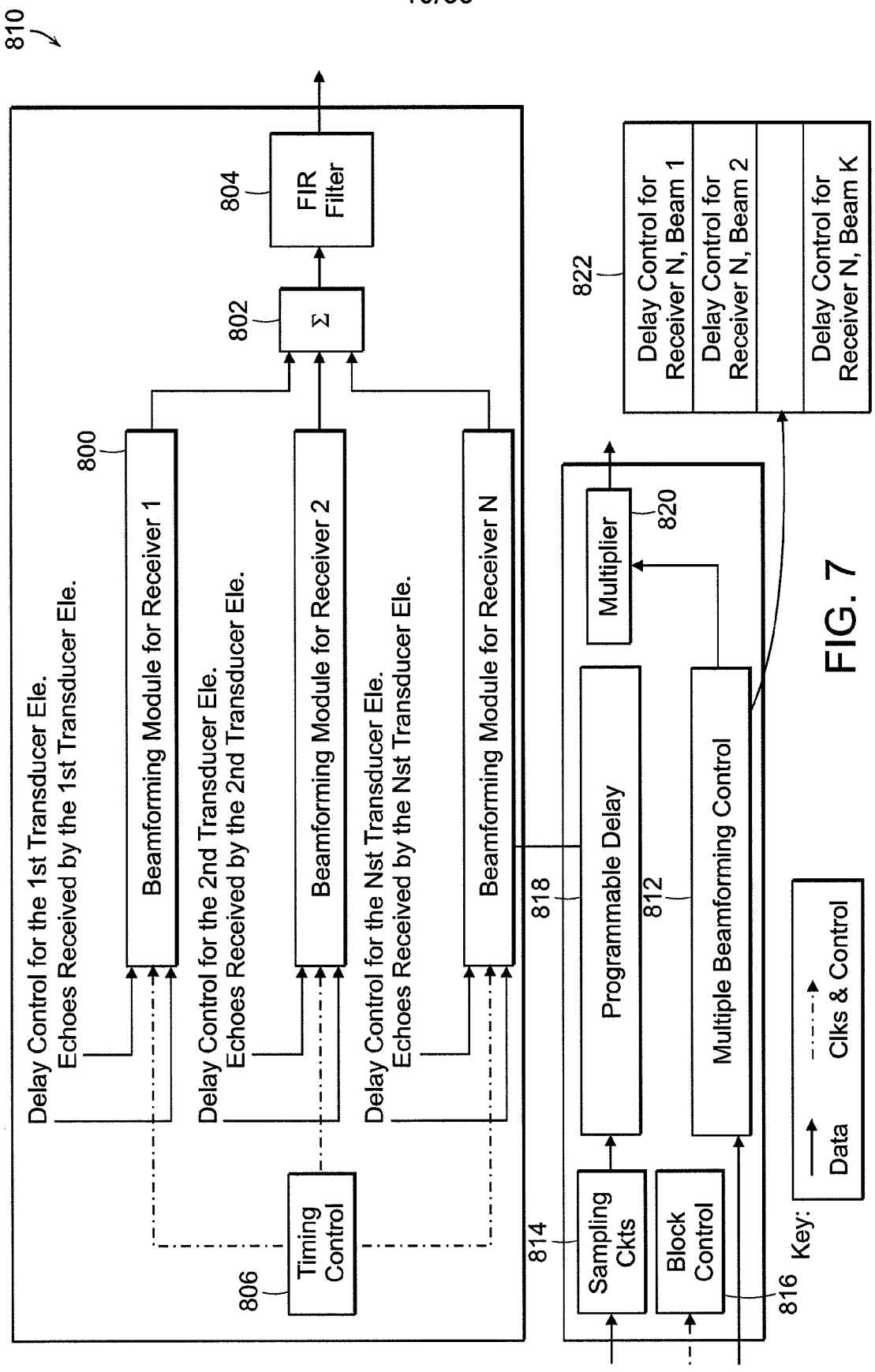

810
804
FIR Filter
802
Σ
800
Beamforming Module for Receiver 1
Beamforming Module for Receiver 2
Beamforming Module for Receiver N
Delay Control for the 1st Transducer Ele. Echoes Received by the 1st Transducer Ele.
Delay Control for the 2nd Transducer Ele. Echoes Received by the 2nd Transducer Ele.
Delay Control for the Nst Transducer Ele. Echoes Received by the Nst Transducer Ele.
806
Timing Control
814
Sampling Ckts
Block Control
816
818
Programmable Delay
812
Multiple Beamforming Control
820
Multiplier
822
Delay Control for Receiver N, Beam 1
Delay Control for Receiver N, Beam 2
Delay Control for Receiver N, Beam K
Key:
Data
Clks & Control

FIG. 7

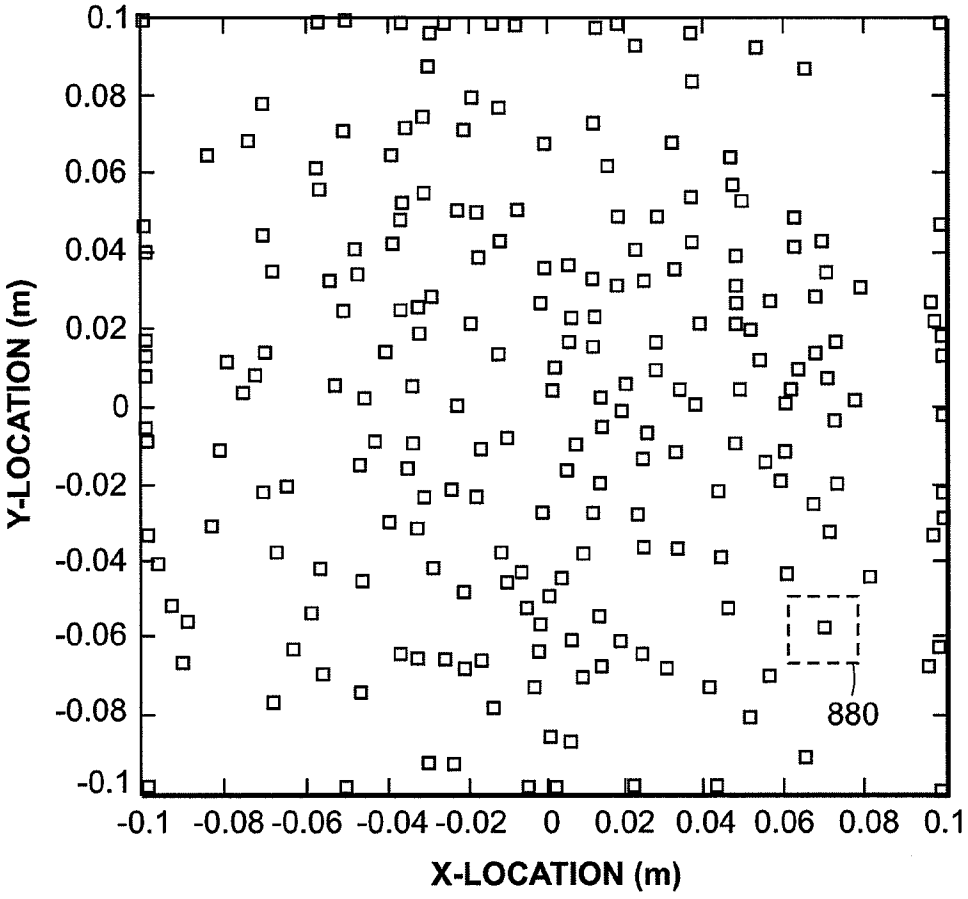

0.1
0.08
0.06
0.04
0.02
0
-0.02
-0.04
-0.06
-0.08
-0.1
Y-LOCATION (m)
-0.1 -0.08 -0.06 -0.04 -0.02 0 0.02 0.04 0.06 0.08 0.1
X-LOCATION (m)
880

FIG. 8A

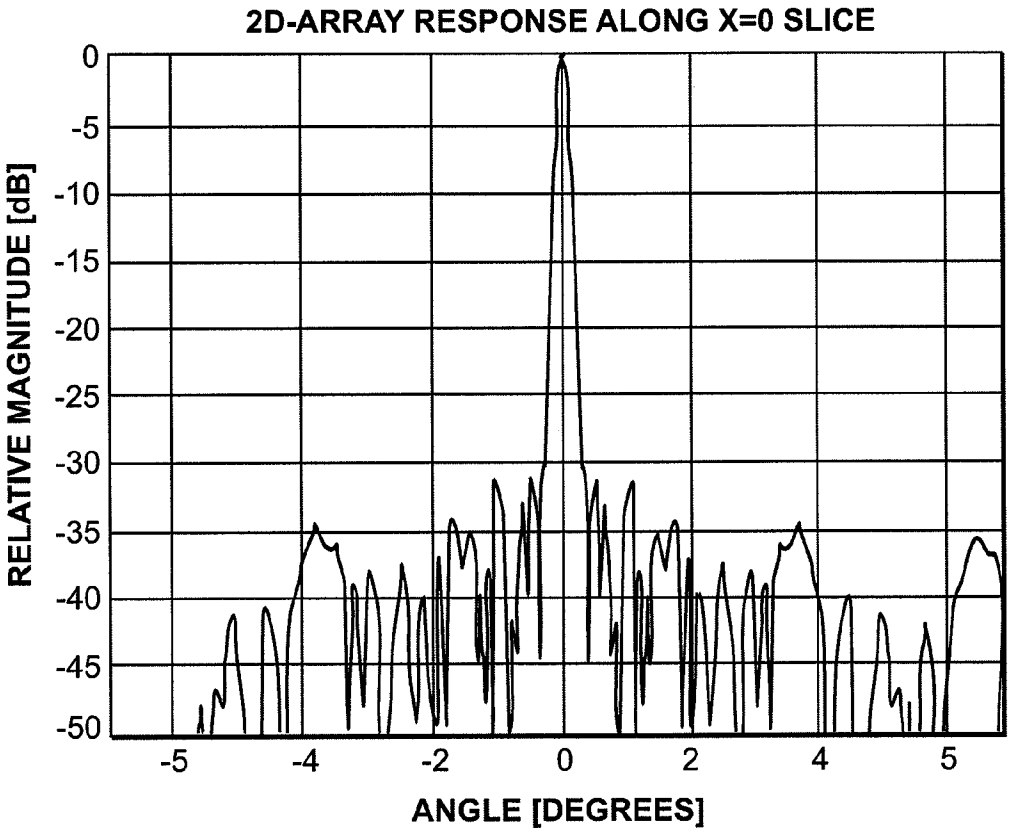

2D-ARRAY RESPONSE ALONG X=0 SLICE
RELATIVE MAGNITUDE [dB]
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
-5
-4
-2
0
2
4
5
ANGLE [DEGREES]

FIG. 8B

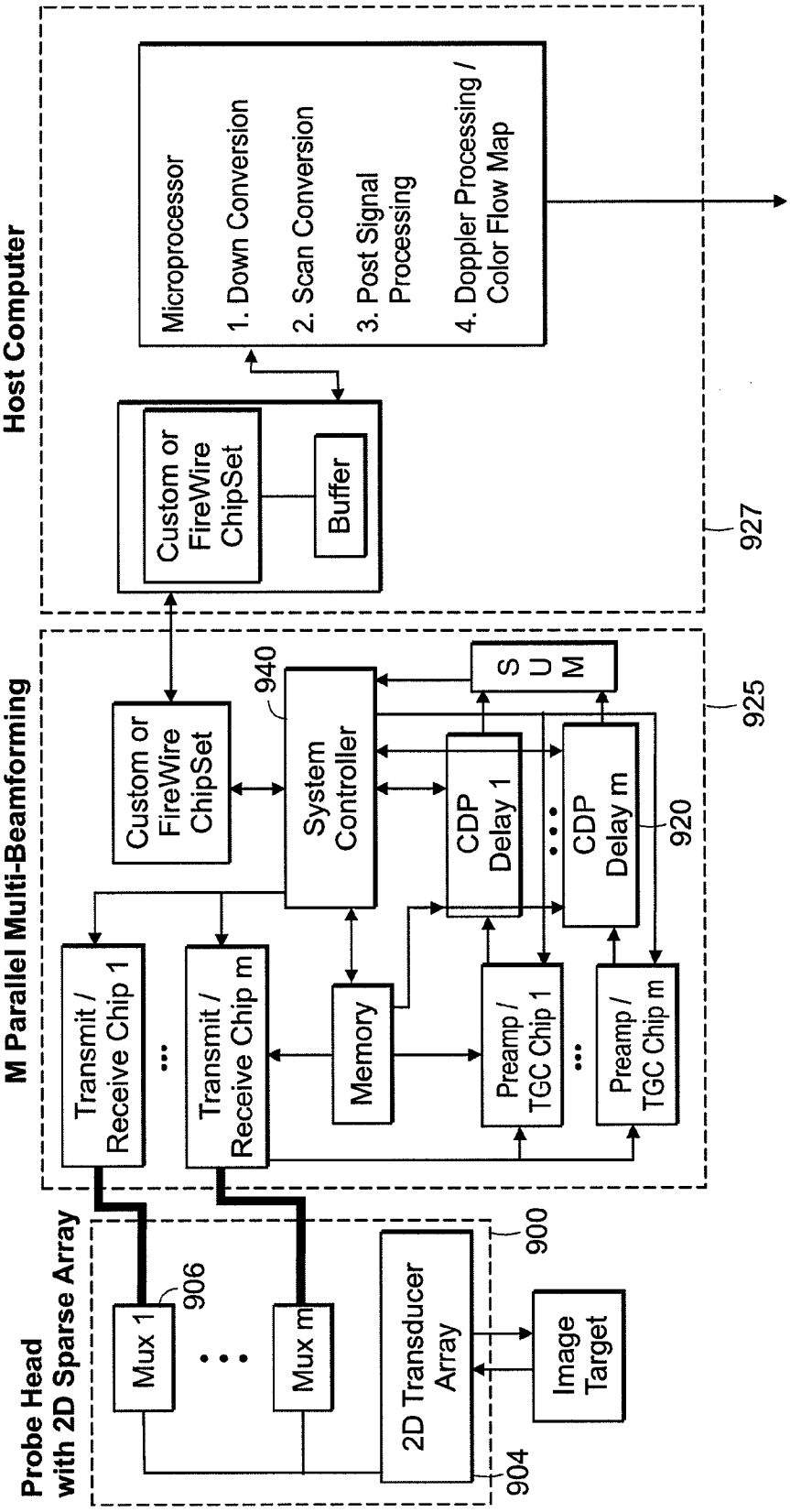

Host Computer
Microprocessor
1. Down Conversion
2. Scan Conversion
3. Post Signal Processing
4. Doppler Processing / Color Flow Map
To Display
To Recording Device
Custom or FireWire ChipSet
Buffer
927
M Parallel Multi-Beamforming
Custom or FireWire ChipSet
940
System Controller
S U M
925
CDP Delay 1
CDP Delay m
920
Transmit / Receive Chip 1
Transmit / Receive Chip m
Memory
Preamp / TGC Chip 1
Preamp / TGC Chip m
Probe Head with 2D Sparse Array
Mux 1
Mux m
906
2D Transducer Array
900
Image Target
904

FIG. 9A

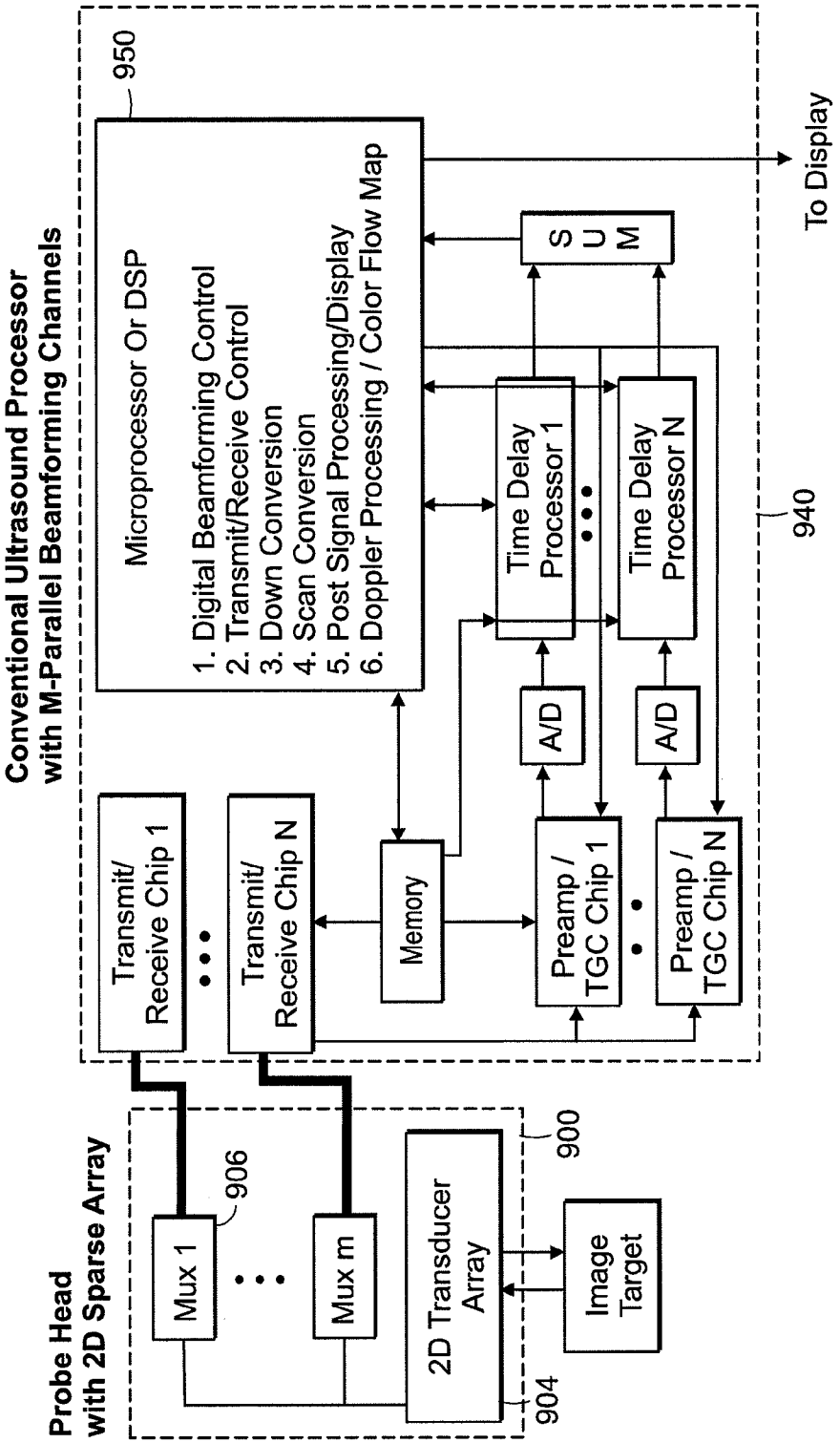

Conventional Ultrasound Processor
with M-Parallel Beamforming Channels
950
Microprocessor Or DSP
1. Digital Beamforming Control
2. Transmit/Receive Control
3. Down Conversion
4. Scan Conversion
5. Post Signal Processing/Display
6. Doppler Processing / Color Flow Map
To Display
S
U
M
Time Delay
Processor 1
Time Delay
Processor N
940
A/D
A/D
Transmit/
Receive Chip 1
Transmit/
Receive Chip N
Memory
Preamp /
TGC Chip 1
Preamp /
TGC Chip N
Probe Head
with 2D Sparse Array
906
Mux 1
Mux m
2D Transducer
Array
900
904
Image
Target

FIG. 9B

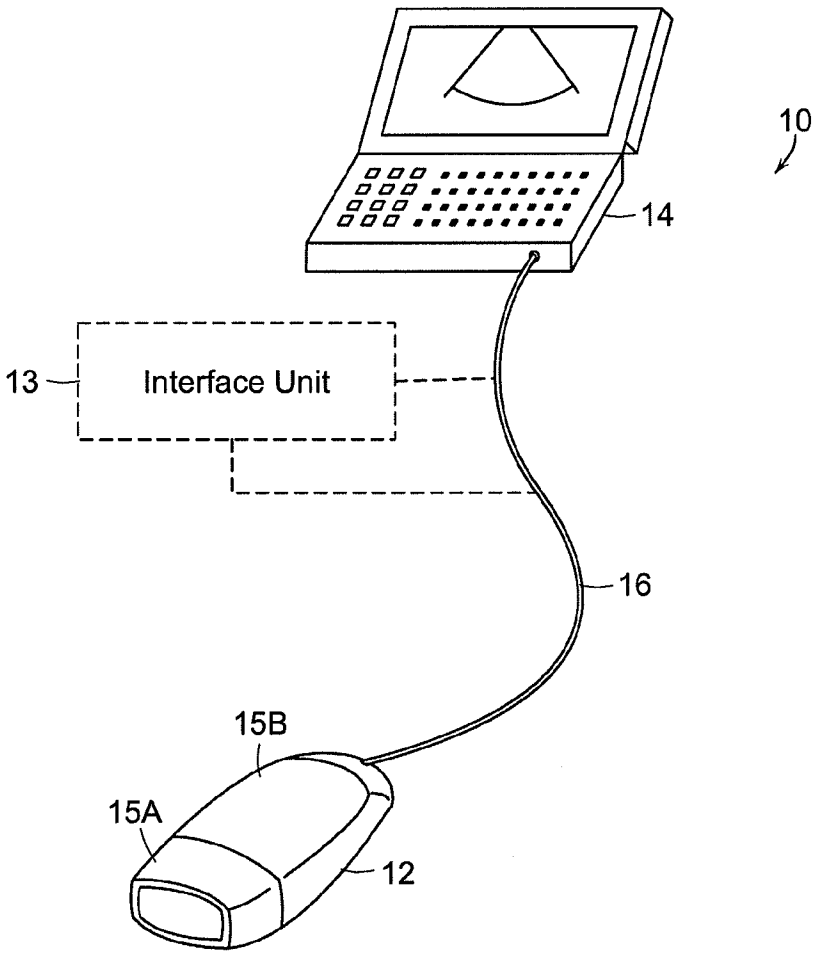


FIG. 10

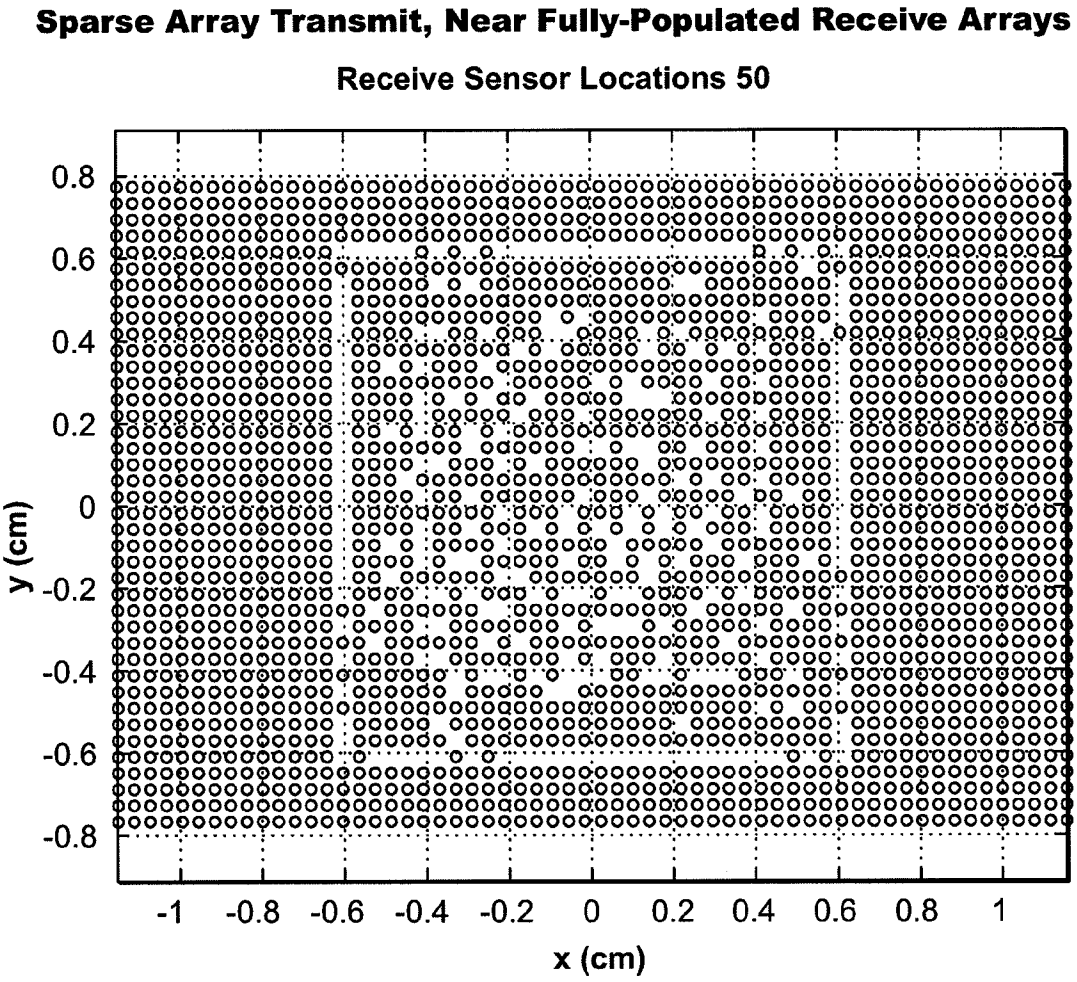

Sparse Array Transmit, Near Fully-Populated Receive Arrays
Receive Sensor Locations 50
y (cm)
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
1
x (cm)

FIG. 11

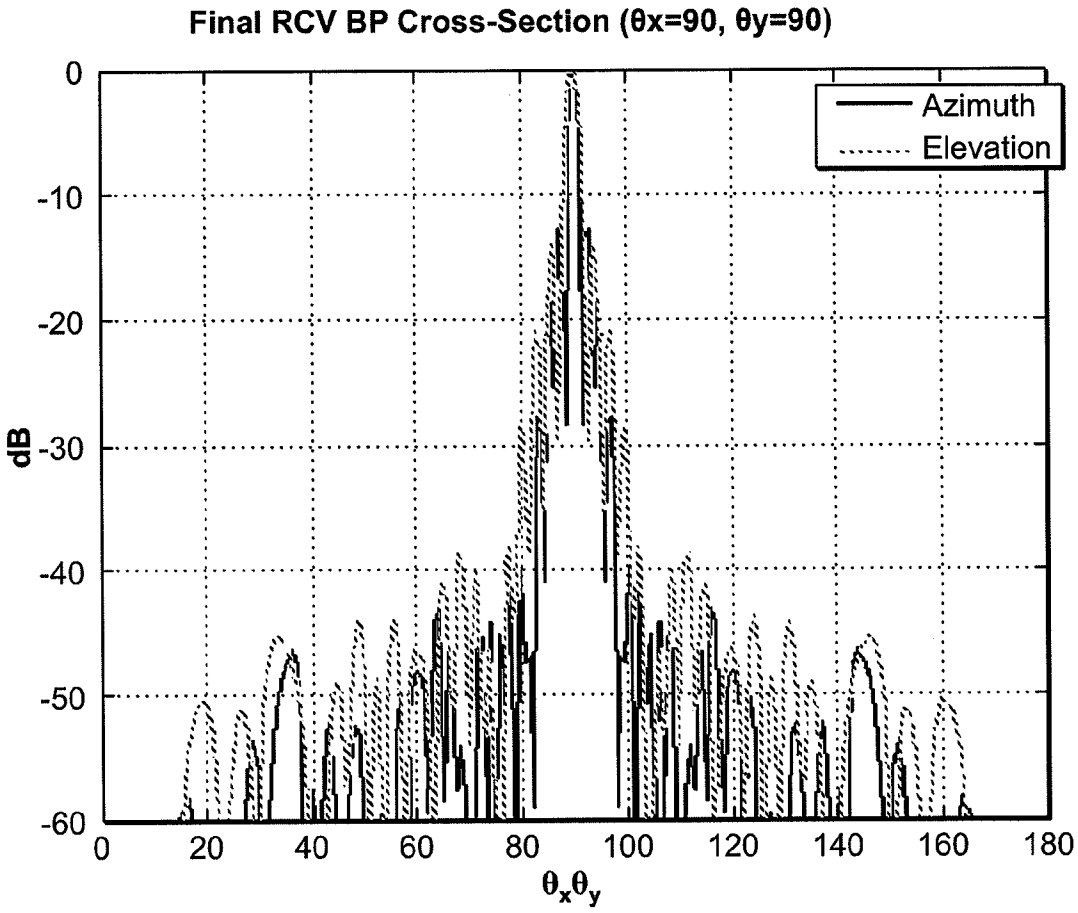

Final RCV BP Cross-Section (θx=90, θy=90)
Azimuth
Elevation
dB
0
-10
-20
-30
-40
-50
-60
0
20
40
60
80
100
120
140
160
180
θxθy

FIG. 12

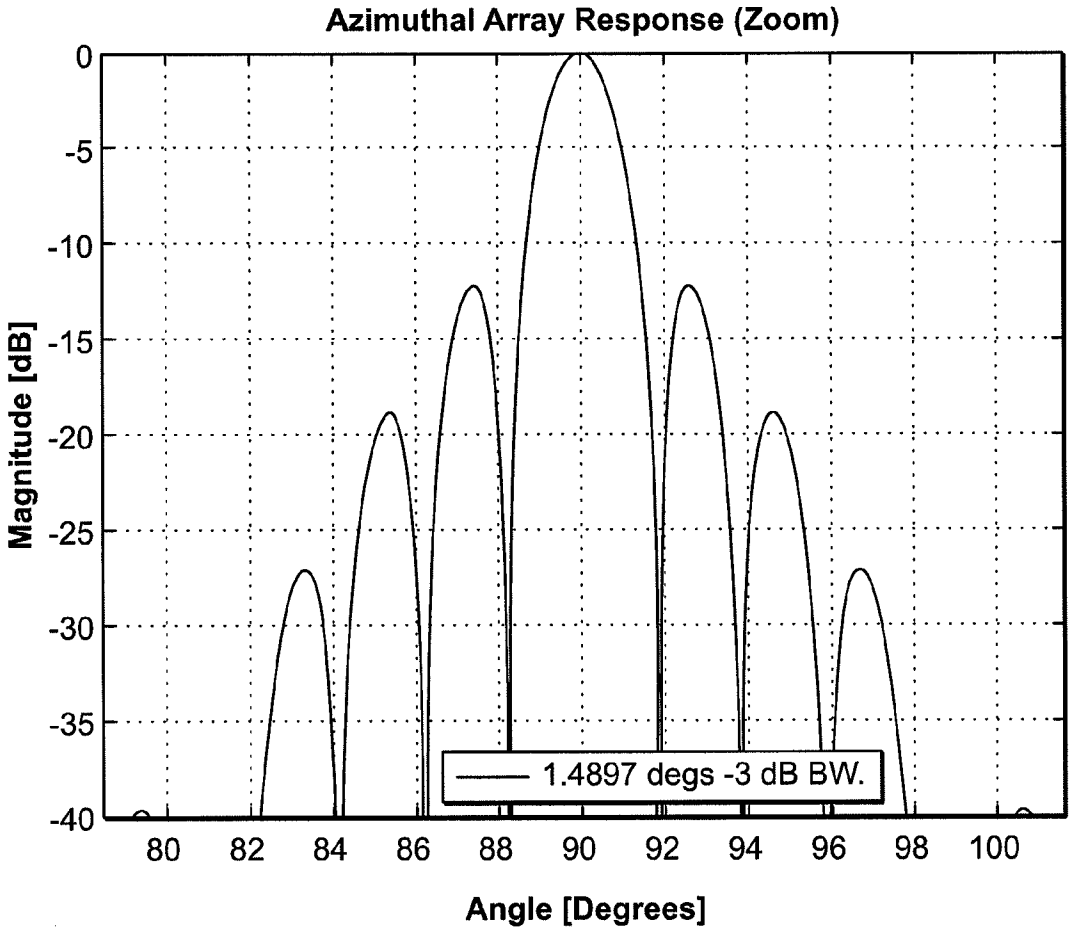

Azimuthal Array Response (Zoom)
Magnitude [dB]
0
-5
-10
-15
-20
-25
-30
-35
-40
80
82
84
86
88
90
92
94
96
98
100
Angle [Degrees]
1.4897 degs -3 dB BW.

FIG. 13

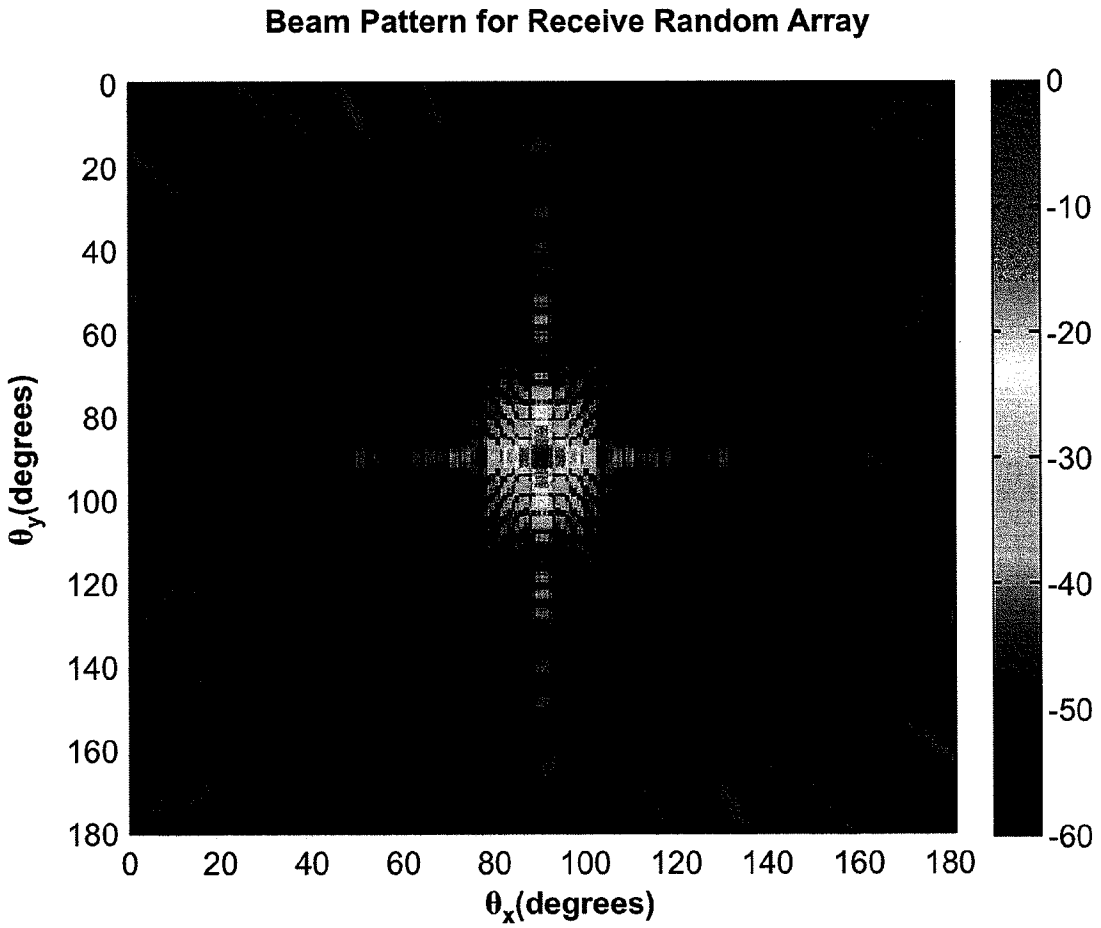

Beam Pattern for Receive Random Array
0
20
40
60
80
100
120
140
160
180
θy(degrees)
0
20
40
60
80
100
120
140
160
180
θx(degrees)
0
-10
-20
-30
-40
-50
-60

FIG. 14

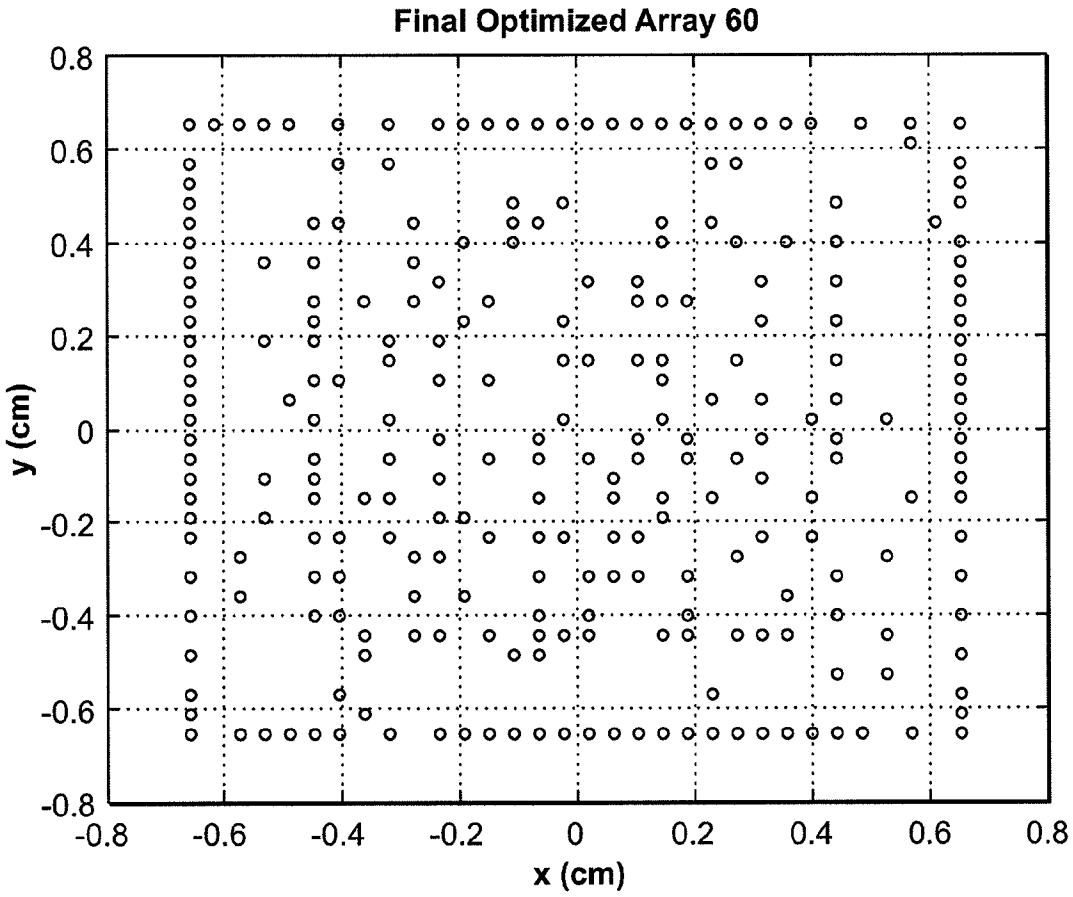

Final Optimized Array 60
0.8
0.6
0.4
0.2
0
-0.2
-0.4
-0.6
-0.8
y (cm)
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
0.6
0.8
x (cm)

FIG. 15

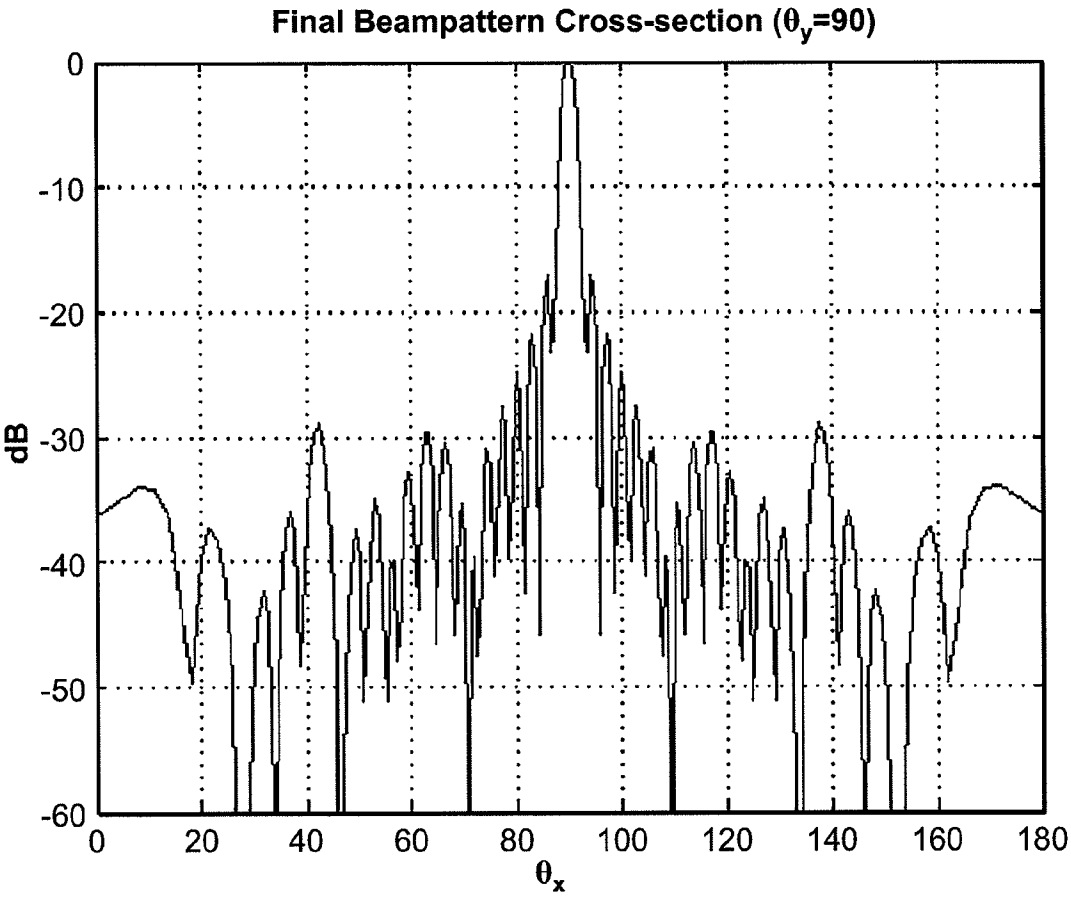

Final Beampattern Cross-section (θ_y=90)
dB
0
-10
-20
-30
-40
-50
-60
0
20
40
60
80
100
120
140
160
180
θ_x

FIG. 16

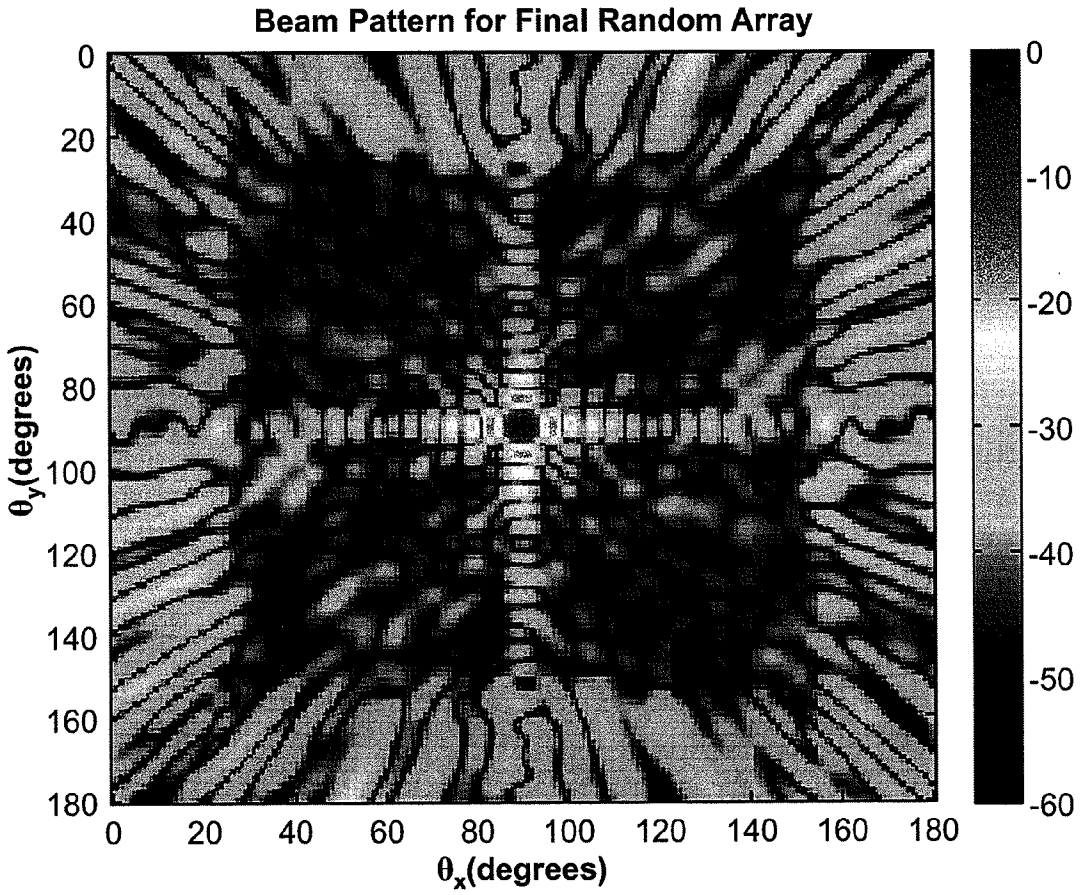

Beam Pattern for Final Random Array
0
20
40
60
80
100
120
140
160
180
θy(degrees)
0
20
40
60
80
100
120
140
160
180
θx(degrees)
0
-10
-20
-30
-40
-50
-60

FIG. 17

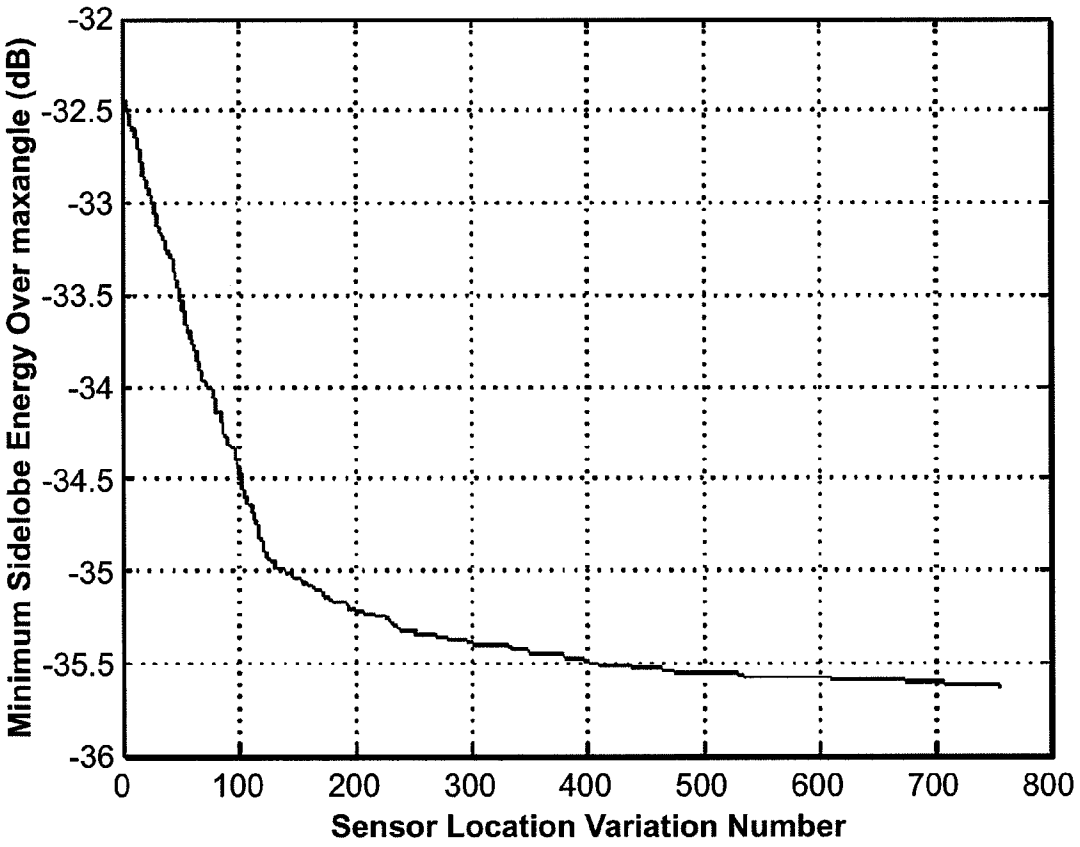
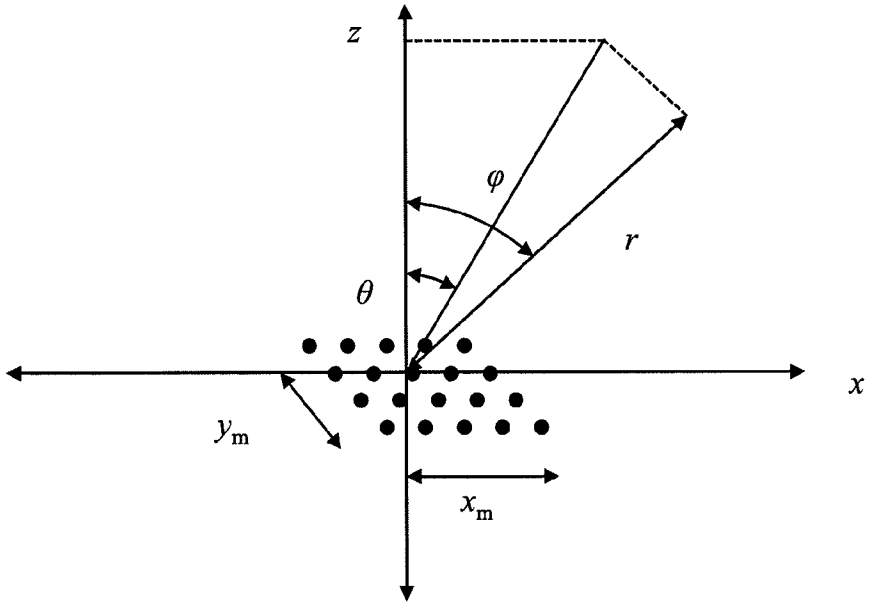

Minimum Sidelobe Energy Over maxangle (dB)
-32
-32.5
-33
-33.5
-34
-34.5
-35
-35.5
-36
0
100
200
300
400
500
600
700
800
Sensor Location Variation Number

FIG. 18

2D-ARRAY DIFFERENTIAL DELAY EQUATION



$$f(r,\theta,\varphi) = r\left[1-\sqrt{1+\frac{x_m^2}{r^2}+\frac{y_m^2}{r^2}-\frac{2x_m\sin\theta\cos\varphi}{r}-\frac{2y_m\cos\theta\sin\varphi}{r}}\right]$$

STEERED TWO-DIMENSIONAL ARRAY

FIG. 19

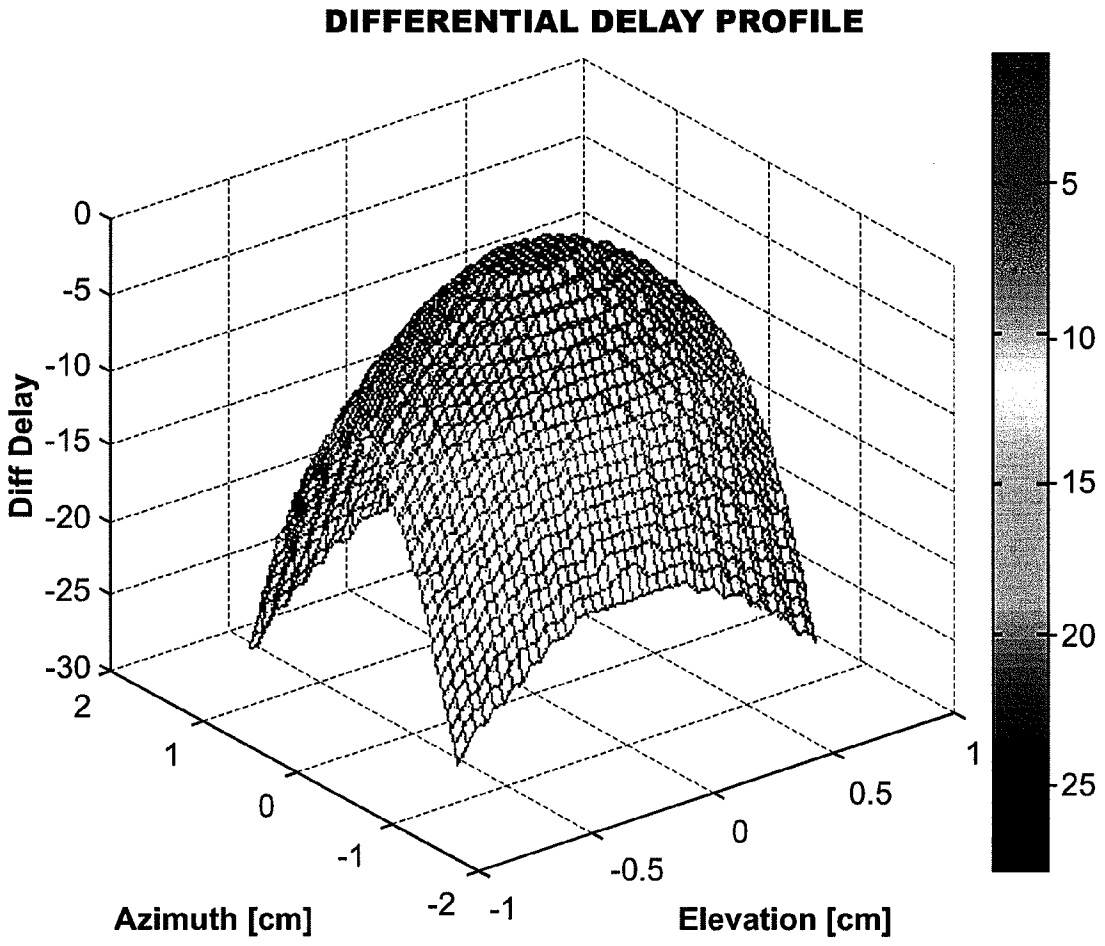

DIFFERENTIAL DELAY PROFILE
Diff Delay
0
-5
-10
-15
-20
-25
-30
2
1
0
-1
-2
Azimuth [cm]
-1
-0.5
0
0.5
1
Elevation [cm]
5
10
15
20
25

FIG. 20

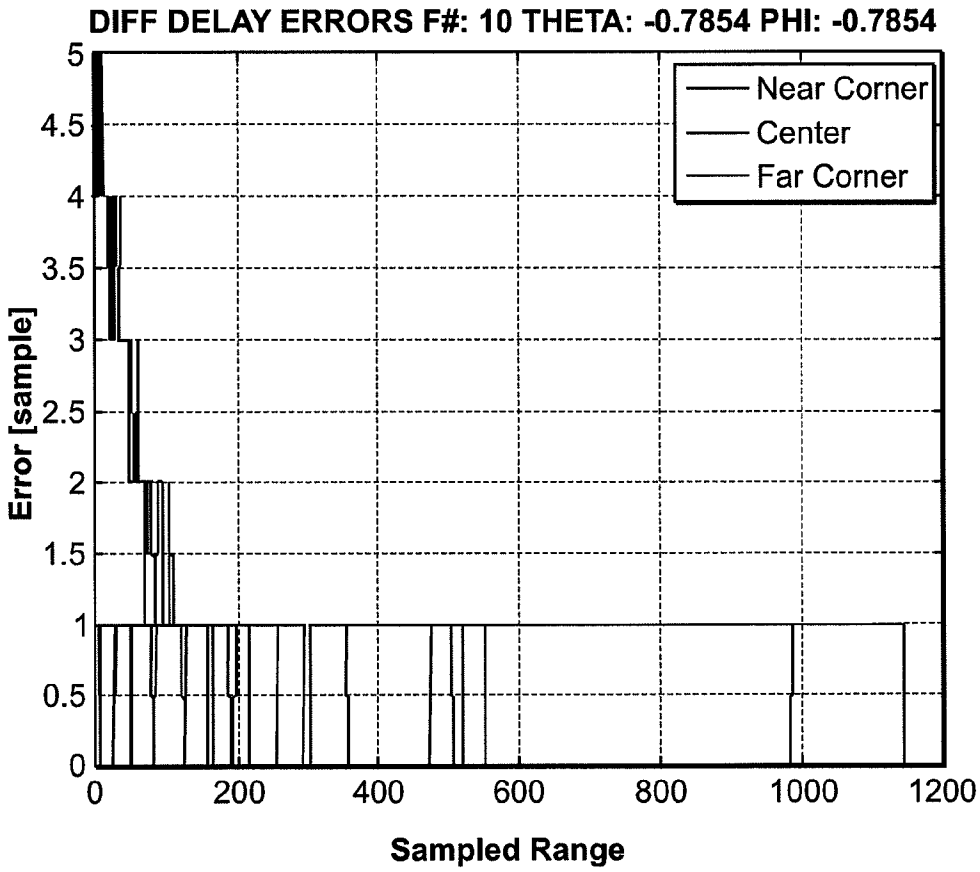

DIFF DELAY ERRORS F#: 10 THETA: -0.7854 PHI: -0.7854
Near Corner
Center
Far Corner
Error [sample]
Sampled Range
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5
0
200
400
600
800
1000
1200

FIG. 21

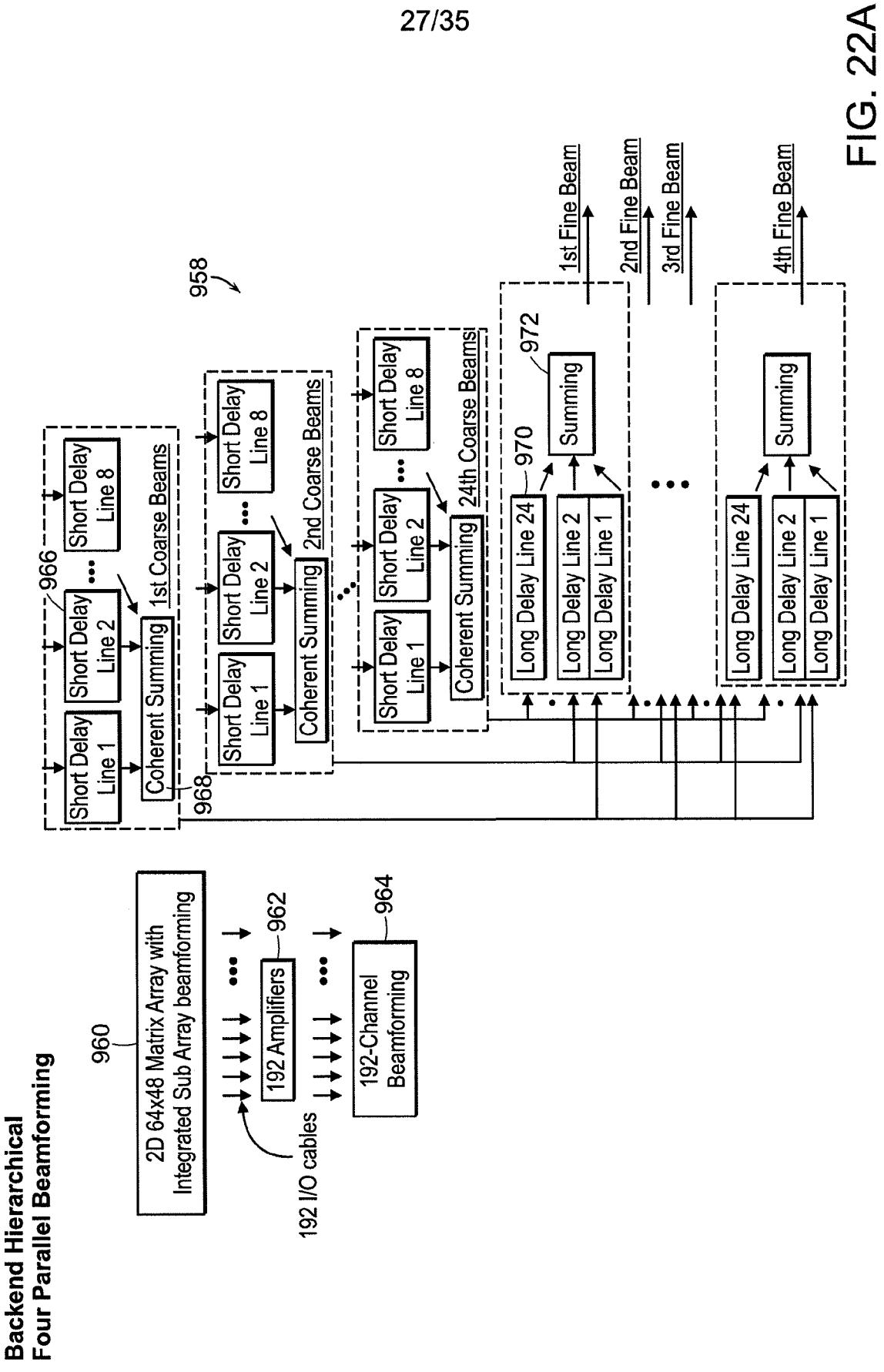

Backend Hierarchical
Four Parallel Beamforming
960
2D 64x48 Matrix Array with Integrated Sub Array beamforming
192 I/O cables
962
192 Amplifiers
964
192-Channel Beamforming
958
966
Short Delay Line 1
Short Delay Line 2
Short Delay Line 8
Coherent Summing
1st Coarse Beams
968
2nd Coarse Beams
24th Coarse Beams
970
Long Delay Line 24
Long Delay Line 2
Long Delay Line 1
972
Summing
1st Fine Beam
2nd Fine Beam
3rd Fine Beam
4th Fine Beam

FIG. 22A

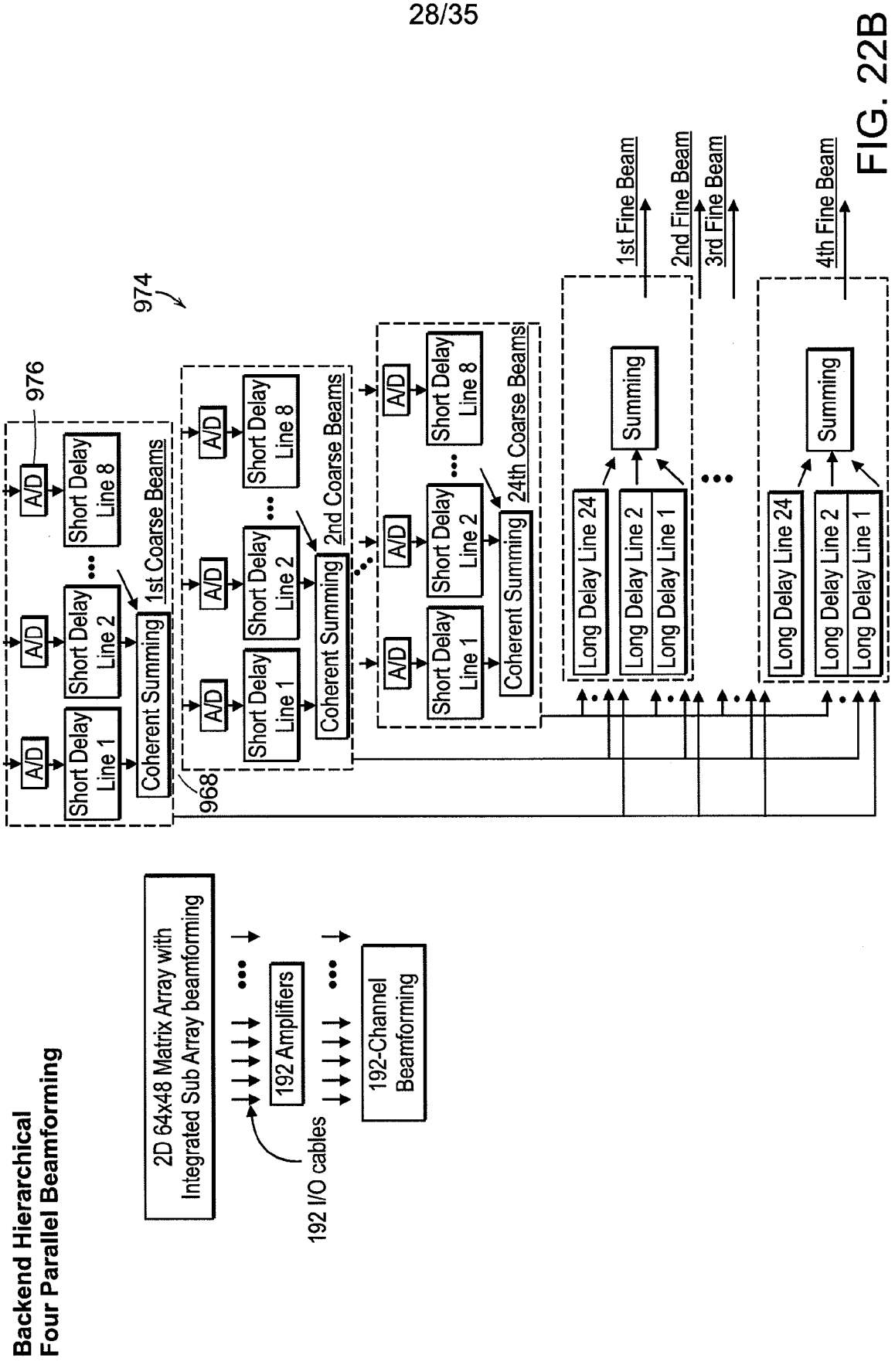

Backend Hierarchical
Four Parallel Beamforming
2D 64x48 Matrix Array with Integrated Sub Array beamforming
192 Amplifiers
192 I/O cables
192-Channel Beamforming
974
976
968
A/D
Short Delay Line 1
Short Delay Line 2
Short Delay Line 8
Coherent Summing
1st Coarse Beams
2nd Coarse Beams
24th Coarse Beams
Long Delay Line 24
Long Delay Line 2
Long Delay Line 1
Summing
1st Fine Beam
2nd Fine Beam
3rd Fine Beam
4th Fine Beam

FIG. 22B

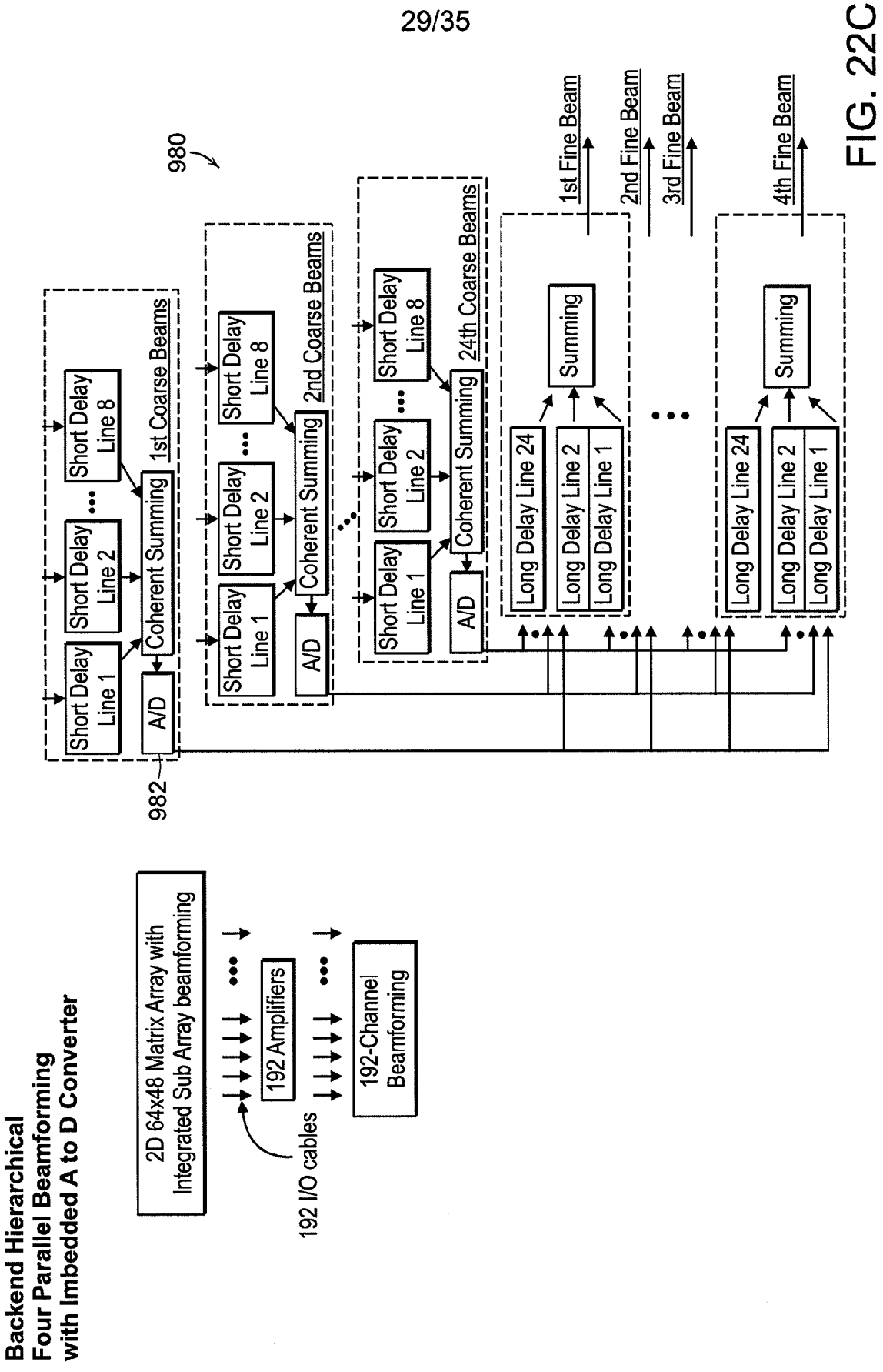

Backend Hierarchical
Four Parallel Beamforming
with Imbedded A to D Converter
2D 64x48 Matrix Array with Integrated Sub Array beamforming
192 I/O cables
192 Amplifiers
192-Channel Beamforming
980
982
Short Delay Line 1
Short Delay Line 2
Short Delay Line 8
A/D
Coherent Summing
1st Coarse Beams
2nd Coarse Beams
24th Coarse Beams
Long Delay Line 24
Long Delay Line 2
Long Delay Line 1
Summing
1st Fine Beam
2nd Fine Beam
3rd Fine Beam
4th Fine Beam

FIG. 22C

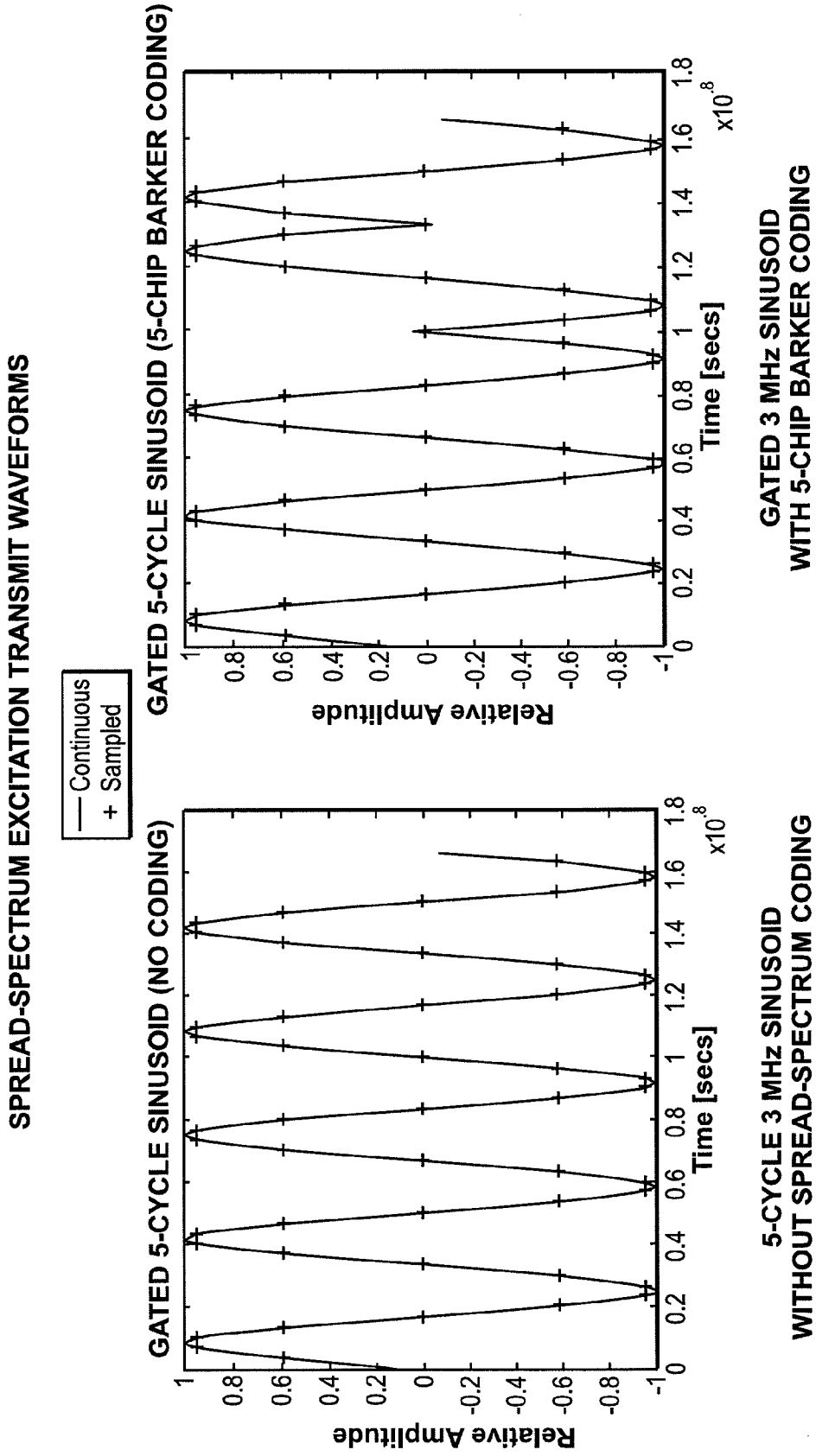


FIG. 23A

FIG. 23B

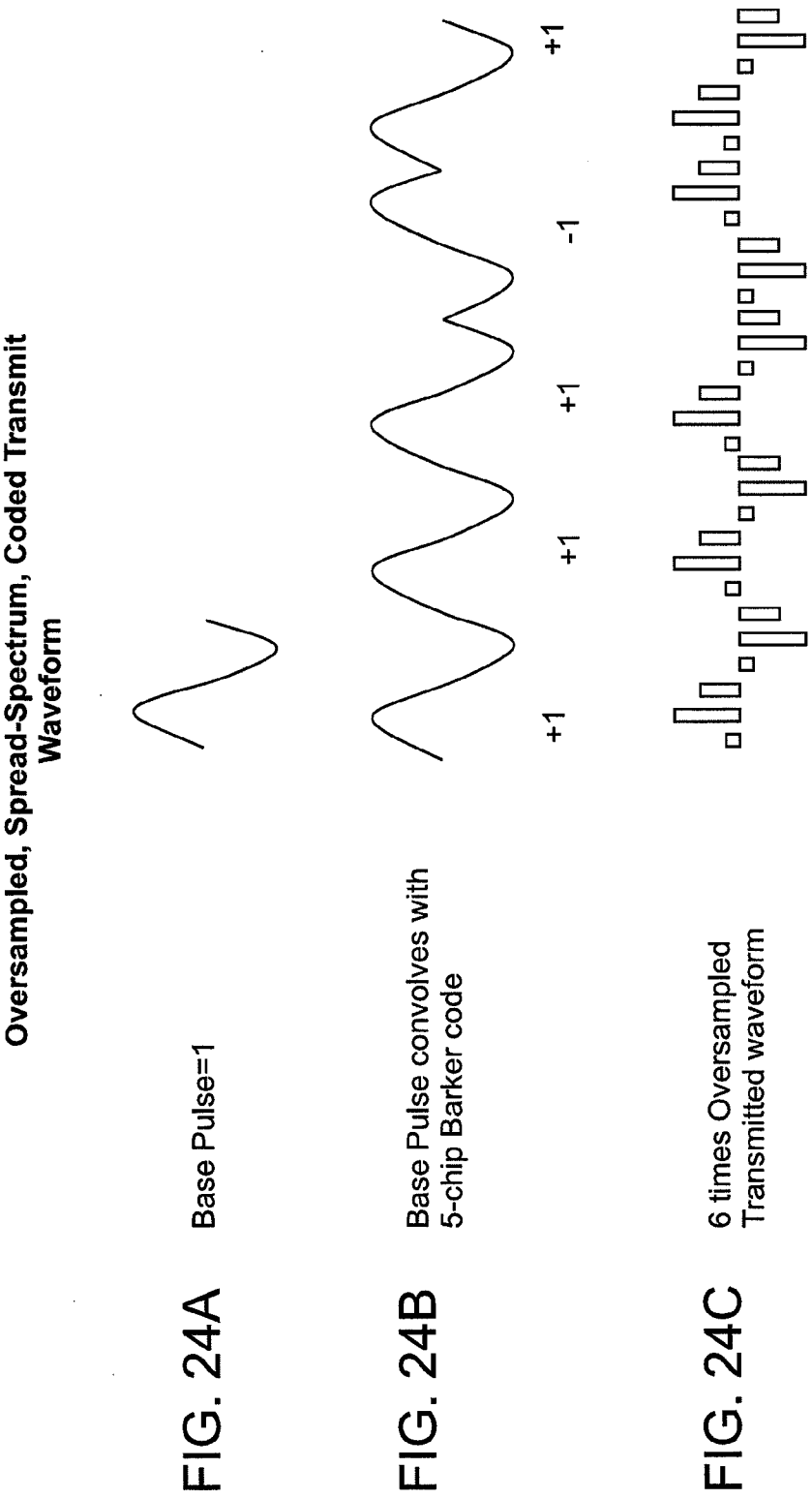


FIG. 24A

FIG. 24B

FIG. 24C

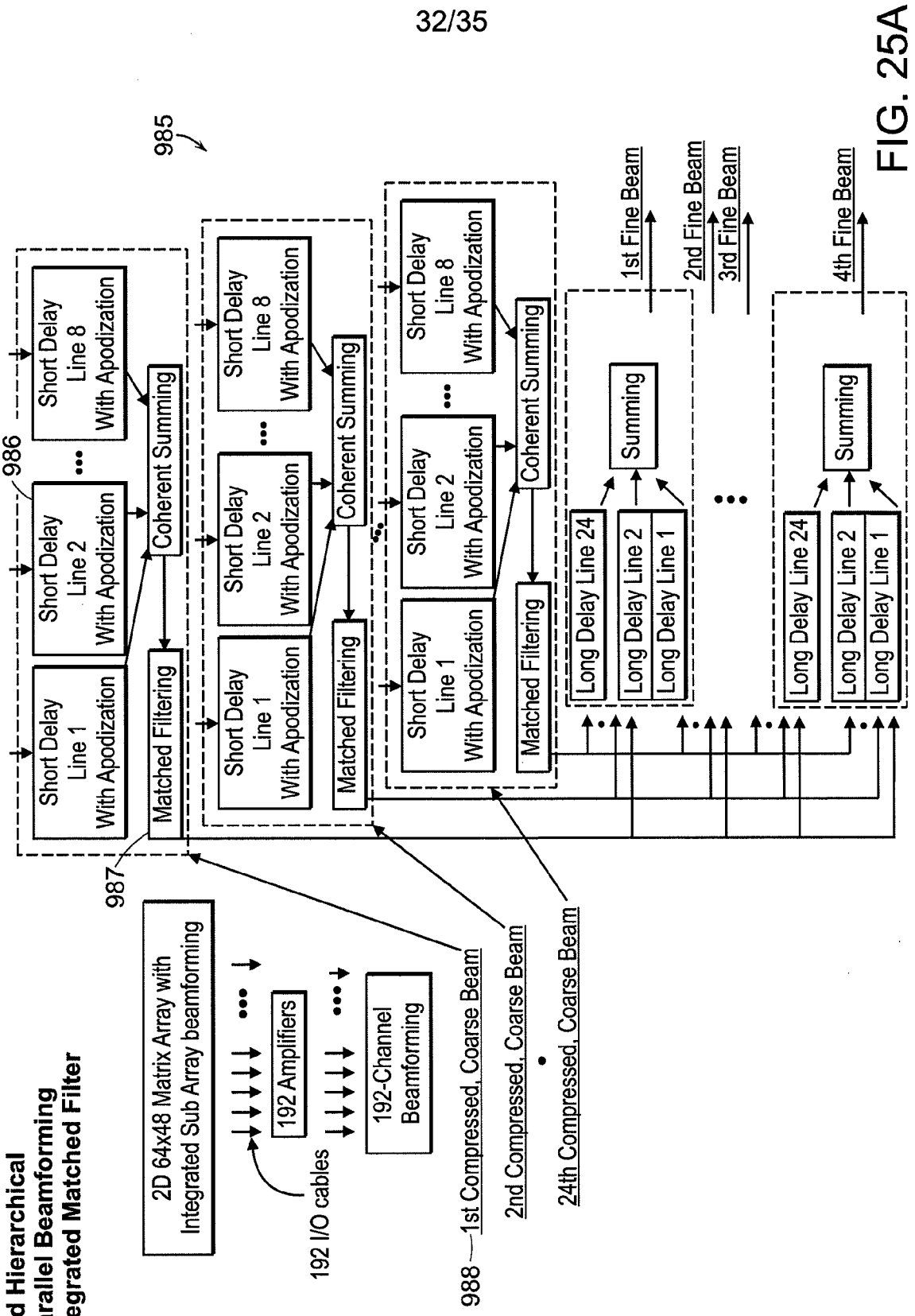

Backend Hierarchical
Four Parallel Beamforming
with Integrated Matched Filter
985
986
987
988
2D 64x48 Matrix Array with Integrated Sub Array beamforming
192 Amplifiers
192 I/O cables
192-Channel Beamforming
1st Compressed, Coarse Beam
2nd Compressed, Coarse Beam
24th Compressed, Coarse Beam
Short Delay Line 1 With Apodization
Short Delay Line 2 With Apodization
Short Delay Line 8 With Apodization
Coherent Summing
Matched Filtering
Long Delay Line 24
Long Delay Line 2
Long Delay Line 1
Summing
1st Fine Beam
2nd Fine Beam
3rd Fine Beam
4th Fine Beam

FIG. 25A

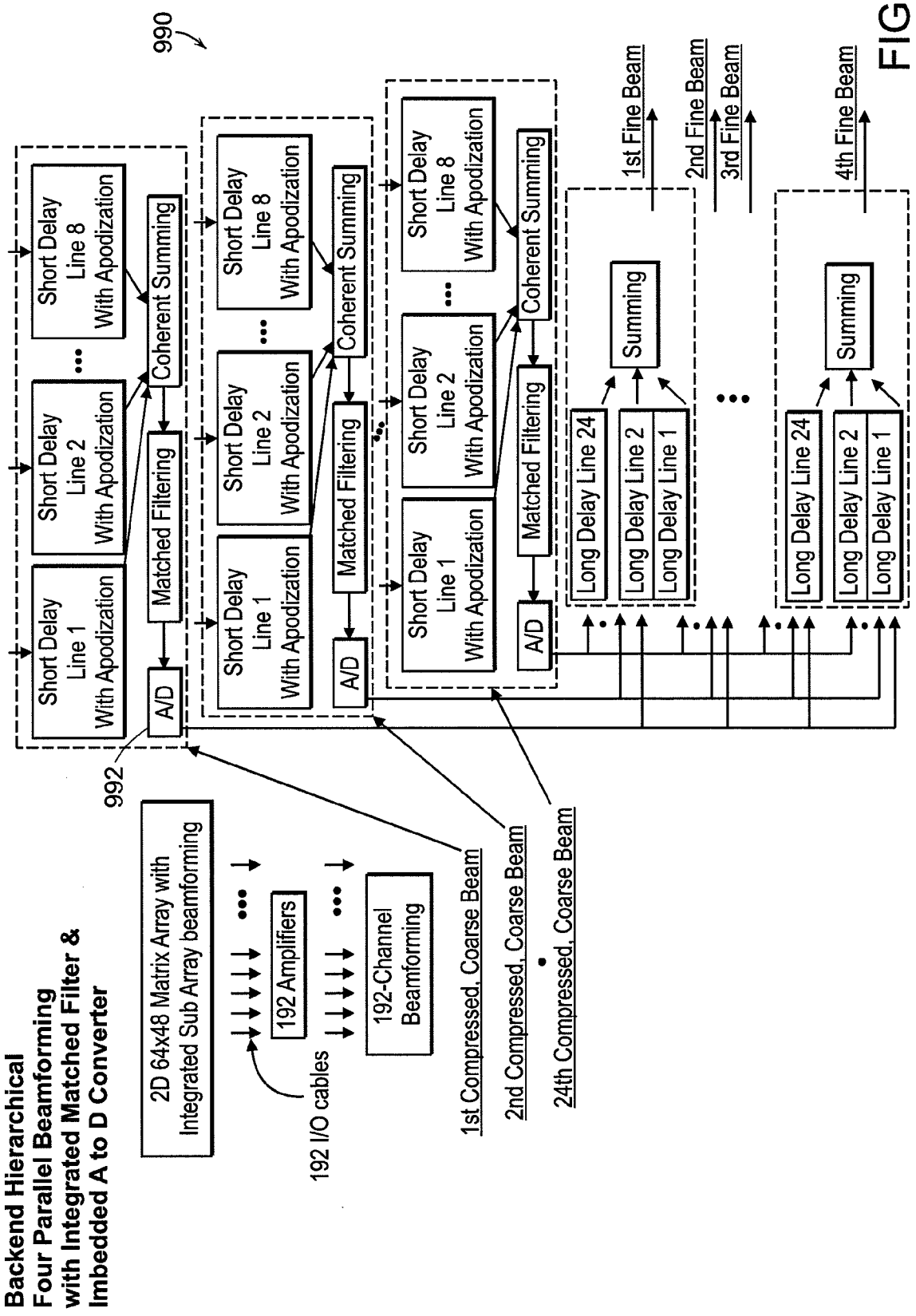

Backend Hierarchical
Four Parallel Beamforming
with Integrated Matched Filter &
Imbedded A to D Converter
2D 64x48 Matrix Array with
Integrated Sub Array beamforming
192 Amplifiers
192 I/O cables
192-Channel
Beamforming
1st Compressed, Coarse Beam
2nd Compressed, Coarse Beam
24th Compressed, Coarse Beam
990
992
A/D
Short Delay
Line 1
With Apodization
Short Delay
Line 2
With Apodization
Short Delay
Line 8
With Apodization
Matched Filtering
Coherent Summing
Long Delay Line 24
Long Delay Line 2
Long Delay Line 1
Summing
1st Fine Beam
2nd Fine Beam
3rd Fine Beam
4th Fine Beam

FIG. 25B

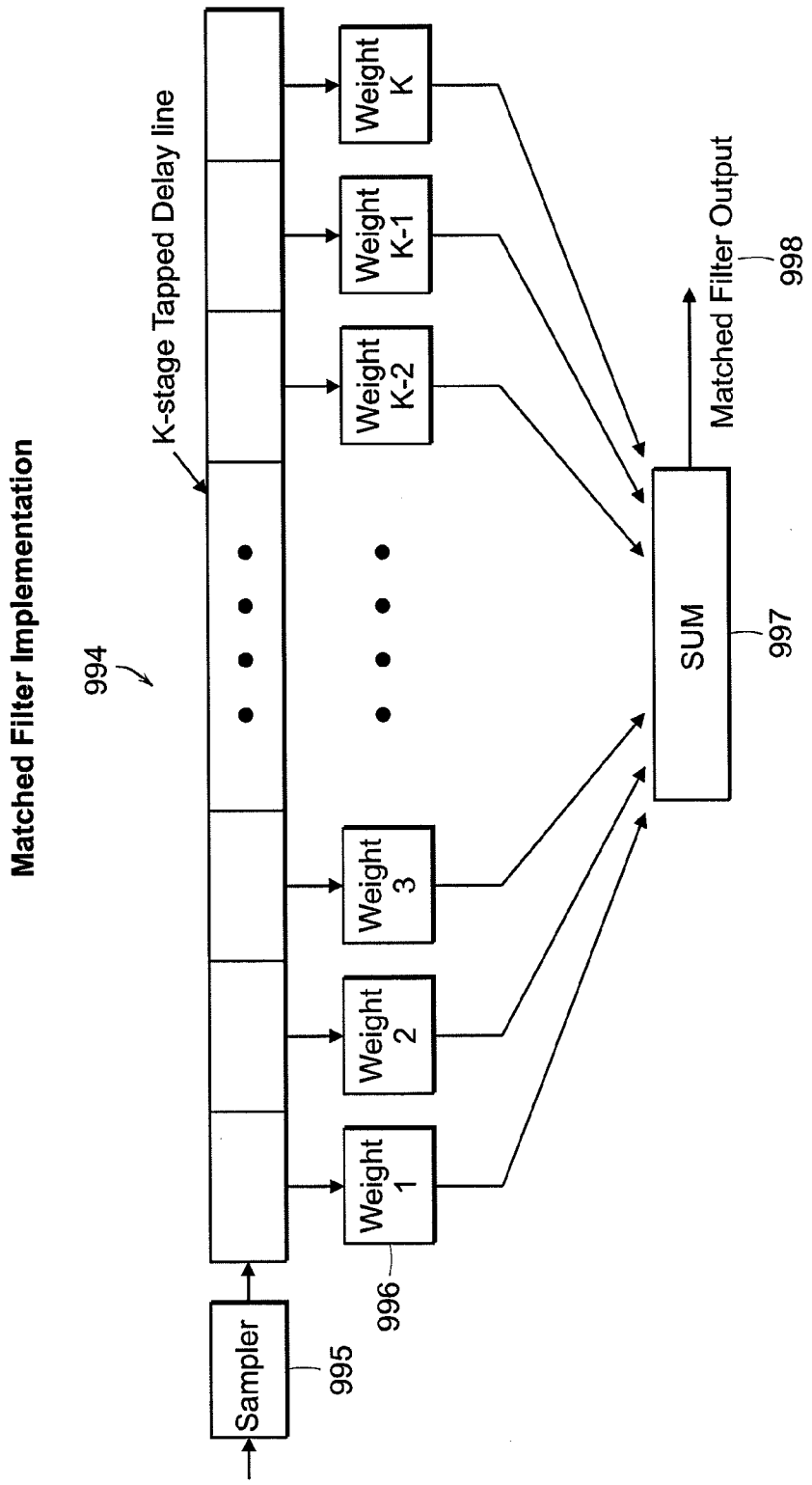

Matched Filter Implementation
994
K-stage Tapped Delay line
Weight K
Weight K-1
Weight K-2
Weight 3
Weight 2
Weight 1
996
Sampler
995
SUM
997
Matched Filter Output
998

FIG. 25C

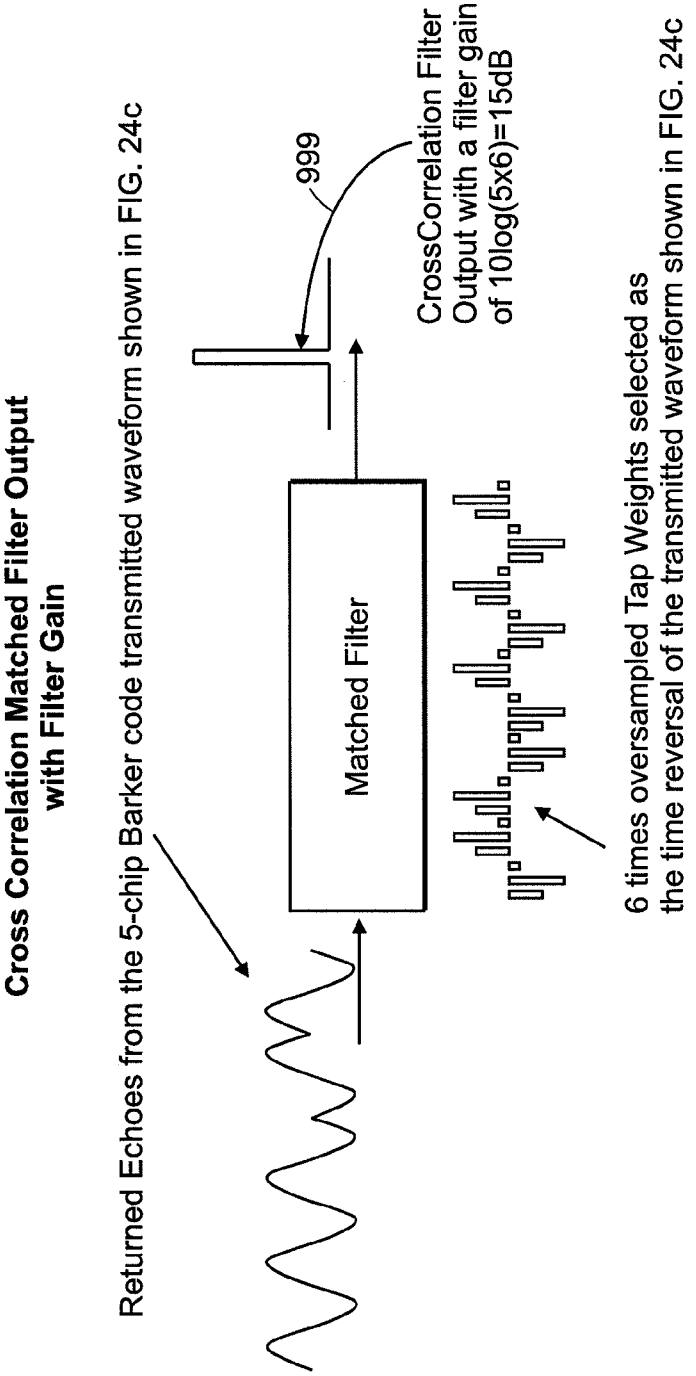

Cross Correlation Matched Filter Output
with Filter Gain
Returned Echoes from the 5-chip Barker code transmitted waveform shown in FIG. 24c
Matched Filter
999
CrossCorrelation Filter
Output with a filter gain
of 10log(5x6)=15dB
6 times oversampled Tap Weights selected as
the time reversal of the transmitted waveform shown in FIG. 24c

FIG. 25D

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/056995

A. CLASSIFICATION OF SUBJECT MATTER
INV. A61B8/00 G01S15/89

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
A61B G01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2008/002464 A2 (TERATECH CORP [US]; CHIANG ALICE M [US]; BRODSKY MICHAEL [US]; HE XING) 3 January 2008 (2008-01-03)	1-5, 7-11, 13-17, 20-21, 23-32, 34-38,40
Y	page 1, two last pars. pages 6-8 page 10, 2nd par. claims 1-3 figures 3A-6B	6,12, 18-19, 22,33,39
X	US 2005/243812 A1 (PHELPS ROBERT N [US]) 3 November 2005 (2005-11-03) paragraphs [0016] - [0024] figures 1, 2	1-2,5-8, 28,33

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 November 2009	02/12/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Dydenko, Igor

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/056995

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 1 491 913 A2 (ALOKA CO LTD [JP]) 29 December 2004 (2004-12-29) paragraphs [0010] - [0021] figure 1	1,28
X	US 6 491 634 B1 (LEAVITT STEVEN C [US] ET AL) 10 December 2002 (2002-12-10)	28-29,31
A	column 3, line 27 - column 7, line 42 claim 1	4
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Y	US 2002/091317 A1 (CHIAO RICHARD YUNG [US]) 11 July 2002 (2002-07-11)	12,18,39
A	paragraph [0027] paragraphs [0041], [0 42]	11,38
Y	US 5 938 611 A (MUZILLA DAVID JOHN [US] ET AL) 17 August 1999 (1999-08-17)	19
A	column 6, line 48 - column 8, line 22	11,18,38

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/056995

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专利名称(译)	超声3D成像系统		
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[标]申请(专利权)人(译)	泰拉科技公司		
申请(专利权)人(译)	TERATECH CORPORATION		
当前申请(专利权)人(译)	TERATECH CORPORATION		
[标]发明人	CHIANG ALICE HE XINGBAI WONG WILLIAM BERGER NOAH		
发明人	CHIANG, ALICE HE, XINGBAI WONG, WILLIAM BERGER, NOAH		
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优先权	12/286555 2008-09-30 US 61/192063 2008-09-15 US		
外部链接	Espacenet		

摘要(译)

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