US 20200146581A1

(19) **United States**

(12) **Patent Application Publication** (10) **Pub. No.: US 2020/0146581 A1**

Rhodes et al. (43) **Pub. Date: May 14, 2020**

(54) **INTEGRITY VERIFICATION SYSTEM FOR TESTING HIGH CHANNEL COUNT NEUROMONITORING RECORDING EQUIPMENT**

(71) Applicant: **Cadwell Laboratories, Inc.**, Kennewick, WA (US)

(72) Inventors: **Ethan Rhodes**, Benton City, WA (US); **Richard A. Villarreal**, West Richland, WA (US); **John A. Cadwell**, Richland, WA (US); **Rose Rehfeldt**, Kennewick, WA (US)

(21) Appl. No.: **16/678,482**

(22) Filed: **Nov. 8, 2019**

Related U.S. Application Data

(60) Provisional application No. 62/758,320, filed on Nov. 9, 2018.

Publication Classification

(51) **Int. Cl.**

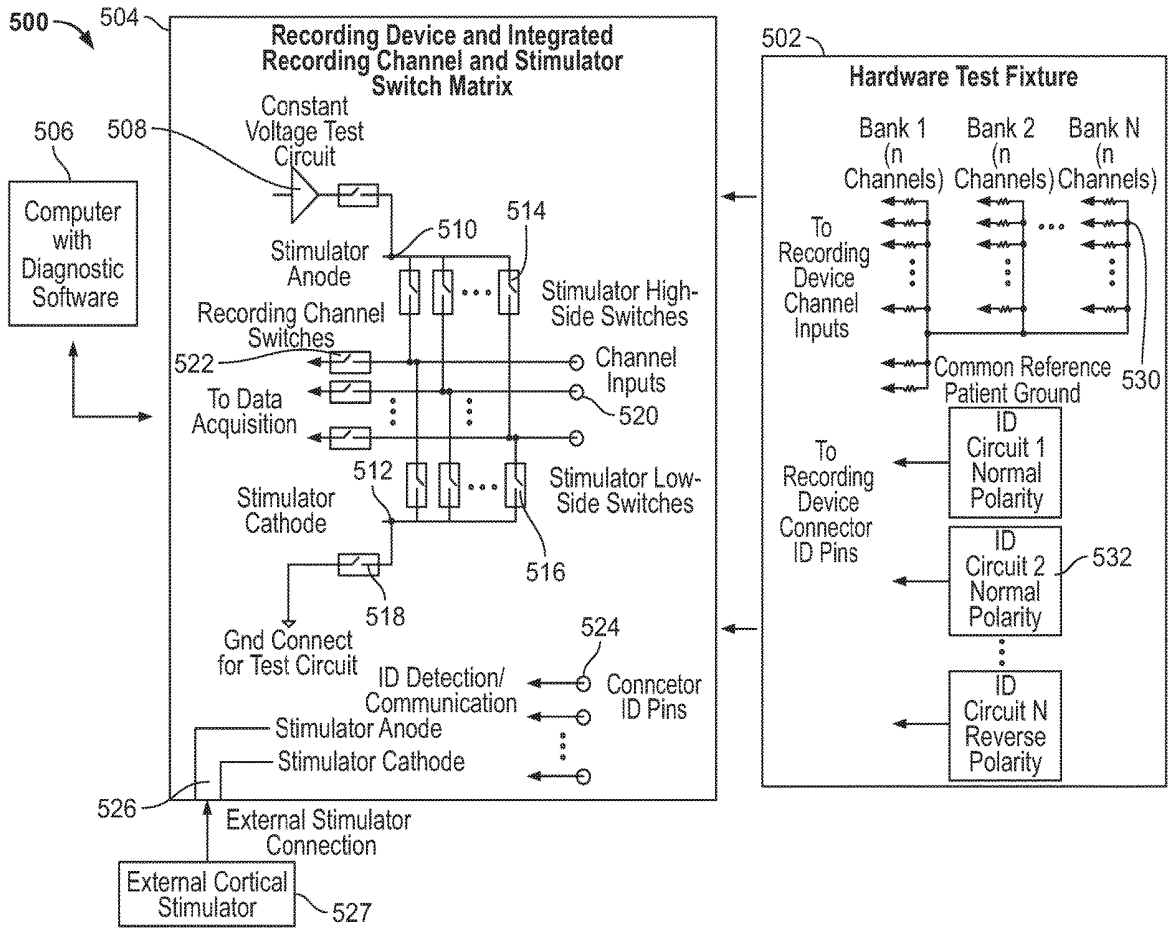
A61B 5/0478	(2006.01)
A61B 5/00	(2006.01)
G01R 31/28	(2006.01)

(52) **U.S. Cl.**

CPC ***A61B 5/0478*** (2013.01); ***G01R 31/2829*** (2013.01); ***G01R 31/2812*** (2013.01); ***A61B 5/7221*** (2013.01)

(57) **ABSTRACT**

Methods of performing diagnostic tests on electroencephalography (EEG) recording devices comprising at least one stimulator coupled with a plurality of EEG electrode recording channels and corresponding recording channel connectors are performed by a test fixture comprising a plurality of resistors coupled with one or more of the EEG electrode recording channels and corresponding recording channel connectors. The methods include performing an impedance test for determining if each EEG recording channel of the EEG recording device has a predefined impedance, performing a channel uniqueness test for each EEG recording channel, performing a test for verifying the state of a switch of the stimulator of the EEG recording device, and performing a test for verifying connector IDs of the recording channel connectors connecting the EEG electrodes to respective EEG recording channels.



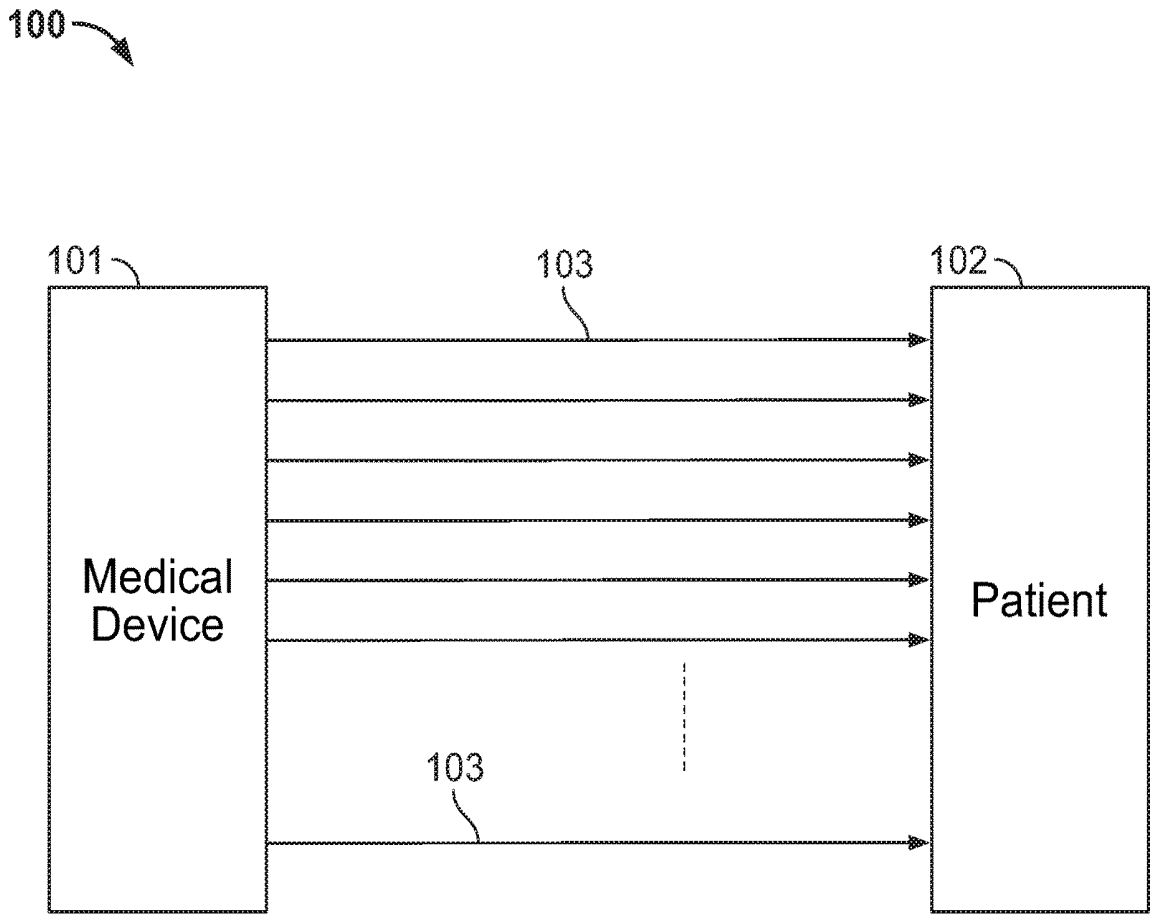


FIG. 1

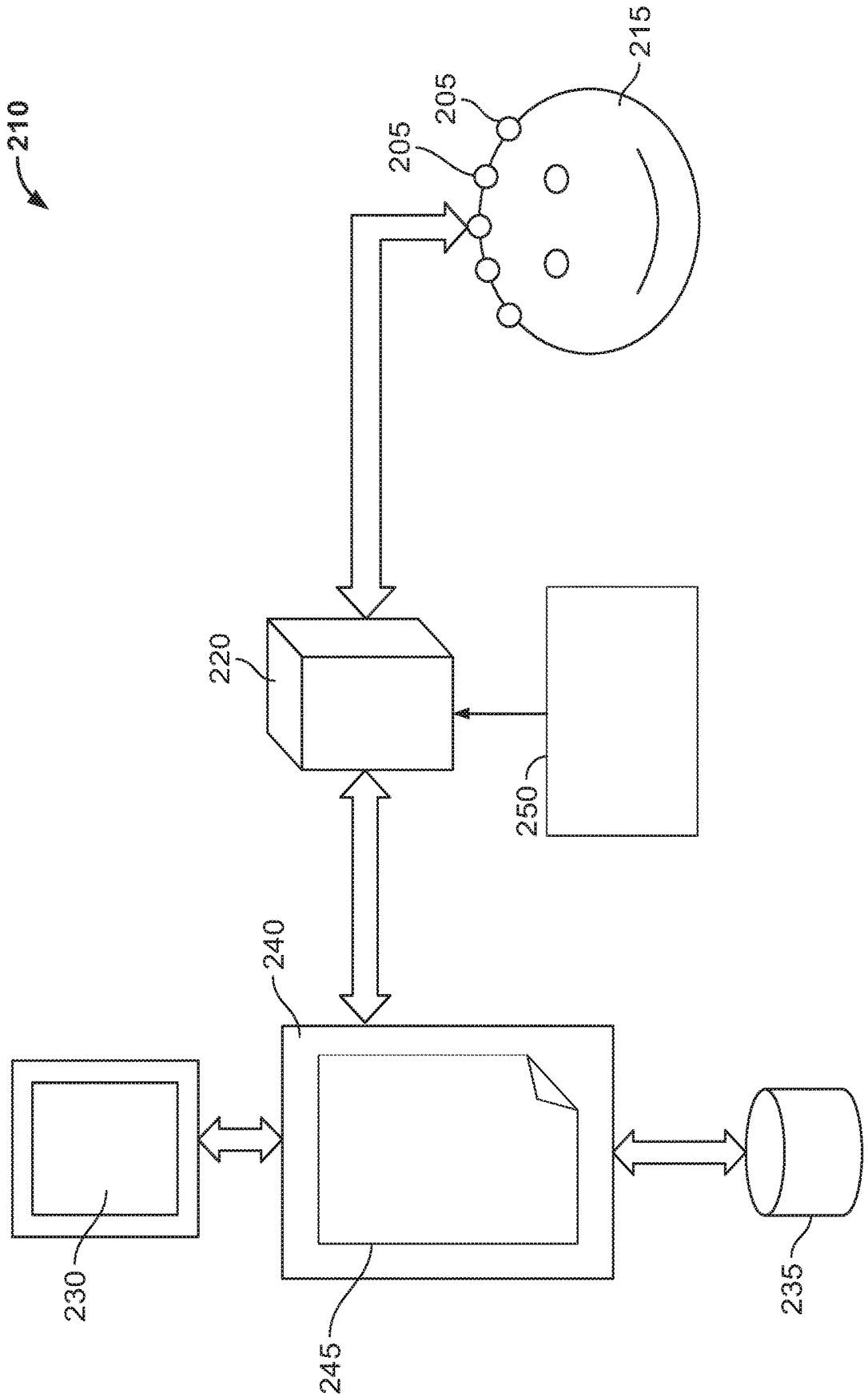


FIG. 2

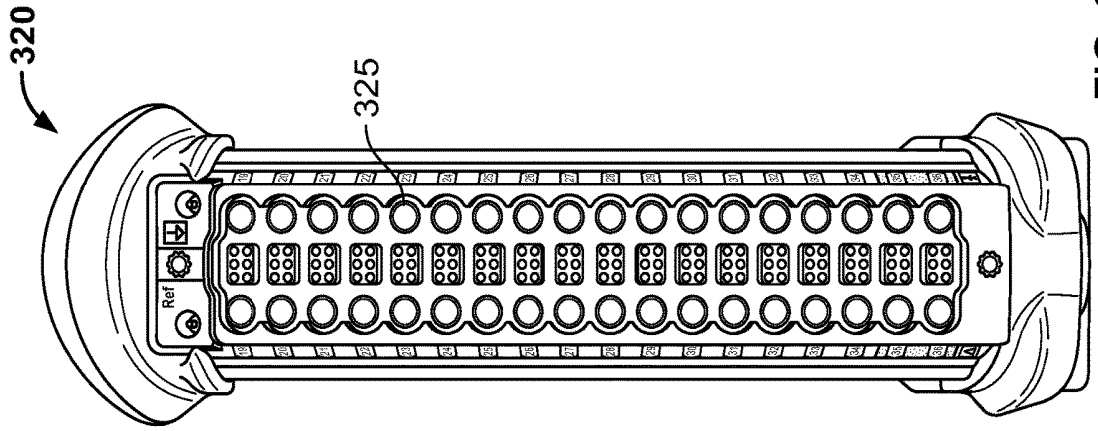


FIG. 3B

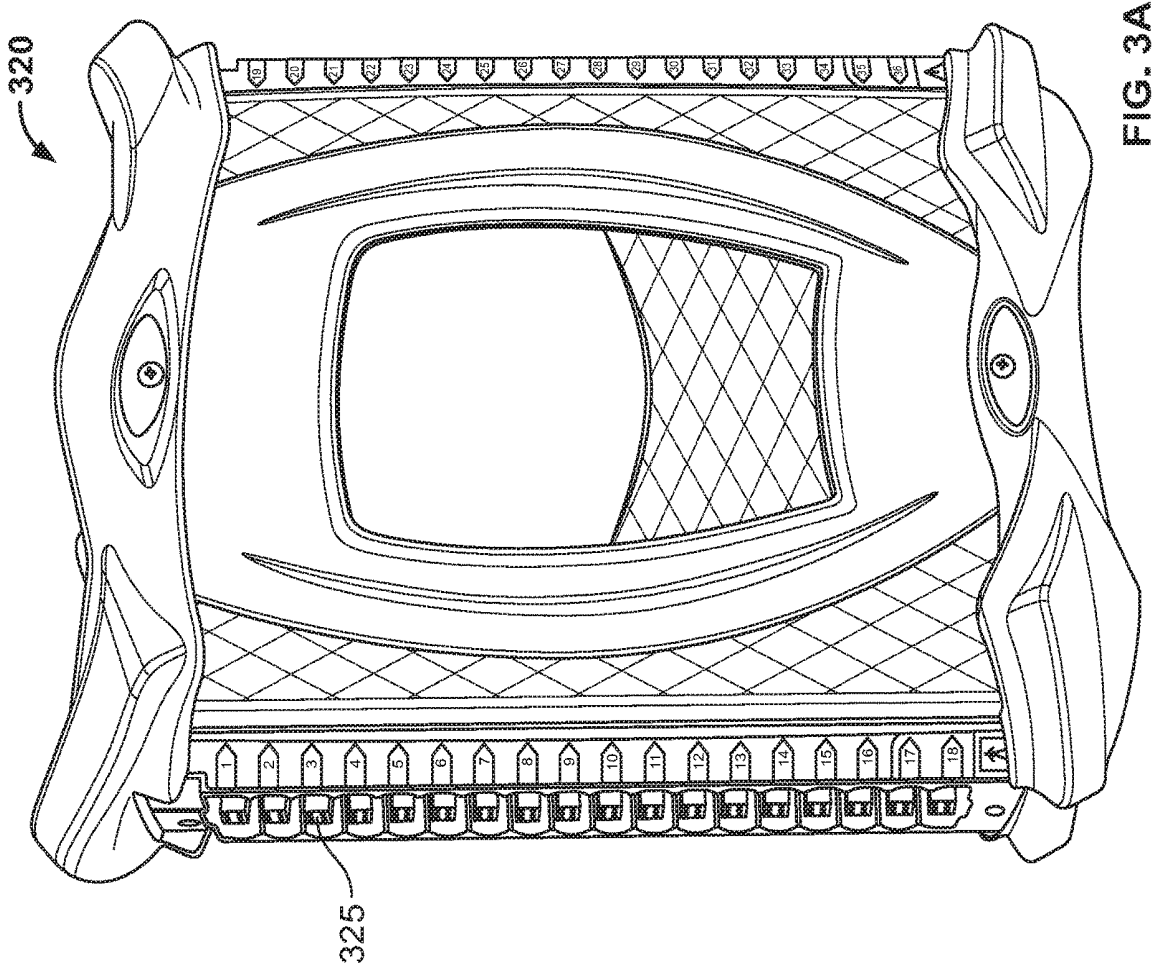


FIG. 3A

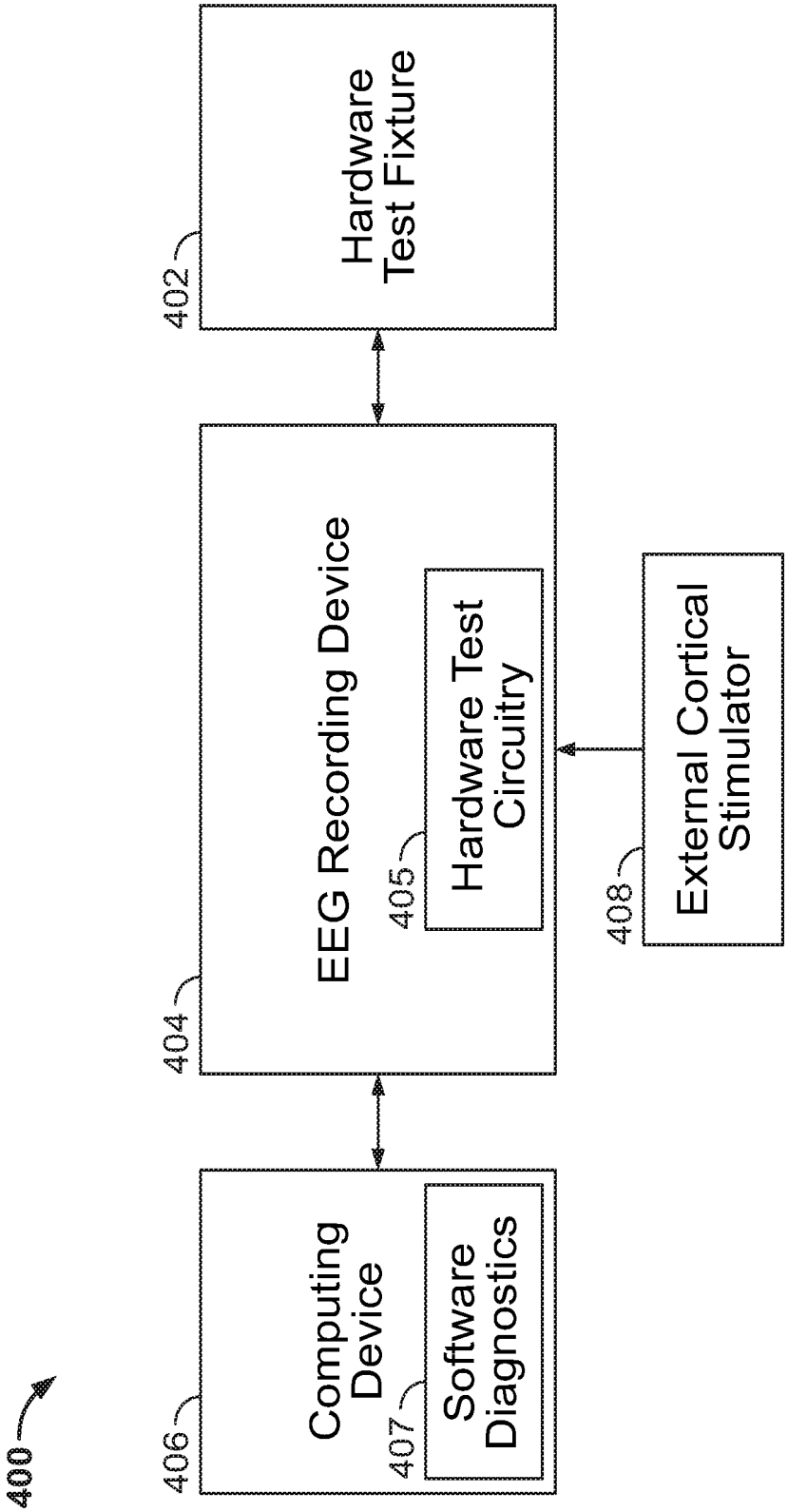

400
406
Computing Device
407
Software Diagnostics
404
EEG Recording Device
405
Hardware Test Circuitry
408
External Cortical Stimulator
402
Hardware Test Fixture

FIG. 4

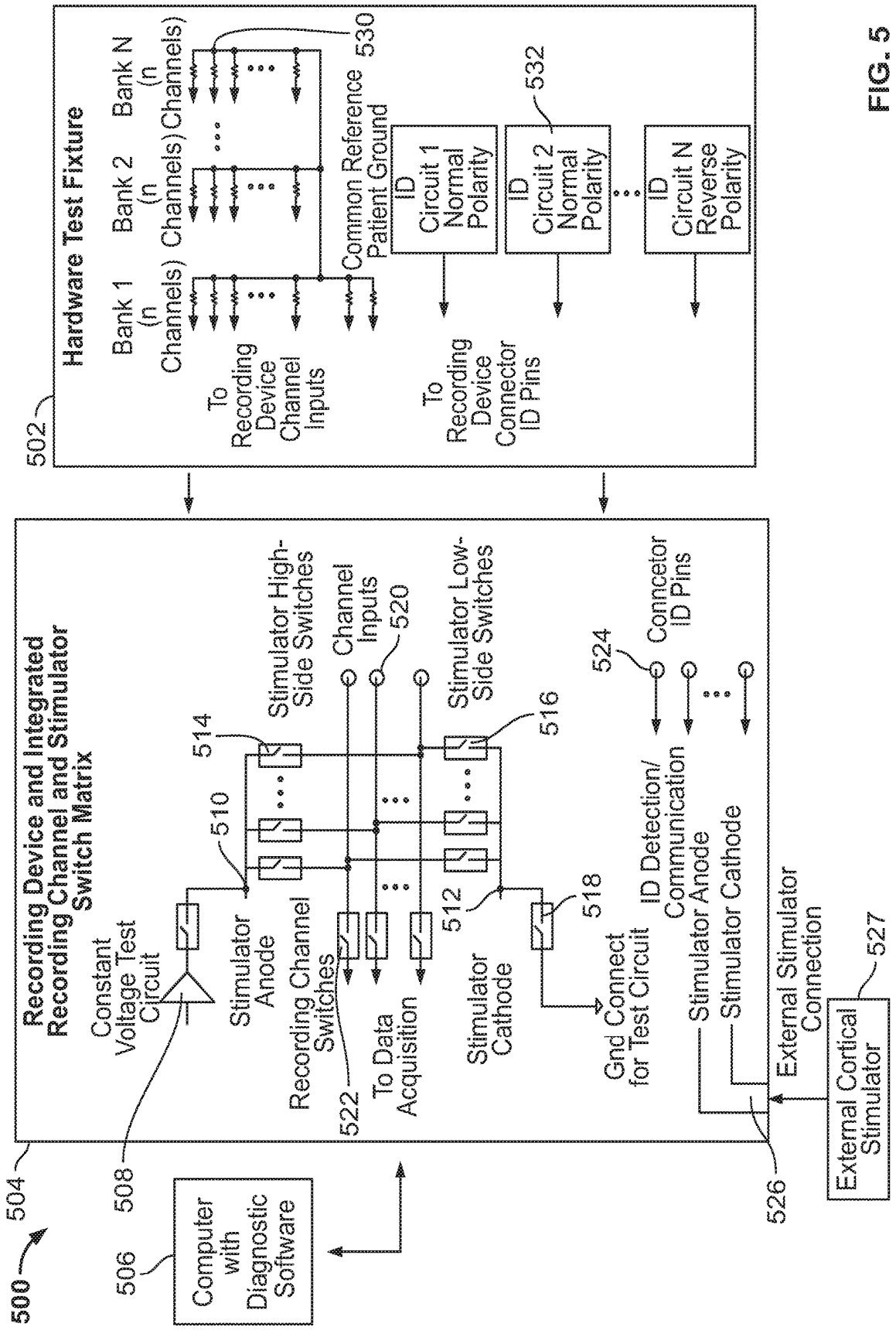

500
504
506
Computer with Diagnostic Software
508
Recording Device and Integrated Recording Channel and Stimulator Switch Matrix
Constant Voltage Test Circuit
Stimulator Anode
Recording Channel Switches
To Data Acquisition
522
510
514
Stimulator High-Side Switches
Channel Inputs
520
Stimulator Low-Side Switches
516
512
Stimulator Cathode
518
Gnd Connect for Test Circuit
524
Conncetor ID Pins
ID Detection/ Communication
Stimulator Anode
Stimulator Cathode
External Stimulator Connection
526
External Cortical Stimulator
527
502
Hardware Test Fixture
Bank 1 (n Channels)
Bank 2 (n Channels)
Bank N (n Channels)
530
Common Reference Patient Ground
To Recording Device Channel Inputs
ID Circuit 1 Normal Polarity
ID Circuit 2 Normal Polarity
532
ID Circuit N Reverse Polarity
To Recording Device Connector ID Pins

FIG. 5

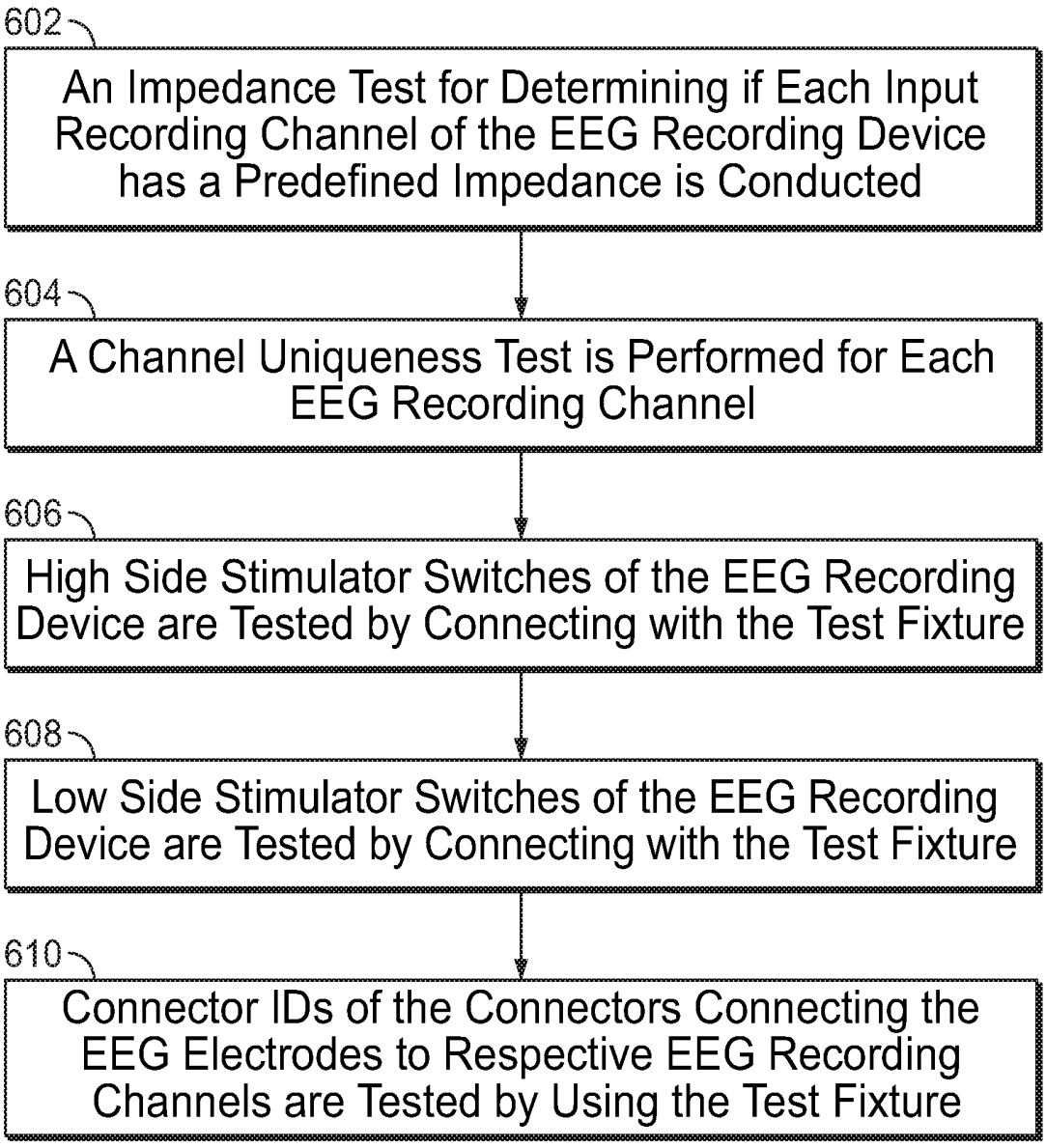

602
An Impedance Test for Determining if Each Input Recording Channel of the EEG Recording Device has a Predefined Impedance is Conducted
604
A Channel Uniqueness Test is Performed for Each EEG Recording Channel
606
High Side Stimulator Switches of the EEG Recording Device are Tested by Connecting with the Test Fixture
608
Low Side Stimulator Switches of the EEG Recording Device are Tested by Connecting with the Test Fixture
610
Connector IDs of the Connectors Connecting the EEG Electrodes to Respective EEG Recording Channels are Tested by Using the Test Fixture

FIG. 6

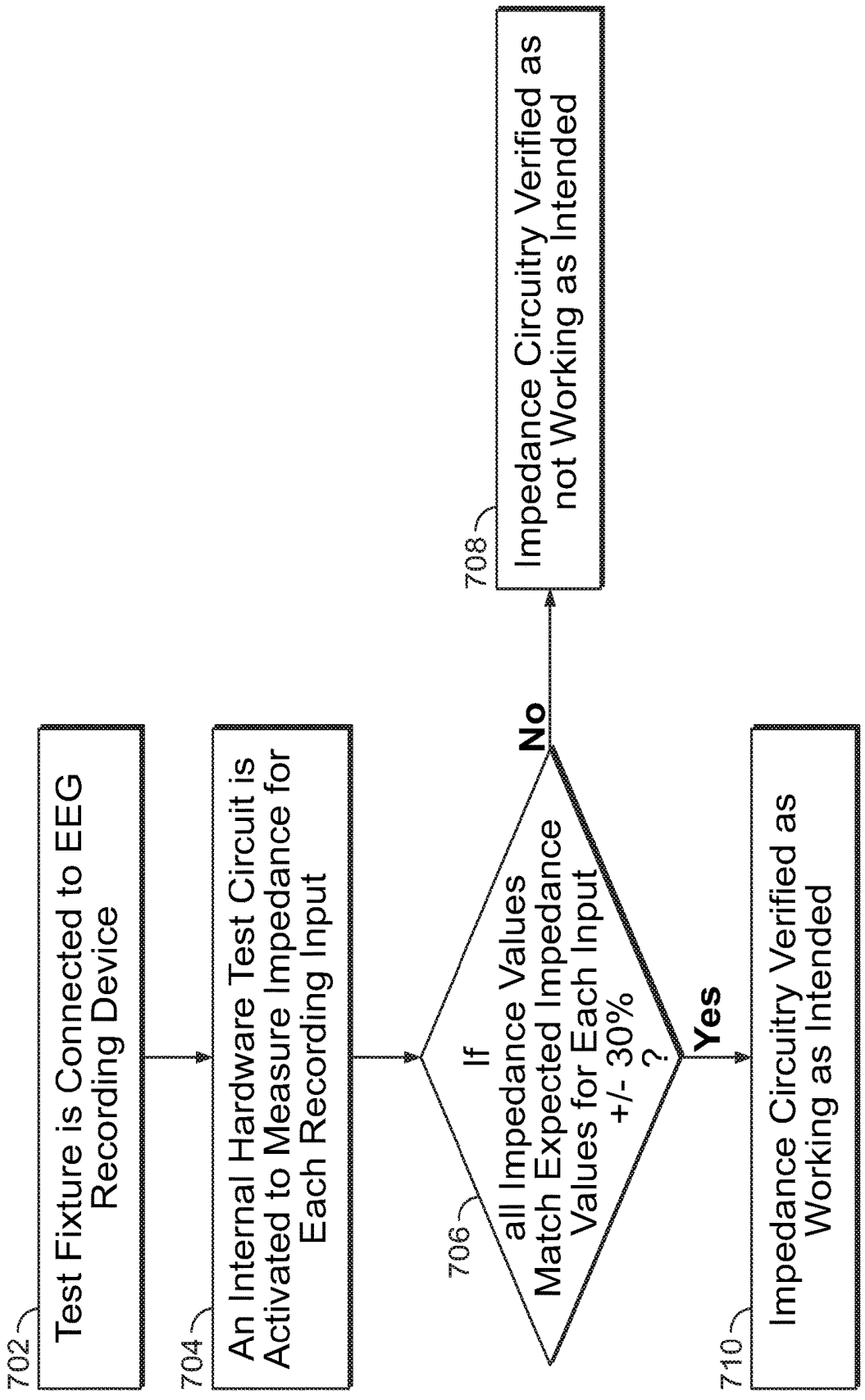

Test Fixture is Connected to EEG Recording Device
702
An Internal Hardware Test Circuit is Activated to Measure Impedance for Each Recording Input
704
If all Impedance Values Match Expected Impedance Values for Each Input +/- 30% ?
706
No
Yes
Impedance Circuitry Verified as not Working as Intended
708
Impedance Circuitry Verified as Working as Intended
710

FIG. 7

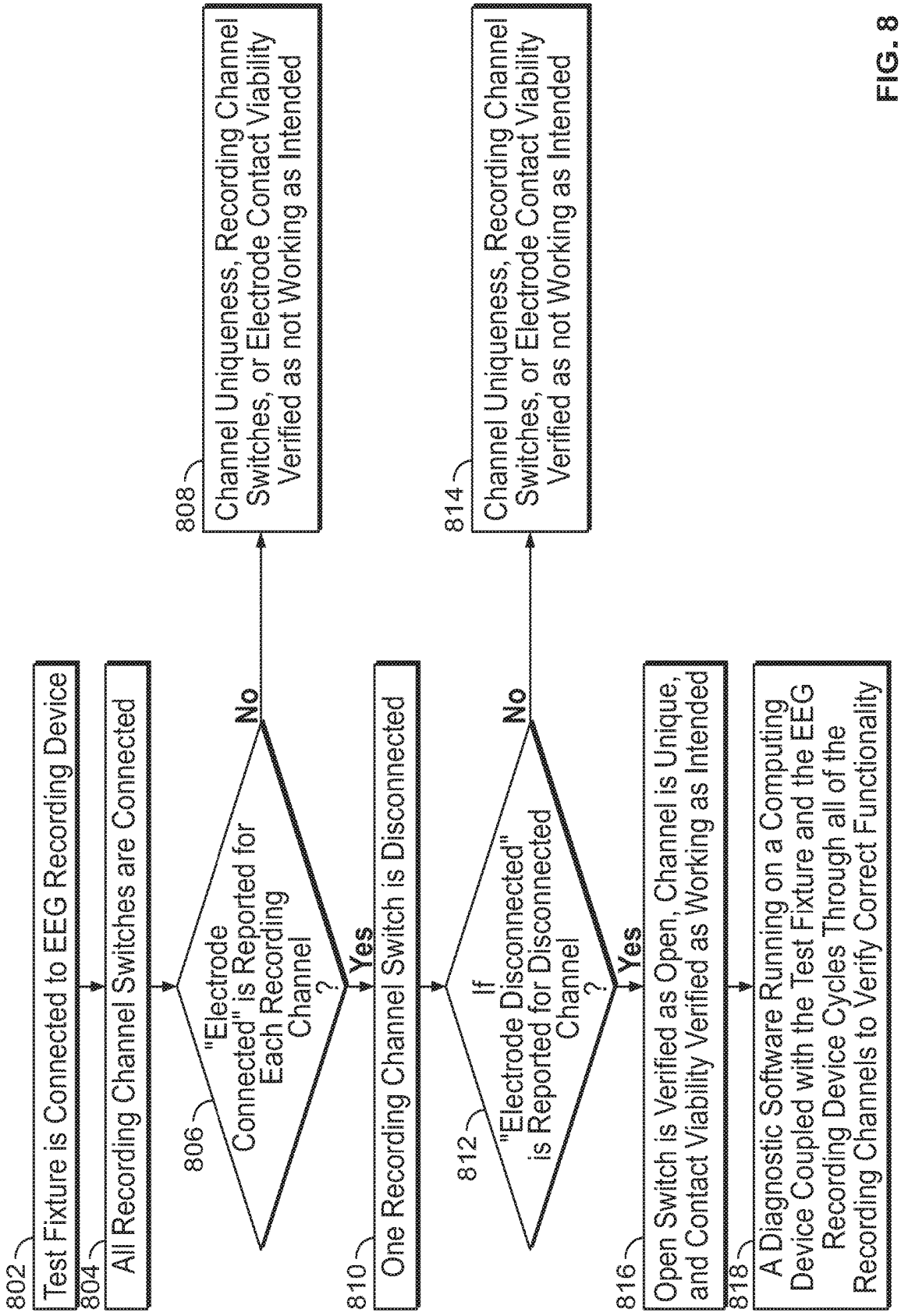

802
Test Fixture is Connected to EEG Recording Device
804
All Recording Channel Switches are Connected
806
"Electrode Connected" is Reported for Each Recording Channel ?
No
808
Channel Uniqueness, Recording Channel Switches, or Electrode Contact Viability Verified as not Working as Intended
Yes
810
One Recording Channel Switch is Disconnected
812
If "Electrode Disconnected" is Reported for Disconnected Channel ?
No
814
Channel Uniqueness, Recording Channel Switches, or Electrode Contact Viability Verified as not Working as Intended
Yes
816
Open Switch is Verified as Open, Channel is Unique, and Contact Viability Verified as Working as Intended
818
A Diagnostic Software Running on a Computing Device Coupled with the Test Fixture and the EEG Recording Device Cycles Through all of the Recording Channels to Verify Correct Functionality

FIG. 8

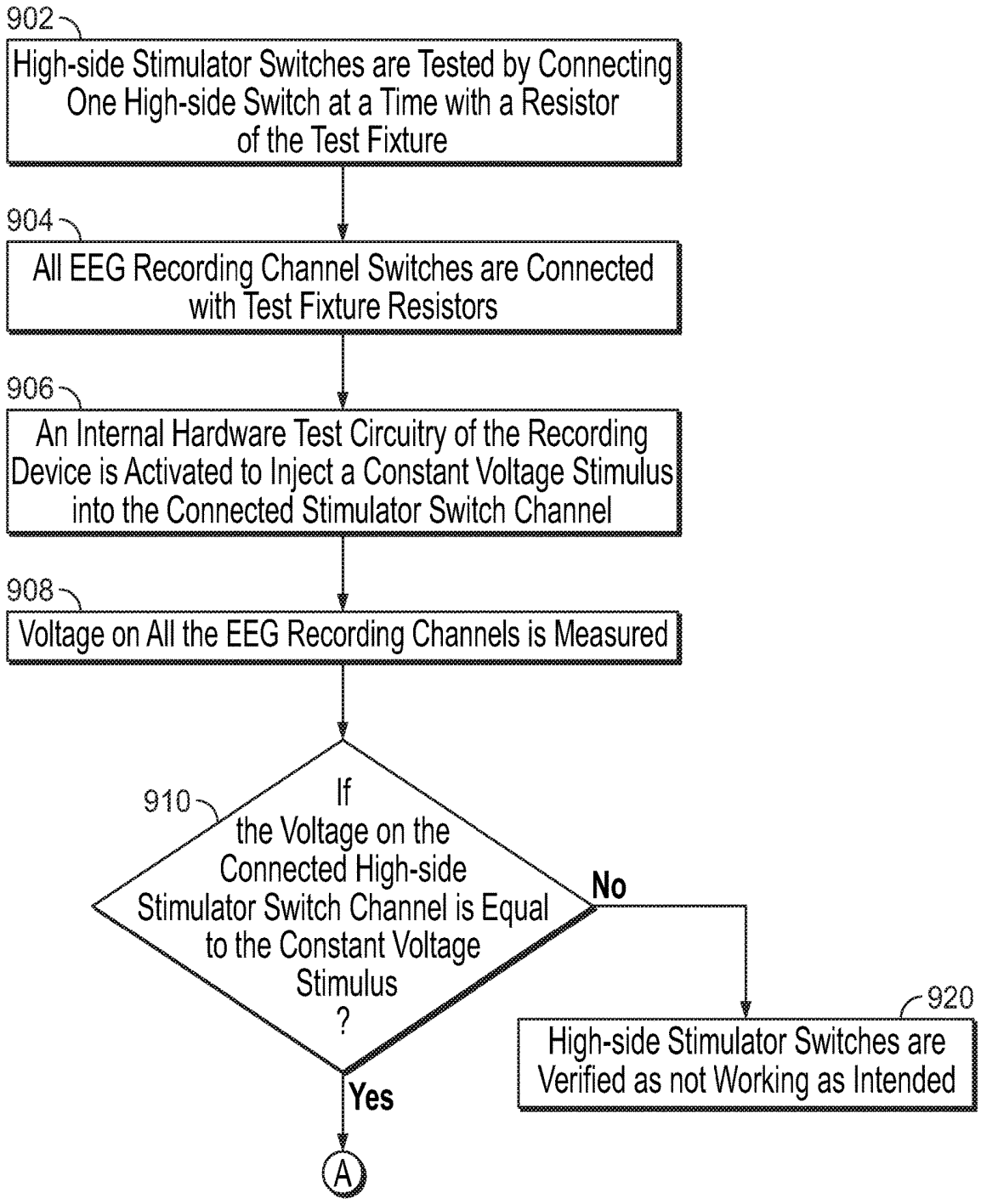

902
High-side Stimulator Switches are Tested by Connecting One High-side Switch at a Time with a Resistor of the Test Fixture
904
All EEG Recording Channel Switches are Connected with Test Fixture Resistors
906
An Internal Hardware Test Circuitry of the Recording Device is Activated to Inject a Constant Voltage Stimulus into the Connected Stimulator Switch Channel
908
Voltage on All the EEG Recording Channels is Measured
910
If the Voltage on the Connected High-side Stimulator Switch Channel is Equal to the Constant Voltage Stimulus ?
No
920
High-side Stimulator Switches are Verified as not Working as Intended
Yes
A

FIG. 9

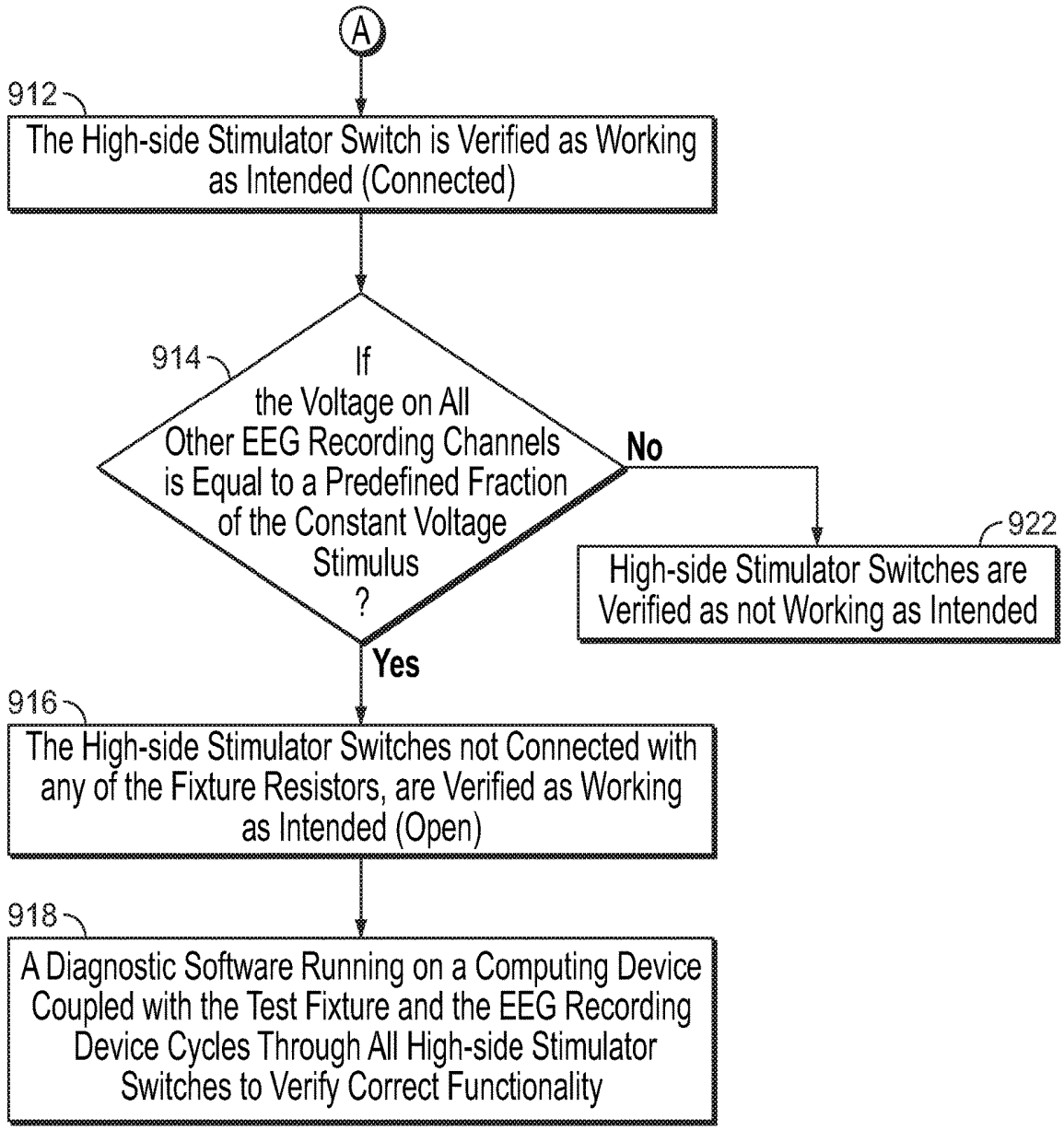

A
912
The High-side Stimulator Switch is Verified as Working as Intended (Connected)
914
If the Voltage on All Other EEG Recording Channels is Equal to a Predefined Fraction of the Constant Voltage Stimulus ?
No
922
High-side Stimulator Switches are Verified as not Working as Intended
Yes
916
The High-side Stimulator Switches not Connected with any of the Fixture Resistors, are Verified as Working as Intended (Open)
918
A Diagnostic Software Running on a Computing Device Coupled with the Test Fixture and the EEG Recording Device Cycles Through All High-side Stimulator Switches to Verify Correct Functionality

FIG. 9 (Cont.)

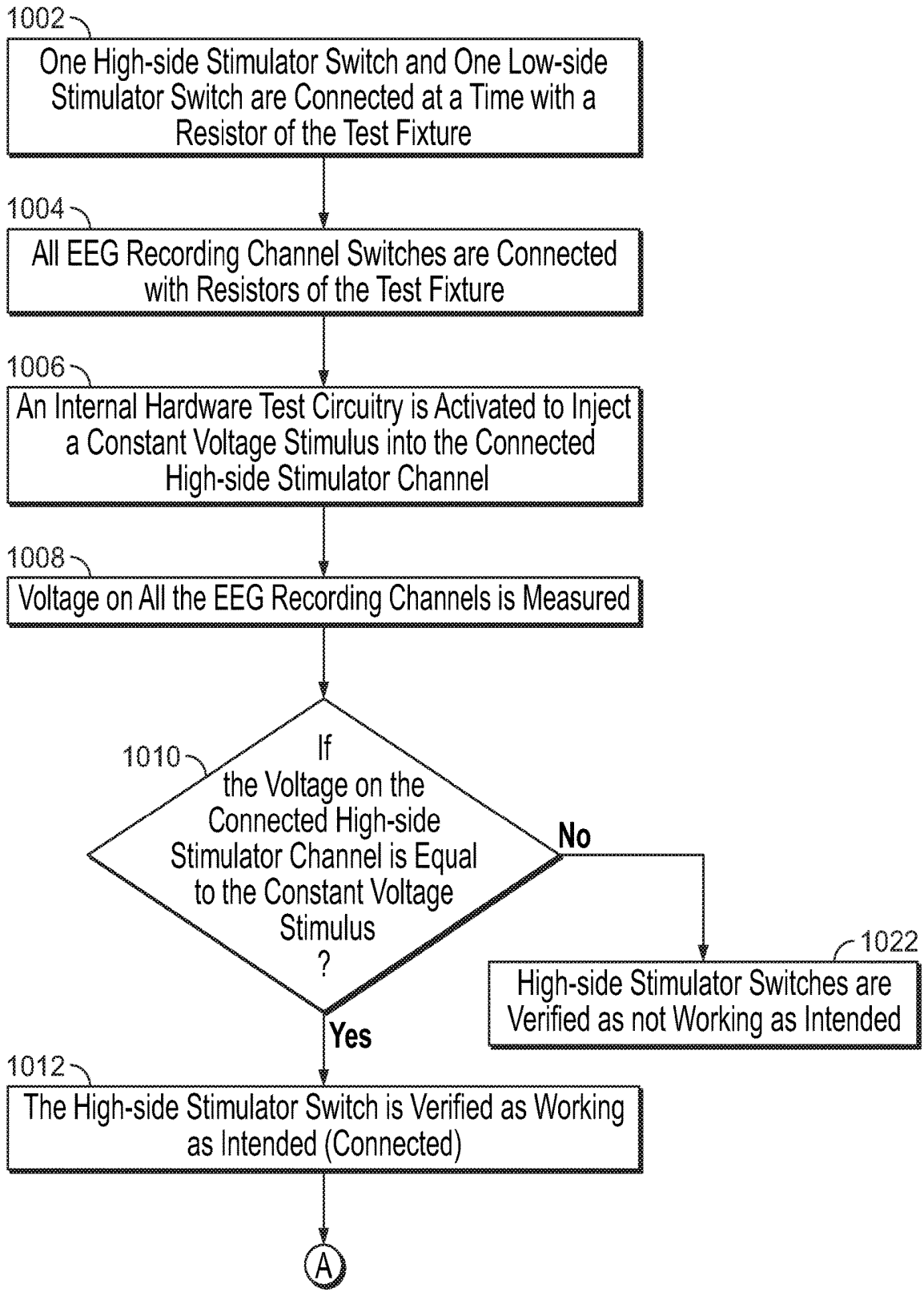

1002
One High-side Stimulator Switch and One Low-side Stimulator Switch are Connected at a Time with a Resistor of the Test Fixture
1004
All EEG Recording Channel Switches are Connected with Resistors of the Test Fixture
1006
An Internal Hardware Test Circuitry is Activated to Inject a Constant Voltage Stimulus into the Connected High-side Stimulator Channel
1008
Voltage on All the EEG Recording Channels is Measured
1010
If the Voltage on the Connected High-side Stimulator Channel is Equal to the Constant Voltage Stimulus ?
No
1022
High-side Stimulator Switches are Verified as not Working as Intended
Yes
1012
The High-side Stimulator Switch is Verified as Working as Intended (Connected)
A

FIG. 10

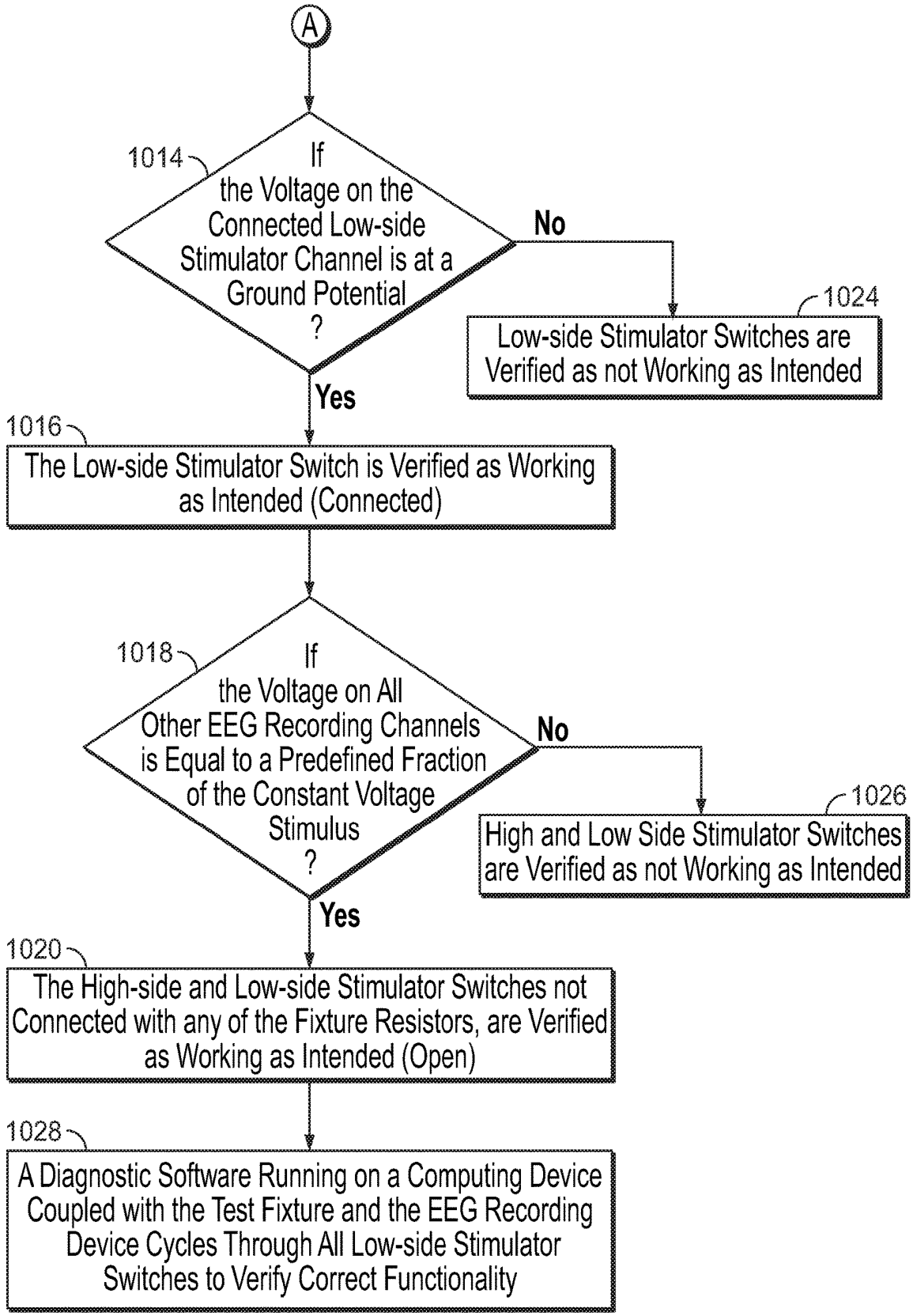

A
1014
If the Voltage on the Connected Low-side Stimulator Channel is at a Ground Potential ?
No
1024
Low-side Stimulator Switches are Verified as not Working as Intended
Yes
1016
The Low-side Stimulator Switch is Verified as Working as Intended (Connected)
1018
If the Voltage on All Other EEG Recording Channels is Equal to a Predefined Fraction of the Constant Voltage Stimulus ?
No
1026
High and Low Side Stimulator Switches are Verified as not Working as Intended
Yes
1020
The High-side and Low-side Stimulator Switches not Connected with any of the Fixture Resistors, are Verified as Working as Intended (Open)
1028
A Diagnostic Software Running on a Computing Device Coupled with the Test Fixture and the EEG Recording Device Cycles Through All Low-side Stimulator Switches to Verify Correct Functionality

FIG. 10 (Cont.)

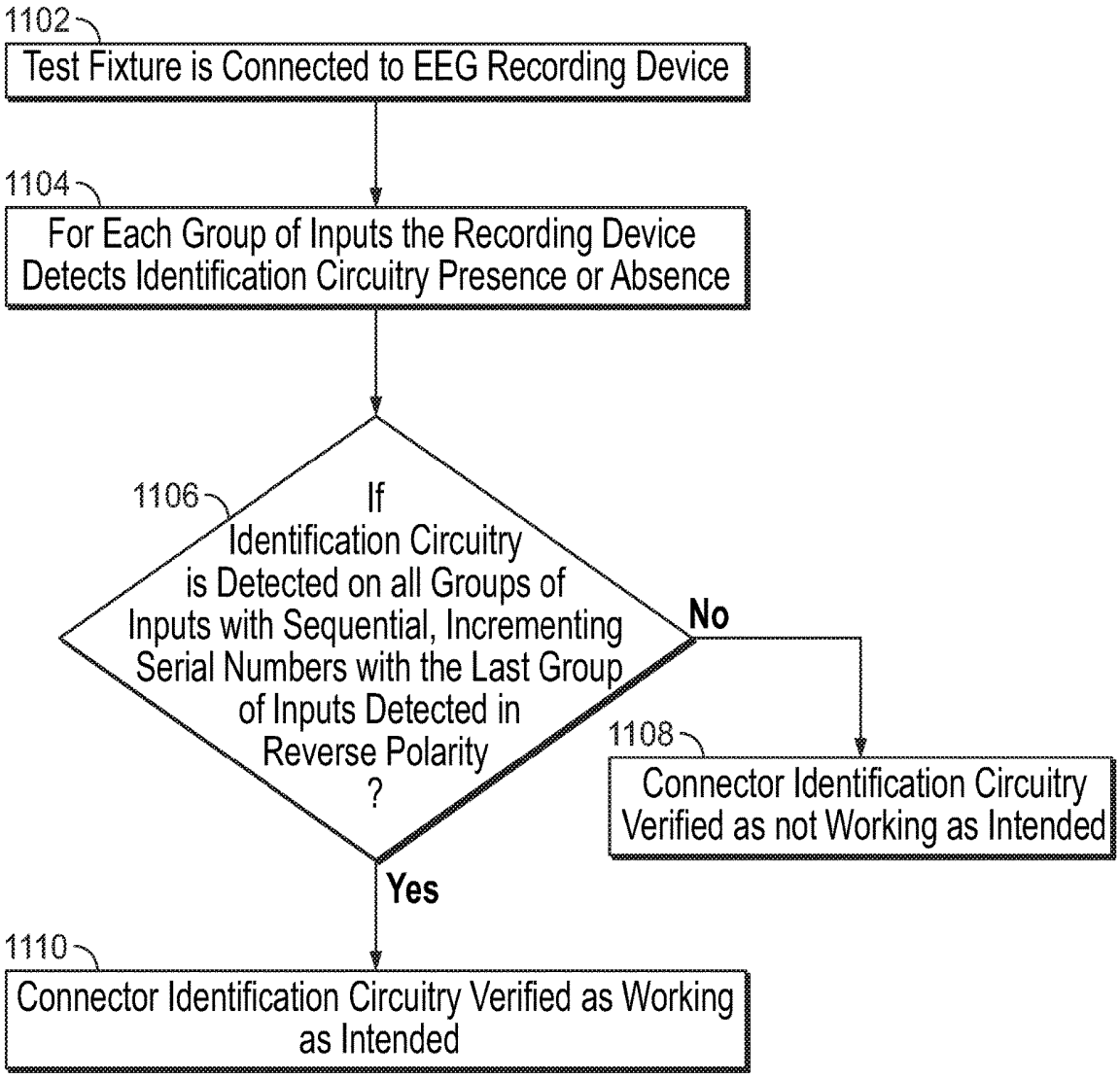

1102
Test Fixture is Connected to EEG Recording Device
1104
For Each Group of Inputs the Recording Device Detects Identification Circuitry Presence or Absence
1106
If Identification Circuitry is Detected on all Groups of Inputs with Sequential, Incrementing Serial Numbers with the Last Group of Inputs Detected in Reverse Polarity ?
No
1108
Connector Identification Circuitry Verified as not Working as Intended
Yes
1110
Connector Identification Circuitry Verified as Working as Intended

FIG. 11

INTEGRITY VERIFICATION SYSTEM FOR TESTING HIGH CHANNEL COUNT NEUROMONITORING RECORDING EQUIPMENT

CROSS-REFERENCE

[0001] The present application relies on U.S. Patent Provisional Application No. 62/758,320, entitled "Integrity Verification System for Testing High Channel Count Neuromonitoring Recording Equipment" and filed on Nov. 9, 2018, for priority, which is herein incorporated by reference in its entirety.

FIELD

[0002] The present specification is related generally to the field of electroencephalography (EEG), particularly electrocorticography (ECoG) and stereoelectroencephalography (sEEG). More specifically, the present specification is related to an integrity verification system (IVS) for verifying operational integrity of an ECoG or sEEG recording device prior to starting a neuromonitoring recording procedure.

BACKGROUND

[0003] Neuromonitoring is the use of electrophysiological methods, such as electroencephalography (EEG), electromyography (EMG), and evoked potentials, to monitor the functional integrity of certain neural structures (e.g., nerves, spinal cord and parts of the brain) during surgery. The purpose of neuromonitoring is to reduce the risk to the patient of iatrogenic damage to the nervous system, and/or to provide functional guidance to the surgeon and anesthesiologist, for example, to map the brain of epileptic patients to determine candidates for surgical treatment. Generally, neuromonitoring procedures such as EEG involve a large number of electrodes coupled to the human body. In an EEG procedure, the electrodes are used to record and monitor the electrical activity corresponding to various parts of the brain for detection and treatment of various ailments such as epilepsy, sleep disorders and coma. EEG procedures are either non-invasive or invasive. In non-invasive EEG, a number of electrodes are deployed on the human scalp for recording electrical activity in portions of the underlying brain. In invasive EEG, through surgical intervention, the electrodes are placed directly over sections of the brain, in the form of a strip or grid, or are positioned in the deeper areas of the brain. Each of these electrodes is coupled to a wire lead which, in turn, is connected to a control unit adapted to receive and transmit electrical signals. The electrical activity pattern captured by various electrodes is analyzed using standard algorithms to localize or spot the portion of brain which is responsible for causing the specific ailment.

[0004] The number of electrodes in EEG systems typically varies between 21 and 256 and can be more than 500. Increasing the number of electrodes in EEG procedures helps decrease the localization error and thus more ably assist the physician to better plan for surgical procedures. Accordingly, advanced EEG systems involve a high density electrode configuration with more than 256 electrodes for separately mapping the electrical activity corresponding to every portion of the brain. However, the overall set up and verification process becomes more time consuming and error prone as the number of electrodes increases in the EEG procedures. An error in the EEG data presented to the physician could have severe adverse effects on the patient involved. Thus, as the number of channels increase it is vital that the methods to verify a required functionality of the EEG equipment also increasingly improve in efficiency and efficacy.

[0005] In neuromonitoring, as each electrode is positioned at a different location to capture the electrical activity in its vicinity, the input recorded from each electrode has to be processed independently. The system is required to maintain the identity of each electrode and accordingly process the input received from that electrode. Surgical applications in EEG also use grid electrodes which inherently combine multiple leads (up to 16) into a single connector, which is then attached to an adapter with 16 individual leads, and then to an amplifier that has inputs for each individual channel.

[0006] An intracranial EEG procedure requires accurate information such as but not limited to electrode impedance values, and electrode contact viability from the EEG recording device being used. If the EEG recording device includes an integrated switch matrix for an internal or external cortical stimulator, the respective ON/OFF states of the recording channel switches and stimulator switches must also be functional and correct to provide accurate information to a physician. It is also important that each channel input is acting uniquely (i.e. no shorts between channels) and that each channel is designated correctly from the patient to the software. If the patient connections to the recording device use programmed unique identifiers to be correctly designated in the software, this functionality is also vital for providing accurate information to the physician.

[0007] Electrocorticography (ECoG) and stereoelectroencephalography (sEEG) are methods of EEG monitoring and cortical mapping that require high channel count recording and stimulating devices. In ECoG, electrodes are placed on the cerebral cortex via a craniotomy. In sEEG, depth electrodes may be placed via small holes (burr holes) drilled in the patient's skull. ECoG and sEEG may be used when standard EEG monitoring results are inconclusive, particularly for epilepsy patients. Since ECoG and sEEG use strip or grid electrodes and depth electrodes on the surface of the brain and in the brain respectively, they provide a benefit of using electrodes that are closer to the area(s) producing seizures than electrodes placed on the scalp in standard EEG monitoring. In addition, placed directly on or in the brain have the advantage of recording signals without the interference of skin, fat tissue, muscle or bone. ECoG and sEEG may be used to monitor, assess and map the brains of epilepsy patients who have may benefit from surgery and have not responded to less invasive treatments including pharmaceuticals. Mapping will indicate to physicians' areas of an epileptic brain for resection and functional areas of the brain to be safeguarded during surgery. Functional mapping involves using a cortical stimulator to generate stimulus through the electrodes (grid or strip) to stimulate the brain and record signals to identify the underlying function of a brain region, such as language, sensation, or motor function, to precisely map an origin of seizures. When a discrete epileptogenic region of the brain is identified and can be removed without the introduction of unacceptable additional neurological deficits, respective surgery is performed. Prior to performing this EEG monitoring, multiple aspects of a recording device with integrated recording channel and

stimulator switch matrix must be tested to ensure the equipment is working as intended. This testing can be burdensome with large channel count systems.

[0008] Prior art patent publications disclose a number of methods of impedance measurement in an EEG recording device. US Patent Publication No. 20060020218 discloses "[a] method comprising: sending a test signal to a sensor of physiological data, said sensor having an impedance; receiving a combined signal comprising a physiological signal component and a test signal component; filtering the combined signal to separate the physiological signal component from the test signal component; and detecting changes in the impedance of the sensor by a comparison of test signal components."

[0009] WIPO Publication No. WO2018102855A1 discloses "[a] biological amplifier for measuring an electrical activity of nerve cells of a physiological function in a subject, comprising: (a) a plurality of electrodes, at least one of which is a sensor electrode for measuring the electrical activity, the or each sensor electrode adapted to be placed on the skin of the subject above the nerve cells, and (b) means for measuring contact impedance between the skin of the subject and the or each sensor electrode due to a voltage applied between the plurality of electrodes, wherein the contact impedance measuring means operates continuously and concurrently with the measuring of the electrical activity of the nerve cells of the physiological function by the biological amplifier."

[0010] Some prior art publications also disclose methods for measuring electrode lead integrity in EEG recording devices. US Patent Publication No. 20090299201 discloses "[a] method comprising: obtaining impedance trend data for an electrical path, the electrical path comprising a plurality of electrodes; obtaining additional diagnostic data that is associated with the electrical path, the additional diagnostic data being distinct from the impedance trend data; and combining both the impedance trend data and the additional diagnostic data into a displayable report that indicates whether there is a possible condition with the electrical path."

[0011] US Patent Publication No. 20100023084 discloses "[a] method comprising: sensing a physiological signal of a patient via one or more electrodes on at least one implantable medical lead; detecting saturation of the signal; and triggering a lead integrity test of the implantable medical lead in response to the detection."

[0012] Switching a cortical stimulator between multiple recording channels is described in US Patent Publication No. 20100298907A1 which discloses "[a] cortical stimulator system, comprising: a stimulation device having a switch configured to selectively control various electrodes; and a user interface device operatively connected to the stimulation device for controlling the electronic switch and stimulation device, the cortical stimulator system configured to provide a report of provided stimulation."

[0013] However, none of the prior art mentioned above disclose a verification system or an integrity verification system (IVS) which incorporates a hardware test fixture, associated hardware test circuitry, and software diagnostics for testing multiple aspects of an EEG recording device and integrated switch matrix. Hence, there is need for an IVS that can verify the functionality of impedance measurement, electrode contact viability measurement, both recording channel and stimulator switch ON/OFF states, channel uniqueness, and correct identification (ID) of the unique identifiers of the patient connections prior to beginning a procedure.

SUMMARY

[0014] The following embodiments and aspects thereof are described and illustrated in conjunction with systems, tools and methods, which are meant to be exemplary and illustrative, and not limiting in scope. The present application discloses numerous embodiments.

[0015] The present specification discloses a method of performing a diagnostic test on an electroencephalography (EEG) recording device, wherein the EEG recording device comprises 1) at least one stimulator coupled with a plurality of EEG electrode recording channels and 2) recording channel connectors connecting one or more EEG electrodes to the plurality of EEG electrode recording channels and wherein the diagnostic test is performed by a hardware testing device comprising a plurality of resistors coupled with one or more of the plurality of EEG electrode recording channels and corresponding recording channel connectors, the method comprising: performing an impedance test for determining if each EEG recording channel of the plurality of EEG electrode recording channels has a predefined impedance; performing a channel uniqueness test for each EEG recording channel of the plurality of EEG electrode recording channels; performing a test for verifying a state of a switch of the at least one stimulator of the EEG recording device; and performing a test for verifying correct functionality of connector identification detection and communication for electrode connections.

[0016] Optionally, the at least one stimulator comprises hardware test circuitry comprising a constant voltage test stimulator. Optionally, the constant voltage test stimulator comprises a stimulator anode to connect to the stimulator high side switches, a stimulator cathode to connect to the stimulator low side switches, and a ground connect for the constant voltage test stimulator. Optionally, performing a test for verifying the state of a switch of the stimulator of the EEG recording device comprises performing a test for verifying a state of the high side stimulator switches. Optionally, performing a test for verifying the state of a switch of the stimulator of the EEG recording device comprises performing a test for verifying a state of the low side stimulator switches. Optionally, performing a test for verifying the state of the high side stimulator switches comprises: connecting one of the high side simulator switches with one of the plurality of resistors of the hardware testing device; connecting the plurality of EEG electrode recording channels with the plurality of resistors of the hardware testing device; injecting a stimulus into the one of the high side simulator switches, wherein the stimulus is defined by a voltage or current level; measuring a voltage on the plurality of EEG electrode recording channels; verifying that the one of the high-side stimulator switches is connected with at least one of the plurality of resistors if the measured voltage is equal to the expected stimulus level; and verifying that the one of the high-side stimulator switches is not connected with any of the plurality of resistors, if the measured voltage is equal to a predefined fraction of the stimulus voltage. Optionally, wherein injecting the stimulus comprises injecting a constant-voltage stimulus. Optionally, injecting a stimulus comprises injecting a constant-current stimulus.

[0017] Optionally, performing a test for verifying the state of the low side stimulator switches comprises: connecting one of the high-side stimulator switches to one of the plurality of resistors and one of the low-side stimulator switches to one of the plurality of resistors; connecting the plurality of EEG electrode recording channels with the plurality of resistors; injecting a stimulus into the one of the high-side stimulator switches; measuring a voltage on at least one of the plurality of EEG electrode recording channels; and verifying that the one of the low-side stimulator switches is working if the measured voltage is at a ground potential. Optionally, injecting the stimulus comprises injecting a constant-voltage stimulus. Optionally, injecting a stimulus comprises injecting a constant-current stimulus.

[0018] The at least one stimulator may comprise a stimulator external to the EEG recording device.

[0019] Optionally, performing the channel uniqueness test for each of the plurality of EEG electrode recording channels includes performing a lead-off functionality test.

[0020] Optionally, performing the channel uniqueness test comprises: connecting the hardware testing device to the EEG recording device; connecting the plurality of resistors of the hardware testing device to the plurality of EEG electrode recording channels; determining if an electrode connected status is reported for each of the plurality of EEG electrode recording channels; and determining one or more of: a recording channel uniqueness, a recording channel component, or an electrode contact viability as not working as intended if an electrode connected status is not reported for each of the plurality of EEG electrode recording channels. Optionally, performing the channel uniqueness test further comprises: disconnecting one of the plurality of EEG electrode recording channels from one or more of the plurality of resistors of the hardware testing device and determining if an electrode disconnected status is reported for the disconnected one of the plurality of EEG electrode recording channels. Optionally, performing the channel uniqueness test further comprises: verifying one or more of a recording channel uniqueness, a recording channel component, or an electrode contact viability as not working as intended if an electrode disconnected status is not reported for the disconnected one of the plurality of EEG electrode recording channels; and determining a working status of the one of the plurality of EEG electrode recording channels if an electrode disconnected status is reported for the disconnected one of the plurality of EEG electrode recording channels.

[0021] Optionally, the method further comprises cycling through the plurality of EEG electrode recording channels using a diagnostic software running on a computing device coupled with the hardware testing device and the EEG recording device to verify a required functionality.

[0022] Optionally, performing a test for verifying a state of a switch of the at least one stimulator comprises verifying a state of device switches and integrated stimulation switch matrix switches.

[0023] Optionally, performing the impedance test comprises: connecting the hardware testing device to the EEG recording device; activating a mode within the EEG recording device to measure an impedance for each of the plurality of EEG electrode recording channels; determining if measured impedance values match expected impedance values within a predetermined margin of error; determining that the one or more of the plurality of EEG electrode recording channels are not working as intended if the measured impedance values do not match the expected impedance values within the predetermined margin of error; and verifying that the one or more of the plurality of EEG electrode recording channels are working as intended if the measured impedance values match the expected impedance values within the predetermined margin of error. Optionally, the predetermined margin of error is +/−30% of the expected impedance value.

[0024] Optionally, performing the test for verifying correct functionality of connector identification detection and communication for electrode connections comprises: connecting the hardware testing device to the EEG recording device; detecting a presence or absence of a connector identification circuitry with respect to predefined groups of the plurality of EEG electrode recording channels; determining if the connector identification circuitry is detected on the groups of the plurality of EEG electrode recording channels, wherein the detected connector identification circuitry comprises sequential, incrementing serial numbers corresponding to sequential groups of recording channels; determining the connector identification circuitry as not working as intended if the connector identification circuitry is not detected on the plurality of EEG electrode recording channels and comprises sequential, incrementing serial numbers; and verifying the connector identification circuitry as working as intended if the connector identification circuitry is detected on the plurality of EEG electrode recording channels and comprises sequential, incrementing serial numbers. Optionally, at least one of the connector identification circuitries has a polarity that is a reverse of a polarity of the other connector identification circuitries. Optionally, the plurality of EEG electrode recording channels is grouped into predefined groups of inputs for each side of the EEG recording device, wherein each of the predefined groups comprises 4 recording channels.

[0025] The present specification also discloses a method of performing diagnostic tests on an EEG recording device comprising at least one stimulator coupled with a plurality of EEG electrode recording channels and corresponding recording channel connectors connecting one or more EEG electrodes to the recording channels. The diagnostic tests are performed by a test fixture comprising a plurality of resistors coupled with one or more of the EEG electrode recording channels and corresponding recording channel connectors, the method comprising: performing an impedance test for determining if each EEG recording channel of the EEG recording device has a predefined impedance; performing a channel uniqueness test for each EEG recording channel; performing a test for verifying the state of a switch of the stimulator of the EEG recording device; and performing a test for verifying connector IDs of the recording channel connectors connecting the one or more EEG electrodes to respective EEG recording channels.

[0026] Optionally, the at least one stimulator comprises hardware test circuitry comprising a constant voltage test stimulator. The constant voltage test stimulator may comprise a stimulator anode, a stimulator cathode, a plurality of stimulator high side switches, a plurality of stimulator low side switches, and a ground connect for the voltage test stimulator. Optionally, performing a test for verifying the state of a switch of the stimulator of the EEG recording

device comprises performing a test for verifying the state of the high side stimulator switches of the EEG recording device.

[0027] Optionally, performing a test for verifying the state of a switch of the stimulator of the EEG recording device comprises performing a test for verifying the state of the low side stimulator switches of the EEG recording device.

[0028] Optionally, performing a test for verifying the state of the high side stimulator switches of the EEG recording device comprises: connecting one high-side switch at a time with a resistor of the test fixture; connecting all the EEG recording channels with the test fixture resistors; injecting a stimulus into the connected high-side switch; measuring the voltage on all the EEG recording channels; verifying that the high-side stimulator switch is working as intended (connected) if the voltage on the connected high-side stimulator switch channel is equal to the constant voltage stimulus; and verifying that the high-side stimulator switches are not connected with any of the fixture resistors, if voltage on all other EEG recording channels is equal to a predefined fraction of the constant voltage stimulus.

[0029] Optionally, injecting a stimulus into the connected high-side switch comprises injecting a constant-voltage stimulus. Optionally, injecting a stimulus into the connected high-side switch comprises injecting a constant-current stimulus.

[0030] Optionally, performing a test for verifying the state of the low side stimulator switches of the EEG recording device comprises: connecting one high-side stimulator switch and one low-side stimulator switch at a time with a resistor of the test fixture; connecting all the EEG recording channels with the test fixture resistors; injecting a constant-voltage stimulus into the connected high-side switch; measuring the voltage on all the EEG recording channels; and verifying that the low-side stimulator switch is working as intended (connected), if the voltage on the connected low-side stimulator channel is at a ground potential.

[0031] Optionally, the at least one stimulator comprises an external stimulator. Optionally, performing a channel uniqueness test for each EEG recording channel includes a "lead-off" functionality test.

[0032] Optionally, performing a channel uniqueness test for each EEG recording channel comprises: connecting the test fixture to the EEG recording device; connecting the plurality of resistors of the hardware testing device to the recording channels of the EEG recording device; determining if a status of "electrode connected" is reported for each recording channel; verifying one or more of: a recording channel uniqueness, a recording channel component, or an electrode contact viability as 'not working as intended', if a status of "electrode connected" is not reported for each recording channel; disconnecting one recording channel from the plurality of resistors of the hardware testing device, if a status of "electrode connected" is reported for each recording channel; determining if a status of "electrode disconnected" is reported for the disconnected channel; verifying one or more of: a recording channel uniqueness, a recording channel component, or an electrode contact viability as 'not working as intended', if a status of "electrode disconnected" is not reported for the disconnected channel; and verifying an 'as intended' working of the recording channels of the EEG recording device, if a status of "electrode disconnected" is reported for the disconnected channel.

[0033] Optionally, verifying that a recording channel component is 'not working as intended' comprises verifying that a switch of the recording channel is 'not working as intended'. Optionally, when performing a channel uniqueness test for each EEG recording channel, the method further comprises the step of cycling through all of the recording channels using a diagnostic software running on a computing device coupled with the test fixture and the EEG recording device to verify a required functionality.

[0034] Optionally, performing a test for verifying the state of a switch of the stimulator of the EEG recording device includes verifying the state of device switches and integrated stimulation switch matrix switches.

[0035] Optionally, performing an impedance test for determining if each EEG electrode recording channel of the EEG recording device has a predefined impedance comprises: connecting the test fixture to the EEG recording device; activating an internal hardware test circuit of the test fixture to measure impedance for each EEG electrode recording channel; determining if the measured impedance values match an expected impedance value allowing for a predetermined margin of error; verifying that the electrode recording channels are 'not working as intended', if the measured impedance values do not match the expected impedance value allowing for a predetermined margin of error; and verifying that the electrode recording channels are 'working as intended', if all impedance values match the expected impedance value allowing for a predetermined margin of error. In an embodiment, the predetermined margin of error is +/−30% of the expected impedance value.

[0036] Optionally, performing a test for verifying connector IDs of the recording channel connectors connecting the one or more EEG electrodes to respective EEG recording channels comprises: connecting the test fixture to the EEG recording device; detecting the presence or absence of a connector identification circuitry with respect to each of predefined groups of recording channels; determining if the connector identification circuitry is detected on all the groups of recording channels, wherein the detected identification circuitry comprises sequential, incrementing serial numbers corresponding to sequential groups of recording channels; verifying the connector identification circuitry as 'not working as intended', if the identification circuitry is not detected on all groups of recording channels, and comprises sequential, incrementing serial numbers; and verifying the connector identification circuitry as 'working as intended' if the identification circuitry is detected on all groups of recording channels, and comprises sequential, incrementing serial numbers.

[0037] Optionally, at least one identification circuitry has a polarity reverse of the polarity of the remaining identification circuitry. Optionally, the recording channels are grouped into 18 groups of inputs recording channels for each side of the recording device, wherein each group comprises 4 recording channels.

[0038] The aforementioned and other embodiments of the present shall be described in greater depth in the drawings and detailed description provided below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0039] These and other features and advantages of the present specification will be further appreciated, as they

become better understood by reference to the following detailed description when considered in connection with the accompanying drawings:

[0040] FIG. **1** shows a block diagram of a medical system comprising a large number of electrodes deployed on a patient body;

[0041] FIG. **2** illustrates an EEG system for detecting, diagnosing, or predicting neurological events from EEG signals, in accordance with some embodiments of the present specification;

[0042] FIG. **3**A is a perspective view of a multi-channel recording device, in accordance with an embodiment of the present specification;

[0043] FIG. **3**B is a side view of the multi-channel recording device of FIG. **3**A;

[0044] FIG. **4** is a block diagram illustrating a test fixture, coupled to an EEG recording device, used for testing a plurality of parameters of said device, in accordance with an embodiment of the present specification;

[0045] FIG. **5** is a circuit diagram illustrating a hardware test fixture, coupled with an EEG recording device, associated hardware test circuitry and computer, and associated software diagnostics, used for testing a plurality of parameters of said device, in accordance with an embodiment of the present specification;

[0046] FIG. **6** is a flowchart illustrating the steps of diagnostic testing of a EEG recording device performed by using the hardware test fixture, associated hardware test circuitry, and software diagnostics as shown in FIG. **5**;

[0047] FIG. **7** is a flowchart illustrating the steps of testing impedance with an EEG recording device by using a test fixture, in accordance with an embodiment of the present specification;

[0048] FIG. **8** is a flowchart illustrating the steps of testing channel uniqueness of an EEG recording device by using a test fixture, in accordance with an embodiment of the present specification;

[0049] FIG. **9** is a flowchart illustrating the steps of testing high side stimulator switches of a EEG recording device by using a hardware test fixture, associated hardware test circuitry, and software diagnostics such as that described in the present specification, in accordance with an embodiment;

[0050] FIG. **10** is a flowchart illustrating the steps of testing low side stimulator switches of a EEG recording device by using a hardware test fixture, associated hardware test circuitry, and software diagnostics such as that described in the present specification, in accordance with an embodiment;

[0051] and

[0052] FIG. **11** is a flowchart illustrating the steps of verifying connector IDs of an EEG recording device by using a test fixture, in accordance with an embodiment of the present specification.

DETAILED DESCRIPTION

[0053] The term 'user' is used interchangeably to refer to a surgeon, neuro-physician, neuro-surgeon, neuro-physiologist, technician or operator of the EEG system and/or other patient-care personnel or staff.

[0054] A "computing device" is at least one of a cellular phone, PDA, smart phone, tablet computing device, patient monitor, custom kiosk, or other computing device capable of executing programmatic instructions. It should further be appreciated that each device and monitoring system may have wireless and wired receivers and transmitters capable of sending and transmitting data. Each "computing device" may be coupled to at least one display, which displays information about the patient parameters and the functioning of the system, by means of a GUI. The GUI also presents various menus that allow users to configure settings according to their requirements. The system further comprises at least one processor (not shown) to control the operation of the entire system and its components. It should further be appreciated that the at least one processor is capable of processing programmatic instructions, has a memory capable of storing programmatic instructions, and employs software comprised of a plurality of programmatic instructions for performing the processes described herein. In one embodiment, the at least one processor is a computing device capable of receiving, executing, and transmitting a plurality of programmatic instructions stored on a volatile or non-volatile computer readable medium. In addition, the software comprised of a plurality of programmatic instructions for performing the processes described herein may be implemented by a computer processor capable of processing programmatic instructions and a memory capable of storing programmatic instructions.

[0055] "Electrode" refers to a conductor used to establish electrical contact with a nonmetallic part of a circuit. EEG electrodes are small metal discs or cylinders usually made of stainless steel, tin, gold, platinum or silver covered with a silver chloride coating. They are typically placed on the scalp or in the body on predetermined locations.

[0056] The "integrity verification system (IVS)" consists of a hardware test fixture, hardware test circuitry and software diagnostics used to verify baseline operation for running tests. The purpose of these is to establish a definitive known environment and test sequence which will allow detecting fault conditions prior to using the equipment on an actual patient.

[0057] The term "impedance test" shall mean methods for verifying the correct functionality of the electrode impedance measurement capability of the EEG recording device, as further described herein.

[0058] The term "channel uniqueness test" shall mean methods for verifying that each channel of the EEG recording device is displaying data for that channel only and with the expected physical to graphical mapping, as further described herein. This test also verifies the correct functionality of the patient connection switches for each EEG recording device channel, as further described herein.

[0059] The term "test for verifying a state of a switch" shall mean methods for verifying the correct functionality of each high and low side stimulator switch within the switch matrix of the EEG recording device, as further described herein.

[0060] The term "test for verifying connector IDs" shall mean methods for verifying the correct functionality of the detection and communication capability of the EEG recording device with identification circuitry within electrode connections, as further described herein.

[0061] The present specification is directed towards multiple embodiments. The following disclosure is provided in order to enable a person having ordinary skill in the art to practice the invention. Language used in this specification should not be interpreted as a general disavowal of any one specific embodiment or used to limit the claims beyond the meaning of the terms used therein. The general principles

defined herein may be applied to other embodiments and applications without departing from the spirit and scope of the invention. Also, the terminology and phraseology used is for the purpose of describing exemplary embodiments and should not be considered limiting. Thus, the present invention is to be accorded the widest scope encompassing numerous alternatives, modifications and equivalents consistent with the principles and features disclosed. For purpose of clarity, details relating to technical material that is known in the technical fields related to the invention have not been described in detail so as not to unnecessarily obscure the present invention.

[0062] In the description and claims of the application, each of the words "comprise" "include" and "have", and forms thereof, are not necessarily limited to members in a list with which the words may be associated. It should be noted herein that any feature or component described in association with a specific embodiment may be used and implemented with any other embodiment unless clearly indicated otherwise.

[0063] As used herein, the indefinite articles "a" and "an" mean "at least one" or "one or more" unless the context clearly dictates otherwise.

[0064] The present specification provides a hardware test fixture, associated hardware test circuitry, and software diagnostics that can be used with an EEG recording device, particularly for ECoG and sEEG monitoring and preferably with an integrated switch matrix, to test at least one functionality of the device before starting an EEG recording procedure.

[0065] FIG. **1** shows a block diagram of a conventional medical system **100** comprising a large number of electrodes positioned on the body of a patient **102**. The medical device **101** represents any conventional neuromonitoring medical system which comprises a large number of electrodes, such as an EEG (electroencephalography) system, which is used for monitoring the neurological state of a patient for diagnosis and preventive treatment of certain diseases and for monitoring patients during anesthesia, among other procedures. As shown in FIG. **1**, the medical device **101** is coupled to the patient **102** through a plurality of electrical leads **103** such that each of the leads **103** is coupled to an electrode (not shown) positioned at an appropriate location on the body of the patient. In applications that require a large number of electrodes to be coupled to the human body, the setup, placement and management of electrodes is a cumbersome process. As each electrode is positioned at a different location to capture the electrical activity in its vicinity, the input voltage recorded from each electrode has to be processed independently. Therefore, the system is required to maintain the identity of each of the electrical leads **103** and accordingly process the input received from it. After positioning any electrode at its required location on the body of the patient **102**, the user is required to correctly connect the electrode lead **103** corresponding to each electrode to a specific input channel designated for that electrode in the medical device **101**.

[0066] FIG. **2** illustrates an EEG system **210** for detecting, diagnosing, or predicting neurological events from EEG signals, in accordance with some embodiments of the present specification. The figure shows a plurality of EEG sensors or electrodes **205** spatially positioned on a layer of tissue, such as the scalp of a patient **215**, or intracranially on the surface of the brain as grid or strip electrodes or within the brain as depth electrodes. The plurality of electrodes **205** are connected to a multi-channel recording device **220** that is in data communication with a computing device **240**. In an embodiment, the computing device **240** comprises a cortical stimulator **250** which is connected to the recording device for use with functional mapping. The computing device **240** is in data communication with a display unit **230** and at least one database **235**.

[0067] In various embodiments, the plurality of electrodes **205** are small metal discs or cylinders typically made of stainless steel, tin, gold, platinum or silver covered with a silver chloride coating. In some embodiments, the plurality of electrodes **205** are placed on the scalp or in the body of patient **215**. In another embodiment, electrodes **205** are placed as intracranial electrodes as a combination of one or more depth electrodes, grid electrodes, and strip electrodes. The plurality of electrodes **205** sense electrical signals (EEG signals) on the patient's brain and the analog signals enter the multi-channel recording device **220** that amplifies the signals, converts the signals from analog to digital, and communicates the resultant digital EEG signal to the computing device **240** over a communication link. Stimulus from the cortical stimulator **250** is routed into selected electrodes on the patient **215** via the integrated switch matrix within the recording device **220**. In various embodiments, the cortical stimulator **250** is integrated within the recording device **220** or is an external device. In embodiments, the communication link between recording device **220** and computing device **240** may be a wired or wireless link.

[0068] The computing device **240** includes an input/output controller, at least one communications interface and system memory. The system memory includes at least one random access memory (RAM) and at least one read-only memory (ROM). These elements are in communication with a central processing unit (CPU) to enable operation of the computing device **240**. In various embodiments, the computing device **240** may be a conventional standalone computer or alternatively, the functions of the computing device **240** may be distributed across multiple computer systems and architectures. For example, in a distributed architecture the at least one database **235** and processing circuitry are housed in separate units or locations. Some units perform primary processing functions and contain at a minimum a general controller or a processing circuitry and a system memory.

[0069] The computing device **240** executes EEG software **245** to process, store, retrieve and display, on the display unit **230**, the patient's EEG data. In embodiments, the EEG software **245** processes the received signals, extracts parameters that characterize the EEG data, and generates a display of the data for a user. The processed EEG data is either displayed on the display unit **230** in real-time or stored in at least one database **235** for later analyses.

[0070] In some embodiments, execution of sequences of programmatic instructions enable or cause the CPU to perform various functions and processes. In alternate embodiments, hard-wired circuitry may be used in place of, or in combination with, software instructions for implementation of the processes of systems and methods described in this application. Thus, the systems and methods described are not limited to any specific combination of hardware and software.

[0071] FIGS. **3**A and **3**B show perspective and side views, respectively, of an exemplary multi-channel recording device **320**, in accordance with some embodiments of the

present specification. The multi-channel recording device **320** is configured for ECoG and sEEG monitoring. The recording device **320** has a plurality of electrode input channels or ports **325**. In some embodiments, the recording device **320** is configured to record up to 576 channels at an 8 kHz sampling rate. In some embodiments, the recording device **320** includes an onboard battery and data storage to allow for patient mobility. In embodiments, the recording device **320** is configured so that a user may select any input as ground on any recording device and select any other input as the recording reference. Further, a user may create montages up to, and including, all electrodes with a single click on an associated graphical user interface (GUI). In some embodiments, the recording device **320** is configured to streamline electrode layout with automated input mapping. In some embodiments, referring back to FIG. **2**, the EEG software **245** is configured to control integrated switch matrix stimulation. Additionally, in some embodiments, the software **245** allows a user to monitor multiple patients from one computer, control IP camera switching and functions, and simplify data review with trends and detection software. In some embodiments, all case settings, including montages, follow the patient record. In some embodiments, the software **245** includes a feature to automatically synchronize stimulus to response annotations.

[0072] Referring to FIGS. **2**, **3**A and **3**B, in an embodiment, each of the plurality of electrodes **205** (FIG. **2**) is grouped in a connector which has wired data communication with the corresponding input channel or port **325**. Each connector corresponding to a plurality of electrodes is programmed with a unique identifier. Thus, each connector and its plurality of electrodes can be uniquely identified and located according to its placement within the range of input channels or ports **325**. Consequently, each of the EEG signals acquired by the recording device **220** is uniquely identified with the associated electrode. The multi-channel recording device **320** of FIGS. **3**A and **3**B may be used in ECoG and sEEG systems to monitor, assess and map the brains of epilepsy patients who have may benefit from surgery and have not responded to less invasive treatments including pharmaceuticals.

[0073] An intracranial EEG procedure requires accurate information such as but not limited to electrode impedance values, and electrode contact viability from the EEG recording device being used. In embodiments where the EEG recording device includes an integrated switch matrix for an internal or external cortical stimulator, the respective ON/OFF states of the recording channel switches and stimulator switches must also be functional and correct to provide accurate EEG information to a physician. Further, for EEG data and stimulator routing, it is also imperative to ensure that the channel mapping from patient to a computer screen is accurate and that each channel is acting independently, before starting an EEG recording procedure.

[0074] The present specification provides an integrated verification system (IVS) which consists of a hardware test fixture, hardware test circuitry, and software diagnostics that can be used with an EEG recording device with integrated switch matrix to test the necessary functionality of the device before starting an EEG recording procedure. The IVS verifies a required functionality of the impedance measurement and electrode contact viability measurement within the EEG device. The IVS also verifies that each recording channel acts independently (channel uniqueness) and that the identification of unique identifiers in the electrode connections is functioning correctly. In embodiments, the IVS confirms that the recording channel and stimulator switches are functioning as expected. Hence, in various embodiments, the IVS ensures the EEG device is in working order before an EEG procedure begins.

[0075] FIG. **4** is a block diagram illustrating an integrated verification system (IVS) **400** in accordance with some embodiments of the present specification. The IVS **400** consists of a hardware test fixture, or hardware testing device, **402** coupled with an EEG recording device **404**, and its associated hardware test circuitry **405**, which in turn is coupled with a computing device **406** with software diagnostics **407**, for testing a plurality of parameters of said recording device, in accordance with an embodiment of the present specification. As shown, hardware test fixture **402** is coupled with the EEG recording device **404** for testing a plurality of pre-defined parameters of said device, which in turn is controlled by the computing device **406**. In an embodiment, the EEG recording device **404** comprises a plurality of electrodes that record electrical signals (EEG signals) from a patient's brain and communicate the signals to the computing device **406** over a communication link. The computing device **406** executes diagnostic EEG software to test a plurality of predefined EEG data parameters. In an embodiment, the hardware test fixture **402** comprises individual resistors corresponding to each electrode channel input of the EEG device, patient ground, and common reference. These resistors are connected at a common node on the fixture. Impedance measurement is implemented by injecting a known current through each channel input through the test fixture resistors to a common node. The current flows from that common node through a known resistance value to the recording device ground or midpoint voltage bias. The voltage produced over each resistor is sensed by the EEG recording device **404** and can be used to calculate the value of that resistor. The common node allows every channel input to be measured in the same way without changing configuration.

[0076] In embodiments, the recording device **404** can measure impedances from nominally 0 Ohm to some maximum value with some expected measurement error. The hardware test fixture **402** presents resistor values to each channel input that are less than the maximum measurable value. When the impedance measurement test is run, each measured channel resistance is verified to be within the expected measurement error of the resistor value for the corresponding test fixture input.

[0077] In an embodiment, the test fixture **402** further comprises a uniquely programmed identification circuit for each group of inputs on the EEG recording device **404**. An identification circuit simulates a number of different electrode connectors provided at a side of the recording device **404** at the same time. Each identification circuit in the test fixture **402** is programmed with a unique value, corresponding to a location of the connectors. In embodiments, at least one of these identification circuits has a reverse polarity. This requires the recording device **404** to communicate in reverse polarity mode with said identification circuit for verifying that the recording device **404** is functioning correctly and can communicate in either normal or reverse polarity. In order to verify that the detection and mapping of connectors on the EEG recording device **404** is functioning as required, communication is established between each of

the unique identification circuits and the corresponding groups of connectors and the different positions of each of the connectors is verified by the software diagnostics **407**.

[0078] Examples of the parameters that are tested/verified by the software diagnostics **407** comprise impedance measurement of EEG electrodes, channel uniqueness of each EEG channel, electrode contact viability detection, both recording channel and stimulator switch ON/OFF states, and correct identification of all connectors of the EEG electrodes.

[0079] In an embodiment, one hardware test fixture **402** is connected to the EEG recording device **404**, internal hardware test circuitry **405** is activated as needed, and software diagnostics are run to complete the parameter testing. Alternatively, if the EEG recording device's **404** electrode channel count requires more than one test fixture, in embodiments, more than one of the identical hardware test fixtures **402** may be connected to the EEG recording device **404**. In another embodiment, an external stimulator **408** is used to test the stimulator switch ON/OFF states. The external cortical stimulator **408** is used for functional mapping during a procedure. In various embodiments, either an internal constant voltage stimulator or an external cortical stimulator **408** is used to verify the switch functionality as a part of the IVS **400**. One advantage of using the external cortical stimulator **408** is that voltage and current compliance through the recording device and integrated switch matrix can be verified with the actual pulse parameters used for cortical stimulation. The diagnostic software **407** controls the hardware setup of the test hardware circuitry **405** and processes acquired data to verify test results.

[0080] FIG. **5** is a circuit diagram illustrating an IVS **500** which consists of a hardware test fixture **502** coupled with an EEG recording device **504** and associated hardware test circuitry and a computing device **506** with software diagnostics for testing a plurality of parameters of said recording device, in accordance with an embodiment of the present specification. As shown, hardware test fixture **502** is coupled with an EEG recording device **504** for testing a plurality of pre-defined parameters (for example, impedance measurement, channel uniqueness, switch functionality, and identification of unique identifiers in electrode connections) of said device, which in turn is controlled by a computing device **506**. In an embodiment, the EEG recording device **504** comprises a plurality of electrodes that record electrical signals (EEG signals) from a patient's brain and communicate the signals to the computing device **506** over a communication link. The computing device **506** executes diagnostic EEG software to test a plurality of predefined EEG data parameters. In the circuit diagram shown in FIG. **5**, the EEG recording device **504** comprises a constant voltage test circuit or stimulator **508**, a stimulator anode **510**, a stimulator cathode **512**, a plurality of stimulator high side switches **514**, a plurality of stimulator low side switches **516**, a ground connect **518** for the constant voltage test circuit **508**, EEG electrode channel connectors **520** and corresponding recording channel switches **522**. The EEG recording device **504** also comprises a plurality of connector identification pins **524** and external stimulator connector **526**. In embodiments, the stimulator anode **510** is used as a connection point for a test stimulator to connect to a selected stimulator switch connection. In embodiments, the stimulator cathode **512** is used as a return for the current produced by the test stimulator through the selected stimulation switch connection, i.e. one high side and one low side switch connected. In embodiments, the stimulator anode **510** and stimulator cathode **512** comprise separate entities to allow either the constant voltage test circuit **508** or the external cortical stimulator **527** to be used as the test stimulator. The high side switches **514** and low side switches **516** are used to route a test stimulus to a given pair of electrode connections. In various embodiments, only one of either the constant voltage test circuit **508** or external cortical stimulator **527** will be connected to the stimulator anode **510** and stimulator cathode **520** at one time. The constant voltage test circuit can be connected to the stimulator anode and cathode for testing the stimulator switch ON/OFF states. Alternatively, the constant voltage test circuit can be disconnected from the stimulator anode and cathode and the external stimulator can be connected for testing the stimulator switch ON/OFF states.

[0081] In an embodiment, the test fixture **502** comprises individual resistors **530** corresponding to each electrode channel input of the EEG device, patient ground, and common reference. The resistors **530** are arranged in groups (banks) for connecting with EEG device channel inputs and are connected at a common node on the fixture **502**. The fixture **502** also comprises a plurality of uniquely programmed identification circuits **532** for connecting with the EEG device connector identification pins.

[0082] FIG. **6** is a flowchart illustrating the steps of diagnostic testing of an EEG recording device performed by using the test fixture shown in FIG. **5**. At step **602** an impedance test for determining if each input recording channel of the EEG recording device measures at a predefined impedance is conducted. FIG. **7** is a flowchart illustrating the steps of testing impedance with an EEG recording device by using a test fixture, in accordance with an embodiment of the present specification. At step **702**, a test fixture is connected to the EEG recording device. An internal hardware test circuit is activated to measure impedance for each input recording channel of the EEG recording device at step **704**. At step **706** it is determined if all impedance values match expected impedance values for each input while allowing for a measurement error margin of +/−30% of the expected impedance value. In some embodiments, the expected impedance value ranges from 499 Ohms to 49.9 kOhms. If all impedance values do not match expected impedance values for each input in a range of +/−30% of the expected impedance value, the impedance circuitry is verified as not working as intended at step **708**. If all impedance values do match expected impedance values for each input in a range of +/−30% of the expected impedance value, the impedance circuitry is verified as working at step **710**.

[0083] In an embodiment, the test fixture applies a sequence of resistance values within a range of 499 ohms to 49.9K ohms, one for each EEG channel input, patient ground, and common reference. Since the EEG recording device is physically arranged in banks of n channels, the resistors in the test fixture sequentially increase through n+1 unique values so that each adjacent bank of EEG recording channels has a unique set of resistor values. This reduces the likelihood of error when correlating test results with each bank of EEG recording channels. In an embodiment, for an EEG recording device comprising 8 EEG recording channels, each bank of channels has a unique sequence of values. For example, with reference to FIG. **5**, bank 1 of hardware

test fixture **502** may be associated with value 1, value 2, . . . value 8. Bank 2 may be associated with value 9, value 1, . . . value 7 etc. Each bank (such as the banks of hardware test fixture **502**) corresponds to an individual ADC IC. When the software parses out data from an individual ADC IC, the sequence of values are unique when compared to any other ADC in the group. This makes it easier to differentiate between the data from two separate ADCs. In embodiments, the resistor values are spaced far enough to allow for expected error in impedance measurement. In some embodiments, the span between resistor values exceeds the expected measurement error margin of the impedance measurements. For example, in an embodiment, an expected measurement error margin is +/−30% and the impedance value of the resistors are spaced+/−40% apart from each other so that the spacing of the resistor values exceeds the measurement error margin.

[0084] In various embodiments, any shorted channels within a bank of a hardware test fixture are detectable when testing the impedance of each channel. For example, in some embodiments, if a channel 1 of a bank 1 of a test fixture has a low resistance value and a channel 2 of the bank 1 has a high resistance value and these 2 channels are shorted together, the short may not be detected when measuring channel 1 impedance as the low resistance in parallel with high resistance may be within the expected tolerance of the low resistance value. However, when channel 2 impedance is measured, the parallel resistance will be well out of tolerance from the expected high resistance value and a short will be detected. Since, all resistor values used on the test fixture fall within the measurement range of the recording device, a failed open input will also be detected. A diagnostic software running on a computing device coupled with the test fixture and the EEG recording device verifies expected impedance on each EEG recording channel.

[0085] Referring back to FIG. **6**, at step **604** a channel uniqueness test is performed for each EEG recording channel. FIG. **8** is a flowchart illustrating the steps of testing channel uniqueness of an EEG recording device by using a test fixture, in accordance with an embodiment of the present specification. At step **802** a text fixture is connected to the EEG recording device. A plurality of resistors of the text fixture is connected to a plurality of EEG electrode recording channels. All recording channel switches are connected at step **804**. At step **806**, it is determined if a status of "electrode connected" is reported for each recording channel. If a status of "electrode connected" is not reported for each recording channel, channel uniqueness, recording channel switches, or electrode contact viability is verified as not working as intended at step **808**. If a status of "electrode connected" is reported for each recording channel, one recording channel is disconnected at step **810**. The EEG electrode recording channel is disconnected from the plurality of resistors of the text fixture. Then, at step **812**, it is determined if a status of "electrode disconnected" is reported for the disconnected channel. If a status of "electrode disconnected" is not reported for the disconnected channel, channel uniqueness, recording channel switches, or electrode contact viability is verified as not working as intended at step **814**. If a status of "electrode disconnected" is reported for the disconnected channel, an open switch is verified as open, the channel is unique, and contact viability is verified as working as intended at step **816**. At step **818**, a diagnostic software running on a computing device coupled with the test fixture and the EEG recording device cycles through all of the recording channels to verify the functionality of said channels.

[0086] In some embodiments, the channel uniqueness test combines a functional test of the recording channel switch ON/OFF states with a functional test of the electrode contact viability measurement. The test verifies 3 functions: 1) the recording channel switch "closed" and "open" functionality; 2) whether the "lead-off" function is working for that channel; and, 3) when an "electrode-disconnected" state is detected for that specific channel it is confirmed that the channel with the "electrode-disconnected" state matches the channel where the recording channel switch is opened, verifying channel uniqueness. The "lead-off" detection will flag an "electrode-disconnected" state if the resistance on the input is above a predefined minimum resistance from device ground. This minimum "electrode-disconnected" resistance value is above any resistor value used on the test fixture. This ensures that an "electrode-disconnected" state will not be detected if the recording channel is connected to the test fixture. The resistor values in the hardware test fixture are chosen to be below the minimum value of resistance required to generate an "electrode disconnected" state from the electrode contact viability measurement. This guarantees every channel connected to its corresponding test fixture resistor will produce an "electrode connected" state. For this test, the recording channel switches are opened one at a time with the test fixture connected. The diagnostic software confirms an "electrode disconnected" state on the EEG recording channel having an open switch. All other EEG recording channels having closed switches convey an "electrode connected" state. This test is repeated for each individual EEG recording channels. By verifying that the selected channel for an open switch matches the channel with an "electrode disconnected" state, channel uniqueness is confirmed. This test also verifies that the recording channel switches and electrode contact viability measurement are functioning as expected.

[0087] Referring back to FIG. **6**, at step **606** high side stimulator switches of the EEG recording device are tested by connecting said switches with the test fixture. FIG. **9** is a flowchart illustrating the steps of testing high side stimulator switches of an EEG recording device by using the test fixture, in accordance with an embodiment of the present specification. In an embodiment, at step **902**, the high-side stimulator switches are tested by connecting one high-side switch at a time with a resistor of the test fixture. At step **904** all EEG recording channel switches are connected with test fixture resistors. Next, in one embodiment, at step **906** an internal hardware test circuitry within the recording device is activated to inject a constant voltage stimulus into the connected stimulator switch channel. At step **908** the voltage on all the EEG recording channels is measured. At step **910** it is determined if the voltage on the connected high-side stimulator switch channel is equal to the constant voltage stimulus. At step **912** if the voltage on the connected high-side stimulator switch channel is equal to the constant voltage stimulus, the high-side stimulator switch is verified as working as intended (connected). At step **914** it is determined if the voltage on all EEG recording channels is equal to a predefined fraction of the constant voltage stimulus. In some embodiments, a constant voltage pulse generator produces a low voltage pulse in the mV range. If a channel with a high side switch measures this voltage

value+/−some expected error, the high side switch for that channel is considered to be working. In embodiments, the other channels will be at a fraction of that voltage, 1/10 for example. If all other channels measure 1/10 of the pulse voltage value+/−some expected error, the high side switches for these channels will be considered to be working. This predefined fraction depends on the value of a resistance divider being applied to the signal in the channel being tested. At step **916** if the voltage on all other recording channels is equal to a predefined fraction of the constant voltage stimulus, the high-side stimulator switches not connected with any of the fixture resistor, are verified as working as intended (open). If the conditions of step **910** and **914** are not met, the corresponding high-side stimulator switches are verified as not working as intended, at steps **920** and **922** respectively. At step **918** a diagnostic software running on a computing device coupled with the test fixture and the EEG recording device cycles through all high-side stimulator switches to verify a required functionality.

[0088] Referring back to FIG. **6**, at step **608** low side stimulator switches of the EEG recording device are tested by connecting with the test fixture. FIG. **10** is a flowchart illustrating the steps of testing low side stimulator switches of an EEG recording device by using the test fixture, in accordance with an embodiment of the present specification. At step **1002**, one high-side stimulator switch and one low-side stimulator switch are connected at a time with a resistor of the test fixture. At step **1004**, all EEG recording channel switches are connected with a resistor of the test fixture. At step **1006**, an internal hardware test circuitry is activated to inject a constant voltage stimulus into the connected high-side stimulator channel. At step **1008** the voltage on all the connected EEG recording channels is measured. In embodiments, during testing, a test stimulator current travels from the high side switch connection/channel input through one fixture resistor to a common node in the fixture, through a second fixture resistor to the channel input with the low side switch connection, and to ground. At step **1010** it is determined if the voltage on the connected high-side stimulator channel is equal to the constant voltage stimulus. At step **1012** if the voltage on the connected high-side stimulator channel is equal to the constant voltage stimulus, the high-side stimulator switch is verified as working as intended (connected). At step **1014** it is determined if the voltage on the connected low-side stimulator channel is at a ground potential. At step **1016** if the voltage on the connected low-side stimulator channel is at a ground potential, the low-side stimulator switch is verified as working as intended (connected). At step **1018** it is determined if the voltage on all EEG recording channels is equal to a predefined fraction of the constant voltage stimulus. In some embodiments, the predefined fraction is at least 1/10. At step **1020** if the voltage on all other recording channels is equal to a predefined fraction of the constant voltage stimulus, the high-side and low side stimulator switches not connected with any of the fixture resistor, are verified as working as intended (open). If the conditions of step **1010**, **1014** and **1018** are not met, the corresponding high and/or low-side stimulator switches are verified as not working as intended, at steps **1022**, **1024** and **1026** respectively. At step **1028** a diagnostic software running on a computing device coupled with the test fixture and the EEG recording device cycles through all low-side stimulator switches to verify a required functionality.

[0089] In an embodiment, the working states of the stimulator switches may be tested by firing a constant current pulse instead of a constant voltage pulse. This constant current pulse can be generated by the internal hardware test circuitry or by an external stimulator which is connected to the Stimulator Anode and Stimulator Cathode connections of the test fixture. Voltage measurement from EEG recording channels and the diagnostic software are used to determine if the said switches are functioning as expected.

[0090] Referring back to FIG. **6**, at step **610** connector identification of the connectors connecting the EEG electrodes to respective EEG recording channels are tested by using the hardware test fixture. FIG. **11** is a flowchart illustrating the steps of verifying connector IDs of an EEG recording device by using a test fixture, in accordance with an embodiment of the present specification. At step **1102** a test fixture is connected to the EEG recording device. For each group of inputs, the recording device detects the presence or absence of identification circuitry at step **1104**. In various embodiments, the identification circuitry is a part of the test fixture and is identical to identification circuitry that would be in an actual electrode connector. The test process verifies that the identification detection and communication functionality of the EEG recording devices is working on all connection ports. Polarity detection is a part of the capability of this function as the electrode connectors could be oriented in different directions on the EEG recording device connection ports. Identification circuitry is described with reference to FIG. **5**. At step **1106**, it is determined if identification circuitry is detected on all groups of inputs with sequential, incrementing serial numbers with the last group of inputs detected in reverse polarity. If identification circuitry is not detected on all groups of inputs with sequential, incrementing serial numbers with the last group of inputs detected in reverse polarity, the connector identification circuitry is verified as not working as intended at step **1108**. If identification circuitry is detected on all groups of inputs with sequential, incrementing serial numbers with the last group of inputs detected in reverse polarity, the connector identification circuitry is verified as working as intended at step **1110**. In embodiments, the test fixture comprises identification circuitry equivalent to that used in actual patient electrode connectors. Each group of adjacent EEG recording channels has its own unique value programmed into the test fixture identification circuitry. In various embodiments, a predefined number of groups of adjacent EEG recording channels are provided for each recording device and at least one ID group is provided per predefined number of channels. For example, in an embodiment, there are 18 groups of inputs recording channels for each side of the recording device, wherein each group has 4 recording channels. At least one of the identification circuits on the test fixture is reverse polarized, as described above, to exercise reversible connection identification in the recording device. The test fixture is connected to the recording device and all connectors are scanned. The diagnostic software verifies expected values for all recording device ID connections and correct addressing of acquired ID values. In embodiments, the test fixture can only be applied to the EEG recording device in one position or orientation, meaning a unique serial number programmed into each ID circuitry block must correspond with the expected serial number for that location. If all the serial numbers are correct, correct addressing is verified.

[0091] The above examples are merely illustrative of the many applications of the system and method of present specification. Although only a few embodiments of the present specification have been described herein, it should be understood that the present specification might be embodied in many other specific forms without departing from the spirit or scope of the specification. Therefore, the present examples and embodiments are to be considered as illustrative and not restrictive, and the specification may be modified within the scope of the appended claims.

We claim:

1. A method of performing a diagnostic test on an electroencephalography (EEG) recording device, wherein the EEG recording device comprises 1) at least one stimulator coupled with a plurality of EEG electrode recording channels and 2) recording channel connectors connecting one or more EEG electrodes to the plurality of EEG electrode recording channels and wherein the diagnostic test is performed by a hardware testing device comprising a plurality of resistors coupled with one or more of the plurality of EEG electrode recording channels and corresponding recording channel connectors, the method comprising:

performing an impedance test for determining if each EEG recording channel of the plurality of EEG electrode recording channels has a predefined impedance;

performing a channel uniqueness test for each EEG recording channel of the plurality of EEG electrode recording channels;

performing a test for verifying a state of a switch of the at least one stimulator of the EEG recording device; and

performing a test for verifying correct functionality of connector identification detection and communication for electrode connections.

2. The method of claim 1, wherein the at least one stimulator comprises hardware test circuitry comprising a constant voltage test stimulator.

3. The method of claim 2, wherein the constant voltage test stimulator comprises a stimulator anode to connect to the stimulator high side switches, a stimulator cathode to connect to the stimulator low side switches, and a ground connect for the constant voltage test stimulator.

4. The method of claim 3, wherein performing a test for verifying the state of a switch of the stimulator of the EEG recording device comprises performing a test for verifying a state of the high side stimulator switches.

5. The method of claim 3, wherein performing a test for verifying the state of a switch of the stimulator of the EEG recording device comprises performing a test for verifying a state of the low side stimulator switches.

6. The method of claim 4, wherein performing a test for verifying the state of the high side stimulator switches comprises:

connecting one of the high side simulator switches with one of the plurality of resistors of the hardware testing device;

connecting the plurality of EEG electrode recording channels with the plurality of resistors of the hardware testing device;

injecting a stimulus into the one of the high side simulator switches, wherein the stimulus is defined by a voltage or current level;

measuring a voltage on the plurality of EEG electrode recording channels;

verifying that the one of the high-side stimulator switches is connected with at least one of the plurality of resistors if the measured voltage is equal to the expected stimulus level; and

verifying that the one of the high-side stimulator switches is not connected with any of the plurality of resistors, if the measured voltage is equal to a predefined fraction of the stimulus voltage.

7. The method of claim 6, wherein injecting the stimulus comprises injecting a constant-voltage stimulus.

8. The method of claim 6, wherein injecting a stimulus comprises injecting a constant-current stimulus.

9. The method of claim 5, wherein performing a test for verifying the state of the low side stimulator switches comprises:

connecting one of the high-side stimulator switches to one of the plurality of resistors and one of the low-side stimulator switches to one of the plurality of resistors;

connecting the plurality of EEG electrode recording channels with the plurality of resistors;

injecting a stimulus into the one of the high-side stimulator switches;

measuring a voltage on at least one of the plurality of EEG electrode recording channels; and

verifying that the one of the low-side stimulator switches is working if the measured voltage is at a ground potential.

10. The method of claim 9, wherein injecting the stimulus comprises injecting a constant-voltage stimulus.

11. The method of claim 9, wherein injecting a stimulus comprises injecting a constant-current stimulus.

12. The method of claim 1, wherein the at least one stimulator comprises a stimulator external to the EEG recording device.

13. The method of claim 1, wherein performing the channel uniqueness test for each of the plurality of EEG electrode recording channels includes performing a lead-off functionality test.

14. The method of claim 1, wherein performing the channel uniqueness test comprises:

connecting the hardware testing device to the EEG recording device;

connecting the plurality of resistors of the hardware testing device to the plurality of EEG electrode recording channels;

determining if an electrode connected status is reported for each of the plurality of EEG electrode recording channels; and

determining one or more of: a recording channel uniqueness, a recording channel component, or an electrode contact viability as not working as intended if an electrode connected status is not reported for each of the plurality of EEG electrode recording channels.

15. The method of claim 14, wherein performing the channel uniqueness test further comprises:

disconnecting one of the plurality of EEG electrode recording channels from one or more of the plurality of resistors of the hardware testing device; and

determining if an electrode disconnected status is reported for the disconnected one of the plurality of EEG electrode recording channels.

16. The method of claim 15, wherein performing the channel uniqueness test further comprises:

verifying one or more of a recording channel uniqueness, a recording channel component, or an electrode contact viability as not working as intended if an electrode disconnected status is not reported for the disconnected one of the plurality of EEG electrode recording channels; and

determining a working status of the one of the plurality of EEG electrode recording channels if an electrode disconnected status is reported for the disconnected one of the plurality of EEG electrode recording channels.

17. The method of claim **1**, further comprising cycling through the plurality of EEG electrode recording channels using a diagnostic software running on a computing device coupled with the hardware testing device and the EEG recording device to verify a required functionality.

18. The method of claim **1**, wherein performing a test for verifying a state of a switch of the at least one stimulator comprises verifying a state of device switches and integrated stimulation switch matrix switches.

19. The method of claim **1**, wherein performing the impedance test comprises:

connecting the hardware testing device to the EEG recording device;

activating a mode within the EEG recording device to measure an impedance for each of the plurality of EEG electrode recording channels;

determining if measured impedance values match expected impedance values within a predetermined margin of error;

determining that the one or more of the plurality of EEG electrode recording channels are not working as intended if the measured impedance values do not match the expected impedance values within the predetermined margin of error; and

verifying that the one or more of the plurality of EEG electrode recording channels are working as intended if the measured impedance values match the expected impedance values within the predetermined margin of error.

20. The method of claim **19**, wherein the predetermined margin of error is +/−30% of the expected impedance value.

21. The method of claim **1**, wherein performing the test for verifying correct functionality of connector identification detection and communication for electrode connections comprises:

connecting the hardware testing device to the EEG recording device;

detecting a presence or absence of a connector identification circuitry with respect to predefined groups of the plurality of EEG electrode recording channels;

determining if the connector identification circuitry is detected on the groups of the plurality of EEG electrode recording channels, wherein the detected connector identification circuitry comprises sequential, incrementing serial numbers corresponding to sequential groups of recording channels;

determining the connector identification circuitry as not working as intended if the connector identification circuitry is not detected on the plurality of EEG electrode recording channels and comprises sequential, incrementing serial numbers; and

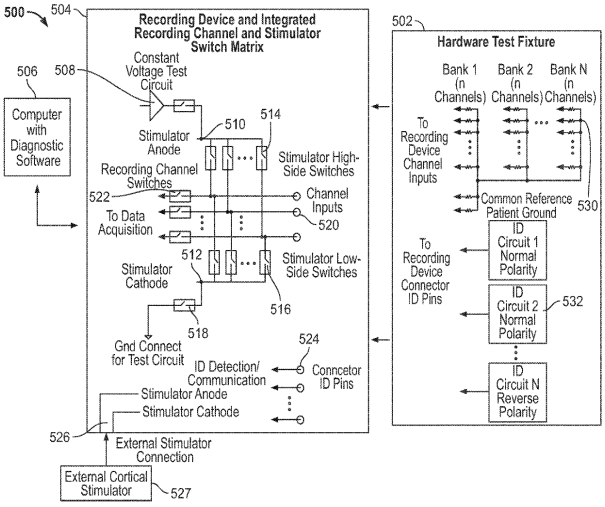
verifying the connector identification circuitry as working as intended if the connector identification circuitry is detected on the plurality of EEG electrode recording channels and comprises sequential, incrementing serial numbers.

22. The method of claim **21**, wherein at least one of the connector identification circuitries has a polarity that is a reverse of a polarity of the other connector identification circuitries.

23. The method of claim **21**, wherein the plurality of EEG electrode recording channels is grouped into predefined groups of inputs for each side of the EEG recording device, wherein each of the predefined groups comprises 4 recording channels.

* * * * *

专利名称(译)	用于测试高通道数神经监控记录设备的完整性验证系统		
公开(公告)号	US20200146581A1	公开(公告)日	2020-05-14
申请号	US16/678482	申请日	2019-11-08
[标]申请(专利权)人(译)	卡德韦尔LAB		
申请(专利权)人(译)	卡德韦尔实验室，INC.		
当前申请(专利权)人(译)	卡德韦尔实验室，INC.		
[标]发明人	VILLARREAL RICHARD A CADWELL JOHN A		
发明人	RHODES, ETHAN VILLARREAL, RICHARD A. CADWELL, JOHN A. REHFELDT, ROSE		
IPC分类号	A61B5/0478 A61B5/00 G01R31/28		
CPC分类号	A61B5/7221 G01R31/2829 A61B5/0478 G01R31/2812		
优先权	62/758320 2018-11-09 US		
外部链接	Espacenet USPTO		

摘要(译)

在包括至少一个刺激器和多个EEG电极记录通道以及相应的记录通道连接器的脑电图（EEG）记录设备上执行诊断测试的方法由测试夹具执行，该测试夹具包括与一个或多个EEG耦合的多个电阻器 电极记录通道和相应的记录通道连接器。 该方法包括执行阻抗测试以确定该EEG记录设备的每个EEG记录通道是否具有预定义的阻抗；对每个EEG记录通道执行一个通道唯一性测试；执行一个测试以验证该刺激器的刺激器的开关状态。 EEG记录设备，并执行测试以验证将EEG电极连接到各个EEG记录通道的记录通道连接器的连接器ID。