

(19) (KR)
(12) (A)

(51) 。 Int. Cl.⁷ (11) 10-2004-0075718
G09G 3/30 (43) 2004 08 30

(21) 10-2004-0007150
(22) 2004 02 04

(30) JP-P-2003-00044369 2003 02 21 (JP)

(71) 가 가 2 4-1

(72) 가 3-3-5 가 가

(74)

:

(54) , ,

(3) (2) (P)가 (P) (C), (INV), OLED
(70) 1 3 (TR1 TR3) , (C)
(INV) , 2 (C)
(VDDM) (TR2) (VSSM) .

2

, , , ,

1 1 .
2 (AA) (P) .

3		(P)	가	.
4	3	가		.
5	(P)		,	
6		(P)	가	.
7	6	가		.
8	2			.
9		(AA)	(P')	.
10		(P')	가	.
11	10	가		.
12	(P')			.
13		(P')	가	.
14	13	가		.
15				.
16				.
17				.

< >

2 :

3 :

70 : OLED ()

100 :

200 :

300 : ()

400 : ()

P, P' :

C :

VDDM :

VSSM :

VDD : 1

VHH : 2

VSS : 1
VLL : 2
INV : ()
SW1 SW4 : (1 4)
TR1 TR6 : 1 6
AA :

, , .
 , 가 .
 , SRAM(Static Random Access Memory) , (1).
 17 , (LC), (Tr1 Tr3), (Tr4 Tr5) , (LC) 1 가
 , Tr2 Tr3 , Tr2: (LC) , Tr3: → Tr2: , Tr3: → Tr2: , Tr3: (off)
 , (LC) , Tr2 , Tr3 .
 , 가 가 , (3)
(1)
2002-207453 (22, 24)

, (, OLED)
 , 가 , 가 가 , 가 , OLED 가
 OLED 2 가

2 3 가 3 , 1 2
2 3 , 3
3
1 2 2 3 3 가 ,
2 2
4 1 1
1 4
1 2 1 2
1 1 2
1 2
가
2 가
가
()
<1. 1 >
<1-1 : >
OLED
1 1 (AA), (300), (400),
(500)
(AA) (A), (100),
(200)가
(A)
(Thin Film Transistor : , 'TFT')
(A) , 1 (2) X
(3) , Y (2) (3)
(P)가 (P) (P) OLED
(70)
(400) (AA) (300)
1 (FLD1) 2 (FLD2) 1 (P)
X (SPX) (active) 1
X (CKX) (D)
Y (SPY)
(YCK) 2 Y

(300) 1 (VDD), 2 (VHH), 1 (VSS), 2 (VLL)
 (VDD) 2 (VHH) (VDDM) 1
 (VSS) 2 (VLL) (VSSM) 2 (VLL) (VSSM) (VSS)
 (VSSM) 1 (VDD) (VDDM) (VSSM) (P) (300)
 (AA) (VCOM) (300) (100),
 (200), (400), (500)
 (100) (WRT) , Y (YCK) Y (YCK) (P) (Dout) 가
 X (200) (SPX) X (CKX) 1 2 (D) (D) (L P)
 , 1 2 (Dout)

<1-2 : >

2 1 (TR2), 3 (TR3), (INV), (C) OLED (P) 1 (TR1), 2 (INV)
 , 4 (TR4) 5 (TR5)
 TFT
 1 (TR1) (3) (2) (WRT)가 (Dout)
 (C) (3) 가 1 (TR1) (C) (C)
 가 2 (L2)
 2 (TR2) (C) (INV) 가 (C)
 (INV) (L2) 2 (C)
 FLD2)가 (C) 3 (TR3) (C) (INV) 1
 가 (L1) 1 (FLD1)가 2 (TR2) 3 (TR3) O
 (C) (INV) 가 , OLED (70) (VDDM) (VSSM) (I
 LED (70) (L3 L4)
 NV) ,
 OLED (70) 가 ,

<1-3 : (AA) >

(AA)
 (3) (Dout) (P) (Dout) (P)
 (Dout) (P)

<1-3-1 : >

(P) (3) 가
 (WRT) 1 (TR1)

3, 2 (TR2), (SW3) (P) 3 가 (SW2 (C))
) , OLED (70) 4 (TR3) 3 가 (T1) (T2)
) , (T1) (T2) (T1) (T2) (前者)
 , (T1) (T1A) 1 (FLD1) 2 (FLD2)가 ()
 , (INV) (C)) 가 (INV) (OLED (70)) (SW2)
 가 , (T1B) 2 (FLD2) 가 1 (FLD1)가 (
) , (SW3)가 (C)) (INV) (OLED
 (70)) (INV) 가
 , (T1C) 1 (FLD1) 2 (FLD2)가 , (T1D) 1
 ((FLD1) (C)) 가 (INV) (OLED (70)) (FLD2)가 (INV) (SW2)가
 ((FLD1) (C)) 가 (INV) (FLD2)가 (INV)
 , (T1E) 1 (FLD1) 2 (FLD2)가 , (T1F) 2 (FLD
 2) (C)) (INV) (OLED (70)) (FLD1)가 , (SW3)가
 가 (C)) (INV) (T1B) (T1F) 2 ,
 (T1) 가 , (T1) (P) (INV)
 , (T1G) , 1 (FLD1) 2 (FLD2)가 ,
 ((C)) (INV) (OLED (70))
 (T1) , (P) (P)
 , (SW2)가 , (SW3)가 1 , (SW2)가
 (SW3)가 2 1 1 1 1 ,
 , 1 1 1 1 1 ,
 , (SW2) (SW3) 3 , 1 2
 , 3 (INV) , (SW2) (SW3)가
 , (T2) , 1 (FLD1)가 , 2 (FLD2)가 (INV)
) () , (SW2)가 , (T1) (T1)
 , (T2) , (OLED (70)) (極) 1 (T1)
 가 , 2 (T1) (T2) , (T1)
 가 ,

(VDDM) 2 (VHH) (VDDM) (VSSM) 2 (VLL) (T1) (T2)
 (VDDM) 1 (VDD) (VSSM) 1 (VSS) (INV) 4
 (T1) 5 (TR4 TR5) (INV) 5

5 (P) (C) 2 3 (TR2 TR3) 'STG' 2
) 'PXL' (INV) (,
 (C) Ch1, (INV) Cin 가 (T1)
 (VDDM) 1 (VDD) (VSSM) 1 (VSS) (STG)가
 , STG=VDD (T1) (C) (Q)
 $Q = Ch1 \cdot VDD$

(T1) (T2) 2 (TR2)가
 (C) (Cin) (C) 가 (Cin)
 (INV) (V) $V = Ch1 \cdot VDD / (Ch1 + Cin)$ (INV) (V)
 1 (VDD) (TR4) 4 (TR4) ,
 4 (TR4) 가

(T1) (VDDM) 2 (VHH) (C) (Q)
 $Q = Ch1 \cdot VHH$ (T1) (T2) (C) (Cin)
) (INV) (V) $V = Ch1 \cdot VHH / (Ch1 + Cin)$
 2 (VHH) 1 (VDD) (T1) (INV)
 (V) 4 (TR4)

4 (TR4) Vth4 (TR4)
 $|V_{th4}| > |Ch1 \cdot VHH / (Ch1 + Cin) - VDD|$ (TR4) -
 (Vth4) (TR4)
 5 (TR5) Vth5 (TR5) , |V
 $th5| > |Ch1 \cdot VLL / (Ch1 + Cin) - VSS|$ (TR5) -
 (Vth5) 5 (TR5)
 5 (T2) (STG)(V))가 1 (VDD)
 4 (TR4)

<1-3-2 : >

가 (WRT) 1 (P) (3)
 (TR1)
 6 2 (P) 가 (SW1)
) 1 (TR1) 7 6 가
 (T3) (Dout)가 (P) (P)
 가 (2) (3) 가
 (T3) (WRT)가 (SW1)(1 (TR1))가

(3) (Dout)가 (P) , (Dout)
 (INV) (t1) (Dout)
 (1) 1 (VSS) 1 (V
 DD)

<2. 2 >

2 (P') , (400) (V
 VOFF) , 1 1 가 .

8 2 (AA) 1 (P') , 9 2 (P') (INV) OLED (70)
 6 (TR6) , 2 1 (P) 가 .

10 , 9 (P') 가 , (S
 W4) 6 (TR6) .

(FLD1) (AA) 2 (FLD2) , (VDDM) 11 , (VSSM) 1

11 4 , (VOFF)가 (T1C) (T1)
 () , (SW4)가 (INV) 가

1 , (T1B) (SW3)가 , (INV)가
 , (INV) , (T1D) (SW2)가
 (T1D) , (T1) , 1 : (:) 가 : (:)
 , 가 , (T1D) 가
 (T1) , (INV)

2 (T1D) (T1) , (SW4)
 (INV)

1 , (VOFF) (T1D) (SW4)
 (T1C) (VOFF)

12 (P') , 2 1 가 (V
 DDM) (INV) , (VDDM) (VSSM) (VSSM) (VLL) , (T1) , (T2) ,
 (VDDM) 1 (VDD) , (VSSM) 2 (VSS) , (TR4) 5 (TR5)
 (T1) (INV) (V)

4 (TR4) (Vth4) 1 (VDD) 2 (VHH) , 1
 가 $|V_{th4}| > |Ch1 \cdot V_{HH} / (Ch1 + C_{in}) - V_{DD}|$, 5 (TR5) (Vth5) 1 (VSS) 2 (VLL) , 1 가 $|V_{th5}| > |Ch1 \cdot V_{LL} / (Ch1 + C_{in}) - V_{SS}|$

가 , (WRT) 1 (P') (3)
 (TR1)

13 , 9 (P') 가 , (SW1)
 1 (TR1) , (SW4) 6 (TR6)

14 13 가 , (T3) ,
 (Dout)가 (P') . , ,
 가 , ,
 (2) (3) ,

(T3) , (WRT)가 , (VOFF)가 , 1 (FLD1)가
 2 (FLD2)가 , (SW1)가 , (SW3)가 ,
 (SW2)가 , (SW4)가 , 13 가

14 (T3) (t1) , (Dout)가 ,
 (INV) , (P') OLED (70)가 ,

<3. >

<3-1 : >

, (AA) , 15
 (1206) , (1200) (1202) (1204) ,

<3-2-2 : >

, (AA) (1300) (1302) 16 (AA) .

, 15 16 , , , , , POS ,

(57)

1.

3

2.

1

2

3

4

3.

4.

3

1

2

3

2

가

가

(off)

3

가

3

가 (on)

1

2

1

2

3

2

2

1

3

1

1

1

2

5.

4

2

3

가

3

1

2

2

3

3

6.

4 5 , 4 , 1 4 , 1 가 1 .

7.

3 , 1 2 , 1 1 2 1 .

8.

3 , P N , 1 3 .

9.

3 , , .

10.

3 , , , , , , , , , .

11.

10 , 1 , 2 3 , 2 가 3 , 가 3 , 1 , 2 , 2 가 가 , 2 3 , 가 3 , 1 , 1 , 1 , 1 , 1 , 2 .

2 3

12.

11 ,
2 3 가 3 ,
1 2 3 , 3
2 3 .

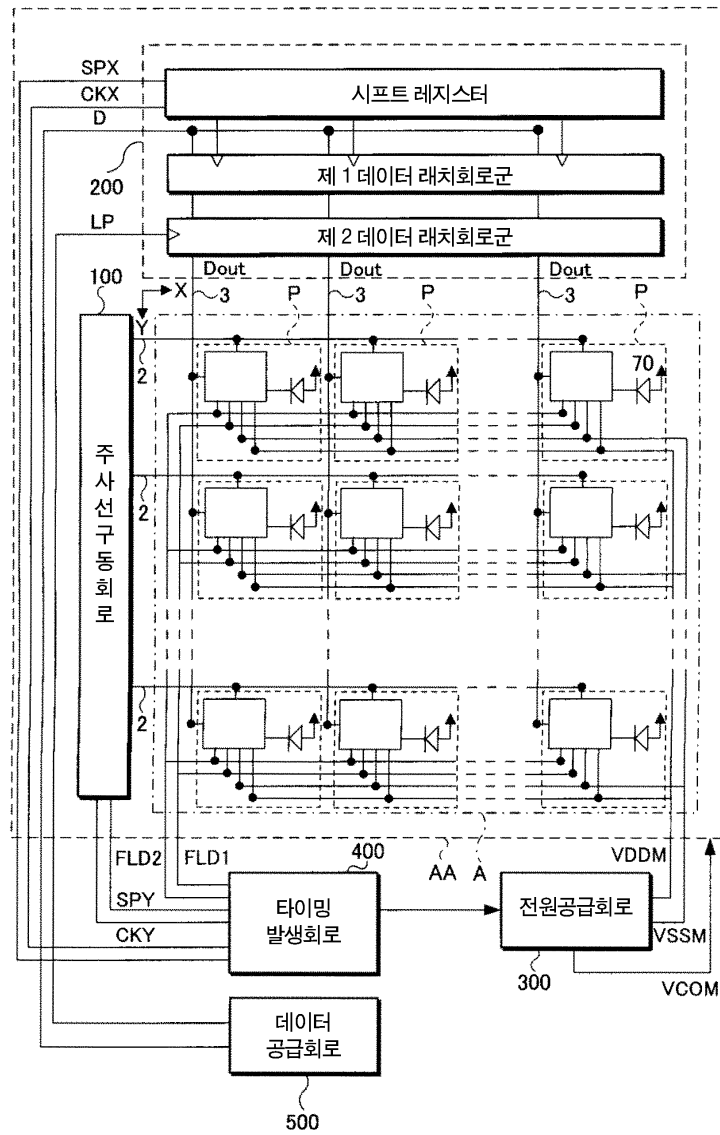
13.

11 12 ,
4
,
1 1 가 1
4

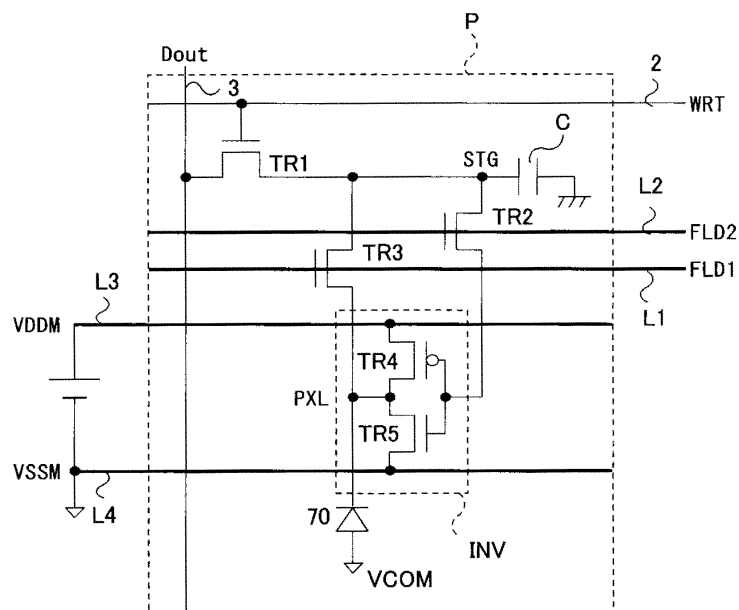
14.

11 ,
,
1 1
,
, 1 2
1 2 1 2
.

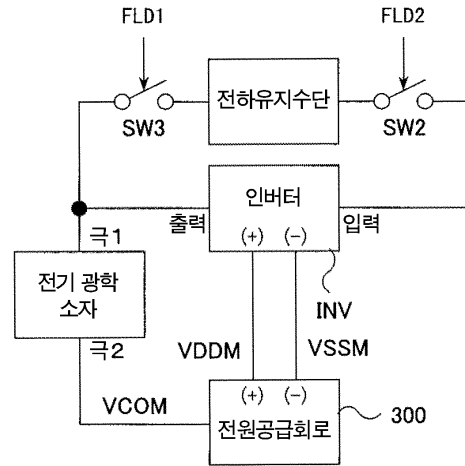
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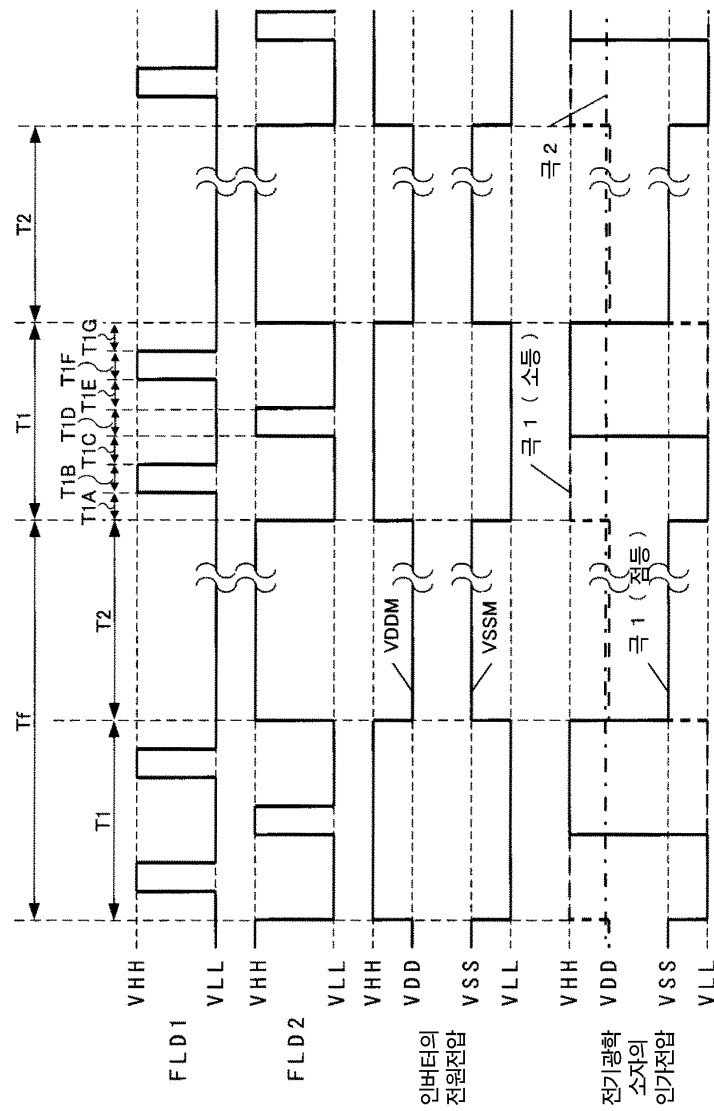
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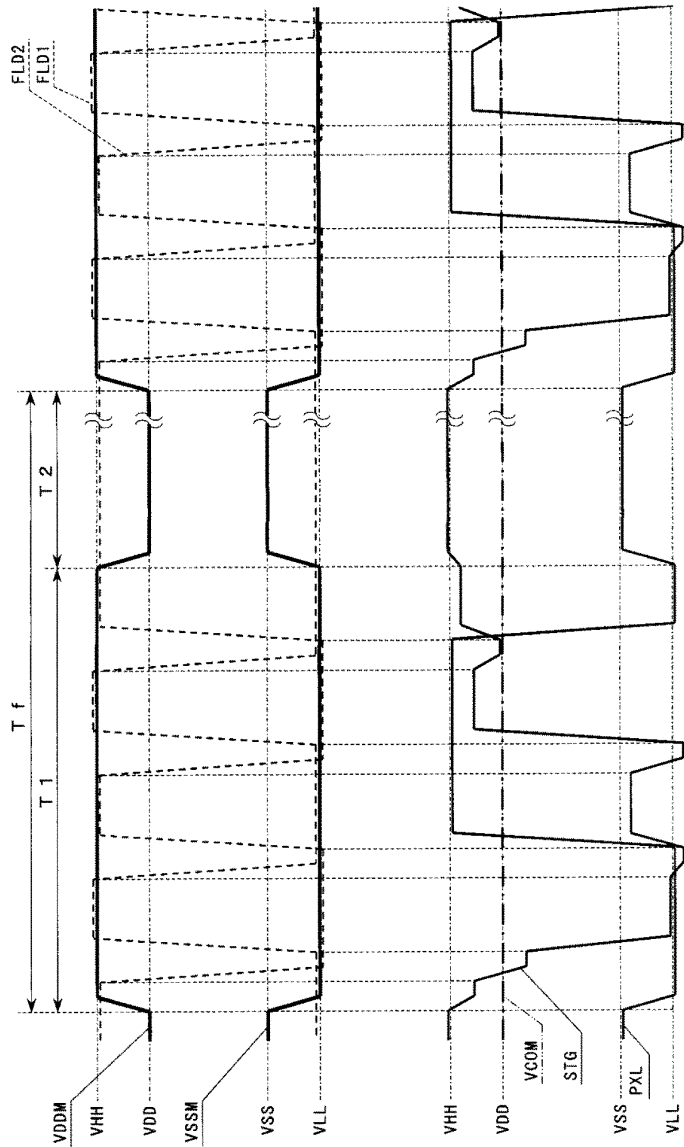
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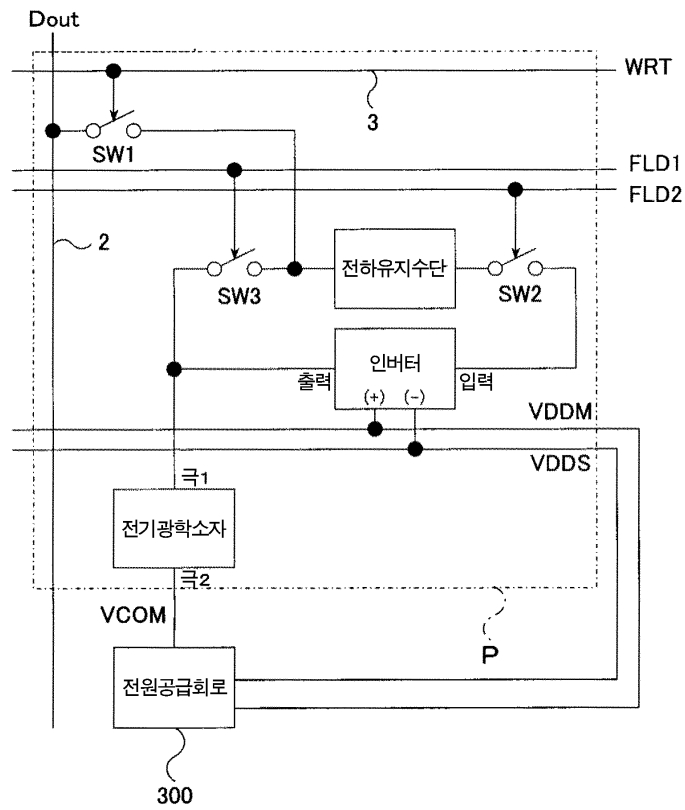
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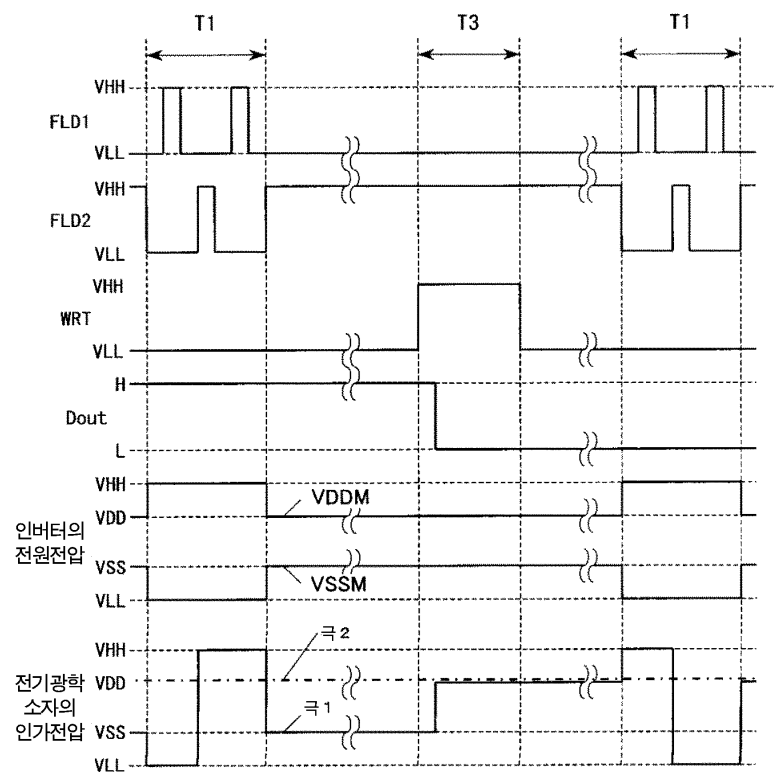
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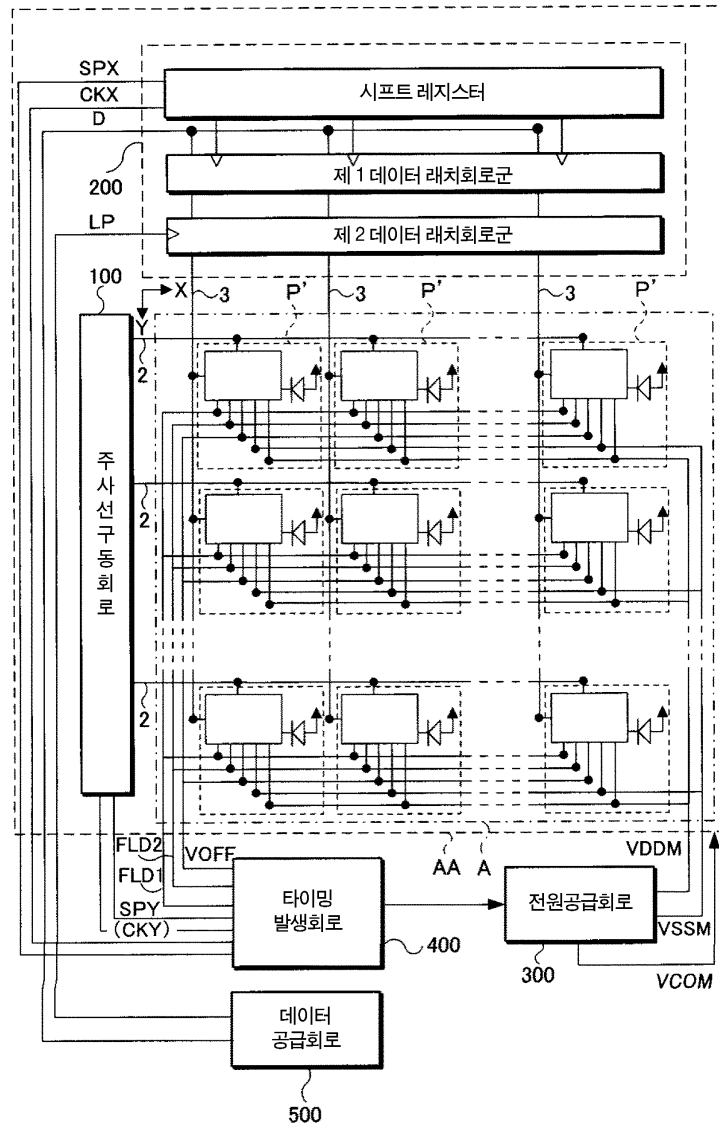


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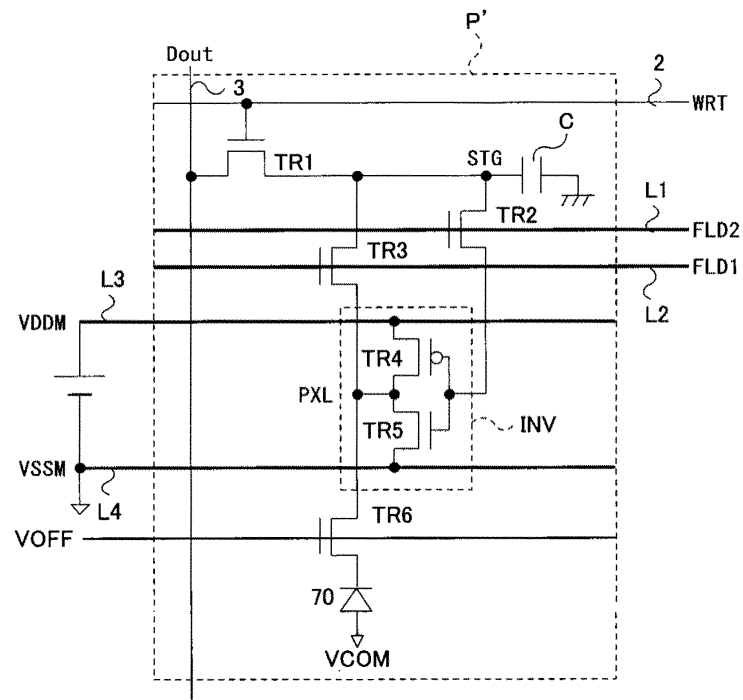


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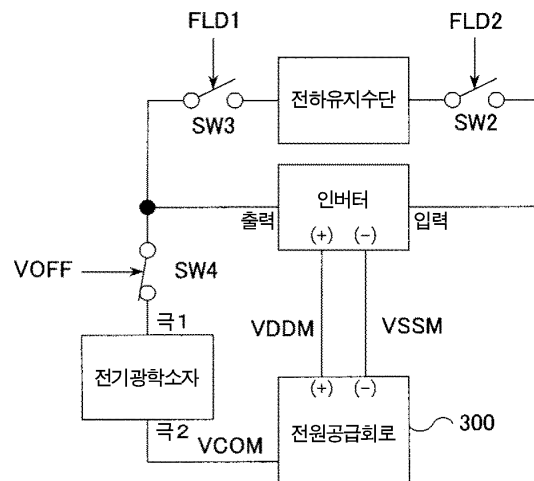


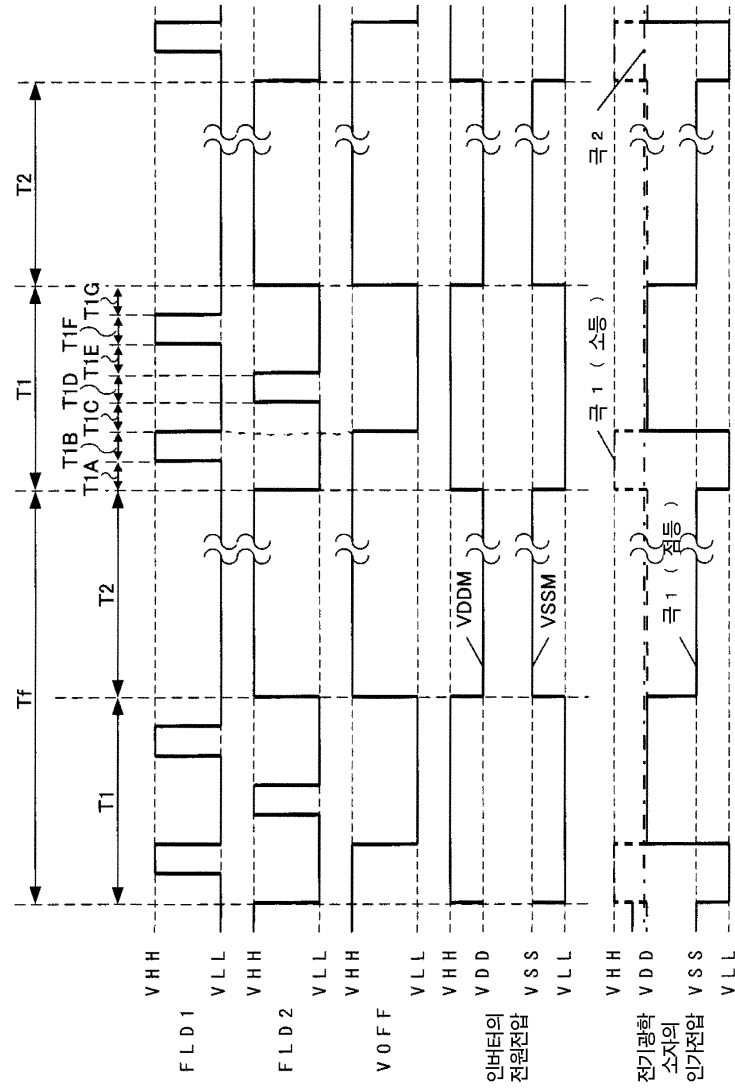


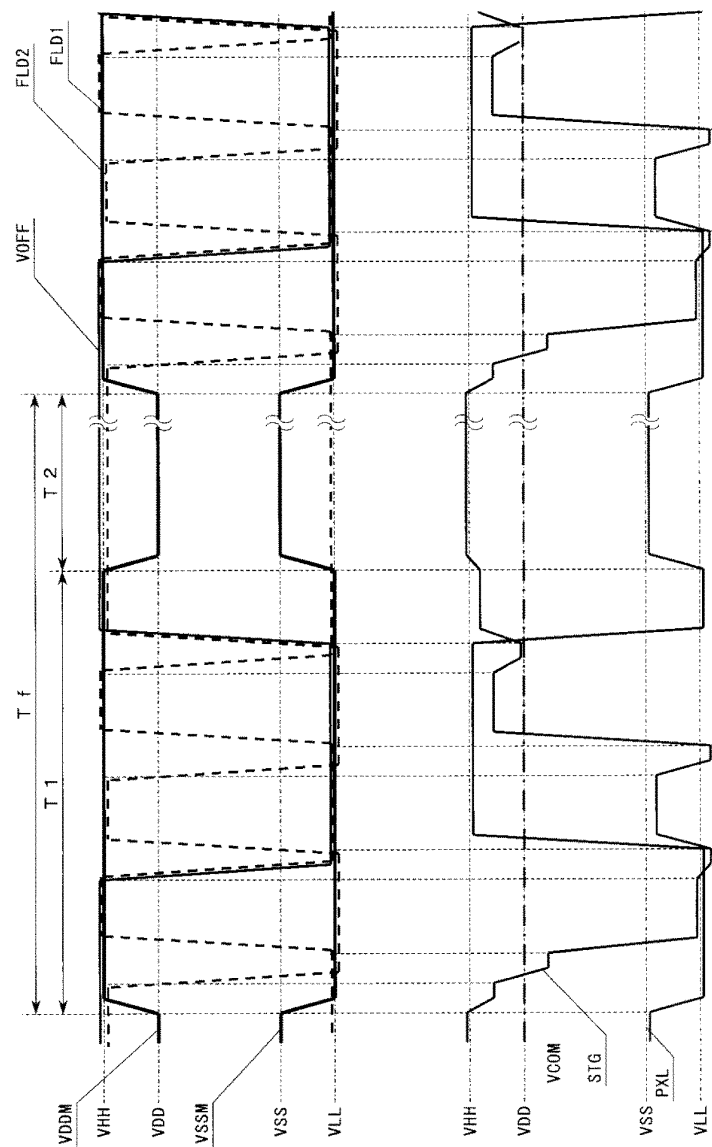
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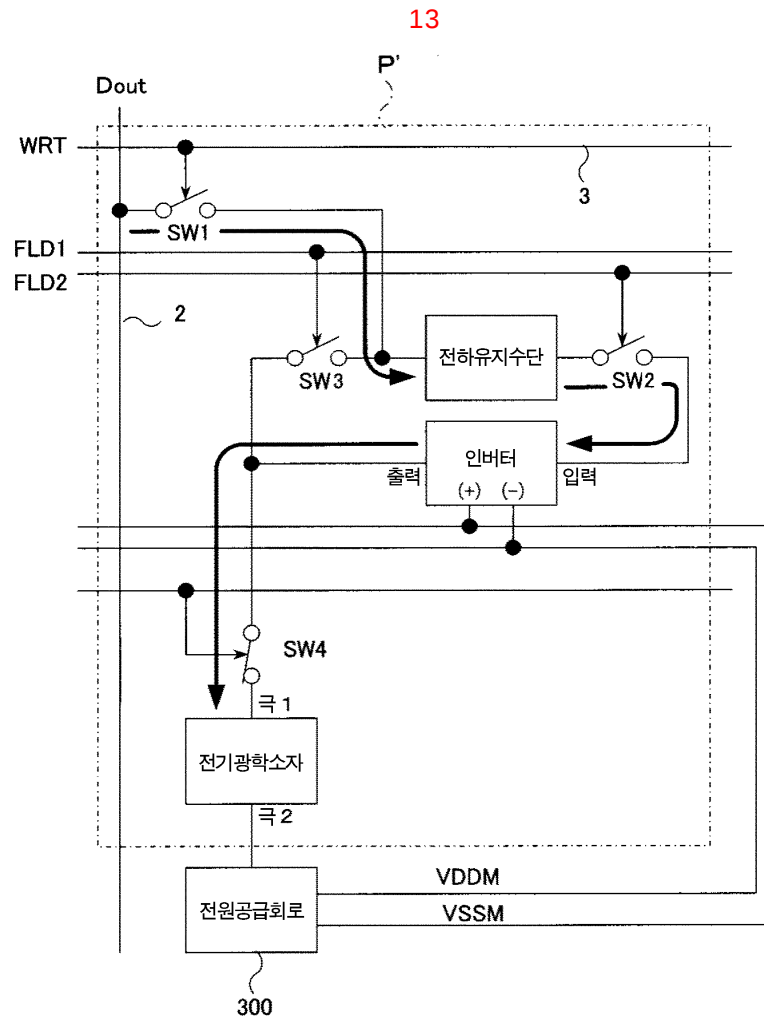


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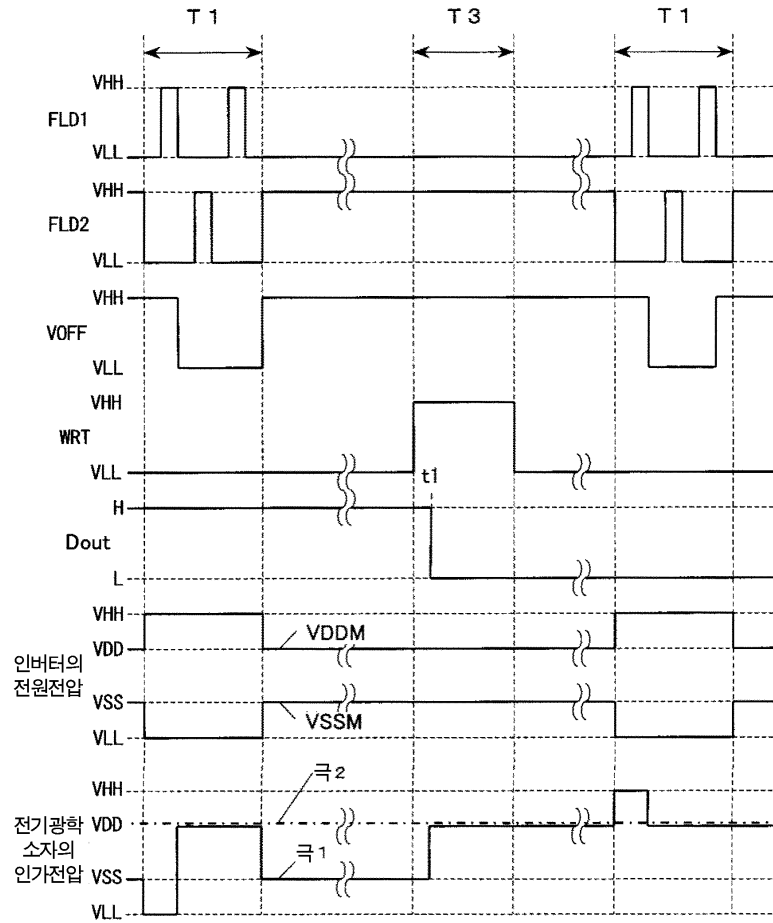




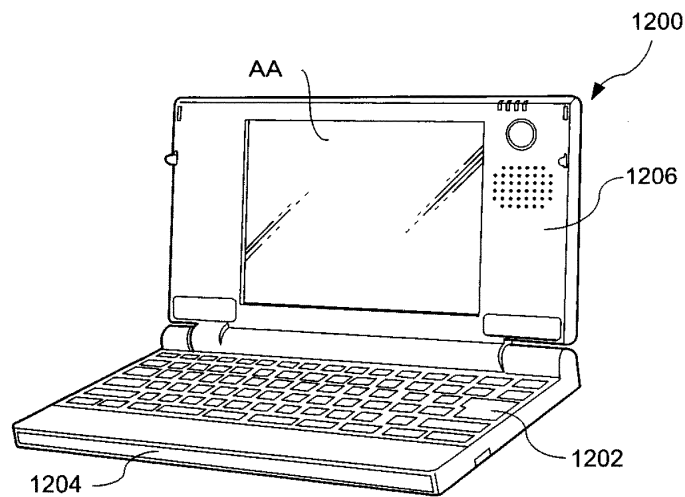


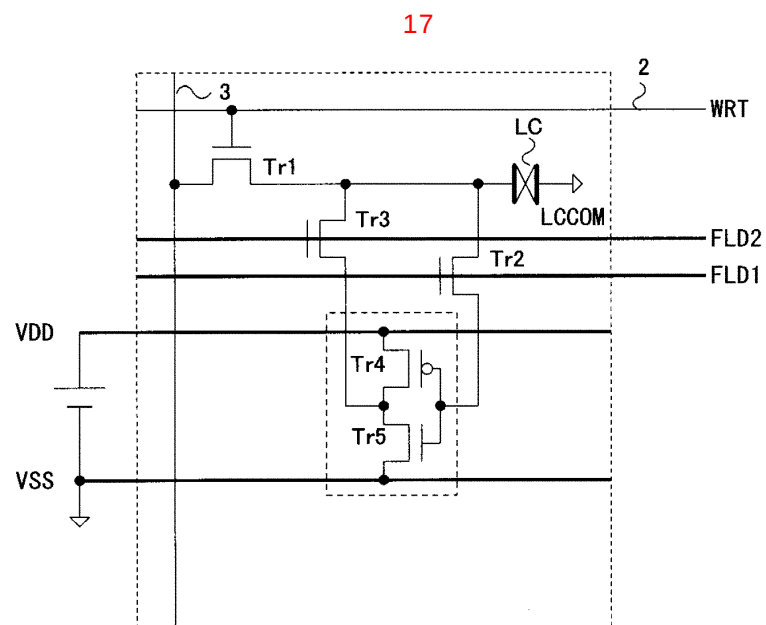
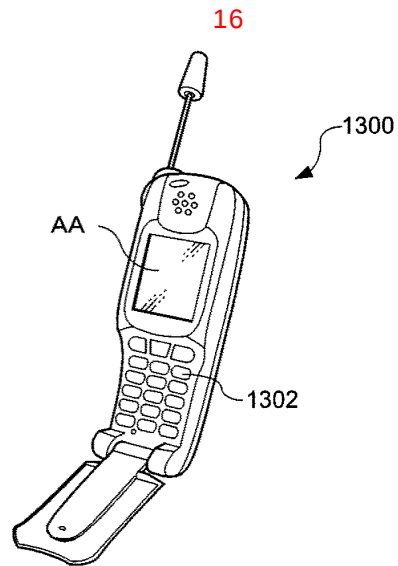


14



15





专利名称(译)	电光面板，驱动电路及其驱动方法，		
公开(公告)号	KR1020040075718A	公开(公告)日	2004-08-30
申请号	KR1020040007150	申请日	2004-02-04
[标]申请(专利权)人(译)	精工爱普生株式会社		
申请(专利权)人(译)	精工爱普生株式会社		
当前申请(专利权)人(译)	精工爱普生株式会社		
[标]发明人	OZAWA TOKURO		
发明人	OZAWA,TOKURO		
IPC分类号	G09G3/30 H01L51/50 G09G3/32 G09G3/20		
CPC分类号	G09G3/3258 G09G2300/0842 G09G2300/0861 G09G2330/021 G09G2300/0833		
代理人(译)	MOON，KI桑		
优先权	2003044369 2003-02-21 JP		
其他公开文献	KR100539991B1		
外部链接	Espacenet		

摘要(译)

并且数据以简单的配置存储在像素中。对应于数据线3和扫描线2的交叉点设置像素P。像素P具有保持电容器C，反相器INV，OLED元件70以及第一至第三晶体管TR1至TR3。在读取时段中，存储在保持电容器C中的数据被反相器INV反相，并且在保持电容器C中执行重写偶数次，从而可以保持保持电容器C的逻辑电平。在维持周期中，第二晶体管TR2导通。在读取时段中，高电位电源VDDM的电位升高到较高电位，并且与维持时段相比，低电位电源VSSM的电位降低。2 指数方面 像素电极，电源电路，公共电极，像素，

