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(12)

(KR)  
(B1)

(51) 。 Int. Cl.<sup>7</sup>  
G09G 3/30

(45)  
(11)  
(24)

2004 05 27  
10-0433216  
2004 05 17

(21) 10-2001-0068871  
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10-2003-0037608  
2003 05 14

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(54)

ED) (OLED) ; (OL  
2 1 (PMOS) (PMOS) (OLED) (VDD) ,  
, 3 1 (PMOS) , 1 2 (PMOS)  
4 (PMOS) , 1 2 (PMOS)

8

1  
2 1  
3 2  
4a 4b  
5 2  
6 5

7a	7b	
8		1
9	8	
10a	10b	
11		2
12	11	
13		3
14	13	
15		4
16	15	
17		5
18	17	
19		6
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21		7
22	21	
23		8
24	23	

< >  
 10,20 : EL      12,22 :  
 14,24 :              16,40,42,44 : EL

(Cathode Ray Tube)  
 (Liquid Crystal Display : 'LCD' ), (Field Emission  
 Display), (Plasma Display Panel : 'PDP' ) (Electro-Lu  
 minescence : 'EL' ) EL

, EL  
 EL (DL1 DLn) , 가 (10) 가 (GL1 GLm) (DL1 DLn) GLm  
 (PE) (PE) (GL1 GLn) (D  
 L) EL (12)가 (GL1 GLm) (12) (GL1  
 GLm) (14)가 (DL1 DLn) (14) (DL1 DLn) (PE)  
 (GND) (12) EL (OLED) , EL (OLED) (PE) 2 (16)  
 2 1 (PE) (GL) (DL)  
 4 TFT(T1, T2, T3, T4) (GND) EL (OLED) , EL (OLED) (  
 DL) EL (OLED) (16) (VDD)  
 EL (16) EL (OLED), (DL) 1 2 PMOS T  
 FT(T1,T2) ; 2 PMOS TFT(T2), (GL) (GL)  
 3 PMOS TFT(T3) ; 1 PMOS TFT(T1) 2 PMOS TFT(T2) , (GL)

3 PMOS TFT(T3) (VDD) 4 PMOS TFT(T4); 1 PMOS TFT(T1) (Cst) 2 PMOS TFT(T2)

4 PMOS TFT(T4) (GL) 3 PMOS TFT(T3) (LOW) 가 3 PMOS TFT(T3) (DL)

4) (Cst) 1 PMOS TFT(T1) 2 PMOS TFT(T2) (VDD)

(GL) (DL) 2 PMOS TFT(T2) 1

가 (Cst) (DL) 3 PMOS TFT(T3) 4 PMOS TFT(T4) 1 가 (Holding) (Cst)

(DL) 가 EL (OLED) EL (OLED)

1 (Cst) EL (OLED)

가 가 3 PMOS TFT(T3) 4 PMOS TFT(T4)가 2 PMOS TFT(T2)

(Vgs) EL (OLED)

가

5 2 (PE) (GND) EL (OLED) , EL (OLED) (

DL) EL (OLED) (26) (VDD) 1 2 PMOS T

EL (26) EL (OLED), (DL) 1 (GL1) (GL)

FT(T1, T2) ; 2 PMOS TFT(T2), 3 PMOS TFT(T3) ; 1 PMOS TFT(T1) 2 PMOS TFT(T2) , 2

(GL2) 3 PMOS TFT(T3) (VDD) 4 PMOS TFT(T4); 1 PMOS TFT(T1) 2 PMOS TFT(T2)

(Cst)

3 PMOS TFT(T3) 1 2 (GL1,GL2) 6 (LOW) 가

4 PMOS TFT(T4)가 - 3 PMOS TFT(T3) 가 4 PMOS TFT(T4)가 -

(DL) 가 가 3 PMOS TF

T(T3) 4 PMOS TFT(T4) (Cst) 2 PMOS TFT(T2) (VDD) 1

(Cst) 1 PMOS TFT(T1) (DL) 1

2 (GL1,GL2) (GL1) (GL1)

PMOS TFT(T4) (GL1) 1 (GL1) 7a 4

xel). 1 (Vdrain) (Vpixel) 7b

1 2 (GL1,GL2) 가 가 가

2

4TFT 가 4 PMOS TFT

(OLED)

(OLED) (OLED) ;

(OLED) 2 1 (PMOS) (VDD)

OS) (OLED) 3 1 (PMOS)

1 2 (PMOS)

S) , 1 2 (PMOS) 4 (PMO

(OLED) (OLED) ; (VDD) , (OL

ED) 2 1 (PMOS) , 1 (PMOS) 1

2 (PMOS) 4 (PMOS) , 1 2 (PMO

S) .

8 24

(GL1 GLm) 1 EL 1 (10) (GL1 GLm) (DL1 DLn)

(PE) (GL1 GLn) (DL1 DLn) (D

L) EL (12)가 (GL1 GLm) (DL1 DLn) (GL1 (PE)

GLm) (14)가 (DL1 DLn) (14) (DL1 DLn) (DL1 DLn) (PE)

8 1

(PE) (VDD) EL (OLED) , EL (OLED) (36)

EL (36) EL (OLED), (VDD) 1 2 PMOS T

FT(T1, T2) ; 2 PMOS TFT(T2) (VDD) (GL)

L) 3 PMOS TFT(T3) ; 1 PMOS TFT(T1) 2 PMOS TFT(T2) (D

FT(T1) 2 PMOS TFT(T2) (VDD) 4 PMOS TFT(T4); 1 PMOS T

(Cst)

4 PMOS TFT(T4)가 (GL) 9 (LOW) 가 3 PMOS TFT(T3)

3 PMOS TFT(T3) 가 4 PMOS TFT(T4)가 (DL)

st) 1 (N1) (Vdata), (Vdrain), (Vpixel) 10a

2 PMOS TFT(T2)

3 PMOS TFT(3) (DL)

(GL) 2 PMOS TFT(T2) 10b 3 PMOS TFT(T3) 2 PMOS TF

T(T2) (VDD) - (Pull-Up) 4 PMOS TFT(T4)가

1 PMOS TFT(T1)

(Cst) (DL) 3 PMOS TFT(T3) 4 PMOS TFT(T4) 가

(DL) 가 EL (OLED) (Holding) (Cst)

1 EL (OLED) EL (OLED)

11 2

(PE) (VDD) EL (OLED) , EL (OLED) (46)

EL (46) EL (OLED), (VDD) 1 2 PMOS T

FT(T1, T2) ; 2 PMOS TFT(T2) (VDD) (GL)

L) 1 NMOS TFT(T3) ; 1 PMOS TFT(T1) 2 PMOS TFT(T2) (D

FT(T1) 2 PMOS TFT(T2) (VDD) 2 NMOS TFT(T4); 1 PMOS T

(Cst)

2 NMOS TFT(T4)가 (GL) 12 (HIGH) 가 1 NMOS TFT(T3) (DL)  
 (Cst) 1 (N1) (Vdata), 가 2 NMOS TFT(T4) (Vpixel)  
 2 PMOS TFT(T2) (VDD)  
 1 NMOS TFT(T3) (DL)  
 (VDD) 2 PMOS TFT(T2)  
 (GL)  
 I-Up) 1 NMOS TFT(T3) 2 PMOS TFT(T2) (VDD) - (Pul  
 OS TFT(T1) 2 NMOS TFT(T4)가 1 PM  
 (DL) (DL) (Cst)  
 (DL) 가 EL (OLED) (Holding) 가 (Cst) . 1  
 (Cst) EL (OLED)  
 13 3  
 (PE) (VDD) EL (OLED) , EL (OLED) (56)  
 EL (56) EL (OLED), (VDD) 1 2 NMOS T  
 FT(T1, T2) ; 2 NMOS TFT(T2) (VDD) (GL)  
 3 PMOS TFT(T3) ; 1 NMOS TFT(T1) 2 NMOS TFT(T2) (D  
 L) (GL) (DL) 4 PMOS TFT(T4); 1 NMOS T  
 FT(T1) 2 NMOS TFT(T2) (VDD) (Cst)  
 (GL) 14 (LOW) 가 3 PMOS TFT(T3)  
 4 PMOS TFT(T4)가 (DL) 4 PMOS TFT(T4) (DL)  
 (Cst) 1 (N1) (Vdata), 가 4 PMOS TFT(T4) (Vpixel)  
 2 PMOS TFT(T2) (DL)  
 3 PMOS TFT(3) (VDD) 2 PMOS TFT(T2)  
 (GL)  
 (VDD) 3 PMOS TFT(T3) 2 PMOS TFT(T2)  
 I-Up) 2 PMOS TFT(T2) (VDD) - (Pul  
 MOS TFT(T1) 4 PMOS TFT(T4)가 1 P  
 (DL) (DL) (Cst)  
 (DL) 가 EL (OLED) (Holding) 가 (Cst) . 1  
 (Cst) EL (OLED)  
 15 4  
 (PE) (VDD) EL (OLED) , EL (OLED) (66)  
 EL (66) EL (OLED), (VDD) 1 2 NMOS T  
 FT(T1, T2) ; 2 NMOS TFT(T2) (VDD) (GL)  
 3 NMOS TFT(T3) ; 1 NMOS TFT(T1) 2 NMOS TFT(T2) (D  
 DL) (GL) (DL) 4 NMOS TFT(T4); 1 NMOS  
 TFT(T1) 2 NMOS TFT(T2) (VDD) (Cst)  
 (GL) 16 (HIGH) 가 3 NMOS TFT(T3)  
 4 NMOS TFT(T4)가 (DL) 4 NMOS TFT(T4) (DL)  
 (Cst) 1 (N1) (Vdata), 가 4 NMOS TFT(T4) (Vpixel)  
 2 NMOS TFT(T2) (DL)  
 3 NMOS TFT(T3) (VDD) 2 NMOS TFT(T2)

(GL) 3 NMOS TFT(T3) 2 NMOS TFT(T2)  
 (VDD) 2 NMOS TFT(T2) (VDD) - (  
 Pull-Up) 4 NMOS TFT(T4)가 1  
 NMOS TFT(T1)  
 3 NMOS TFT(T3) 4 NMOS TFT(T4) 가 (Cst)  
 (DL) 1 (Holding)  
 (DL) 가 EL (OLED) (Cst)  
 1 EL (OLED)  
 17 5  
 (PE) (VDD) EL (OLED), EL (OLED) (76)  
 EL (76) EL (OLED), (VDD) 1 2 PMOS T  
 FT(T1, T2); 2 PMOS TFT(T2) (VDD) (GL)  
 3 PMOS TFT(T3); 1 PMOS TFT(T1) 2 PMOS TFT(T2) (  
 GL) (DL) 4 PMOS TFT(T4); 1 PMOS TFT(T1) 4 PM  
 OS TFT(T4) (VDD) (Cst)  
 (DL) 2 PMOS TFT(T2) 4 PMOS TFT(T4)  
 4 PMOS TFT(T4)가 - (GL) 18 (LOW) 가 3 PMOS TFT(T3)  
 3 PMOS TFT(T3) 4 PMOS TFT(T4)가 - (DL)  
 가 가 4 PMOS TFT(T4)  
 (Cst)  
 1 (N1) (Vdata), (Vpixel) 2  
 PMOS TFT(T2) (VDD) 3 PMOS TFT(T3)  
 (DL) (VDD) 2 PMOS  
 TFT(T2)  
 (GL) 3 PMOS TFT(T3) 2 PMOS TFT(T2)  
 (VDD) 2 PMOS TFT(T2) (Vdata) (VDD)  
 - (Pull-Up) (Vdata) 4 PMOS TFT(T4)가  
 1 1 PMOS TFT(T1) (Cst) EL (OLED)  
 19 6  
 (PE) (VDD) EL (OLED), EL (OLED) (86)  
 EL (86) EL (OLED), (VDD) 1 2 PMOS T  
 FT(T1, T2); 2 PMOS TFT(T2) (VDD) (GL)  
 1 NMOS TFT(T3); 1 PMOS TFT(T1) 2 PMOS TFT(T2) (  
 GL) (DL) 2 NMOS TFT(T4); 1 PMOS TFT(T1) 4 N  
 MOS TFT(T4) (VDD) (Cst)  
 (DL) 2 PMOS TFT(T2) 2 NMOS TFT(T2)  
 2 NMOS TFT(T4)가 - (GL) 20 (HIGH) 가 1 NMOS TFT(T3)  
 1 NMOS TFT(T3) 2 NMOS TFT(T4)가 - (DL)  
 가 가 4 PMOS TFT(T4)  
 (Cst)  
 1 (N1) (Vdata), (Vpixel) 2  
 PMOS TFT(T2) (VDD) 1 NMOS TFT(T3)  
 (DL) (VDD) (VDD) 2 PM  
 OS TFT(T2)  
 (GL) 1 NMOS TFT(T3) 2 PMOS TFT(T2)  
 (VDD) (VDD) (Vdata)  
 (VDD) - (Pull-Up) (Vdata) 2 NMOS TFT(  
 T4)가 - 1 PMOS TFT(T1)  
 가 (Cst) (DL) 1 NMOS TFT(T3) 2 NMOS TFT(T4)  
 (DL) 1 (Holding)  
 (Cst) 가 EL (OLED) EL (OLED)

21 (PE) 7 (VDD) EL (OLED) , EL (OLED) (96)

EL (96) EL (OLED), (VDD) 1 2 NMOS T  
 FT(T1, T2) ; 2 NMOS TFT(T2) (VDD) (GL)

GL) 1 PMOS TFT(T3) ; 1 NMOS TFT(T1) 2 NMOS TFT(T2) ( (

MOS TFT(T4) (DL) 2 PMOS TFT(T4); 1 NMOS TFT(T1) 2 P

(DL) 2 NMOS TFT(T2) (VDD) 2 PMOS TFT(T4) (Cst)

2 PMOS TFT(T4)가 (GL) 22 (LOW) 가 1 PMOS TFT(T3)

(Cst) 1 PMOS TFT(T3) 2 PMOS TFT(T4)가 (DL)

(DL) 2 PMOS TFT(T4)가 2 PMOS TFT(T4)

(Cst) 1 (N1) (Vdata), (Vpixel) 2

NMOS TFT(T2) (DL) (VDD) 1 PMOS TFT(T3)

OS TFT(T2) (GL) - 1 PMOS TFT(T3) 2 NMOS TFT(T2) 2 NM

(VDD) 2 NMOS TFT(T2) (Vdata) (VDD)

(Pull-Up) (Vdata) 2 PMOS TFT(T4)가

1 NMOS TFT(T1) 1 PMOS TFT(T3) 2 PMOS TFT(T4) 가

(Cst) (DL) (DL) 1 (Holding) (Cst)

(DL) 가 EL (OLED) EL (OLED)

(Cst) (Cst) EL (OLED)

23 (PE) 8 (VDD) EL (OLED) , EL (OLED) (106)

EL (106) EL (OLED), (VDD) 1 2 NMOS

TFT(T1, T2) ; 2 NMOS TFT(T2) (VDD) (GL)

GL) 3 NMOS TFT(T3) ; 1 NMOS TFT(T1) 2 NMOS TFT(T2) ( (

MOS TFT(T4) (DL) 4 NMOS TFT(T4); 1 NMOS TFT(T1) 4 N

(DL) 2 NMOS TFT(T2) (VDD) 4 NMOS TFT(T4) (Cst)

4 NMOS TFT(T4)가 (GL) 24 (HIGH) 가 3 NMOS TFT(T3)

(Cst) 3 NMOS TFT(T3) 4 NMOS TFT(T4)가 (DL)

4 NMOS TFT(T4)가 4 NMOS TFT(T4)

(Cst) 1 (N1) (Vdata), (Vpixel) 2

NMOS TFT(T2) (DL) (VDD) 3 NMOS TFT(T3)

OS TFT(T2) (GL) - 3 NMOS TFT(T3) 2 NMOS TFT(T2) 2 NM

(VDD) 2 NMOS TFT(T2) (Vdata) (VDD)

(Pull-Up) (Vdata) 4 NMOS TFT(T4)가

1 NMOS TFT(T1) 3 NMOS TFT(T3) 4 NMOS TFT(T4) 가

(Cst) (DL) (DL) 1 (Holding) (Cst)

(DL) 가 EL (OLED) EL (OLED)

(Cst) (Cst) EL (OLED)

2 1 가

2 1

(57)

1.

DD) , (OLED) ; (OLED) (V

1 (PMOS) 2 (PMOS)

1 3 1 (PMOS) 4 (PMOS)

1 2 (PMOS)

2.

DD) , (OLED) ; (OLED) (V

1 (PMOS) 2 (PMOS)

1 1 1 (PMOS) (NMOS) 2 (PMOS) 2 (NMOS)

1 2 (PMOS)

3.

DD) , (OLED) ; (OLED) (V

1 (NMOS) 2 (NMOS)

1 1 1 (NMOS) (PMOS) (NMOS) 2 (PMOS)

1 2 (NMOS)

4.

(OLED) ; (OLED)

DD) , (OLED) ; (OLED) (V  
 1 (NMOS)  
 (OLED) 2 (NMOS) ,  
 1 3 1 (NMOS)  
 (NMOS) (PMOS) ,  
 1 2 (PMOS) 4 (NMOS)  
 , 1 2 (NMOS)  
 .  
**5.**

(OLED) ; (OLED) (V  
 (OLED) ; (OLED)  
 DD) , 1 (PMOS)  
 (OLED) 2 (PMOS) ,  
 1 (PMOS)  
 3 (PMOS)  
 1 2 (PMOS) ,  
 4 (PMOS) ,  
 1 2 (PMOS)  
 .  
**6.**

(OLED) ; (OLED) (V  
 (OLED) ; (OLED)  
 DD) , 1 (PMOS)  
 (OLED) 2 (PMOS) ,  
 1 (PMOS)  
 1 (NMOS)  
 1 2 (PMOS) ,  
 2 (NMOS) ,  
 1 2 (PMOS)  
 .  
**7.**

(OLED) ; (OLED) (V  
 (OLED) ; (OLED)  
 DD) , 1 (NMOS)  
 (OLED) 2 (NMOS) ,  
 1 (NMOS)  
 1 (PMOS)  
 1 2 (NMOS) ,  
 2 (NMOS) ,  
 1 2 (NMOS)  
 .  
**8.**

(OLED) ; (OLED) (V)

(OLED) (OLED) (V)

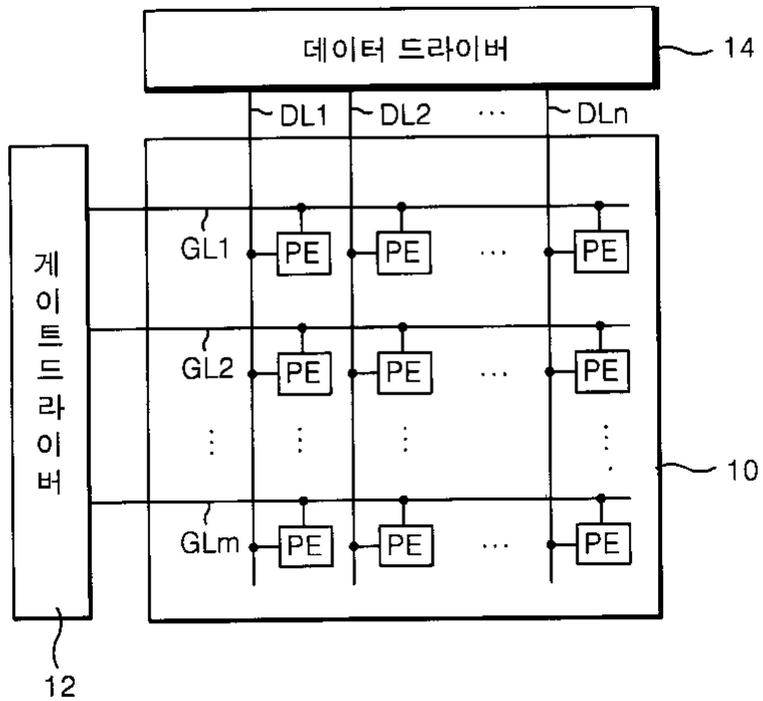
DD) ,

1 (NMOS) 2 (NMOS)

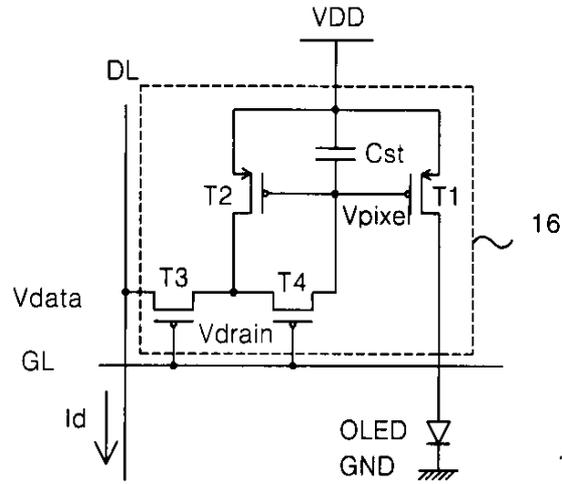
1 (PMOS) 3 (NMOS) 1 2 (NMOS)

1 2 (NMOS) 4 (NMOS)

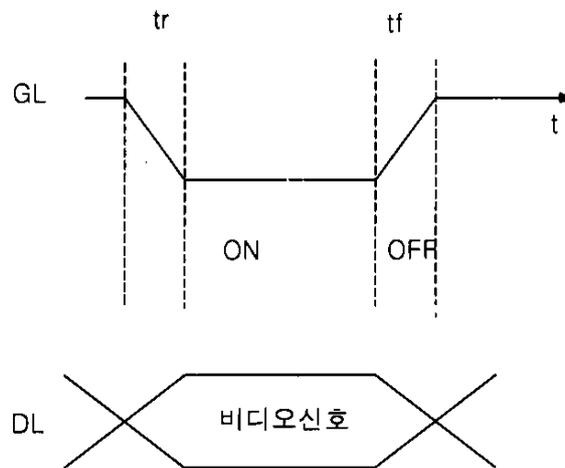
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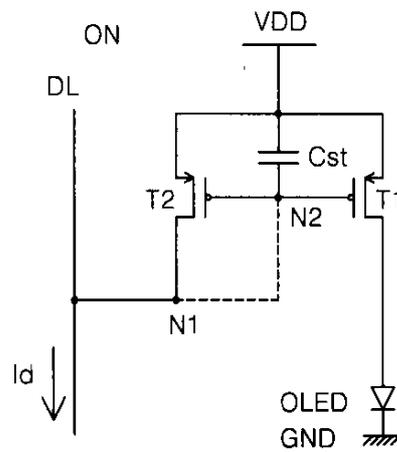
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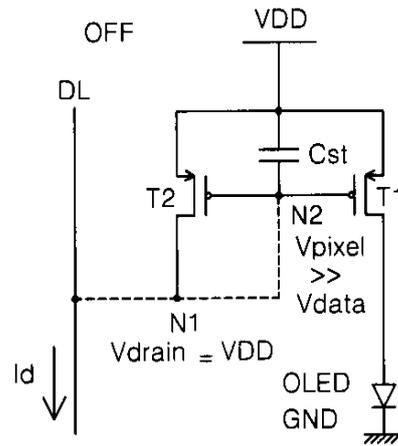
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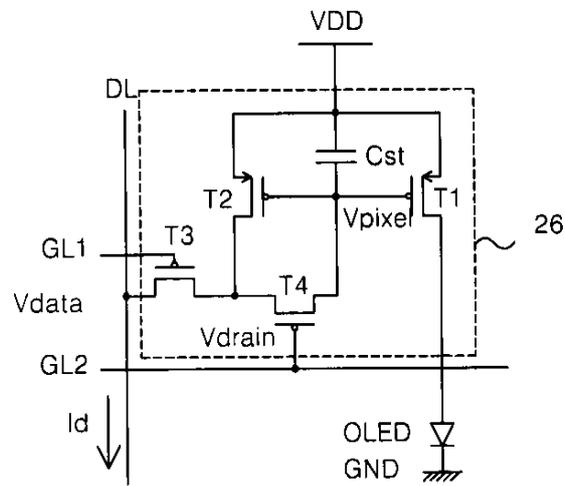
4a



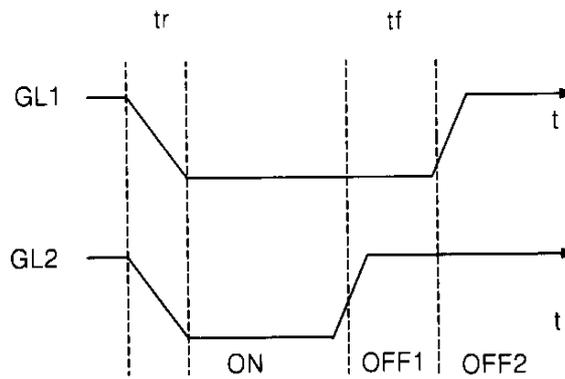
4b



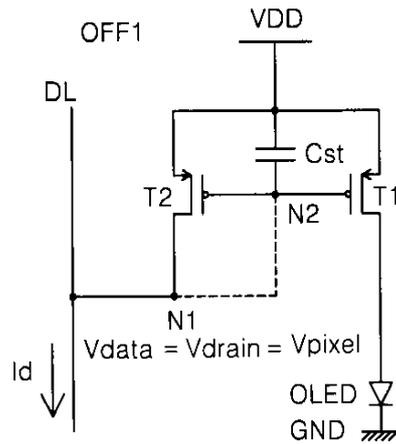
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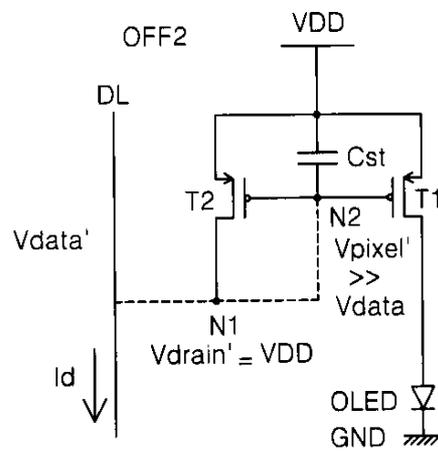
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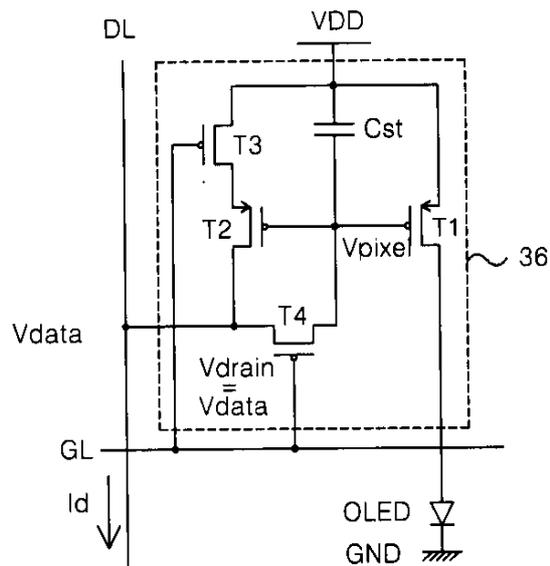
7a



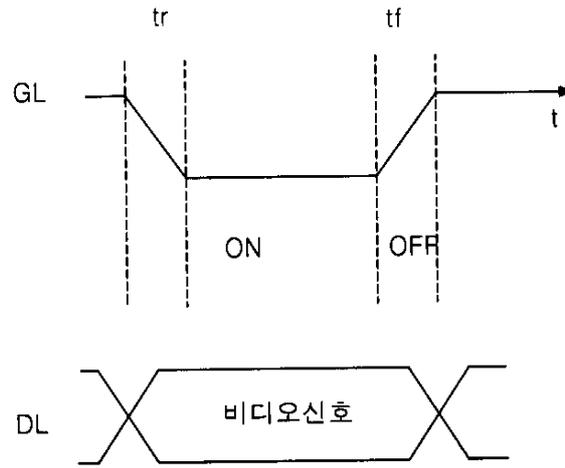
7b



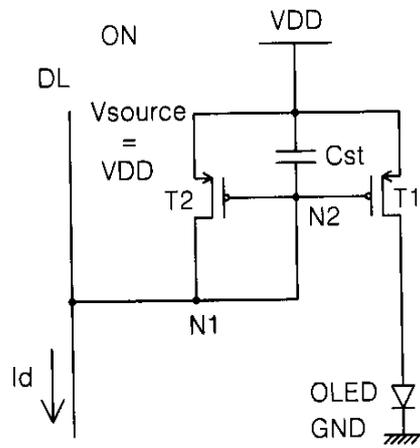
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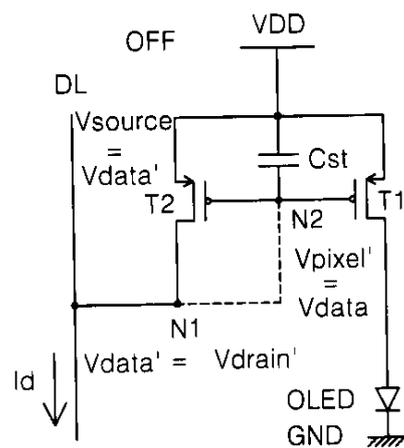
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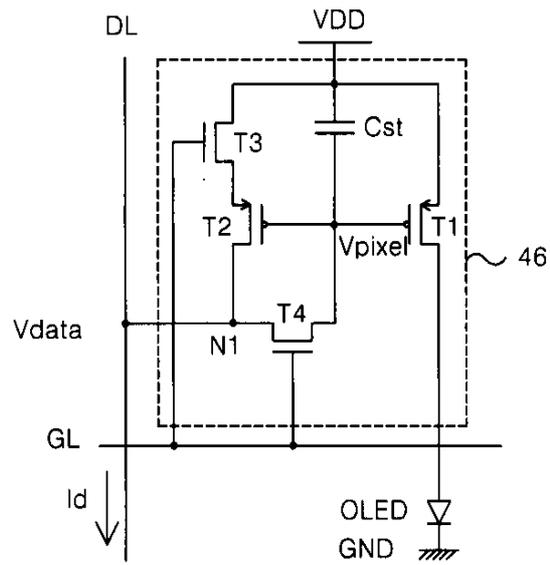
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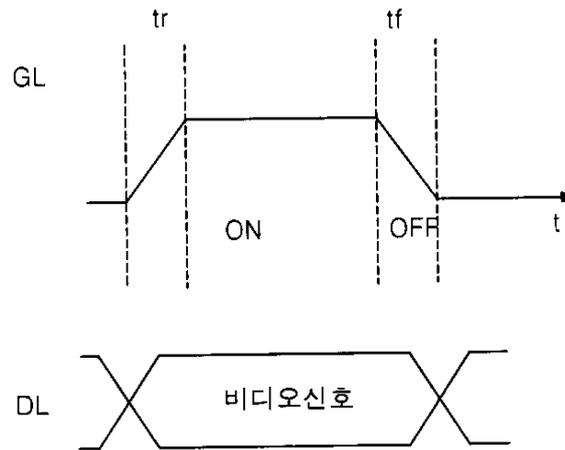
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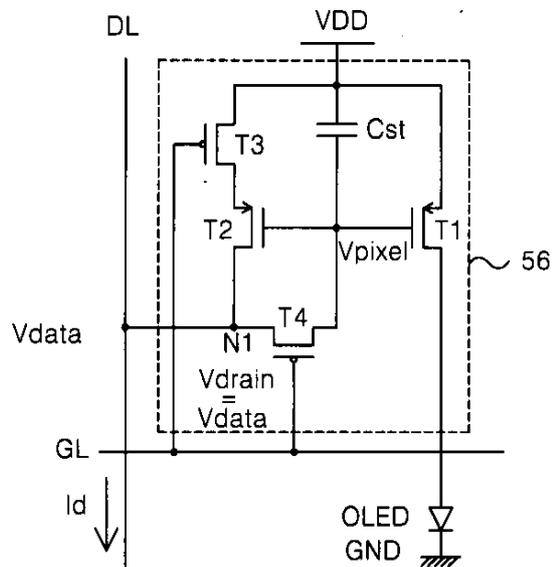
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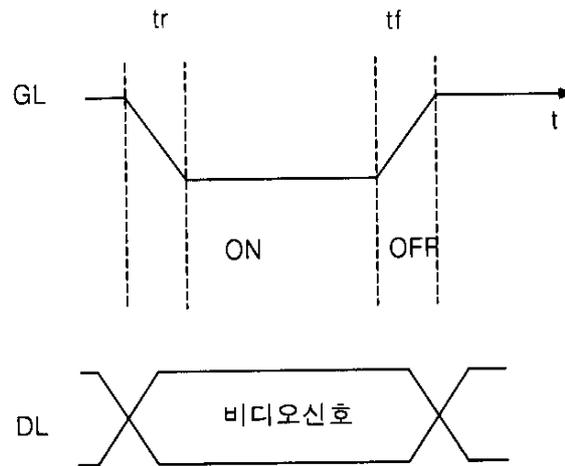
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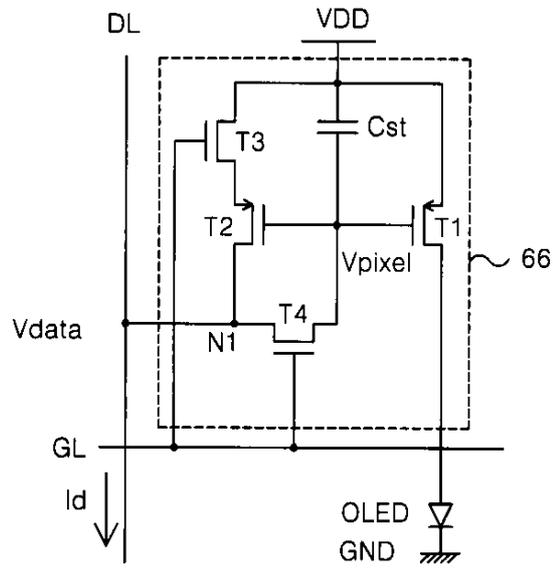
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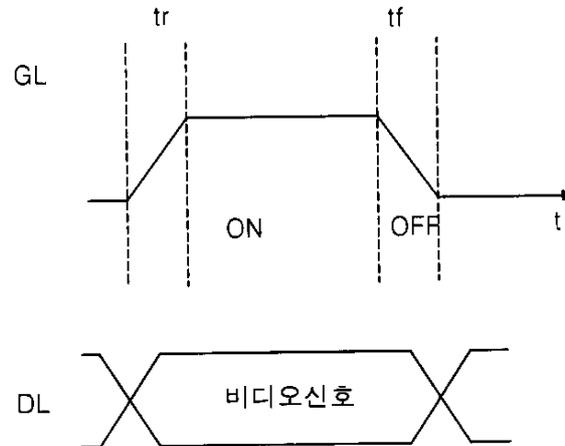
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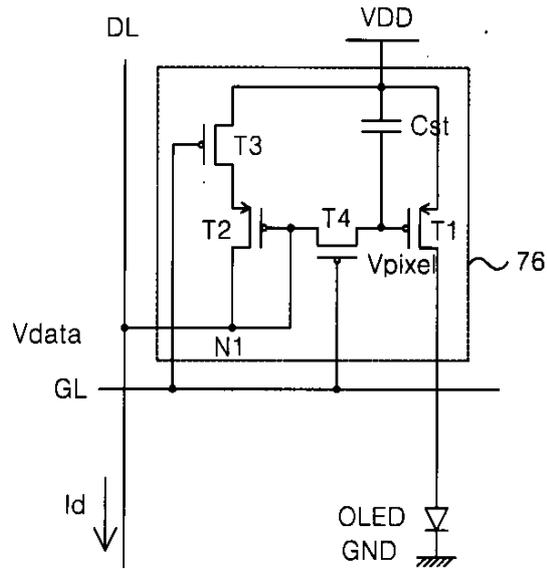
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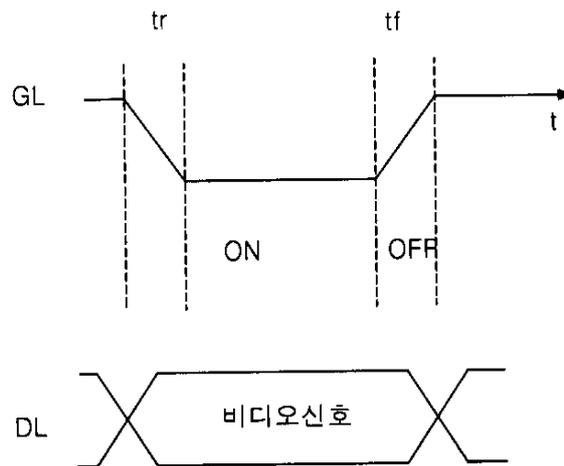
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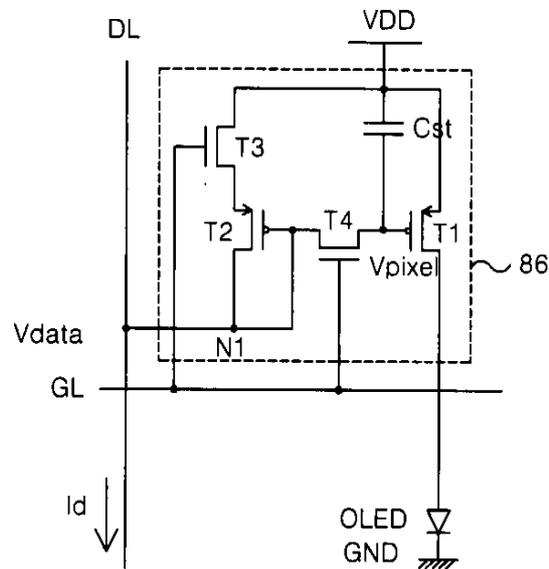
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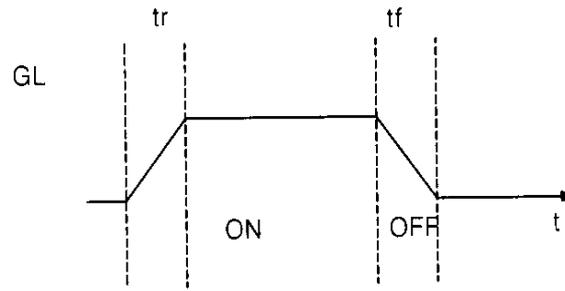
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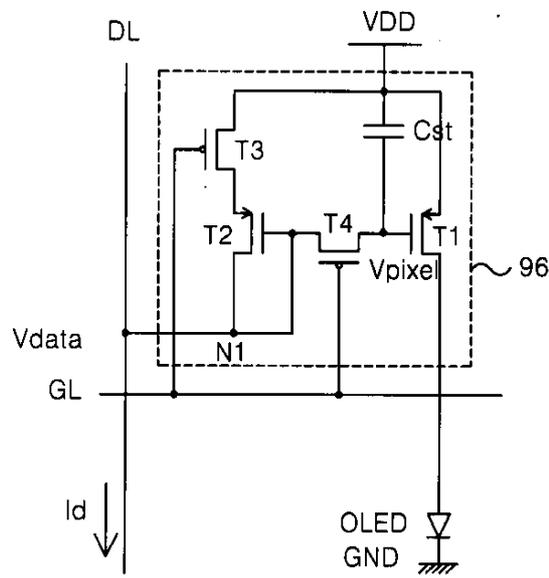
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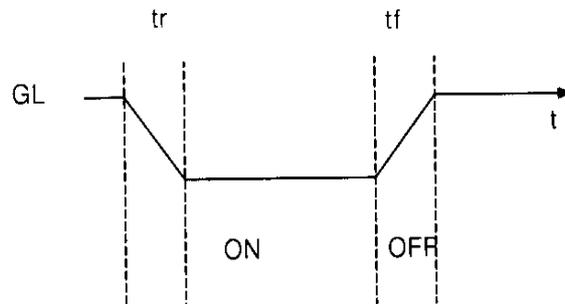
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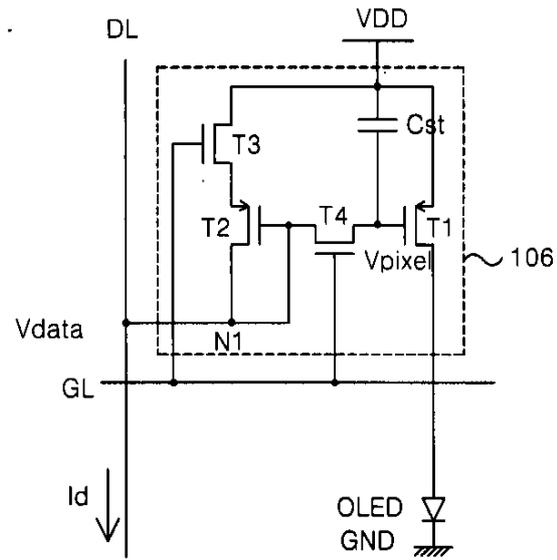
21



22



23



24

