(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
08 March 2018 (08.03.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/042079 A1

(51) International Patent Classification:
H05B 33/22 (2006.01) *C09K 11/57* (2006.01)
H05B 33/20 (2006.01) *C09K 11/08* (2006.01)
H05B 33/14 (2006.01) *C23C 16/455* (2006.01)
C23C 16/40 (2006.01)

(21) International Application Number:
PCT/FI2017/050608

(22) International Filing Date:
30 August 2017 (30.08.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20165652 02 September 2016 (02.09.2016) FI

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(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,

(54) Title: INORGANIC TFEL DISPLAY ELEMENT AND MANUFACTURING

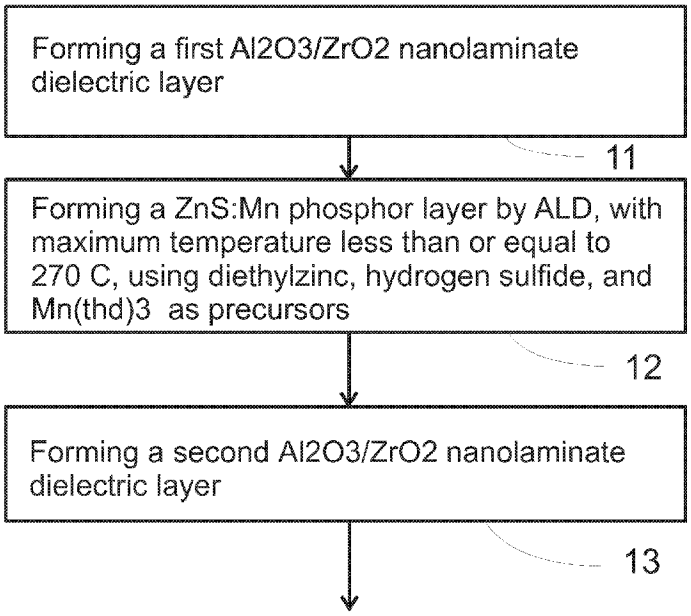

Fig. 1

(57) Abstract: A method for manufacturing an inorganic thin film electroluminescent display element comprises forming a layer structure, said forming the layer structure comprising forming a first dielectric layer (11); forming a luminescent layer (12), comprising manganese doped zinc sulfide ZnS:Mn, on the first dielectric layer, andforming a second dielectric layer (13) on the luminescent layer. Each of the first and the second dielectric layers are formed so as to comprise nanolaminate with alternating aluminum oxide Al_2O_3 and zirconium oxide ZrO_2 sub-layers.

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TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

INORGANIC TFEL DISPLAY ELEMENT AND MANUFACTURING

FIELD OF THE INVENTION

The present invention relates to electroluminescent displays, specifically to inorganic thin film electroluminescent displays.

BACKGROUND OF THE INVENTION

Electroluminescent displays (below also ”EL display”) have specific properties, such as durability and capacity of functioning at low temperatures, which make them as excellent display technology for the most challenging operating environments and conditions.

At a general level, the operation of EL displays is based on a luminescent material that emits light when exposed to an external electric field.

In inorganic EL displays provided as thin film structures, the luminescent material is arranged as a thin luminescent layer generally having a thickness of less than 1000 nanometers, typically approximately 500 – 750 nanometers. For low voltage applications, the thickness may be also lower. The luminescent layer is provided between two conductive electrode layers that are electrically insulated from the luminescent layer with thin dielectric layers serving for electrical insulating. A voltage difference between the electrodes provides an electric field, by the effect of which the electrons move in the luminescent layer and some of them excite, in the luminescent layer, so-called luminescent centers which are formed by the doping materials of the luminescent layer. Light is emitted as the excitation of the luminescent centers is relaxed.

The basic technology of EL displays is generally known and has been described extensively e.g. in "Electroluminescent Displays" (Yoshimasa A. Ono, World Scientific Publishing Co., 1995 (ISBN 981-02-1920-0) in Chapters 3,5 and 8.

An EL display element is typically manufactured by forming the core operating layers, namely, the dielectric layers, the phosphor layer, and the electrode layers, on a glass substrate having a thickness in the range of 1 mm. For many applications, this is not practical. For example, in applications where an EL display panel is to be laminated within a glass panel for automotive windscreen, there is only a narrow gap which may have a thickness of some hundreds of micrometers only available for the entire stack of the EL display, including the glass substrate thereof.

Substrates with lower thickness are also required in applications where a completed EL display element is to be laminated on a curved, i.e. non-planar external substrate, and in other applications of flexible display structure.

Thus, there is a need for EL display elements with glass substrates having as low thickness as possible while ensuring sufficient rigidity of the EL element.

Unfortunately, the high process temperatures of current manufacturing processes of the commonly used EL display structures are close to the softening temperatures of the commonly used glass substrate materials, thereby preventing the use of sufficiently thin glass substrates to meet that need.

SUMMARY OF THE INVENTION

This summary is provided to introduce a selection of concepts in a simplified form that are further described below in the Detailed Description. This Summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter

A method is disclosed which may be used for manufacturing an inorganic, possibly AC (alternating current) drivable, thin film electroluminescent display element which may be transparent. The method comprises forming a layer structure, said forming the layer structure comprising: forming a first dielectric layer, forming a luminescent layer, comprising manganese doped zinc sulfide ZnS:Mn, on the first dielectric layer, and forming a second dielectric layer on the luminescent layer.

Each of the first and the second dielectric layers are formed in the method so as to comprise nanolaminate material with alternating aluminum oxide Al_2O_3 and zirconium oxide ZrO_2 sub-layers. The luminescent layer may be formed by atomic layer deposition using maximum process temperature less than or equal to 250 °C. Then, diethylzinc, hydrogen sulfide, and tris(2,2,6,6-tetramethyl-3,5-heptanedione)manganese (hereinafter referred to as "Mn(thd)3") may be used as precursors.

Many of the attendant features will be more readily appreciated as the same becomes better understood by reference to the following detailed description considered in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The present description will be better understood from the following detailed description read in light of the accompanying drawings, wherein:

FIG. 1 illustrates a flow chart of a method for manufacturing an electroluminescent display element; and

FIG. 2 illustrates an electroluminescent display element; and

FIG. 3 shows test results of electroluminescent display elements.

The drawing of FIG. 2 is not in scale.

DETAILED DESCRIPTION

The method of FIG. 1 may be used for manufacturing an inorganic thin film electroluminescent display element.

Generally, a complete inorganic thin film electroluminescence/electroluminescent ("EL") display element manufactured utilizing the method may comprise a dielectric layer - luminescent layer - dielectric layer positioned between a first and a second conductive electrode layers. The entire layer stack is formed and lies on a transparent substrate formed of glass or some other suitable material. In operation, with suitable electric field provided in the luminescent layer by supplying a voltage difference between the conductive electrode layers, electrons are discharged into the luminescent layer, giving rise to light emission as luminescence centers excited by the electrons return to their ground state.

A "display element" refers to a structure for a display, which element can be a complete, operable,

stand-alone display device. Alternatively, the "element" can refer to a modular or inseparably integrated element as a part of a larger display device or display unit. For example, in the case of a multi-pixel display, a display element can comprise one or more pixels.

"Inorganic" refers to inorganic type of materials of the display element.

"Thin film" refers to the total thickness of the operational thin film layers of the EL display element, i.e. the layer stack without the transparent substrate thereof being less than some tens of micrometres, for example, in the range of 1 to 10 µm. Typically, that thickness is less than or equal to 3 µm.

The method of FIG. 1 comprises, in operation 11, forming a first dielectric layer which comprises nanolaminate material with alternating aluminum oxide Al_2O_3 and zirconium oxide ZrO_2 sub-layers.

"Nanolaminate" refers to the thickness of the alternating sub-layers in nanometer scale, i.e. in a range of a few to some dozens of nanometers. Nanolaminate may comprise any appropriate number of pairs of two adjacent sub-layers of different materials.

One or more, possibly most or all ZrO_2 sub-layers may have, for example, a thickness in the range of 1 to 9 nanometers, preferably in the range of 3 to 7, or 4 to 6 nm. With such thickness, ZrO_2 sub-layers may be formed with dense tetragonal (111) phase, i.e. "t-ZrO_2" phase of the zirconium crystal. Small crystal size may result high resistance over the ZrO_2 sub-

layer, in turn resulting in low leakage current in the EL display element. Further, said crystal structure also produces high permittivity which is an advantageous feature in the dielectric layers.

One or more, possibly most or all Al_2O_3 sub-layers may have, for example, a thickness in the range of 1 to 15 nm, preferably in the range of 3 to 10, or 5 to 10 nm. Al_2O_3 sub-layers with such thicknesses serve for producing suitable stress to the ZrO_2 sub-layers so that they may stay in their t-ZrO_2 phase.

As the first and/or the last sub-layer of the dielectric layer, an Al_2O_3 sub-layer may be formed which has a higher thickness than the other Al_2O_3 sub-layers superposed between the ZrO_2 sub-layers.

Next, in operation 12, a luminescent layer comprising, possibly completely consisting of, manganese doped zinc sulfide ZnS:Mn is formed on the first dielectric layer by atomic layer deposition ALD with a maximum process temperature in the range of 150 to 270 °C, preferably 200 to 270 °C or 225 to 260 °C, for example 250 °C, using diethylzinc DEZ, hydrogen sulfide H_2S, and Mn(thd)3 as precursors. Other possible Mn precursors are $Mn(C_5H_5)_2$ and its alkyl-, aryl- or carbonyl- substituted derivatives.

As discussed above, the "luminescent layer" serves as a core part of the completed electroluminescent display element, emitting light when exposed to suitable electric field. This layer and/or the light emitting material thereof may also be called "phosphor".

Depositing a further layer "on" a previous layer refers merely to deposition that layer after the

previous layer. It does not necessitate deposition "directly" on the previous layer, but one or more intermediate layers may be formed therebetween. Correspondingly, a layer or a layer structure lying "on" another layer or element does not necessarily lie "directly" on that another layer or element. For example, a layer structure of dielectric layer - luminescent layer - dielectric layer lying on a transparent substrate does not exclude the possibility of a conductive electrode layer lying between the substrate and said layer structure.

"Atomic layer deposition ALD" refers to a thin film technology enabling accurate and well controlled production of thin film coatings with nanometer-scaled thicknesses. ALD may also be called Atomic Layer Epitaxy ALE. In an ALD process, the substrate is alternately exposed to at least two precursors, one precursor at a time, to form on the substrate a coating by alternately repeating essentially self-limiting surface reactions between the surface of the substrate (on the later stages, naturally, the surface of the already formed coating layer on the substrate) and the precursors. As a result, the deposited material is "grown" on the substrate molecule layer by molecule layer.

In conventional ALD processes for depositing ZnS:Mn, maximum temperatures in the range of 500 - 530 °C are typically used. Some examples of depositing a ZnS:Mn luminescent layer in an EL display with ATO dielectric layers using diethylzinc DEZ, hydrogen sulfide H2S, and Mn(thd)3 as precursors is discussed in US 6113977 A. In those examples, process temperatures of 350 and 450 °C were used.

The inventors have now surprisingly found, in contrast to the established understanding in the art, that high quality and stable ZnS:Mn of an EL display element with Al_2O_3/ZrO_2 nanolaminate in the dielectric layers may be produced in as low temperatures as 270 °C and lower. Using such temperatures may provide great advantages in that the entire process of forming the dielectric layers and the luminescent layer may take place in temperatures, for example, not substantially exceeding 270 °C. This enables forming the EL display element layers on very thin glass substrates having thicknesses, for example, in the range of 100 – 250 µm or even lower without the risk that the glass substrate would lose its rigidity in result of softening. The latter is of particular importance when taking into account that in typical manufacturing processes, the glass sheets are conveyed automatically and, to save floor space of the manufacture, the glasses are held and transferred vertically or almost vertically, e.g. at 80 degrees angle relative to horizon. Then, if the glass sheets become so thin that they start bending under their own weight, the conveying process becomes considerably more difficult. Further, in higher temperatures, the very thin sheets start to deform from a uniform and flat shape to an unwanted wrinkled or crumpled shape if they are not completely evenly supported, even when held horizontally, let alone in vertical or semi-vertical position.

Such thin substrates facilitate producing the entire EL display element so as to have total thickness clearly below that of the conventional EL displays. For example, this may enable manufacturing of EL display elements with a total thickness allowing laminating the EL display within a glass panel for automotive wind screen. A typical laminated wind

screen assembly comprises a glass plate with a thickness of 2.5 mm, an interlayer of a binder, such as Polyvinyl butyral (PVB), and another glass plate of 2.5 mm. Typical standard thicknesses for the binder layer are 0.38 mm, 0.76 mm, and 1.14 mm. Such assemblies may be referred to, according to the overall thickness thereof, for example, as "5.38 laminated glass". With this kind of glass assembly, the transparent EL display shall have a thickness of less than 0.38/0.76/1.14 mm, taking into account that usually a binder layer of 10 µm or somewhat less is needed at least on one side of the EL display to attach the display to the assembly.

Further, with such low glass substrates, the EL display element may be formed so as to be flexible allowing, for example, laminating thereof on curved and/or flexible external substrates.

"Maximum temperature" of the ALD process refers to both the maximum temperature in the ALD reactor chamber as well as the maximum temperatures of the precursors and any carrier gases supplied therein. Thus, neither the temperature of the reactor chamber nor the temperature of any gas supplied therein may exceed the maximum temperature.

In operation 13, a second dielectric layer comprising nanolaminate material with alternating aluminum oxide Al_2O_3 and zirconium oxide ZrO_2 sub-layers is formed on the on the luminescent layer. The second dielectric layer may be formed similarly to the first dielectric layer discussed above.

Also the first and/or the second dielectric layers may be formed by atomic layer deposition ALD.

In FIG. 1, manufacturing of only the layer structure of the dielectric layers and the luminescent layer is illustrated. Complete manufacturing process may further comprise, for example, forming a first conductive electrode layer on the transparent substrate, and forming a second conductive electrode layer on the second dielectric layer.

The first and the second conductive electrode layers may be patterned to form rows and columns, whereby pixels are formed at the sites where the rows and the columns of the different electrode layers intersect. As a voltage is applied between such intersecting electrodes, electroluminescence appears in the phosphor layer at the relevant pixel. Apart from such matrix-type displays, also other display types can be designed and manufactured using TFEL technology. For example, instead of a regular array of pixels, the active areas, i.e. the light emitting areas of the display can be arranged to form e.g. 7-segment number displays or designs displaying discrete icons or symbols at predetermined locations.

The EL display element 20 of FIG. 2 may be manufactured generally in accordance with the method discussed above with reference to FIG. 1. What is stated about the details of the EL display manufactured by the method discussed above with reference to FIG. 1 applies, mutatis mutandis, also to the EL display element 20 of FIG. 2. The same applies vice versa.

The EL display element 20 comprises, and the layers thereof are formed on a glass substrate 21 which may have a thickness, for example, in the range of 100 to 250 µm. Most preferably, the thickness is less than or equal to 100 µm.

A first or lower conductive layer 22 is formed as adjacent conductor stripes on the glass substrate. A first or lower dielectric layer 23, comprising nanolaminate with alternating Al_2O_3 and ZrO_2 sub-layers 24, 25 lie on the glass substrate 21 and the first conductive electrode layer 22. The ZrO_2 and Al_2O_3 sub-layers may have thicknesses as discussed above with reference to FIG. 1.. As the outermost sub-layers of the first dielectric layer, there are Al_2O_3 sub-layers which have thicknesses higher than those of the other. Those thicknesses may be, for example, in a range of 15 to 30 nm, whereas the rest of the Al_2O_3 sub-layers may have a thickness, for example, in a range of 5 to 15 nm. The total thickness of the first dielectric layer may be, for example, in a range of 100 to 300 nm.

A luminescent layer 26 formed of ZnS:Mn, deposited by ALD with maximum process temperature as discussed above with reference to FIG. 1, using DEZ, H_2S, and Mn(thd)3 as precursors, lies on the first dielectric layer. Other possible Mn precursors are $Mn(C_5H_5)_2$ and its alkyl-, aryl- or carbonyl- substituted derivatives. The luminescent layer may have thickness, for example, in a range of 400 to 1000 nm.

On the luminescent layer, there is a second dielectric layer 27 which may be substantially similar to the first dielectric layer, comprising nanolaminate with alternating Al_2O_3 and ZrO_2 sub-layers 28, 29.

On the second dielectric layer, i.e. on top of the structure illustrated in FIG. 2, there is a second conductive electrode layer 30 which may be substantially similar to the first dielectric layer, with the stripes 31 thereof however being directed

perpendicular or otherwise at an angle relative to the conductor stripes of the first dielectric layer 22.

The display element 20 of FIG. 2 thus has a matrix electrode configuration. In other embodiments, segmented electrode configurations may be used.

In the matrix electrode configuration, light-emitting areas in the form of pixels 32 are formed in the luminescent layer 26 at positions where the conductor stripes of the first and the second conductive electrode layers intersect.

Any appropriate further layers and/or elements may be present in an EL display element in addition to those illustrated in FIG. 2.

In any embodiment of the method and the EL display element discussed above, zirconium content of the first and/or the second dielectric layer is preferably at least 10% by mass. This refers to the mass of the zirconium contained in a dielectric layer being at least 10% of the overall mass of that layer.

In first and/or second dielectric layer where the zirconium content is at least 10% by mass, aluminum content is preferably at least 5% by mass. This refers to the mass of the aluminum contained in such dielectric layer being at least 5% of the overall mass of that layer.

In any embodiment of the method and the EL display element discussed above, Zn to Mn ratio in the luminescent layer preferably lies in the range of 200:1 to 30:1, more preferably in the range of 100:1 to 50:1. It may be, for example, equal to 50:1.

The EL display element of FIG. 2 may provide various great advantages. First, as discussed above with reference to FIG. 1, the thin glass substrate serves for achieving a low overall thickness of the EL display component. This, in turn, enables having the overall EL display element as a flexible structure which may be further laminated or otherwise attached to a flexible and/or curved external substrate.

In addition, the EL display element in accordance with that of FIG. 2 has been found to have excellent aging and stability performance. This is discussed further below with reference to FIG. 3.

In FIG. 1, only operations of forming the dielectric-phosphor-dielectric stack are shown. Naturally, manufacturing an entire EL display element may comprise further operations, such as forming the conductive electrode layers and any appropriate additional layers, for example, for protective and/or passivating purposes. In such operations, principles and processes as such known in the art may be used. In the following, one example of a more complete manufacturing process, which is generally in accordance with that illustrated and discussed above with reference to FIG. 1, is discussed.

Example

The exemplary process starts by providing a cleaned glass substrate. The glass substrate may be formed of, for example, soda lime glass, borosilicate glass, or any other material with sufficient transparency. In some embodiments, substrates other than glass materials may be suitable, such as polymer substrates which may provide greater mechanical durability or flexibility than glass. Preferably, the glass

substrate has a thickness of less than or equal to 250 µm, more preferably less than or equal to 100 µm.

Next, a first conductive, transparent electrode layer is formed on the cleaned glass substrate by sputtering or by using ALD. In the case of sputtering, the first conductive electrode layer may be formed of indium tin oxide ITO. In the case of ALD, suitable materials include, for example, aluminum doped zinc oxide AZO.

The transparent electrode layer is patterned in accordance with a predetermined segment or matrix configuration by utilizing any appropriate lithographic operations.

Next, a first dielectric layer is deposited in an ALD reactor chamber heated to a temperature of 250 °C. Nanolaminate of Al_2O_3/ZrO_2 sub-layers is deposited by ALD using trimethylaluminum TMA, zirconium chloride $ZrCl_4$, and water H_2O as precursors, with following source temperatures: TMA at room temperature, $ZrCl_4$ at 225 °C, and H_2O at 13 °C. A total thickness of 145 nm is deposited, starting by depositing one Al_2O_3 sub-layer with a thickness of 15 nm. After this first sub-layer, seven 10 nm Al_2O_3 / 5 nm ZrO_2 sub-layer pairs are deposited. Finally, a last Al_2O_3 sub-layer with a thickness of 15 nm is deposited as the last sub-layer of the first dielectric layer.

A luminescent layer of ZnS:Mn with a thickness of 950 nm is deposited by ALD on the first dielectric layer, using diethylzinc DEZ, hydrogen sulfide H_2S, and Mn(thd)3 as precursors. The ALD reactor chamber where the deposition is carried out, which may be the same as, or different from, the reactor chamber used for deposition of the first dielectric layer and the second dielectric layer discussed below, is heated to

250 °C, and the precursors are supplied at following source temperatures: DEZ and H_2S at room temperature, and Mn(thd)3 at 140 °C. The luminescent layer is deposited with zinc to manganese ratio of 50:1.

A second dielectric layer is deposited by ALD on the luminescent layer, substantially similarly to the deposition of the first dielectric layer.

It is also possible to deposit the main portions of the dielectric layers in a different reactor chamber than the luminescent layer but to deposit a last part of the first dielectric layer and a first part of the second dielectric layer in the reactor chamber used for depositing the luminescent layer.

A second conductive electrode layer is formed on the luminescent layer. If a transparent EL display element is to be manufactured, the second conductive electrode layer may be deposited similarly to the first conductive electrode layer. In the case of non-transparent EL display element, the second conductive electrode layer may be formed, for example, by sputtering some suitable metal such as aluminum. The transparent electrode layer is patterned in accordance with the predetermined segment or matrix configuration by utilizing any appropriate lithographic operations.

In Figure 3, test results of an EL display element manufactured in accordance with the above example are shown as compared with test results of a reference EL display element with ATO as the material of the dielectric layers, and the ZnS:Mn luminescent layer having been deposited by ALD at reactor chamber temperature of 525 °C, using zinc chloride $ZnCl_2$, H_2S, and $MnCl_2$ as precursors. The EL display elements were manufactured with similar matrix configurations of the

conductive electrode layers, with light emitting pixels formed at points of the matrix where conductors of the first and the second conductive electrode layers intersect.

The graphs of FIG. 3 show voltage-luminance curves measured for corresponding pixels of the tested EL display elements of fresh samples and after sequential aging steps. Each aging step was carried out by driving the samples by driving voltage of 134 V RMS (root mean square) with a frequency of 500 Hz for 23 hours. The voltage-luminance relationship was measured for both display elements after each aging step.

Graph (a) represents the results measured from the reference display element, and graph (b) represents the results measured from the El display element manufactured in accordance with the example process described above, hereinafter called "enhanced" EL display element.

As shown in graph (a), the high-voltage luminance, i.e. the luminance with the test pixel of the display element at "ON" state, decreases after each aging. Instead, as shown in graph (b), the ON-state luminance of the corresponding enhanced display element stabilizes already after the first aging step. Further, in the reference display element, in consequence of the aging steps, the voltage-luminance dependency changes from the initial, substantially abrupt curve with well-defined threshold voltage, into a gradually increasing luminance without any such clear threshold voltage. Instead, in the enhanced sample, the threshold voltage drifts from about 170 V to about 190 V in consequence of the first aging step, but stabilizes then substantially without the voltage-luminance curve becoming more gradual.

To summarize, FIG. 3 shows that the enhanced EL display element has excellent aging and stability performance. Enhanced stability results in reduced need for aging the displays in the manufacturing phase. Further, the stability of the voltage-luminance dependency may be greatly advantageous from the display element driving scheme points of view.

It is to be noted that the present invention is not limited to the embodiments and examples above. Instead, the embodiments of the present invention can freely vary within the scope of the claims.

It will be understood that the benefits and advantages described above may relate to one embodiment or example or may relate to several embodiments or examples. The embodiments and examples are not limited to those that solve any or all of the stated problems or those that have any or all of the stated benefits and advantages. It will further be understood that reference to 'an' item refers to one or more of those items.

The term “comprising” is used in this specification to mean including the feature(s) or act(s) followed thereafter, without excluding the presence of one or more additional features or acts.

CLAIMS

1. An inorganic thin film electroluminescent display element (20), comprising a layer structure comprising:

- a first dielectric layer (23),
- a luminescent layer (26), comprising manganese doped zinc sulfide ZnS:Mn, on the first dielectric layer, and
- a second dielectric layer (27) on the luminescent layer,

characterized in that each of the first and the second dielectric layers (23, 27) comprises nanolaminate with alternating aluminum oxide Al_2O_3 and zirconium oxide ZrO_2 sub-layers (24, 25, 28, 29).

2. An electroluminescent display element (20) as defined in claim 1, wherein the luminescent layer (26) is formed by atomic layer deposition using maximum process temperature in the range of 150 to 270 °C, preferably 200 to 270 °C, most preferably 225 to 260°C, for example 250 °C.

3. An electroluminescent display element (20) as defined in claim 2, wherein the luminescent layer (26) is formed using diethylzinc, hydrogen sulfide, and Mn(thd)3 as precursors.

4. An electroluminescent display element (20) as defined in any of claims 1 to 3, wherein the layer structure is formed on a glass substrate (21) having a thickness of less than or equal to 250 µm, preferably less than or equal to 100 µm.

5. An electroluminescent display element (20) as defined in any of claims 1 to 4, wherein a ZrO_2 sub-

layer (25, 29) has a thickness in the range of 1 to 9 nm, preferably 3 to 7 nm, most preferably 4 to 6 nm.

6. An electroluminescent display element (20) as defined in any of claims 1 to 5, wherein an Al_2O_3 sub-layer (24, 28) has a thickness in the range of 1 to 15 nm, preferably 3 to 10 nm, most preferably 5 to 10 nm.

7. An electroluminescent display element (20) as defined in any of claims 1 to 6, wherein zirconium content of the first and/or the second dielectric layer (23, 27) is at least 10% by mass.

8. An electroluminescent display element (20) as defined in claim 7, wherein, in first and/or second dielectric layer (23, 27) where the zirconium content is at least 10%, aluminum content is at least 5% by mass.

9. An electroluminescent display element (20) as defined in any of claims 1 to 8, wherein the display element is transparent.

10. An electroluminescent display element (20) as defined in any of claims 1 to 9, wherein the first and the second dielectric layers (23, 27) are formed by atomic layer deposition.

11. A method for manufacturing an inorganic thin film electroluminescent display element, the method comprising forming a layer structure, said forming the layer structure comprising:

- forming a first dielectric layer (11),
- forming a luminescent layer (12), comprising manganese doped zinc sulfide ZnS:Mn, on the first dielectric layer, and

- forming a second dielectric layer (13) on the luminescent layer,

characterized in that each of the first and the second dielectric layers are formed so as to comprise nanolaminate with alternating aluminum oxide Al_2O_3 and zirconium oxide ZrO_2 sub-layers.

12. A method as defined in claim 11, wherein the luminescent layer is formed by atomic layer deposition using maximum process temperature in the range of 150 to 270 °C, preferably 200 to 270 °C, most preferably 225 to 260°C, for example 250 °C.

13. A method as defined in claim 12, wherein the luminescent layer is formed using diethylzinc, hydrogen sulfide, and Mn(thd)3 as precursors.

14. A method as defined in any of claims 11 to 13, wherein the layer structure is formed on a glass substrate having a thickness of less than or equal to 250 µm, preferably less than or equal to 100 µm.

15. A method as defined in any of claims 11 to 14, wherein a ZrO_2 sub-layer is formed so as to have a thickness in the range of 1 to 9 nm, preferably 3 to 7 nm, most preferably 4 to 6 nm.

16. A method as defined in any of claims 11 to 15, wherein an Al_2O_3 sub-layer is formed so as to have a thickness of in the range of 1 to 15 nm, preferably 3 to 10nm, most preferably 5 to 10 nm.

17. A method as defined in any of claims 11 to 16, wherein the first and/or the second dielectric layer is formed so as to have zirconium content of at least 10% by mass.

18. A method as defined in claim 17, wherein first and/or second dielectric layer being formed so as to have zirconium content of at least 10% by mass, is formed so as to have aluminum content of at least 5% by mass.

19. A method as defined in any of claims 11 to 18, wherein the display element is manufactured so as to be transparent.

20. A method as defined in any of claims 11 to 19, wherein the first and the second dielectric layers are formed by atomic layer deposition.

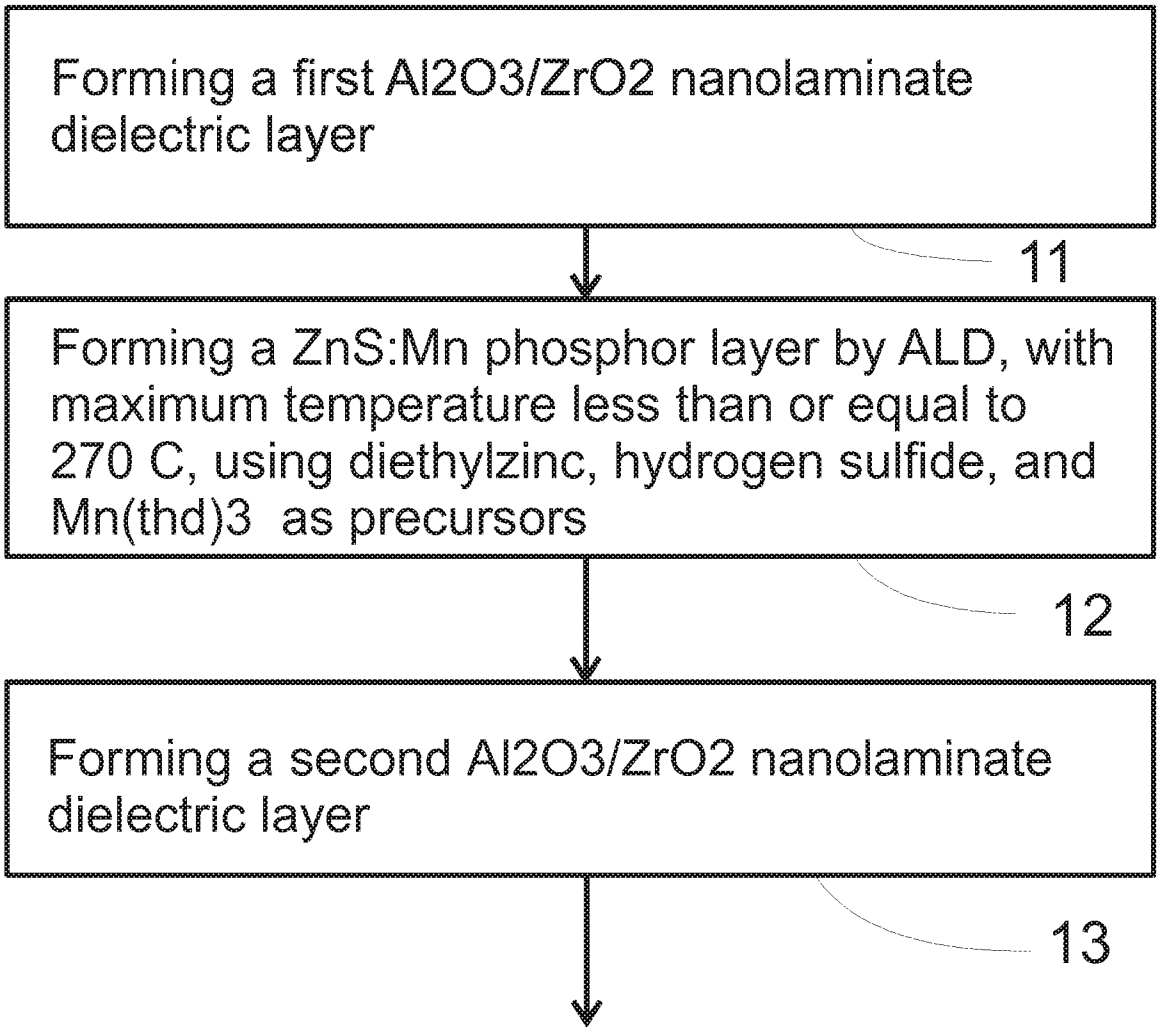

Forming a first Al2O3/ZrO2 nanolaminate dielectric layer
11
Forming a ZnS:Mn phosphor layer by ALD, with maximum temperature less than or equal to 270 C, using diethylzinc, hydrogen sulfide, and Mn(thd)3 as precursors
12
Forming a second Al2O3/ZrO2 nanolaminate dielectric layer
13

Fig. 1

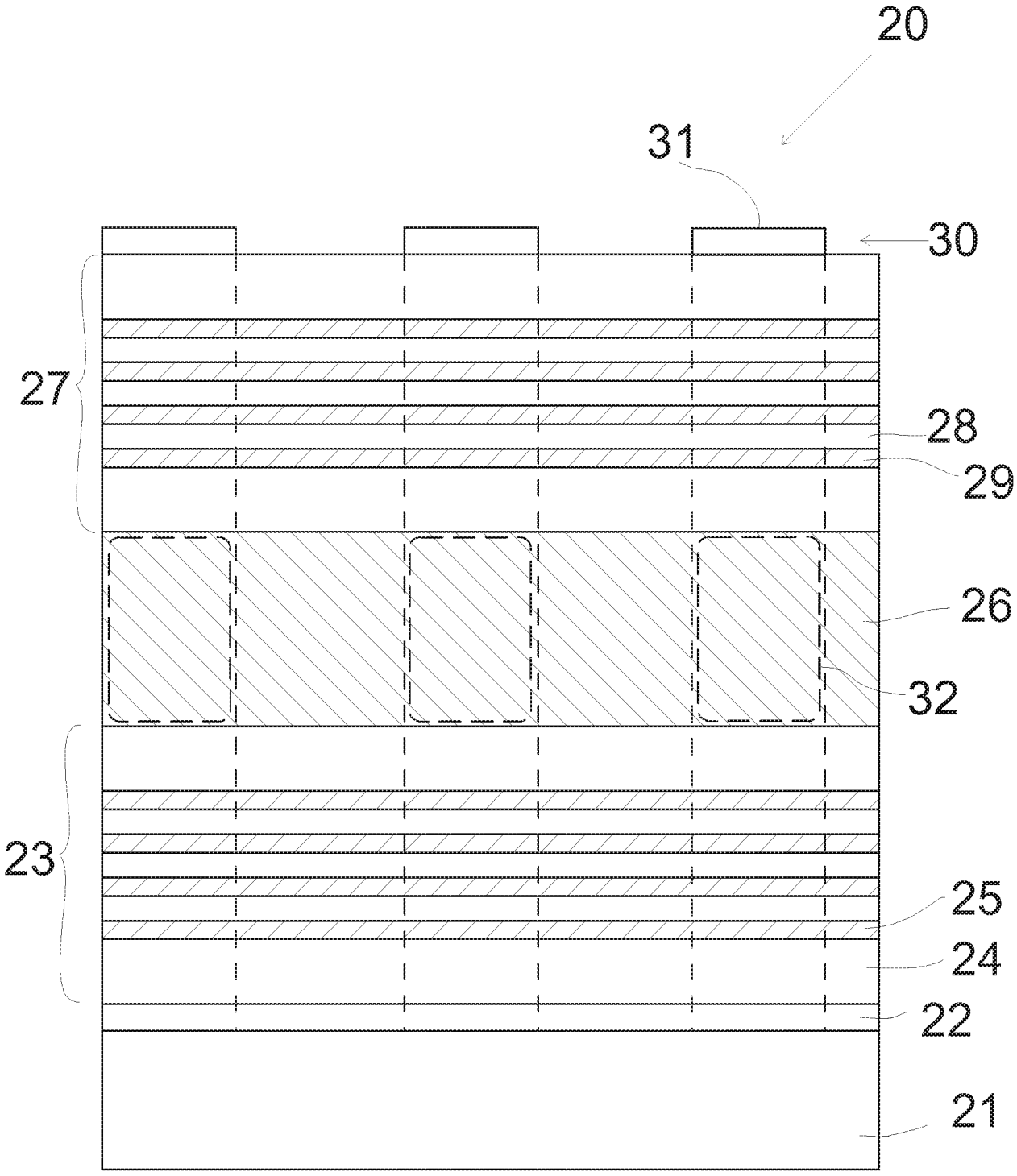
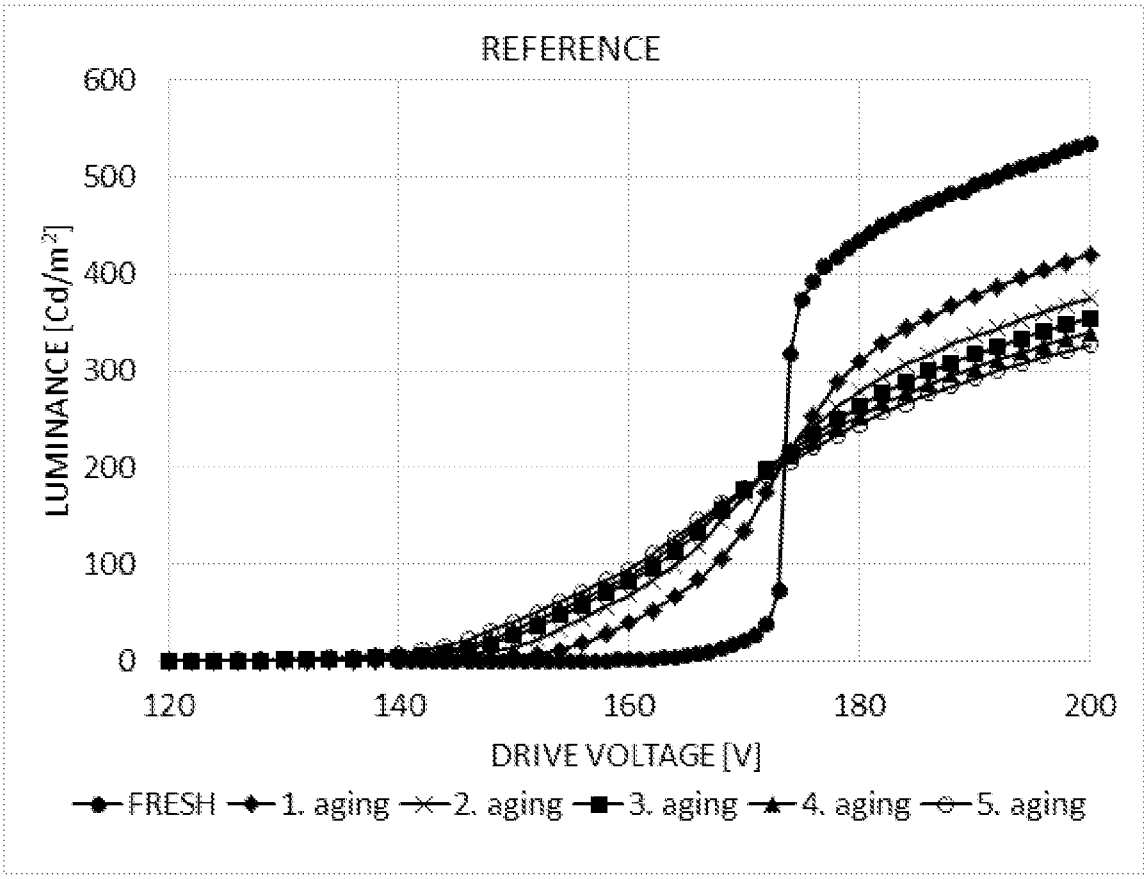
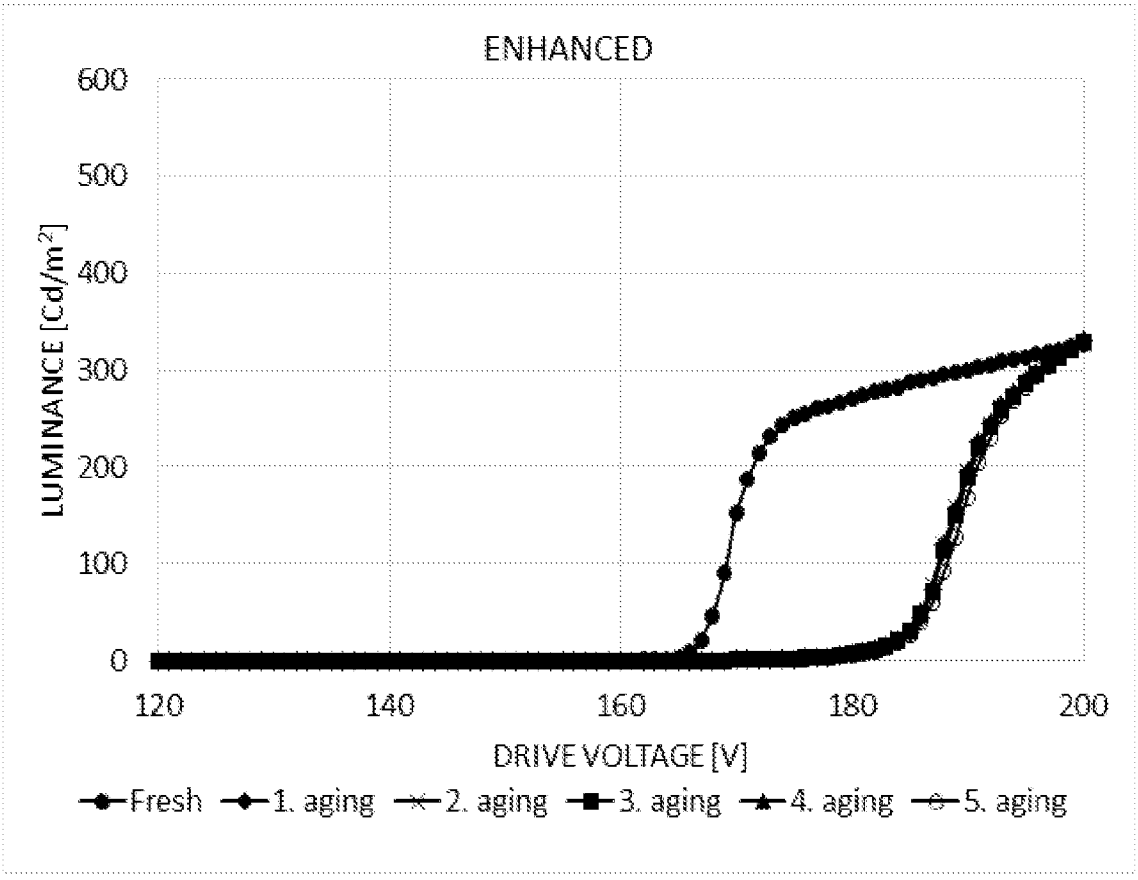


Fig. 2 (not in scale)


REFERENCE
600
500
400
300
200
100
0
LUMINANCE [Cd/m²]
120
140
160
180
200
DRIVE VOLTAGE [V]
FRESH
1. aging
2. aging
3. aging
4. aging
5. aging

a)


ENHANCED
600
500
400
300
200
100
0
LUMINANCE [Cd/m²]
120
140
160
180
200
DRIVE VOLTAGE [V]
Fresh
1. aging
2. aging
3. aging
4. aging
5. aging

b)

Fig. 3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2017/050608

A. **CLASSIFICATION OF SUBJECT MATTER**

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: C09K, C23C, H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

FI, SE, NO, DK

Electronic data base consulted during the international search (name of data base, and, where practicable, search terms used)

EPODOC, EPO-Internal full-text databases, WPIAP, XPI3E, XPESP, COMPDX, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2007099883 A1 (SEMICONDUCTOR ENERGY LAB [JP]) 07 September 2007 (07.09.2007) abstract; paragraphs [0033], [0045]-[0046], [0054], and [0064]-[0066]; figures 1 and 2A-2C	1, 4-11, 14-20
X	US 2005064236 A1 (LIM JUNG WOOK [KR] et al.) 24 March 2005 (24.03.2005) abstract; paragraphs [0012]-[0013], [0024], [0026], [0033], [0037], and [0044]; figure 1	1, 9-11, 19-20
X	US 2003152804 A1 (MIURA NOBORU [JP] et al.) 14 August 2003 (14.08.2003) paragraphs [0015]-[0016], [0025], [0060], [0065], [0070], and [0072]; figure 1	1, 9, 11, 19

☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 December 2017 (20.12.2017)	21 December 2017 (21.12.2017)

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2017/050608

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6207302 B1 (SUGIURA KAZUHIKO [JP] et al.) 27 March 2001 (27.03.2001) claims 10 and 15-17; column 1, lines 15-20; column 2, lines 44-58; column 4, lines 27-49; column 5, lines 43-49; column 7, lines 15-26; figures 1 and 5	1, 11
X	US 6358632 B1 (DICKEY ERIC R [US] et al.) 19 March 2002 (19.03.2002) claims 1, 6, and 18-20; column 1, lines 4-7; column 8, line 63 – column 9, line 55; column 10, line 46 - column 11, line 14; figure 6	1, 11

INTERNATIONAL SEARCH REPORT
Information on Patent Family Members

International application No.
PCT/FI2017/050608

Patent document cited in search report	Publication date	Patent family members(s)	Publication date
WO 2007099883 A1	07/09/2007	JP 2007262391 A	11/10/2007
		KR 20080099870 A	13/11/2008
		US 2007205428 A1	06/09/2007
US 2005064236 A1	24/03/2005	US 7498053 B2	03/03/2009
		KR 20050028980 A	24/03/2005
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		JP 2003238953 A	27/08/2003
US 6207302 B1	27/03/2001	JP H10308283 A	17/11/1998
US 6358632 B1	19/03/2002	CA 2284031 A1	10/05/2000
		JP 2000173768 A	23/06/2000

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI2017/050608

CLASSIFICATION OF SUBJECT MATTER

IPC
H05B 33/22 (2006.01)
H05B 33/20 (2006.01)
H05B 33/14 (2006.01)
C23C 16/40 (2006.01)
C09K 11/57 (2006.01)
C09K 11/08 (2006.01)
C23C 16/455 (2006.01)

专利名称(译)	无机TFEL显示器元件及其制造		
公开(公告)号	EP3508035A4	公开(公告)日	2020-03-11
申请号	EP2017845591	申请日	2017-08-30
[标]申请(专利权)人(译)	本尼克公司		
申请(专利权)人(译)	倍耐克公司OY		
当前申请(专利权)人(译)	倍耐克公司OY		
[标]发明人	SEPPANEN HELI TURKULAINEN TOMMY HARKONEN KARI		
发明人	SEPPÄNEN, HELI TURKULAINEN, TOMMY HÄRKÖNEN, KARI		
IPC分类号	H05B33/22 H05B33/20 H05B33/14 C23C16/40 C09K11/57 C09K11/08 C23C16/455		
CPC分类号	C23C16/306 C23C16/403 C23C16/405 C23C16/45531 H05B33/22 C09K11/574 C23C16/45525 H05B33/145		
优先权	2016005652 2016-09-02 FI		
其他公开文献	EP3508035A1		
外部链接	Espacenet		

摘要(译)

一种用于制造无机薄膜电致发光显示元件的方法，包括形成层结构，所述形成层结构包括形成第一电介质层（11）；以及 在第一介电层上形成包括锰掺杂的硫化锌ZnS：Mn的发光层（12），并在发光层上形成第二介电层（13）。 形成第一介电层和第二介电层中的每一个，以使其包括具有交替的氧化铝Al 2 O 3和氧化锆ZrO 2子层的纳米层压体。