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(54) **Organic electroluminescent display device and driving method thereof**

Organische Elektrolumineszenzanzeigevorrichtung und Verfahren zu ihrer Ansteuerung

Dispositif d'affichage électroluminescent organique et son procédé de commande

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(73) Proprietor: **LG Display Co., Ltd.**
Youngdungpo-gu,
Seoul (KR)

(72) Inventor: **Kim, Seong-Gyun**
Seoul 151-011 (KR)

(74) Representative: **Viering, Jentschura & Partner mbB**
Patent- und Rechtsanwälte
Am Brauhaus 8
01099 Dresden (DE)

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- **PATENT ABSTRACTS OF JAPAN vol. 2003, no. 12, 5 December 2003 (2003-12-05) & JP 2004 117441 A (SONY CORP), 15 April 2004 (2004-04-15) -& JP 2004 117441 A (SONY CORP) 15 April 2004 (2004-04-15)**

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Description

Technical Field

[0001] The present application relates to an organic electroluminescent display device, and more particularly, to an organic electroluminescent display (OELD) device and a method of driving an OELD device.

BACKGROUND

[0002] Display devices have employed cathode-ray tubes (CRT) to display images. However, various types of flat panel displays, such as liquid crystal display (LCD) devices, plasma display panel (PDP) devices, field emission display (FED) devices, and electroluminescent display (ELD) devices, are currently being developed as substitutes for the CRT. Among these various types of flat panel displays, LCD devices have advantages of thin profile and low power consumption, but have disadvantages of using a backlight unit because they are non-luminescent display devices. However, as organic electroluminescent display (OELD) devices are self-luminescent display devices, they are operated at low voltages and have a thin profile. Further, the OELD devices have advantages of fast response time, high brightness and wide viewing angles.

[0003] In a related art OELD shown in FIG. 1, a plurality of gate lines G1, G2, ..., and Gm are extended along a first direction, and a plurality of data lines D1, D2, ..., and Dn are extended along a second direction perpendicular to the first direction. The gate and data lines define respective pixel regions arranged in a matrix form. In each pixel region, a switching thin film transistor P1, a storage capacitor C1, a driving thin film transistor P2 and an organic electroluminescent diode OED are disposed. The switching and driving thin film transistors P1 and P2 include p-type thin film transistors.

[0004] Gate electrodes of the switching thin film transistors P1 are connected to the respective gate lines G1, G2, ..., and Gm, and the source electrodes of the switching thin film transistors P1 are connected to the respective data lines D1, D2, ..., and Dn. A first electrode of the storage capacitor C1 is connected to a drain electrode of the switching thin film transistor P1, and a second electrode of the storage electrode C1 is connected to a power terminal Vdd. Source electrodes of the driving thin film transistor P2 are connected to the power terminal Vdd, the gate electrodes of the driving thin film transistors P2 are connected to the respective drain electrodes of the switching thin film transistors P1, and drain electrodes of the driving thin film transistors P2 are connected to the respective first electrodes of the organic electroluminescent diodes OED. The second electrode of the organic electroluminescent diode OED is connected to a ground terminal.

[0005] An "on" gate signal is applied to a selected gate line G1, G2, ..., or Gm, and the switching thin film transistor P1 connected to the selected gate line G1, G2, ..., or Gm is turned on. When the switching thin film transistor P1 is turned on, a data signal is charged on the storage capacitor C1. The charged data signal is applied to the gate electrode of the driving thin film transistor P2 and adjusts an "on" current in the driving thin film transistor P2. In response to the "on" current, the organic electroluminescent diode OED emits light. In this manner, the respective organic electroluminescent diodes "OED" emit light when the respective gate lines G1, G2,..., and Gm are sequentially selected.

[0006] As the size of the OELD device increases, the gate and data lines have longer paths. Accordingly, a resistance-capacitance (RC) delay of the signal lines having long paths increases, and distortion of display images occurs.

[0007] One means of solving the problem of distortion of the display images, where the display area is subdivided and each of the subdivided areas is operated by a separate driving circuit, has been suggested.

[0008] FIG. 2 is a conceptual view of an OELD device having a subdivided display area. A display area is divided into a first to a sixth six sub-area, S1-S6. The first to sixth sub-areas are operated independently from one another by using corresponding data driving circuits S1-DATA through S6-DATA and corresponding gate driving circuits S1-SCAN through S6-SCAN. Although not shown in FIG. 2, gate driving circuits for the second and fifth sub-areas S2 and S5 are also provided.

[0009] A driving circuit control portion (not shown) controls the driving circuits S1-DATA through S6-DATA and S1-SCAN through S6-SCAN. Data signals are supplied to the driving circuit control portion having a memory device, and the memory device stores the data signals. Data signals of one frame for one display image are divided into six arrays corresponding to the six sub-areas S1 through S6. The driving circuit control portion outputs each array of the data signals to the corresponding data driving circuits S1-DATAthrough S6-DATA. Each data driving circuit S1-DATA through S6-DATA simultaneously outputs the corresponding array of the data signals of one frame to the corresponding sub-areas S1 through S6. In each of the sub-areas S1 through S6, the data signals are applied to pixel regions along the data line sequentially according to scanning the gate lines of each sub-area S1 through S6 by each gate driving circuit S1-SCAN to S6-SCAN, resulting in the display of an image.

[0010] This method of driving a subdivided display area is applicable to an LCD device, but problematic for an OELD device having a fast response time. In particular, method is problematic for the large sized OELD device, as a display image is displayed discontinuously at boundary portions between an upper sub-area and a lower sub-area.

[0011] FIG. 3 is a progressive view illustrating a method of driving a bifurcated display area of an OELD device, and FIG. 4 is a block diagram illustrating a transfer flow of data signals in a driving circuit control portion of an

OELD device of FIG. 3.

[0012] As shown in FIGs. 3 and 4, a display area of the OELD device includes an upper sub-area U and a lower sub-area L. A moving image moves from a first position A to a second position B. In FIG. 3, movement of the moving image is shown sequentially with four steps, ST1 through ST4. Although not shown in FIG. 3, the upper sub-area U is operated by an upper data driving circuit and an upper gate driving circuit, and the lower sub-area L is operated by a lower data driving circuit and a lower gate driving circuit. Each of the sub-areas is scanned from the top to the bottom thereof.

[0013] A driving circuit control portion 10 is supplied with data signals of one frame and simultaneously outputs divided upper and lower data signal arrays of one frame into corresponding upper and lower data driving circuits.

[0014] In detail, the driving circuit control portion 10 is supplied with data signals of a $(n-1)^{th}$ frame, and the data signals of the $(n-1)^{th}$ frame are divided into an upper data signal array and an lower data signal array. The upper and lower data signal arrays of the $(n-1)^{th}$ frame are outputted to the upper and lower data driving circuits and supplied to the upper and lower sub-areas U and L, respectively. Subsequently, data signals of a next frame, i.e., a n^{th} frame, are supplied to the driving circuit control potion 10, divided and outputted to the upper and lower sub-areas U and L.

[0015] The moving image of the first position A is displayed when the upper and lower data arrays of the $(n-1)^{th}$ frame are written on the entire upper and lower sub-areas U and L, respectively. Then, in the first step ST1 corresponding to a first quarter of the n^{th} frame period, an upper portion of the moving image of the lower sub-area L moves to the second position B, but the other portions of the moving image do not yet move. Then, in the second step ST2, between the first quarter and a second quarter of the n^{th} frame period, a lower portion of the moving image of the lower sub-area L moves to the second position B. Then, in the third step ST3, the second quarter and a third quarter of the n^{th} frame period, an upper portion of the moving image of the upper sub-area U moves to the second position B. Then, in the fourth step ST4, during the third quarter and a fourth quarter of the n^{th} frame period, a lower portion of the moving image of the upper sub-area U moves to the second position B.

[0016] When the display area is divided into the upper and lower sub-areas and the two sub-areas are operated simultaneously with the data signals of the same frame and independently from each other, the moving image displayed across the boundary portion between the upper and lower sub-areas moves unnaturally because of the fast response time of the OELD device. Therefore, an observer perceives an unnatural movement of the moving image across the boundary, as if the display image of the present frame overlaps that of the previous frame. JP 3 043783 A discloses a display method for displaying an image in motion normally by arranging plural display devices in a matrix and displaying a video image which is one field delayed behind the display screen of an upper display device on the display screen of a lower device.

SUMMARY

[0017] A method of driving a display device is disclosed as set out in claim 1.

[0018] In another aspect, a display device as set out in claim 4 is disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019]

FIG. 1 is a circuit diagram of an OELD device according to the related art;

FIG. 2 is a conceptual view of an OELD device having a subdivided display area according to the related art;

FIG. 3 is a progressive view illustrating a method of driving a bifurcated display area of an OELD device according to the related art;

FIG. 4 is a block diagram illustrating a transfer flow of data signals in a driving circuit control portion of an OELD device of FIG. 3;

FIG. 5 is a progressive view illustrating a method of driving a bifurcated display area of the OELD device according to an exemplary embodiment;

FIG. 6 is a view illustrating a OELD device according to an exemplary embodiment; and

FIG. 7 is a block diagram illustrating a transfer flow of data signals in a driving circuit control portion of an OELD device of FIG. 6.

DETAILED DESCRIPTION

[0020] Exemplary embodiments may be better understood with reference to the drawings, but these examples are not intended to be of a limiting nature. Like numbered elements in the same or different drawings perform equivalent functions.

[0021] As shown in FIGs. 5 to 7, a display area of the OELD includes an upper sub-area U and a lower sub-area L. Upper and lower data signals are simultaneously written on upper and lower sub-areas U and L, respectively, from a top side to a bottom side thereof. In other words, gate lines, which are extended along a first direction, in each of the upper and lower sub-areas U and L are scanned from the top side to the bottom side along a second direction along which the data lines extend.

Accordingly, the upper and lower data signals are simultaneously written on the upper and lower sub-areas U and L, respectively, from the top side to the bottom side.

[0022] In FIG. 5, movement of the moving image is shown in four sequential steps, ST11 through ST 14. The upper sub-area U is operated by an upper data driving circuit U-DATA and an upper gate driving circuit U-SCAN, and the lower sub-area L is operated by a lower data driving circuit L-DATA and a lower gate driving circuit L-SCAN.

[0023] The upper and lower sub-areas U and L simultaneously display corresponding upper and lower images according to a timing sequence, and thus one display image is displayed during one frame period. In particular, during a first frame period, while upper data signal array of a n^{th} frame are written on the upper sub-area U, lower data signal array of a $(n-1)^{th}$ frame are written on the lower sub-area L. In this manner, writing of the lower data signal array of a present frame on the lower sub-area L and the upper image data signal array of a next frame on the upper sub-area U is conducted continuously.

[0024] In more detail, in the first step ST11 between a start point and a third quarter of the first frame period, three quarters of the upper data signal arrays of the n^{th} frame are written on the upper sub-area U and three quarters of the lower data signal arrays of the $(n-1)^{th}$ frame are written on the lower sub-area L. Accordingly, three quarters of the upper sub-area U are updated so that an upper portion of the moving image of the upper sub-area U moves from the first position A to the second position B, and three quarters of the lower sub-area L are updated so that the moving image of the lower sub-area L are displayed at the first position A.

[0025] Then, in the second step ST12, between the third quarter and a fourth quarter of the first frame period, a residual fourth quarter of the upper data signal arrays of the n^{th} frame are written on the upper sub-area U and a residual fourth quarter of the lower data signal arrays of the $(n-1)^{th}$ frame are written on the lower sub-area L. Accordingly, a residual fourth quarter of the upper sub-area U is updated so that a lower portion of the moving image of the upper sub-area U moves from the first position A to the second position B, and a residual fourth quarter of the lower sub-area L is updated so that the moving image of the lower sub-area L still remains at the first position A.

[0026] In other words, during the first and second steps ST11 and ST12, all of the upper data signal arrays of the n^{th} frame are written on the entire upper sub-area U and all of the lower data signal arrays of the $(n-1)^{th}$ frame are written on the entire lower sub-area L. Accordingly, the entire upper sub-area U are updated so that the moving image of the upper sub-area U moves from the first position A to the second position B, and the entire lower sub-area L is updated so that the moving image of the lower sub-area L is displayed at the first position A.

[0027] Subsequently, in the third step ST13 , between a start point and a first quarter of a second frame period, a first quarter of the upper data signal arrays of a $(n+1)^{th}$ frame are written on the upper sub-area U and a first quarter of the lower data signal arrays of the n^{th} frame are written on the lower sub-area L. Accordingly, a first quarter of the upper sub-area U is updated so that the moving image of the upper sub-area U remains at the second position B, and a first quarter of the lower sub-area L is updated so that an upper portion of the moving image of the lower sub-area L moves from the first position A to the second position B.

[0028] Then, in the fourth step ST 14, between the first quarter and a second quarter of the second frame period, a second quarter of the upper data signal arrays of the $(n+1)^{th}$ frame are written on the upper sub-area U and a second quarter of the lower data signal arrays of the n^{th} frame is written on the lower sub-area L. Accordingly, a second quarter of the upper sub-area U is updated so that the moving image of the upper sub-area U remains at the second position B, and a second quarter of the lower sub-area L is updated so that an lower portion of the moving image of the lower sub-area L moves from the first position A to the second position B.

[0029] In other words, during the third and fourth steps ST 13 and ST14, a first half of the upper data signal array of the $(n+1)^{th}$ frame is written on the half upper sub-area U and a first half of the lower data signal array of the n^{th} frame is written on the half lower sub-area L. Accordingly, the half upper sub-area U is updated so that the moving image of the upper sub-area U is still displayed at the second position B, and the half lower sub-area L is updated so that the moving image of the lower sub-area L moves from the first position A to the second position B.

[0030] As a result, during the first to fourth steps ST11 to ST14, the moving image across the boundary between the upper and lower sub-areas U and L moves from the first position A to the second position B without unnaturalness, by supplying the upper sub-area U with the data signals which are next to the data signals supplied to the lower sub-area L.

[0031] To operate the display area described above, the OELD device includes a display panel 100, gate driving circuits U-SCAN and L-SCAN, data driving circuits U-DATA and L-DATA and a driving circuit control portion 120. In the display panel 100, the display area is divided into the upper and lower sub-areas U and L. The upper sub-area U is operated by the upper gate driving circuit U-SCAN and the upper data driving circuit U-DATA, and the lower sub-area L is operated by the lower gate driving circuit L-SCAN and the lower data driving circuit L-DATA. Accordingly, the upper and lower sub-areas U and L are displayed simultaneously and operated independently from each other.

[0032] The driving circuit control portion 120 includes a storing portion 122. The driving circuit control potion 120 is supplied with data signals from a data supply portion 110 such as a video card. Upper and lower data signal arrays to display one display image at the same time are sequentially stored in the storing portion 122

and outputted to the corresponding data driving circuits U-SCAN and L-SCAN, respectively. The upper and lower data signal arrays correspond to the upper data signal array of the $(n+1)^{th}$ frame and the lower data signal array of the n^{th} frame, respectively.

[0033] The storing portion 122 may have first and second memory devices to store the upper and lower data signal arrays. For example, the storing portion 122 may include a first memory device 122a storing the upper and lower data signal arrays to display a present display image, and a second memory device 122b storing the upper and lower data signal arrays to display a next display image. Each of the first and second memory devices 122a and 122b may include an upper sub-memory device and a lower sub-memory device storing the upper and lower data signal arrays, respectively. The upper sub-memory device stores the upper data signal array of a frame which is next to a frame of the lower data signal array stored in the lower sub-memory device. When the upper and lower data signal arrays of the first memory device 122a have been entirely output, the upper and lower data signal arrays of the second memory device 122b are transferred to and stored in the first memory device 122a. In this manner, the first and second memory devices 122a and 122b repeatedly store and output the upper and lower data signal arrays. In addition, a plurality of first memory devices 122a may be used. The plurality of first memory devices 122a may be arranged in parallel and sequentially output the upper and lower data signal arrays to display the corresponding display images.

[0034] In addition, the storing portion 122 may include a plurality of third memory devices each storing data signals of one frame. Among data signals of one frame in the third memory device, the upper and lower data signal arrays are abstracted and stored in the second memory device 122b. It should be understood that the storing portion 122 may have different structures to output the upper and lower data signal arrays to the upper and lower data driving circuits U-DATA and L-DATA, respectively.

[0035] In the exemplary embodiment the OELD device is used as an example. However, it should be understood that the present invention is applicable to other display devices having subdivided areas independently operable.

[0036] In the exemplary embodiment the two sub-areas are used as an example. However, it should be understood that the present invention is applicable to a plurality of sub-areas and corresponding gate and data driving circuits, as similar to the display device of FIG. 2.

Claims

1. A method of driving a display device, comprising:

storing upper and lower data signal arrays to display a present display image in a first memory device (122a);

storing upper and lower data signal arrays to display a next display image in a second memory device (122b),

wherein each of the first and second memory devices (122a, 122b) includes an upper sub-memory device and a lower sub-memory device storing the upper and lower data signal arrays, respectively, wherein the upper sub-memory device of the first memory device (122a) stores the upper data signal array of an n^{th} frame and the lower sub-memory device of the first memory device (122a) stores the lower data signal array of an $(n-1)^{th}$ frame, and
wherein the upper sub-memory device of the second memory device (122b) stores the upper data signal array of an $(n+1)^{th}$ frame and the lower sub-memory device of the second memory device (122b) stores the lower data signal array of the n^{th} frame;

outputting the upper data signal array of the n^{th} frame from the first memory device (122a) to an upper display area (U) of a display panel (100) during a first frame period;
outputting the lower data signal array of the $(n-1)^{th}$ frame from the first memory device (122a) to a lower display area (L) of the display panel (100) during the first frame period;
transferring the upper data signal array of the $(n+1)^{th}$ frame and the lower data signal array of the n^{th} frame from the second memory device (122b) to the first memory device (122a) and storing the upper data signal array of the $(n+1)^{th}$ frame and the lower data signal array of the n^{th} frame in the first memory device (122a), when the upper data signal array of the n^{th} frame and the lower data signal array of the $(n-1)^{th}$ frame have been entirely output;
storing data signals of one frame in each of a plurality of third memory devices; and
abstracting the upper and lower data signal arrays among the data signals stored in the third memory devices and storing the upper and lower data signal arrays in the second memory device (122b), wherein the first and second memory devices (122a, 122b) repeatedly store and output the upper and lower data signal arrays.

2. The method according to claim 1,
wherein each of the upper and lower data signal arrays are outputted in rows from an upper side to a lower side of each of the upper display area (U) and the lower display area (L).

3. The method according to claim 1,
wherein the display panel (100) is an organic elec-

troluminescent display panel.

4. A display device, comprising:

a display panel (100) having an upper display area (U) and a lower display area (L); and
a driving circuit control portion (120) comprising:

a first memory device (122a) including an upper sub-memory device and a lower sub-memory device;
a second memory device (122b) including an upper sub-memory device and a lower sub-memory device;
a plurality of third memory devices each storing data signals of one frame;

wherein the upper sub-memory device of the first memory device (122a) stores the upper data signal array of an n^{th} frame and the lower sub-memory device of the first memory device (122a) stores the lower data signal array of an $(n-1)^{th}$ frame, and
wherein the upper sub-memory device of the second memory device (122b) stores the upper data signal array of an $(n+1)^{th}$ frame and the lower sub-memory device of the second memory device (122b) stores the lower data signal array of the n^{th} frame;

wherein the driving circuit control portion (120) is configured to:

supply the upper data signal array of the n^{th} frame from the first memory device (122a) to the upper display area (U) during a first frame period and to supply the lower data signal array of the $(n-1)^{th}$ frame from the first memory device (122a) to the lower display area (L) during the first frame period;
transfer the upper data signal array of the $(n+1)^{th}$ frame and the lower data signal array of the n^{th} frame from the second memory device (122b) to the first memory device (122a) and store the upper data signal array of the $(n+1)^{th}$ frame and the lower data signal array of the n^{th} frame in the first memory device (122a), when the upper data signal array of the n^{th} frame and the lower data signal array of the $(n-1)^{th}$ frame have been entirely output; and
subsequently,
supply the first data signal array of the $(n+1)^{th}$ frame from the first memory device (122a) to the upper display area (U) during a second frame period, which is immediately subsequent to the first frame period, and supply the second data signal array of the n^{th}frame from the first memory device (122a) to the lower display area (L) during the second frame period;
abstract the upper and lower data signal arrays among the data signals stored in the third memory devices and store the upper and lower data signal arrays in the second memory device (122b).

5. The device according to claim 4, further comprising a plurality of gate lines in the upper display area (U) and the lower display area (L), the plurality of gate lines in each display area scanned from an upper side to a lower side of the upper display area (U) and the lower display area (L).

6. The device according to claim 4,
wherein the display panel (100) is an organic electroluminescent display panel.

Patentansprüche

1. Ein Verfahren zum Ansteuern einer Anzeigevorrichtung, aufweisend:

Speichern von oberen und unteren Datensignal-Arrays zum Anzeigen eines ersten Anzeigebildes in einer ersten Speichervorrichtung (122a) ;
Speichern von oberen und unteren Datensignal-Arrays zum Anzeigen eines nächsten Anzeigebildes in einer zweiten Speichervorrichtung (122b);

wobei jede der ersten und der zweiten Speichervorrichtung (122a, 122b) eine obere Unter-Speichervorrichtung und eine untere Unter-Speichervorrichtung aufweist, die die oberen bzw. unteren Datensignal-Arrays speichern,
wobei die obere Unter-Speichervorrichtung der ersten Speichervorrichtung (122a) das obere Datensignal-Array eines n-ten Rahmens speichert und die untere Unter-Speichervorrichtung der ersten Speichervorrichtung (122a) das untere Datensignal-Array eines (n-1)-ten Rahmens speichert, und
wobei die untere Unter-Speichervorrichtung der zweiten Speichervorrichtung (122b) das obere Datensignal-Array eines (n+1)-ten Rahmens speichert und die untere Unter-Speichervorrichtung der zweiten

Speichervorrichtung (122b) das untere Datensignal-Array des n-ten Rahmens speichert;

Ausgeben des oberen Datensignal-Arrays des n-ten Rahmens aus der ersten Speichervorrichtung (122a) an einen oberen Anzeigebereich (U) eines Anzeigepanels (100) während einer ersten Rahmenperiode;
Ausgeben des unteren Datensignal-Arrays des (n-1)-ten Rahmens aus der ersten Speichervorrichtung (122a) an einen unteren Anzeigebereich (L) des Anzeigepanels (100) während der ersten Rahmenperiode;
Übertragen des oberen Datensignal-Arrays des (n+1)-ten Rahmens und des unteren Datensignal-Arrays des n-ten Rahmens aus der zweiten Speichervorrichtung (122b) zu der ersten Speichervorrichtung (122a) und Speichern des oberen Datensignals-Arrays des (n+1)-ten Rahmens und des unteren Datensignal-Arrays des n-ten Rahmens in der ersten Speichervorrichtung (122a), wenn das obere Datensignal-Array des n-ten Rahmens und das untere Datensignal-Array des (n-1)-ten Rahmens vollständig ausgegeben wurden;
Speichern von Datensignalen eines Rahmens in jedem von einer Mehrzahl von dritten Speichervorrichtungen; und
Herausziehen der oberen und unteren Datensignal-Arrays aus den in den dritten Speichervorrichtungen gespeicherten Datensignalen und Speichern der oberen und unteren Datensignal-Arrays in der zweiten Speichervorrichtung (122b),
wobei die ersten und zweiten Speichervorrichtungen (122a, 122b) wiederholt die oberen und unteren Datensignal-Arrays speichern und ausgeben.

2. Das Verfahren gemäß Anspruch 1,
wobei jedes des oberen und des unteren Datensignal-Arrays in Reihen von einer oberen Seite zu einer unteren Seite von jeweils dem oberen Anzeigebereich (U) und dem unteren Anzeigebereich (L) ausgegeben werden.

3. Das Verfahren gemäß Anspruch 1,
wobei das Anzeigepanel (100) ein organisches Elektrolumineszenz-Anzeigepanel ist.

4. Eine Anzeigevorrichtung, aufweisend:

ein Anzeigepanel (100), das einen oberen Anzeigebereich (U) und einen unteren Anzeigebereich (L) aufweist; und
einen Ansteuerungsschaltkreis-Steuerungsbereich (120), aufweisend:

eine erste Speichervorrichtung (122a), die eine obere Unter-Speichervorrichtung und eine untere Unter-Speichervorrichtung aufweist;
eine zweite Speichervorrichtung (122b), die eine obere Unter-Speichervorrichtung und eine untere Unter-Speichervorrichtung aufweist;
eine Mehrzahl von dritten Speichervorrichtungen, die jeweils Datensignale eines Rahmens speichern;

wobei die obere Unter-Speichervorrichtung der ersten Speichervorrichtung (122a) das obere Datensignal-Array eines n-ten Rahmens speichert und die untere Unter-Speichervorrichtung der ersten Speichervorrichtung (122a) das untere Datensignal-Array eines (n-1)-ten Rahmens speichert, und
wobei die obere Unter-Speichervorrichtung der zweiten Speichervorrichtung (122b) das obere Datensignal-Array eines (n+1)-ten Rahmens speichert und die untere Unter-Speichervorrichtung der zweiten Speichervorrichtung (122b) das untere Datensignal-Array des n-ten Rahmens speichert;

wobei der Ansteuerungsschaltkreis-Steuerungsbereich (120) eingerichtet ist zum:

Zuführen des oberen Datensignal-Arrays des n-ten Rahmens von der ersten Speichervorrichtung (122a) zu dem oberen Anzeigebereich (U) während einer ersten Rahmenperiode und zum Zuführen des unteren Datensignal-Arrays des (n-1)-ten Rahmens von der ersten Speichervorrichtung (122a) zu dem unteren Anzeigebereich (L) während der ersten Rahmenperiode;
Übertragen des oberen Datensignal-Arrays des (n+1)-ten Rahmens und des unteren Datensignal-Arrays des n-ten Rahmens aus der zweiten Speichervorrichtung (122b) zu der ersten Speichervorrichtung (122a) und Speichern des oberen Datensignals-Arrays des (n+1)-ten Rahmens und des unteren Datensignal-Arrays des n-ten Rahmens in der ersten Speichervorrichtung (122a), wenn das obere Datensignal-Array des n-ten Rahmens und das untere Datensignal-Array des (n-1)-ten Rahmens vollständig ausgegeben wurden; und
danach,
Zuführen des ersten Datensignal-Arrays des (n+1)-ten Rahmens von der ersten Speichervorrichtung (122a) zu dem oberen

Anzeigebereich (U) während einer zweiten Rahmenperiode, die direkt auf die erste Rahmenperiode nachfolgt, und Zuführen des zweiten Datensignal-Arrays des n-ten Rahmens von der ersten Speichervorrichtung (122a) zu dem unteren Anzeigebereich (L) während der zweiten Rahmenperiode;

Herausziehen der oberen und unteren Datensignal-Arrays aus den in den dritten Speichervorrichtungen gespeicherten Datensignalen und Speichern der oberen und unteren Datensignal-Arrays in der zweiten Speichervorrichtung (122b).

5. Die Vorrichtung gemäß Anspruch 4, ferner aufweisend
eine Mehrzahl von Gate-Leitungen in dem oberen Anzeigebereich (U) und dem unteren Anzeigebereich (L), wobei die Mehrzahl von Gate-Leitungen in jedem Anzeigebereich von einer oberen Seite zu einer unteren Seite des oberen Anzeigebereichs (U) und des unteren Anzeigebereichs (L) abgetastet werden.

6. Die Vorrichtung gemäß Anspruch 4,
wobei das Anzeigepanel (100) ein organisches Elektrolumineszenz-Anzeigepanel ist.

Revendications

1. Procédé de commande d'un dispositif d'affichage comprenant :

le stockage de matrices de signaux de données supérieures et inférieures pour afficher une image d'affichage présente dans un premier dispositif de mémoire (122a) ;
le stockage de matrices de signaux de données supérieures et inférieures pour afficher une image d'affichage suivante dans un deuxième dispositif de mémoire (122b),

chacun desdits premier et deuxième dispositifs de mémoire (122a, 122b) comprenant un sous-dispositif de mémoire supérieur et un sous-dispositif de mémoire inférieur stockant respectivement les matrices de signaux de données supérieures et inférieures,
le sous-dispositif de mémoire supérieur du premier dispositif de mémoire (122a) stocke la matrice de signaux de données supérieure d'une n-ième trame et le sous-dispositif de mémoire inférieur du premier dispositif de mémoire (122a) stocke la matrice de signaux de données inférieure d'une (n-1)-ième trame et
le sous-dispositif de mémoire supérieur du deuxième dispositif de mémoire (122b) stocke la matrice de signaux de données supérieure d'une (n+1)-ième trame et le sous-dispositif de mémoire inférieur du deuxième dispositif de mémoire (122b) stocke la matrice de signaux de données inférieure de la n-ième trame ;

l'envoi de la matrice de signaux de données supérieure de la n-ième trame du premier dispositif de mémoire (122a) vers une zone d'affichage supérieure (U) d'un panneau d'affichage (100) pendant une première période de trame ;
l'envoi de la matrice de signaux de données inférieure de la (n-1)-ième trame du premier dispositif de mémoire (122a) vers une zone d'affichage inférieure (L) du panneau d'affichage (100) pendant la première période de trame ;
le transfert de la matrice de signaux de données supérieure de la (n+1)-ième trame et de la matrice de signaux de données inférieure de la n-ième trame du deuxième dispositif de mémoire (122b) vers le premier dispositif de mémoire (122a) et le stockage de la matrice de signaux de données supérieure de la (n+1)-ième trame et de la matrice de signaux de données inférieure de la n-ième trame dans le premier dispositif de mémoire (122a), lorsque la matrice de signaux de données supérieure de la n-ième trame et la matrice de signaux de données inférieure de la (n-1)-ième trame ont été entièrement envoyées ;
le stockage de signaux de données d'une trame dans chacun d'une pluralité de troisièmes dispositifs de mémoire ; et
l'exclusion des matrices de signaux de données supérieure et inférieure parmi les signaux de données stockés dans les troisièmes dispositifs de mémoire et le stockage des matrices de signaux de données supérieure et inférieure dans le deuxième dispositif de mémoire (122b),
le premier et le deuxième dispositif de mémoire (122a, 122b) stockant et envoyant de manière répétitive les matrices de signaux de données supérieure et inférieure.

2. Procédé selon la revendication 1,
dans lequel chacune des matrices de signaux de données supérieure et inférieure sont envoyées par lignes à partir d'un côté supérieur vers un côté inférieur de la zone d'affichage supérieure (U) et de la zone d'affichage inférieure (L).

3. Procédé selon la revendication 1,
dans lequel le panneau d'affichage (100) est un panneau d'affichage électroluminescent organique.

4. Dispositif d'affichage comprenant :

un panneau d'affichage (100) ayant une zone d'affichage supérieure (U) et une zone d'affichage inférieure (L) ; et
une portion de contrôle de circuit de commande (120) comprenant :

un premier dispositif de mémoire (122a) comprenant un sous-dispositif de mémoire supérieur et un sous-dispositif de mémoire inférieur ;
un deuxième dispositif de mémoire (122b) comprenant un sous-dispositif de mémoire supérieur et un sous-dispositif de mémoire inférieur ;
une pluralité de troisièmes dispositifs de mémoire stockant chacun des signaux de données d'une trame ;

le sous-dispositif de mémoire supérieur du premier dispositif de mémoire (122a) stockant la matrice de signaux de données supérieure d'une n-ième trame et le sous-dispositif de mémoire inférieur du premier dispositif de mémoire (122a) stockant la matrice de signaux de données inférieure d'une (n-1)-ième trame et
le sous-dispositif de mémoire supérieur du deuxième dispositif de mémoire (122b) stockant la matrice de signaux de données supérieure d'une (n+1)-ième trame et le sous-dispositif de mémoire inférieur du deuxième dispositif de mémoire (122b) stockant la matrice de signaux de données inférieure de la n-ième trame ;

la portion de contrôle de circuit de commande de (120) étant conçue pour :

introduire la matrice de signaux de données supérieure de la n-ième trame du premier dispositif de mémoire (122a) vers la zone d'affichage supérieure (U) pendant une première période de trame et pour envoyer la matrice de signaux inférieure de la (n-1)-ième trame du premier dispositif de mémoire (122a) vers la zone d'affichage inférieure (L) pendant la première période de trame ;
transférer la matrice de signaux de données supérieure de la (n+1)-ième trame et la matrice de signaux de données inférieure de la n-ième trame du deuxième dispositif de mémoire (122b) vers le premier dispositif de mémoire (122a) et stocker la matrice de signaux de données supérieure de la (n+1)-ième trame et la matrice de signaux de données inférieure de la n-ième trame dans le premier dispositif de mémoire (122a) lorsque la matrice de signaux de données supérieure de la n-ième trame et la matrice de signaux de données inférieure de la (n-1)-ième trame ont été entièrement envoyées ;
et, ensuite
introduire la première matrice de signaux de données de la (n+1)-ième trame du premier dispositif de mémoire (122a) vers la zone d'affichage supérieure (U) pendant une deuxième période de trame, qui suit immédiatement la première période de trame et introduire la deuxième matrice de signaux de données de la n-ième trame du premier dispositif de mémoire (122a) vers la zone d'affichage inférieure (L) pendant la deuxième période de trame ;
exclure les matrices de signaux de données supérieure et inférieure parmi les signaux de données stockés dans les troisièmes dispositifs de mémoire et stocker les matrices de signaux de données supérieure et inférieure dans le deuxième dispositif de mémoire (122b).

5. Dispositif selon la revendication 4, comprenant en outre
une pluralité de lignes de portes dans la zone d'affichage supérieure (U) et la zone d'affichage inférieure (L), la pluralité de lignes de portes de chaque zone d'affichage étant balayée d'un côté supérieur vers un côté inférieur de la zone d'affichage supérieure (U) et de la zone d'affichage inférieure (L).

6. Dispositif selon la revendication 4,
dans lequel le panneau d'affichage (100) est un panneau d'affichage électroluminescent organique.

FIG. 1
RELATED ART

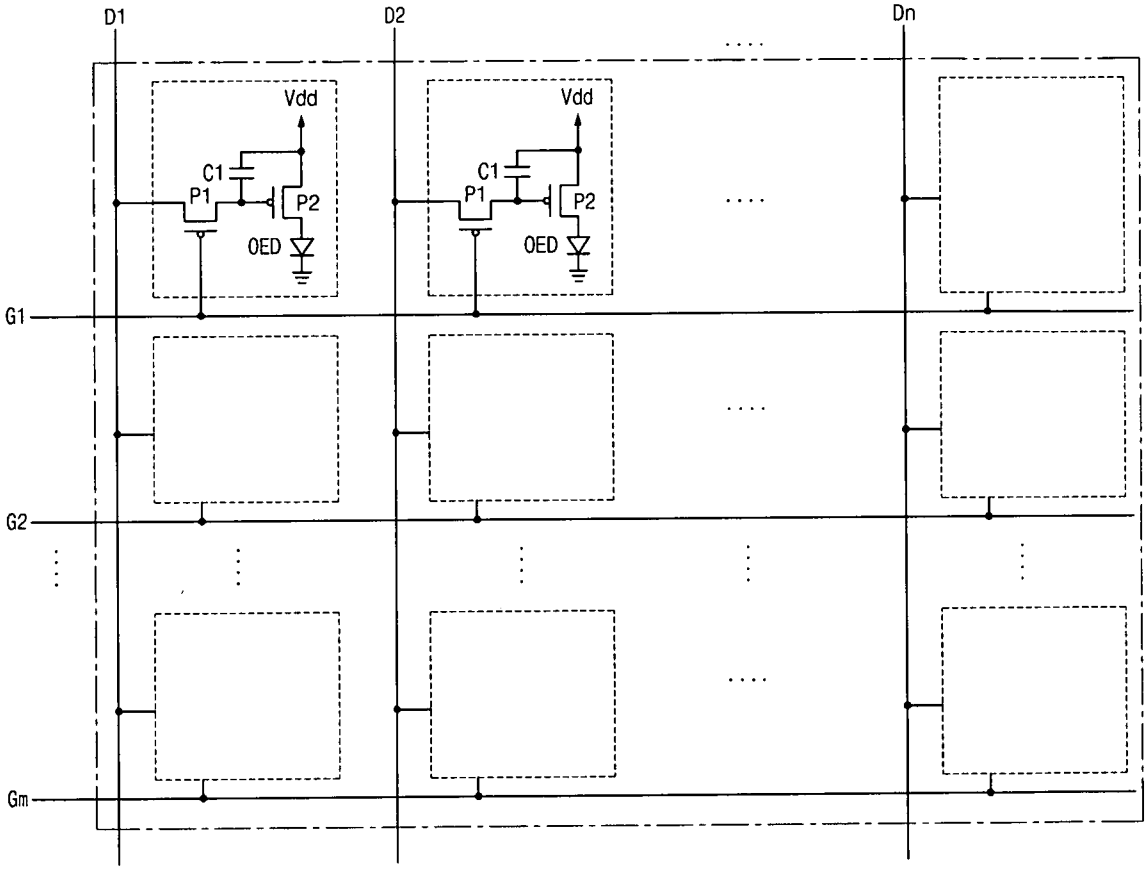


FIG. 2
RELATED ART

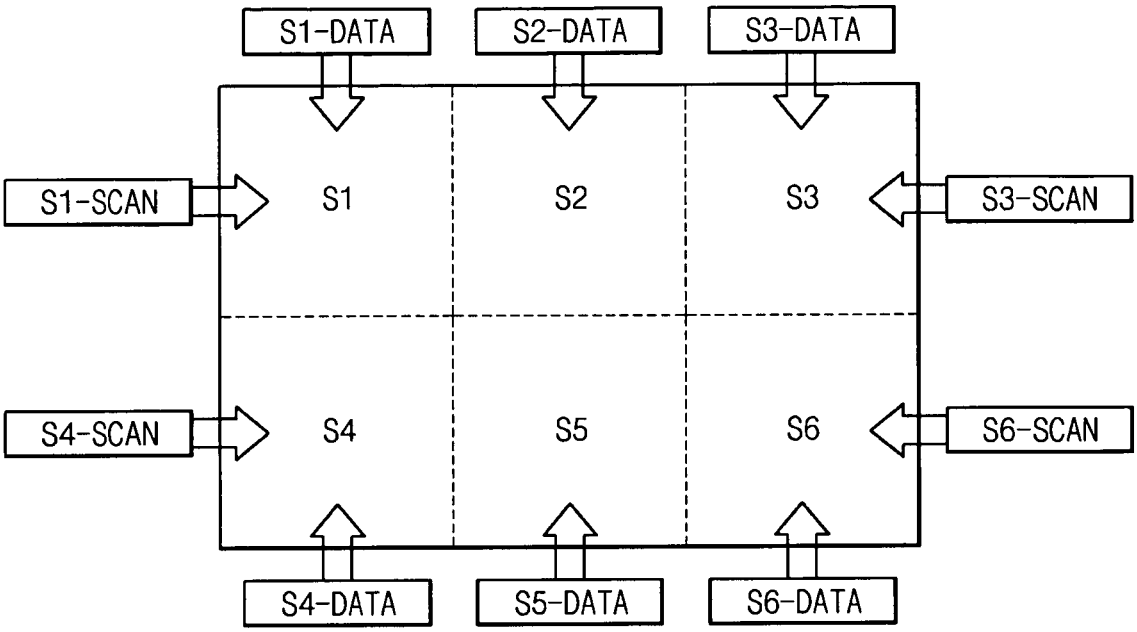


FIG. 3
RELATED ART

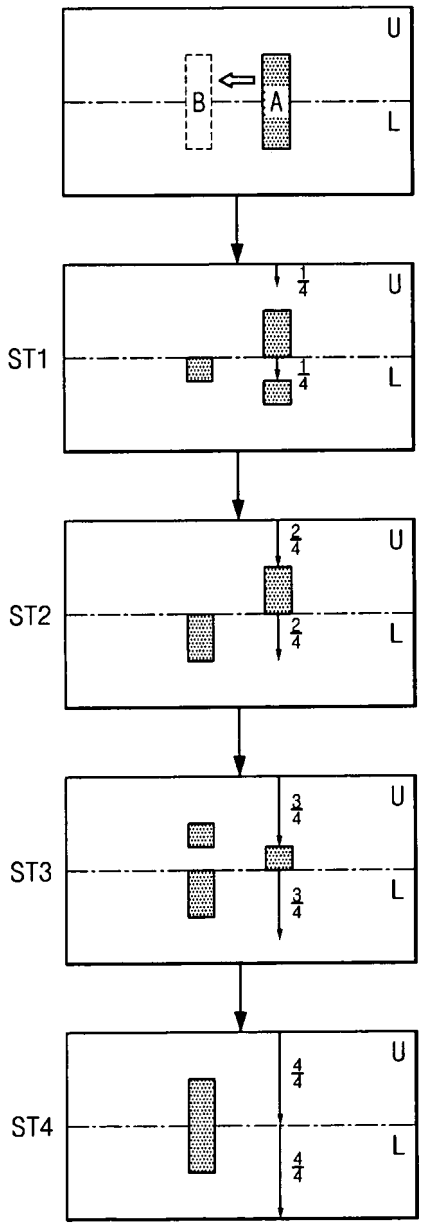


FIG. 4
RELATED ART

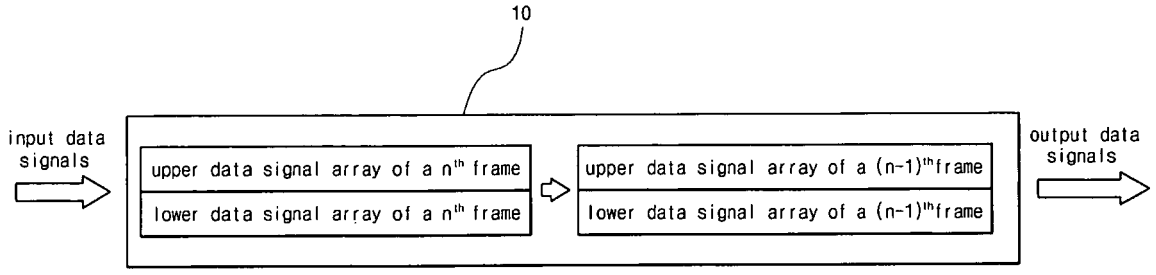
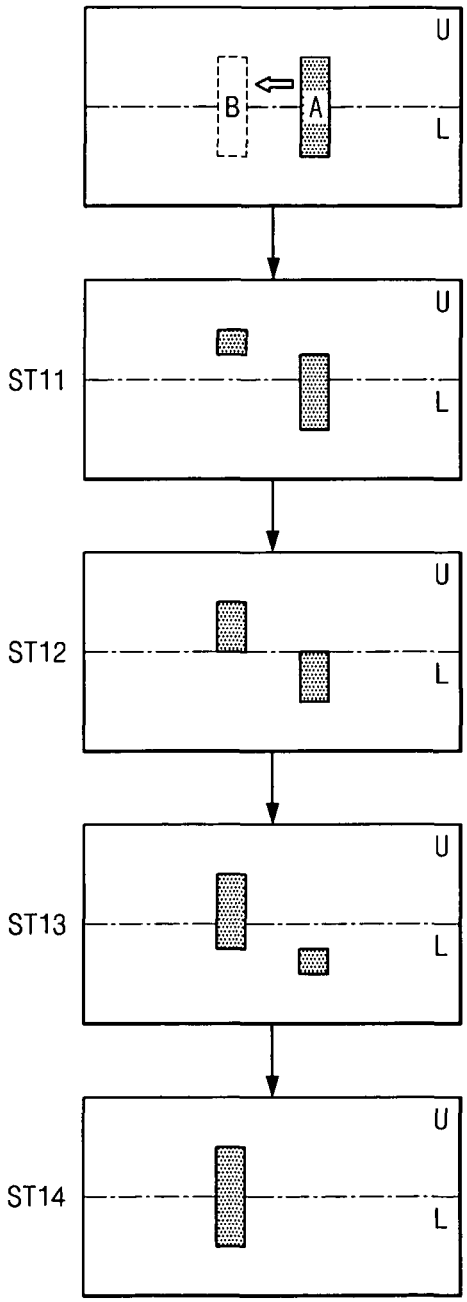


FIG. 5



write three quarters of an upper data signal array of a n^{th} frame

write three quarters of a lower data signal array of a $(n-1)^{th}$ frame

write all of an upper data signal array of a n^{th} frame

write all of a lower data signal array of a $(n-1)^{th}$ frame

write a quarter of an upper data signal array of a $(n+1)^{th}$ frame

write a quarter of a lower data signal array of a n^{th} frame

write a half of an upper data signal array of a $(n+1)^{th}$ frame

write a half of a lower data signal array of a n^{th} frame

FIG. 6

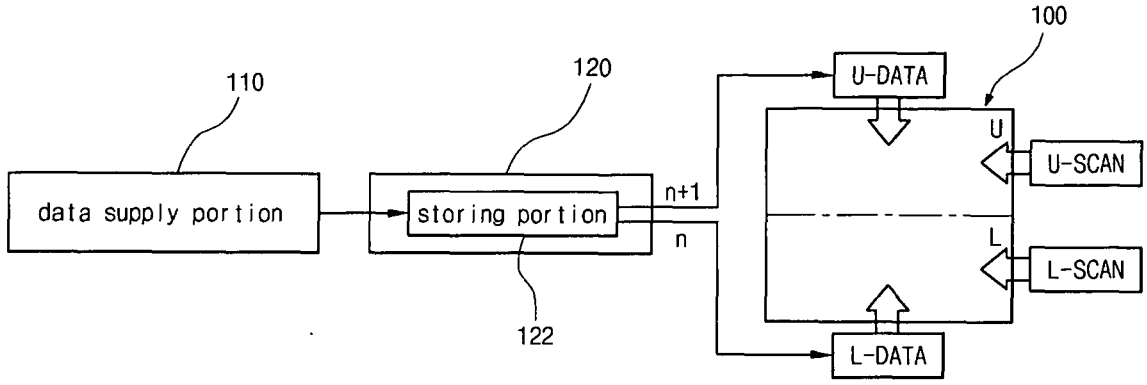
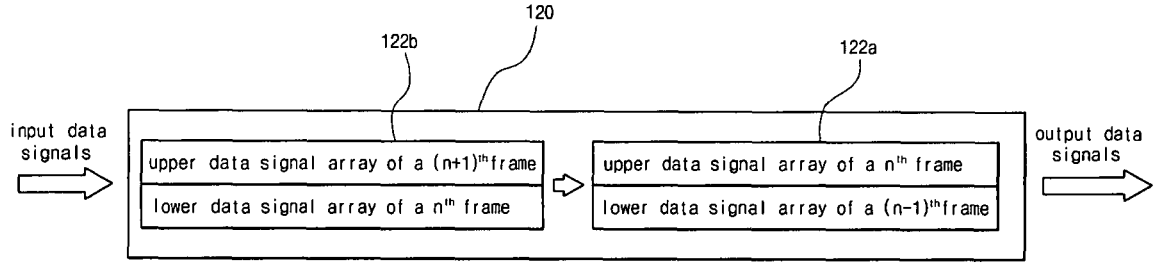

100
110
120
U-DATA
data supply portion
storing portion
n+1
n
U
U-SCAN
L
L-SCAN
122
L-DATA

FIG. 7


120
122b
122a
input data signals
upper data signal array of a (n+1)th frame
lower data signal array of a nth frame
upper data signal array of a nth frame
lower data signal array of a (n-1)th frame
output data signals

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 3043783 A **[0016]**

专利名称(译)	有机电致发光显示装置及其驱动方法		
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[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG.飞利浦液晶CO.LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KIM SEONG GYUN		
发明人	KIM, SEONG-GYUN		
IPC分类号	G09G3/20		
CPC分类号	G09G3/20 G09G3/3225 G09G3/3266 G09G3/3275 G09G2300/0842 G09G2310/0221 G09G2310/08 G09G2320/0261 G09G2360/18		
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外部链接	Espacenet		

摘要(译)

一种驱动显示装置的方法包括在第一帧周期期间将第（n + 1）帧的上数据信号阵列输出到显示面板的上显示区域;并且，提供在第一帧周期期间将第n帧的下数据信号阵列输出到显示面板的下显示区域。显示面板至少具有可独立操作的上显示区域和下显示区域，显示区域与存储装置通信，存储装置存储第（n + 1）帧的信号数据阵列并输出到上显示区域第一帧期间显示面板的显示;并且，在第一帧周期期间，将第n帧的下数据信号阵列输出到显示面板的下显示区域。

FIG. 1
RELATED ART