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(54) Data driving circuit and electroluminescent display using the same

Datenansteuerungsschaltung und Elektrolumineszenzanzeige damit

Circuit de commande de données et affichage électroluminescent l'utilisant

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Description

[0001] The present invention relates to a driving circuit for driving active matrix displays. More particularly, the present invention relates to a data driving circuit that applies a data signal to an electroluminescent display. The present invention also relates to an electroluminescent display.

[0002] Active matrix displays, such as an electroluminescent display, may include a pixel array arranged in the form of a matrix composed of cross points between the data lines and the scan lines, i.e., a matrix pixel unit. That is, the data lines may constitute vertical lines (i.e., column lines) of the matrix pixel unit and the scan lines may constitute horizontal lines (i.e., row lines) of the matrix pixel unit. The data driving circuit may supply data signals into the matrix pixel unit at a predetermined time.

[0003] FIG. 1 illustrates a block diagram of an exemplary configuration of a data driving circuit. Referring to FIG. 1, a data driving circuit may include a shift register 10, a latch unit 20 and a D/A converter 30.

[0004] The shift register 10 may receive a start pulse (/CLK) and a clock (CLK) signal to generate a plurality of shift signals. The shift signals may be generated sequentially and transmitted to a latch unit 20. The latch unit 20 may receive data signals, e.g., video data, and the shift signals. A sampling latch may receive the data signals in series and may output the shift signals in parallel. Accordingly, a row of data signals may be simultaneously applied to a row of pixel units (not illustrated).

[0005] The D/A converter unit 30 may convert data signals, output as digital data signals from the latch unit 20, into analog data signals. The D/A converter unit 30 then may output the analog data signals to a pixel unit (not illustrated). The digital data signals converted into the analog data signals may be used to display colors according to a grey level ratio.

[0006] FIG. 2 illustrates an exemplary configuration of a shift register, which may be used in the data driving circuit illustrated in FIG. 1. Referring to FIG. 2, the shift register may use a master-slave flip/flop arrangement. In an exemplary operation, the shift register may receive and output signals when the clock is at a low level; the shift register may not output signals when the clock is at a high level.

[0007] In this exemplary circuit, a problem may exist because the inverters may output a static current when its input is at a low level. Also, the static current may be generated in half of the inverters inside the flip/flop. Therefore, the overall power consumption of the circuit may be increased since the number of inverters receiving a high-level input in the flip/flop may be the same as the number of inverters receiving a low level input.

[0008] A high level output voltage may be calculated by accounting for the voltage and a resistance that may exist between a supply voltage potential and ground, and the low level output voltage may be higher than a threshold voltage of a transistor, as illustrated in FIG. 2. In other words, the high level input voltage received at every stage may vary according to property deviations of the transistors. Therefore, the circuit may operate erroneously due to these level variations generated at the high level. Also, a low-level deviation of the output voltage may be represented by an ON resistance deviation of input transistors in the inverters illustrated in the circuit of FIG. 2, which may increase a high-level deviation of the input voltage. Transistors, for example, that may be employed in an electroluminescent display may make the above problems even worse due to the substantial property deviations that may exist.

[0009] Additionally, an inverter may charge an output port by allowing a current to flow through an input transistor to the output port. The output port may discharge by allowing a current to flow from the output port to a load transistor. Accordingly, a source- gate voltage of the load transistor may be gradually reduced when the output port is being charged. Therefore, the discharge current may fluctuate and the efficiency of the discharge may be deteriorated.

[0010] US 6 784 864 discloses a digital driver for display devices wherein, by successively inputting digital data to a shift register, the digital data is shifted, and the result is sent out to latch circuits.

[0011] The present invention sets out to provide a data driving circuit and an electroluminescent display employing the same, which substantially overcome one or more of the above described problems arising from the limitations and disadvantages of the related art.

[0012] According to a first aspect of the invention, there is provided a data driving circuit as set out in Claim 1 or 13. Preferred features of this aspect are set out in Claims 2 to 12.

[0013] Embodiments of the present invention provide a data driving circuit that is capable of reducing a power consumption by removing paths through which a static current may flow, and switching an output voltage at the range from a positive power supply voltage to a negative power supply voltage using a bootstrap technique, since the shift register may include a plurality of PMOS or NMOS transistors and a capacitor, and may be operated by 2-phase clock signals.

[0014] According to a second aspect of the invention, there is provided an electroluminescent display as set out in Claim 14.

[0015] Embodiments of the invention will now be described by way of example and with reference to the attached drawings in which:

[0016] FIG. 1 is a block diagram of a data driving circuit;

[0017] FIG. 2 is a shift register that may be used in the data driving circuit illustrated in FIG. 1;

[0018] FIG. 3 illustrates an electroluminescent display according to an embodiment of the present invention;

[0019] FIG. 4 illustrates a data driving circuit for use by the electroluminescent display illustrated in FIG. 3, in accordance with the invention;

[0020] FIG. 5 is a timing diagram illustrating operation of the data driving circuit illustrated in FIG. 4;

[0021] FIG. 6 illustrates a further data driving circuit for use by the electroluminescent display illustrated in FIG. 3, in accordance with the invention;

[0022] FIG. 7 is a timing diagram illustrating operation of the data driving circuit illustrated in FIG. 6;

[0023] FIG. 8 is a circuit diagram of a first stage for use in the data driving circuits illustrated in FIG. 4 and FIG. 6, in accordance with the invention;

[0024] FIG. 9 is a circuit diagram of a second stage for use in the data driving circuits illustrated in FIG. 4 and FIG. 6, in accordance with the invention;

[0025] FIG. 10 is a circuit diagram of a further first stage for use in the data driving circuits illustrated in FIG. 4 and FIG. 6, not in accordance with the invention;

[0026] FIG. 11 is a circuit diagram of a further second stage for use in the data driving circuits illustrated in FIG. 4 and FIG. 6, not in accordance with the invention;

[0027] FIG. 12 is a timing diagram illustrating operation of the data driving circuit illustrated in FIG. 4, in which the first and second stages illustrated in FIG. 10 and FIG. 11 are used; and

[0028] FIG. 13 is a timing diagram illustrating operation of the data driving circuit illustrated in FIG. 6, in which the first and second stages illustrated in FIG. 10 and FIG. 11 are used.

[0029] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are illustrated. The invention may, however, be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the figures, the dimensions of elements may be exaggerated for clarity of illustration. Like reference numerals refer to like elements throughout.

[0030] FIG. 3 illustrates an organic light-emitting display (OLED) according to the present invention. However, it should be understood that an OLED is considered a particular type of an electroluminescent display and should not limit the scope of this invention. Rather, the OLED is being presented as an example of an electroluminescent display for the purposes of illustration and discussion only. Furthermore, the OLED itself is exemplary in nature and the discussion herein should not limit the implementation of such a display, including components utilized, operations performed and connections thereto. Referring to FIG. 3, the OLED has a pixel unit 100, including a plurality of pixels 110 connected with scan lines S1 to Sn and data lines D1 to Dm, a data driving circuit 200 for driving the data lines D1 to Dm, a scan driving circuit 300 for driving the scan lines S1 to Sn, and a timing control unit 400 for controlling the scan driving circuit 300 and the data driving circuit 200.

[0031] The pixel unit 100 is adapted to receive a first power supply (ELVDD) and a second power supply (ELVSS) from an external source (not illustrated), so as to supply the power to each of pixels 110. Each of the pixels 110 receiving the first power supply (ELVDD) and the second power supply (ELVSS) can then generate a light corresponding to data signals by controlling a current flowing from the first power supply (ELVDD) to the second power supply (ELVSS) via, for example, a light-emitting diode (not illustrated), that corresponds to the data signals.

[0032] The data driving circuit 200 is adapted to receive data-driving control signals (DCS) from the timing control unit 400. The data driving circuit 200 receiving the data-driving control signals (DCS) can then generate data signals, and supply the generated data signals to data lines D1 to Dm so that they may be synchronized with the scan signals. The data driving circuit 200 includes a plurality of switching elements. The switching elements may or may not be all the same type. For example, the switching elements may be realized by PMOS transistors, NMOS transistors or other suitable components, either exclusively, respectively or combinations thereof.

[0033] The scan driving circuit 300 is adapted to receive scan-driving control signals (SCS) from the timing control unit 400. The scan driving circuit 300 receiving the scan-driving control signals (SCS) can then generate scan signals and sequentially supply the generated scan signals to scan lines S 1 to Sn. That is, the scan driving circuit 300 can operate to sequentially generate scan signals and supply the generated scan signals to a pixel unit 100 which may then drive a plurality of the pixels.

[0034] The timing control unit 400 is adapted to generate data-driving control signals (DCS) and scan-driving control signals (SCS) to correspond to synchronizing signals supplied from an external source (not illustrated). The DCS generated in the timing control unit 400 are supplied to the data driving circuit 200 and the SCS are supplied to the scan driving circuit 300. The timing control unit 400 may also supply DATA, which may be generated from an external source (not illustrated), to the data driving circuit 200.

[0035] FIG. 4 illustrates a data driving circuit for use with the exemplary OLED illustrated in FIG. 3, according to an embodiment of the present invention. However, it should be understood that this data driving circuit should not be limited to use in the OLED of FIG. 3. Rather, this data driving circuit may be used with other electroluminescent displays.

[0036] Referring to FIG. 4, the data driving circuit 200 includes a shift register and a latch unit. The shift register includes a plurality of first stages 2101 to 2102n, and each of the first stages can be operated by a first clock (CLK1) and a second clock (CLK2), and then the first stage 2101 can output a 1^{st} carrier wave (s[1]) and can transmit the 1^{st} carrier wave (s[1]) to a 2^{nd} first stage 2102, Data signals (for example, video data) can be output with the 1^{st} carrier wave (s[1]). The 2^{nd} first stage 2102 can receive the 1^{st} carrier wave, and then can transmit the 2^{nd} carrier wave to a 3^{rd} first stage and a 1^{st} second stage 2201, and then the 3rd first stage can transmit a 3rd carrier wave to the 4th first stage 2104. That is, the even-numbered first stages 2102, 2104...2102n-2, 2102n can transmit carrier waves to the adjacent first stages (the odd-numbered first stage 2103, 2105... 2102n-3, 2102n-1) and the second stages.

[0037] The latch unit includes a plurality of the second stages 2201 to 220n, and each of the second stages can be operated by a first enable signal (EN1) , a second enable signal (EN2) which can be supplied by first and second enable signal generators. The plurality of the second stages 2201 to 220n are connected to output lines of the even- numbered first stages 2102, 2104... 2102n-2, 2102n to receive data signal (al to an) transmitted from the even- numbered first stages 2102, 2104... 2102n- 2, 2102n to the carrier waves (s2, s4, ...s2n- 2, s2n) . Accordingly, the number of second stages 2201 to 220n is half the number of the first stages 2101 to 2102n. Also, each of the second stages can simultaneously output the data signals (for example, video data) based on the first enable signal (EN1) and the second enable signal (EN2) . Accordingly, the data signals (for example, video data) can be input in series to a plurality of the first stages 2101 to 2102n and can be output in parallel by a plurality of the second stages 2201 to 220n.

[0038] FIG. 5 is a timing diagram illustrating the operation of the data driving circuit shown in FIG. 4. Referring to FIG. 5, the first clock CLK1 is a pulse that is periodically generated and has a longer high period and a shorter low period. The second clock (CLK2) is a similar pulse that is delayed for a predetermined period compared to the first clock (CLK1). The carrier wave (s1) outputs from the 1st first stage 2101 are generated with the same periodicity as the first clock (CLK1), and the carrier wave (s1) outputs the 1st data (a1) when the signal is at a low level.

[0039] The 1st first stage 2101 receives the input data serially, and continues to sequentially output a n-th data of the 1st data (a1) over the carrier wave (s[1]). In turn, the 2nd first stage 2102 receives the 1st carrier wave from the 1st first stage 2101, and then outputs the 2nd carrier wave (s2). Therefore, the 2nd carrier wave (s2) outputs the 1st data (a1) after the 1st data (a1) is delayed for a predetermined time compared to the 1st carrier wave (s1), and sequentially outputs the data from the 1st data (a1) to the nth data (an). In this manner, the nth carrier wave (sn) outputs the data from the 1st data (a1) to the nth data (an). The first and second enable signals (EN1, EN2) are input at a point that the 1st data (a1) to nth data (an) are output over the nth carrier wave (sn) of the 1st carrier wave (s1), and then output simultaneously by a plurality of the second stages 2201 to 220n.

[0040] FIG. 6 illustrates a schematic of another data driving circuit that may be used with the OLED illustrated in FIG. 3, according to an embodiment of the present invention. Again, it should be understood that the data driving circuit should not be limited for use with the OLED of FIG. 3. Rather, this data driving circuit may be used with other electroluminescent displays.

[0041] Referring to FIG. 6, the data driving circuit 200 includes a shift register and a latch unit. The shift register includes a plurality of first stages 2101 to 2102n, and each of the first stages is operated by the first clock (CLK1) and the second clock (CLK2). The first stage 2101 outputs the 1st carrier wave (s1) and transmits the 1st carrier wave (s1) to the 2nd first stage 2102 and the 1st second stage 2201. Data signals (for example, video data) are carried and output in the 1st carrier wave (s1). Thus, the 2nd first stage 2102 receives the 1st carrier wave (s1) and transmits the 2nd carrier wave to a 3rd first stage 2103, and then the 3rd first stage 2103 transmits a 3rd carrier wave (s3) to the 4th first stage and the 2nd second stage 2202. That is, the odd-numbered first stages 2001, 2003...2002n-3, 2002n-1 transmit carrier waves to the adjacent first stages (the even-numbered first stage 2002, 2004...2002n-2, 2002n) and the second stages.

[0042] The latch unit includes a plurality of the second stages 2201 to 220n, and each of the second stages is operated by a first enable signal (EN1) and a second enable signal (EN2). The plurality of the second stages 2201 to 220n are connected to output lines of the odd-numbered first stages 2001, 2003...2002n-3, 2002n-1 to receive data signals (a1 to an) transmitted from the odd-numbered first stages 2001, 2003...2002n-3, 2002n-1. Accordingly, a plurality of the second stages 2201 to 220n have half the number of the plurality of the first stages 2101 to 2102n. Also, each of the second stages simultaneously outputs the data signals (for example, video data) based on the first enable signal (EN1) and the second enable signal (EN2). Accordingly, the data signals (for example, video data) are input in series to a plurality of the first stages 2101 to 2102n and are output in parallel by a plurality of the second stages 2201 to 220n.

[0043] FIG. 7 illustrates a timing diagram of an operation of the data driving circuit illustrated in FIG. 6. Referring to FIG. 7, the first clock CLK1 is a pulse that is periodically generated and has a longer high period and a shorter low period. The second clock (CLK2) is a pulse delayed for a predetermined period compared to the first clock (CLK1) pulse. The carrier wave (s1) output from the 1st first stage 2101 is generated with the same periodicity as the first clock (CLK1), and the carrier wave (s1) outputs data (a1) when the signal is at a low level. The carrier wave (s1) continues to sequentially output a nth data in the 1st data (a1).

[0044] The 2nd first stage 2102 receives the 1st carrier wave (s1) from the 1st first stage and outputs the 2nd carrier wave (s2). The 2nd carrier wave (s2) outputs the 1st data (a1) after the 1st data (a1) is delayed for a predetermined time as compared to the 1st carrier wave (s [1]), and sequentially outputs the data from the 1st data (a1) to the nth data (an). In this manner, the nth first stage 2102n outputs the nth carrier wave (sn). The first and second enable signals (EN1, EN2) are input at a point that the 1st data (a1) to nth data (an) are output over the

n^{th} carrier wave (sn) of the 1^{st} carrier wave (s1), and then are simultaneously output by a plurality of the second stages 2201 to 220n.

[0045] FIG. 8 illustrates a circuit diagram of a first stage that may be used in the data driving circuits illustrated in FIG. 4 and FIG. 6, according to an embodiment of the present invention. FIG. 9 illustrates a circuit diagram of a second stage that may be used in the data driving circuits illustrated in FIG. 4 and FIG. 6, according to an embodiment of the present invention.

[0046] Referring to FIG. 8 and FIG. 9, the first and second stages may have the same configuration, except that the first stage receives a first clock signal (CLK1) and a second clock signal (CLK2), while the second stage receives a first enable signal (EN1) and a second enable signal (EN2). However, although not illustrated, other implementations can be considered where the first and second stages do not have the same configuration. Also, the first stage and the second stage can be realized by PMOS transistors and capacitors. However, other implementations without PMOS transistors and capacitors can be realized.

[0047] Since the first stage and the second stage are connected in the same manner, as discussed above, the first stage and second stage will be described referring to the connection of the first stage only.

[0048] Referring to FIG. 8, in the first transistor (M1), a source is connected to an input terminal (IN), a drain is connected to a first node (N1) and a gate is connected to the second clock (CLK2). In the second transistor (M2), a source is connected to a first clock (CLK1), a drain is connected to a second node (N2), and a gate is connected to the first node (N1). In the third transistor (M3), a source is connected to a third node (N3), a drain is connected to a second power supply (VSS), and a gate is connected to the second clock (CLK2). In the fourth transistor (M4), a source is connected to a second clock (CLK2), a drain is connected to the third node (N3), and a gate is connected to the first node (N1). Also in the fifth transistor (M5), a source is connected to a first power supply (VDD), a drain is connected to an output terminal (OUT), and a gate is connected to the third node (N3). Finally, in a capacitor (C1), a first electrode is connected to the first node (N1), and a second electrode is connected to the second node (N2). The second node (N2) is also connected to the output terminal (OUT). Accordingly, the data signals input through the input terminal (IN) are stored in the capacitor (C1), and then are output through the output terminal (OUT) after a predetermined time.

[0049] FIG. 10 illustrates a circuit diagram of another first stage that may be used in the data driving circuits illustrated in FIG. 4 and FIG. 6. FIG. 11 illustrates a circuit diagram of another second stage. Referring to FIG. 10 and FIG. 11, the first and second stages are realized by NMOS transistors and capacitors. Again, other implementations of the first and second stages can be realized. The first stage is operated after receiving the first clock signal and the second clock signal, and the second stage is operated after receiving the first enable signal and the second enable signal.

[0050] FIG. 12 illustrates a timing diagram of an exemplary operation of the data driving circuit illustrated in FIG. 4, in which the first and second stages illustrated in FIG. 10 and FIG. 11 are used. FIG. 13 illustrates a timing diagram of an exemplary operation of the data driving circuit illustrated in FIG. 6, in which the first and second stages illustrated in FIG. 10 and FIG. 11 are used. Referring to FIG 12 and FIG. 13, waveforms of signals input/output in the first and second stage are realized by NMOS transistors. The signals are reversed, and then input into the first and second stages to operate the data driving circuit, as illustrated in FIG. 6. As a result, a description of FIG. 12 and FIG. 13 is identical to that of FIG. 7.

[0051] As described above, the data driving circuit according to embodiments of the present invention has advantages in that it reduces power consumption by removing paths through which a static current may flow, minimizes a leakage current since the output port is not recharged when a high-level output may be put through the data driving circuit, and also increases an operation rate by minimizing reduction of the current that discharges the output port since the bootstrap is operated when a low-level output is put through the data driving circuit.

[0052] Exemplary embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A data driving circuit (200), comprising:

a shift register unit including a plurality of first stages (2101-2102n) connected in series, the shift register being for receiving data signals and for outputting the data signals, wherein each first stage (2101-2102n) is arranged to receive the data signals output from a preceding first stage (2101-2102n); and

a latch unit including a plurality of second stages (2201-220n), wherein each second stage (2201-220n) is connected to a different predetermined first stage (2101-2102n) and is arranged to receive the data signals output from the predetermined first stage (2101-2102n), wherein the number of second stages (2201-220n) is substantially half the number of the first stages;

wherein each first stage (2101-2102n) is con-

nected to a first clock and a second clock and is arranged to receive first and second clock signals (CLK1, CLK2) as inputs;
CHARACTERISED IN THAT:

each first stage (2101-2102n) is arranged to store data signals when the values of the first and the second clock signals (CLK1, CLK2) are identical to each other and to output the stored data signals when the values of the first and the second clock signals (CLK1, CLK2) are different from each other; wherein each first stage (2101-2102n) comprises:

a first transistor (M1) connected between an input port and a first node (N1) and being arranged to be turned on based on the second clock (CLK2);
a second transistor (M2) connected between the first clock (CLK1) and a second node (N2) and arranged to be turned on based on a voltage of the first node (N1), the second node (N2) connected to an output port;
a third transistor (M3) connected between a third node (N3) and a first power supply (VSS) and arranged to be turned on based on the second clock (CLK2);
a fourth transistor (M4) connected between the second clock (CLK2)and the third node (N3) and arranged to be turned on based on the voltage of the first node (N1);
a fifth transistor (M5) connected between a second power supply (VDD) and the output port and arranged to be turned on based on the voltage of the third node (N3); and
a first capacitor (Cl) connected between the first node (N1) and the output port and arranged to maintain the voltages of the output port and the first node (N1).

2. A data driving circuit according to claim 1, wherein the predetermined first stage (2101-2102n) is an even-numbered one of the plurality of first stages (2101-2102n).

3. A data driving circuit according to claim 1, wherein the predetermined first stage (2101-2102n) is an odd-numbered one of the plurality of first stages (2101-2102n).

4. A data driving circuit (200) according to claim 1, 2 or 3, wherein each of the first stages (2101-2102n) includes PMOS or NMOS transistors.

5. A data driving circuit (200) according to any preceding claims wherein the first and the second clock signals (CLK1, CLK2) include a data-reading period and a data-transmitting period, and the data-reading period is shorter than the data-transmitting period.

6. A data driving circuit (200) according to claim 5, wherein the second clock signal (CLK2) is equivalent to a delayed first clock signal (CLK1).

7. A data driving circuit (200) according to any preceding claim, wherein each second stage (2201-220n) is arranged to receive a first enable signal (EN1) and a second enable signal (EN2) that are input at a same period, wherein each second stage (2201-220n) is arranged to store data signals when the values of the first and the second enable signals (EN1, EN2) are identical to each other and to output the stored data signals when the values of the first and the second enable signals (EN1, EN2) are different from each other.

8. A data driving circuit (200) according to claim 7, wherein each second stage (2201-220n) comprises:

a sixth transistor (M6) connected between an input port and a fourth node (N4) and arranged to be turned on based on the first enable signal (EN1);
a seventh transistor (M7) connected between a second enable signal (EN2) and a fifth node (N5) and arranged to be turned on based on a voltage of the fourth node (N4);
an eighth transistor (M8) connected between a first power supply (VSS) and a sixth node (N6) and arranged to be turned on based on the first enable signal (EN1);
a ninth transistor (M9) connected between the first enable signal (EN1) and the sixth node (N6) and arranged to be turned on based on the voltage of the fourth node (N4);
a tenth transistor (M10) connected between a second power supply and the output port and arranged to be turned on based on a voltage of the sixth node (N6); and
a second capacitor connected between the fourth node (N4) and the output port, the second capacitor being arranged to maintain the voltages of the output port and the fourth node (N4).

9. A data driving circuit (200) according to claim 8, wherein each of the second stages (220l-220n) includes PMOS or NMOS transistors.

10. A data driving circuit (200) according to any one of claims 7 to 9, wherein the second stages (2201-220n) are arranged to output simultaneously the data signals in parallel based on the first and the second enable signals (EN1, ENZ).

11. A data driving circuit (200) according to claim 10, wherein the first and the second enable signals (EN1, ENZ) have waveforms of the first and the second clock signals (CLK1, CLK2) at an applied point.

12. A data driving circuit (200) according to any preceding claim, including a D/A converter connected to the latch unit, wherein the D/A converter receives digital data signals from the latch unit and outputs analog data signals.

13. A data driving circuit (200), comprising:

a shift register unit including a plurality of first stages (2101-2102n) connected in series, the shift register being for receiving data signals and for outputting the data signals, wherein each first stage (2101-2102n) is arranged to receive the data signals output from a preceding first stage (2101-2102n); and
a latch unit including a plurality of second stages (2201-220n), wherein each second stage (2201-220n) is connected to a different predetermined first stage (2101-2102n) and is arranged to receive the data signals output from the predetermined first stage (2101-2102n), wherein the number of second stages (2201-220n) is substantially half the number of the first stages;
wherein each second stage (2201-220n) is arranged to receive a first enable signal (EN1) and a second enable signal (EN2) that are input at a same period, wherein each second stage (2201-220n) is arranged to store data signals when the values of the first and the second enable signals (EN1, EN2) are identical to each other and to output the stored data signals when the values of the first and the second enable signals (EN1, EN2) are different from each other;
CHARACTERISED IN THAT:

each second stage (2201-220n) comprises:

a sixth transistor (M6) connected between an input port and a fourth node (N4) and arranged to be turned on based on the first enable signal (EN1);
a seventh transistor (M7) connected between a second enable signal (EN2) and a fifth node (N5) and arranged to be turned on based on a voltage of the fourth node (N4), the fifth node (N5) connected to an output port;
an eighth transistor (M8) connected between a first power supply (VSS) and a sixth node (N6) and arranged to be turned on based on the first enable signal (EN1);
a ninth transistor (M9) connected between the first enable signal (EN1) and the sixth node (N6) and arranged to be turned on based on the voltage of the fourth node (N4);
a tenth transistor (M10) connected between a second power supply and an output port and arranged to be turned on based on a voltage of the sixth node (N6); and
a second capacitor connected between the fourth node (N4) and the output port, the second capacitor being arranged to maintain the voltages of the output port and the fourth node (N4).

14. An electroluminescent display, comprising:

a pixel unit (100) including pixels for receiving data signals (Dl-Dm) and scan signals (Sl-Sm);
a scan driving circuit (300) for transmitting the scan signals to the pixels; and
a data driving circuit (200) according to any one of claims 1 to 13 for transmitting the data signals to the pixels.

Patentansprüche

1. Daten-Ansteuerungsschaltung (200), umfassend:

eine Schieberegistereinheit, die eine Vielzahl von in Reihe geschalteten ersten Stufen (2101-2102n) aufweist, wobei das Schieberegister zum Empfangen von Datensignalen und zum Ausgeben der Datensignale dient, worin jede erste Stufe (2101-2102n) dafür eingerichtet ist, die von einer vorhergehenden ersten Stufe (2101-2102n) ausgegebenen Datensignale zu empfangen; und
eine Auffangspeichereinheit, die eine Vielzahl von zweiten Stufen (2201-220n) aufweist, worin jede zweite Stufe (2201-220n) mit einer anderen vorbestimmten ersten Stufe (2101-2102n) verbunden ist und dafür eingerichtet ist, die von der vorbestimmten ersten Stufe (2101-2102n) ausgegebenen Datensignale zu empfangen, worin die Anzahl der zweiten Stufen (220l-220n) im Wesentlichen halb so groß wie die Anzahl der ersten Stufen ist;
worin jede erste Stufe (2101-2102n) mit einem ersten Takt und einem zweiten Takt verbunden ist und dafür eingerichtet ist, ein erstes und zweites Taktsignal (CLK1, CLK2) als Eingaben zu empfangen;
dadurch gekenntzeichnet, dass:

jede erste Stufe (2101-2102n) dafür eingerichtet ist, Datensignale zu speichern, wenn die Werte des ersten und des zweiten Taktsignals (CLK1, CLK2) miteinander identisch sind, und die gespeicherten Datensignale auszugeben, wenn sich die Werte des ersten und des zweiten Taktsignals (CLK1, CLK2) voneinander unterscheiden; worin jede erste Stufe (2101-2102n) umfasst:

einen ersten Transistor (M1), der zwischen einen Eingangsanschluss und einen ersten Knoten (N1) geschaltet und dafür eingerichtet ist, auf der Grundlage des zweiten Takts (CLK2) eingeschaltet zu werden;
einen zweiten Transistor (M2), der zwischen den ersten Takt (CLK1) und einen zweiten Knoten (N2) geschaltet und dafür eingerichtet ist, auf der Grundlage einer Spannung des ersten Knotens (N1) eingeschaltet zu werden, wobei der zweite Knoten (N2) mit einem Ausgangsanschluss verbunden ist;
einen dritten Transistor (M3), der zwischen einen dritten Knoten (N3) und eine erste Stromversorgung (VSS) geschaltet und dafür eingerichtet ist, auf der Grundlage des zweiten Takts (CLK2) eingeschaltet zu werden;
einen vierten Transistor (M4), der zwischen den zweiten Takt (CLK2) und den dritten Knoten (N3) geschaltet und dafür eingerichtet ist, auf der Grundlage der Spannung des ersten Knotens (N1) eingeschaltet zu werden;
einen fünften Transistor (M5), der zwischen eine zweite Stromversorgung (VDD) und den Ausgangsanschluss geschaltet und dafür eingerichtet ist, auf der Grundlage der Spannung des dritten Knotens (N3) eingeschaltet zu werden; und
einen ersten Kondensator (C1), der zwischen den ersten Knoten (N1) und den Ausgangsanschluss geschaltet und dafür eingerichtet ist, die Spannungen des Ausgangsanschlusses und des ersten Knotens (N1) beizubehalten.

2. Daten-Ansteuerungsschaltung nach Anspruch 1, worin die vorbestimmte erste Stufe (2101-2102n) eine geradzahlige der Vielzahl von ersten Stufen (2101-2102n) ist.

3. Daten-Ansteuerungsschaltung nach Anspruch 1, worin die vorbestimmte erste Stufe (2101-2102n) eine ungeradzahlige der Vielzahl von ersten Stufen (2101-2102n) ist.

4. Daten-Ansteuerungsschaltung (200) nach Anspruch 1, 2 oder 3, worin jede der ersten Stufen (2101-2102n) PMOS- oder NMOS-Transistoren aufweist.

5. Daten-Ansteuerungsschaltung (200) nach einem der vorhergehenden Ansprüche, worin das erste und zweite Taktsignal (CLK1, CLK2) eine Datenleseperiode und eine Datensendeperiode aufweisen und die Datenleseperiode kürzer als die Datensendeperiode ist.

6. Daten-Ansteuerungsschaltung (200) nach Anspruch 5, worin das zweite Taktsignal (CLK2) äquivalent zu einem verzögerten ersten Taktsignal (CLK1) ist.

7. Daten-Ansteuerungsschaltung (200) nach einem der vorhergehenden Ansprüche, worin jede zweite Stufe (2201-220n) dafür eingerichtet ist, ein erstes Aktivierungssignal (EN1) und ein zweites Aktivierungssignal (EN2) zu empfangen, die in einer gleichen Periode eingegeben werden, worin jede zweite Stufe (2201-220n) dafür eingerichtet ist, Datensignale zu speichern, wenn die Werte des ersten und des zweiten Aktivierungssignals (EN1, EN2) miteinander identisch sind, und die gespeicherten Datensignale auszugeben, wenn sich die Werte des ersten und des zweiten Aktivierungssignals (EN1, EN2) voneinander unterscheiden.

8. Daten-Ansteuerungsschaltung (200) nach Anspruch 7, worin jede zweite Stufe (2201-220n) umfasst:

einen sechsten Transistor (M6), der zwischen einen Eingangsanschluss und einen vierten Knoten (N4) geschaltet und dafür eingerichtet ist, auf der Grundlage des ersten Aktivierungssignals (EN1) eingeschaltet zu werden;
einen siebenten Transistor (M7), der zwischen ein zweites Aktivierungssignal (EN2) und einen fünften Knoten (N5) geschaltet und dafür eingerichtet ist, auf der Grundlage einer Spannung des vierten Knotens (N4) eingeschaltet zu werden;
einen achten Transistor (M8), der zwischen eine erste Stromversorgung (VSS) und einen sechsten Knoten (N6) geschaltet und dafür eingerichtet ist, auf der Grundlage des ersten Aktivierungssignals (EN1) eingeschaltet zu werden;
einen neunten Transistor (M9), der zwischen das erste Aktivierungssignal (EN1) und den sechsten Knoten (N6) geschaltet und dafür eingerichtet ist, auf der Grundlage der Spannung des vierten Knotens (N4) eingeschaltet zu werden;
einen zehnten Transistor (M10), der zwischen eine zweite Stromversorgung und den Ausgangsanschluss geschaltet und dafür eingerichtet ist, auf der Grundlage einer Spannung des sechsten Knotens (N6) eingeschaltet zu werden; und
einen zweiten Kondensator, der zwischen den vierten Knoten (N4) und den Ausgangsanschluss geschaltet ist, wobei der zweite Kondensator dafür eingerichtet ist, die Spannungen des Ausgangsanschlusses und des vierten Kno-

tens (N4) beizubehalten.

9. Daten-Ansteuerungsschaltung (200) nach Anspruch 8, worin jede der zweiten Stufen (220l-220n) PMOS- oder NMOS-Transistoren aufweist.

10. Daten-Ansteuerungsschaltung (200) nach einem der Ansprüche 7 bis 9, worin die zweiten Stufen (2201-220n) dafür eingerichtet sind, die Datensignale auf der Grundlage des ersten und des zweiten Aktivierungssignals (EN1, EN2) gleichzeitig parallel auszugeben.

11. Daten-Ansteuerungsschaltung (200) nach Anspruch 10, worin das erste und das zweite Aktivierungssignal (EN1, EN2) Wellenformen des ersten und des zweiten Taktsignals (CLK1, CLK2) an einem angewendeten Punkt haben.

12. Daten-Ansteuerungsschaltung (200) nach einem der vorhergehenden Ansprüche, aufweisend einen mit der Auffangspeichereinheit verbundenen D/A-Wandler, worin der D/A-Wandler digitale Datensignalen von der Auffangspeichereinbeit empfängt und analoge Datensignale ausgibt.

13. Daten-Ansteuerungsschaltung (200), umfassend:

eine Schieberegistereinheit, die eine Vielzahl von in Reihe geschalteten ersten Stufen (2101-2102n) aufweist, wobei das Schieberegister zum Empfangen von Datensignalen und zum Ausgeben der Datensignale dient, worin jede erste Stufe (2101-2102n) dafür eingerichtet ist, die von einer vorhergehenden ersten Stufe (2101-2102n) ausgegebenen Datensignale zu empfangen; und
eine Auffangspeichereinheit, die eine Vielzahl von zweiten Stufen (220l-220n) aufweist, worin jede zweite Stufe (2201-220n) mit einer anderen vorbestimmten ersten Stufe (2101-2102n) verbunden ist und dafür eingerichtet ist, die von der vorbestimmten ersten Stufe (2101-2102n) ausgegebenen Datensignale zu empfangen, worin die Anzahl der zweiten Stufen (2201-220n) im Wesentlichen halb so groß wie die Anzahl der ersten Stufen ist;
worin jede zweite Stufe (2201-220n) dafür eingerichtet ist, ein erstes Aktivierungssignal (EN1) und ein zweites Aktivierungssignal (EN2) zu empfangen, die in einer gleichen Periode eingegeben werden, worin jede zweite Stufe (2201-220n) dafür eingerichtet ist, Datensignale zu speichern, wenn die Werte des ersten und des zweiten Aktivierungssignals (EN1, EN2) miteinander identisch sind, und die gespeicherten Datensignale auszugeben, wenn sich die Werte des ersten und des zweiten Aktivierungssignals (EN1, EN2) voneinander unterscheiden;
dadurch gekennzeichnet, dass:

jede zweite Stufe (2201-220n) umfasst:

einen sechsten Transistor (M6), der zwischen einen Eingangsanschluss und einen vierten Knotens (N4) geschaltet und dafür eingerichtet ist, auf der Grundlage des ersten Aktivierungssignals (EN1) eingeschaltet zu werden;
einen siebenten Transistor (M7), der zwischen ein zweites Aktivierungssignal (EN2) und einen fünften Knoten (N5) geschaltet und dafür eingerichtet ist, auf der Grundlage einer Spannung des vierten Knotens (N4) eingeschaltet zu werden, wobei der fünfte Knoten (N5) mit einem Ausgangsanschluss verbunden ist;
einen achten Transistor (M8), der zwischen eine erste Stromversorgung (VSS) und einen sechsten Knoten (N6) geschaltet und dafür eingerichtet ist, auf der Grundlage des ersten Aktivierungssignals (EN1) eingeschaltet zu werden;
einen neunten Transistor (M9), der zwischen das erste Aktivierungssignal (EN1) und den sechsten Knoten (N6) geschaltet und dafür eingerichtet ist, auf der Grundlage der Spannung des vierten Knotens (N4) eingeschaltet zu werden;
einen zehnten Transistor (M10), der zwischen eine zweite Stromversorgung und einen Ausgangsanschluss geschaltet und dafür eingerichtet ist, auf der Grundlage einer Spannung des sechsten Knotens (N6) eingeschaltet zu werden; und
einen zweiten Kondensator (2), der zwischen den vierten Knoten (N4) und den Ausgangsanschluss geschaltet ist, wobei der zweite Kondensator (2) dafür eingerichtet ist, die Spannungen des Ausgangsanschlusses und des vierten Knotens (N4) beizubehalten.

14. Elektrolumineszanzeige, umfassend:

eine Bildpunkteinheit (100), die Bildpunkte zum Empfangen von Datensignalen (Dl-Dm) und Abtastsignalen (Sl-Sm) aufweist;
eine Abtastansteuerungseinheit (300) zum Übertragen der Abtastsignale zu den Bildpunkten; und
eine Daten-Ansteuerungsschaltung (200) nach einem der Ansprüche 1 bis 13 zum Übertragen der Datensignale zu den Bildpunkten.

Revendications

1. Circuit de commande de données (200), comprenant :

une unité de registre à décalage incluant une pluralité de premiers étages (2101 - 2102n) connectés en série, le registre à décalage étant destiné à recevoir des signaux de données et à générer en sortie les signaux de données, dans lequel chaque premier étage (2101 - 2102n) est agencé de manière à recevoir les signaux de données générés en sortie à partir d'un premier étage précédent (2101 - 2102n) ; et

une unité de verrouillage incluant une pluralité de seconds étages (2201 - 220n), dans lequel chaque second étage (2201 - 220n) est connecté à un premier étage prédéterminé distinct (2101 - 2102n) et est agencé de manière à recevoir les signaux de données générés en sortie à partir du premier étage prédéterminé (2101 - 2102n), dans lequel le nombre de seconds étages (2201 - 220n) est sensiblement égal à la moitié du nombre des premiers étages;

dans lequel chaque premier étage (2101 - 2102n) est connecté à une première horloge et à une seconde horloge, et est agencé de manière à recevoir des premier et second signaux d'horloge (CLK1, CLK2) en tant qu'entrées ;

caractérisé en ce que :

chaque premier étage (2101 - 2102n) est agencé de manière à stocker des signaux de données lorsque les valeurs des premier et second signaux d'horloge (CLK1, CLK2) sont mutuellement identiques et à générer en sortie les signaux de données stockés lorsque les valeurs des premier et second signaux d'horloge (CLK1, CLK2) sont mutuellement différentes ;

dans lequel chaque premier étage (2101 - 2102n) comprend :

un premier transistor (M1) connecté entre un port d'entrée et un premier noeud (N1), et agencé de manière à être mis sous tension sur la base de la seconde horloge (CLK2 ;

un deuxième transistor (M2) connecté entre la première horloge (CLK1) et un deuxième noeud (N2), et agencé de manière à être mis sous tension sur la base d'une tension du premier noeud (N1), le deuxième noeud (N2) étant connecté à un port de sortie ;

un troisième transistor (M3) connecté entre un troisième noeud (N3) et une première source d'alimentation (VSS), et agencé de manière à être mis sous tension sur la base de la seconde horloge (CLK2) ;

un quatrième transistor (M4) connecté entre la seconde horloge (CLK2) et le troisième noeud (N3), et agencé de manière à être mis sous tension sur la base de la tension du premier noeud (N1) ;

un cinquième transistor (M5) connecté entre une seconde source d'alimentation (VDD) et le port de sortie, et agencé de manière à être mis sous tension sur la base de la tension du troisième noeud (N3) ; et

un premier condensateur (C1) connecté entre le premier noeud (N1) et le port de sortie, et agencé de manière à maintenir les tensions du port de sortie et du premier noeud (N1).

2. Circuit de commande de données selon la revendication 1, dans lequel le premier étage prédéterminé (2101 - 2102n) est un étage pair de la pluralité de premiers étages (2101 - 2102n).

3. Circuit de commande de données selon la revendication 1, dans lequel le premier étage prédéterminé (2101 - 2102n) est un étage impair de la pluralité de premiers étages (2101 - 2102n).

4. Circuit de commande de données (200) selon la revendication 1, 2 ou 3, dans lequel chacun des premiers étages (2101 - 2102n) comprend des transistors PMOS ou NMOS.

5. Circuit de commande de données (200) selon l'une quelconque des revendications précédentes, dans lequel les premier et second signaux d'horloge (CLK1, CLK2) incluent une période de lecture de données et une période de transmission de données, et la période de lecture de données est plus courte que la période de transmission de données.

6. Circuit de commande de données (200) selon la revendication 5, dans lequel le second signal d'horloge (CLK2) est équivalent à un premier signal d'horloge retardé (CLK1).

7. Circuit de commande de données (200) selon l'une quelconque des revendications précédentes, dans lequel chaque second étage (2201 - 220n) est agencé de manière à recevoir un premier signal d'activation (EN1) et un second signal d'activation (EN2) qui sont entrés au cours d'une même période, dans lequel chaque second étage (2201 - 220n) est agencé de manière à stocker des signaux de données lorsque les valeurs des premier et second signaux d'activation (EN1, EN2) sont mutuellement identiques, et à générer en sortie les signaux de données stockés lorsque les valeurs des premier et second signaux d'activation (EN1, EN2) sont mutuellement différentes.

8. Circuit de commande de données (200) selon la revendication 7, dans lequel chaque second étage (2201 - 220n) comprend :

un sixième transistor (M6) connecté entre un

port d'entrée et un quatrième noeud (N4), et agencé de manière à être mis sous tension sur la base du premier signal d'activation (EN1) ;
un septième transistor (M7) connecté entre un second signal d'activation (EN2) et un cinquième noeud (N5), et agencé de manière à être mis sous tension sur la base d'une tension du quatrième noeud (N4) ;
un huitième transistor (M8) connecté entre une première source d'alimentation (VSS) et un sixième noeud (N6), et agencé de manière à être mis sous tension sur la base du premier signal d'activation (EN1) ;
un neuvième transistor (M9) connecté entre le premier signal d'activation (EN1) et le sixième noeud (N6), et agencé de manière à être mis sous tension sur la base de la tension du quatrième noeud (N4) ;
un dixième transistor (M10) connecté entre une seconde source d'alimentation et le port de sortie, et agencé de manière à être mis sous tension sur la base d'une tension du sixième noeud (N6) ; et
un second condensateur connecté entre le quatrième noeud (N4) et le port de sortie, le second condensateur étant agencé de manière à maintenir les tensions du port de sortie et du quatrième noeud (N4).

9. Circuit de commande de données (200) selon la revendication 8, dans lequel chacun des seconds étages (2201 - 220n) comprend des transistors PMOS ou NMOS.

10. Circuit de commande de données (200) selon l'une quelconque des revendications 7 à 9, dans lequel les seconds étages (2201 - 220n) sont agencés de manière à générer en sortie, simultanément, les signaux de données en parallèle, sur la base des premier et second signaux d'activation (EN1, EN2).

11. Circuit de commande de données (200) selon la revendication 10, dans lequel les premier et second signaux d'activation (EN1, EN2) présentent des formes d'onde des premier et second signaux d'horloge (CLK1, CLK2) en un point d'application.

12. Circuit de commande de données (200) selon l'une quelconque des revendications précédentes, incluant un convertisseur numérique à analogique connecté à l'unité de verrouillage, dans lequel le convertisseur numérique à analogique reçoit des signaux de données numériques provenant de l'unité de verrouillage, et génère en sortie des signaux de données analogiques.

13. Circuit de commande de données (200), comprenant :

une unité de registre à décalage incluant une pluralité de premiers étages (2101 - 2102n) connectés en série, le registre à décalage étant destiné à recevoir des signaux de données et à générer en sortie les signaux de données, dans lequel chaque premier étage (2101 - 2102n) est agencé de manière à recevoir les signaux de données générés en sortie à partir d'un premier étage précédent (2101 - 2102n) ; et
une unité de verrouillage incluant une pluralité de seconds étages (2201 - 220n), dans lequel chaque second étage (2201 - 220n) est connecté à un premier étage prédéterminé distinct (2101 - 2102n), et est agencé de manière à recevoir les signaux de données générés en sortie à partir du premier étage prédétermine (2101 - 2102n), dans lequel le nombre de seconds étages (2201 - 220n) est sensiblement égal à la moitié du nombre des premiers étages;
dans lequel chaque second étage (2201 - 220n) est agencé de manière à recevoir un premier signal d'activation (EN1) et un second signal d'activation (EN2) qui sont entrés au cours d'une même période, dans lequel chaque second étage (2201 - 220n) est agencé de manière à stocker des signaux de données, lorsque les valeurs des premier et second signaux d'activation (EN1, EN2) sont mutuellement identiques, et à générer en sortie les signaux de données stockés, lorsque les valeurs des premier et second signaux d'activation (EN1, EN2) sont mutuellement différentes ;
caractérisé en ce que :

chaque second étage (2201 - 220n) comprend :

un sixième transistor (M6) connecté entre un port d'entrée et un quatrième noeud (N4), et agencé de manière à être mis sous tension sur la base du premier signal d'activation (EN1) ;
un septième transistor (M7) connecté entre un second signal d'activation (EN2) et un cinquième noeud (N5), et agencé de manière à être mis sous tension sur la base d'une tension du quatrième noeud (N4), le cinquième noeud (N5) étant connecté à un port de sortie ;
un huitième transistor (M8) connecté entre une première source d'alimentation (VSS) et un sixième noeud (N6), et agencé de manière à être mis sous tension sur la base du premier signal d'activation (EN1) ;
un neuvième transistor (M9) connecté entre le premier signal d'activation (EN1) et le sixième noeud (N6), et agencé de manière à être mis sous tension sur la base de la tension du quatrième noeud (N4) ;
un dixième transistor (M10) connecté entre une

seconde source d'alimentation et un port de sortie, et agencé de manière à être mis sous tension sur la base d'une tension du sixième noeud (N6) ; et
un second condensateur (2) connecté entre le quatrième noeud (N4) et le port de sortie, le second condensateur (2) étant agencé de manière à maintenir les tensions du port de sortie et du quatrième noeud (N4).

14. Affichage électroluminescent, comprenant :

une unité de pixels (100) incluant des pixels pour recevoir des signaux de données (Dl - Dm) et des signaux de balayage (S 1 - Sm) ;
un circuit de commande de balayage (300) destiné à transmettre les signaux de balayage aux pixels ; et
un circuit de commande de données (200) selon l'une quelconque des revendications 1 à 13, destiné à transmettre les signaux de données aux pixels.

FIG. 1
(RELATED ART)

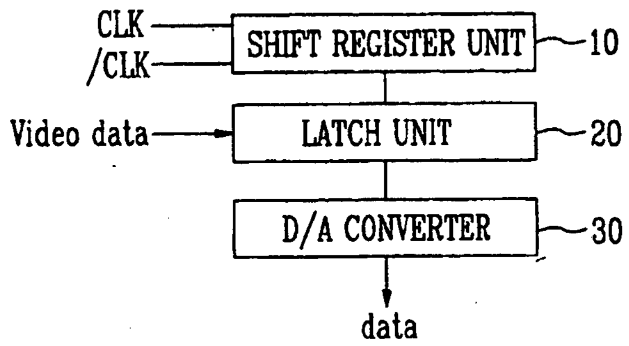


FIG. 2
(RELATED ART)

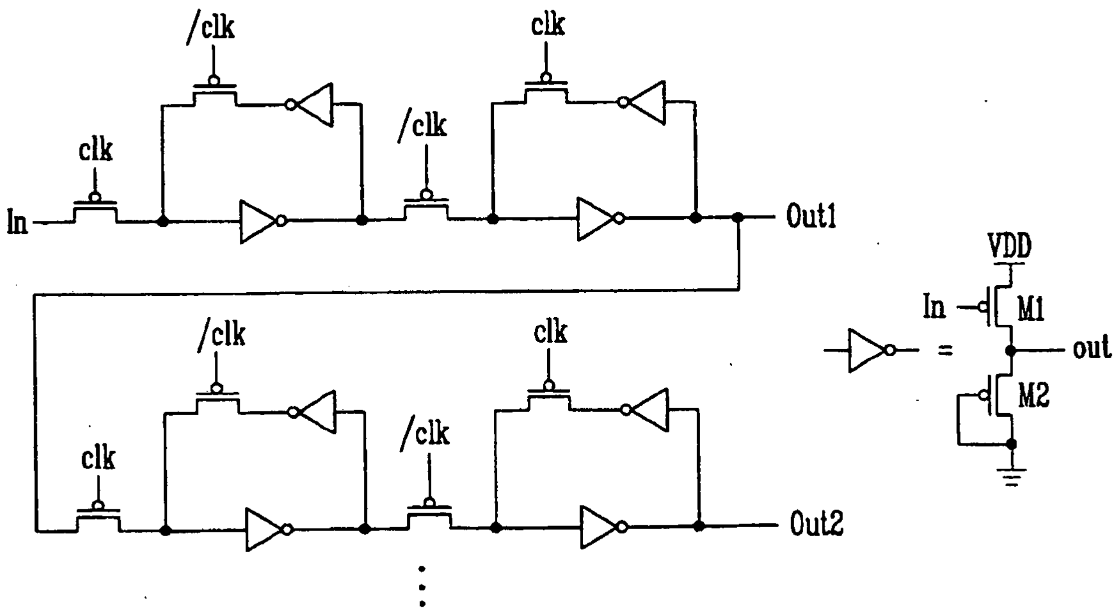


FIG. 3

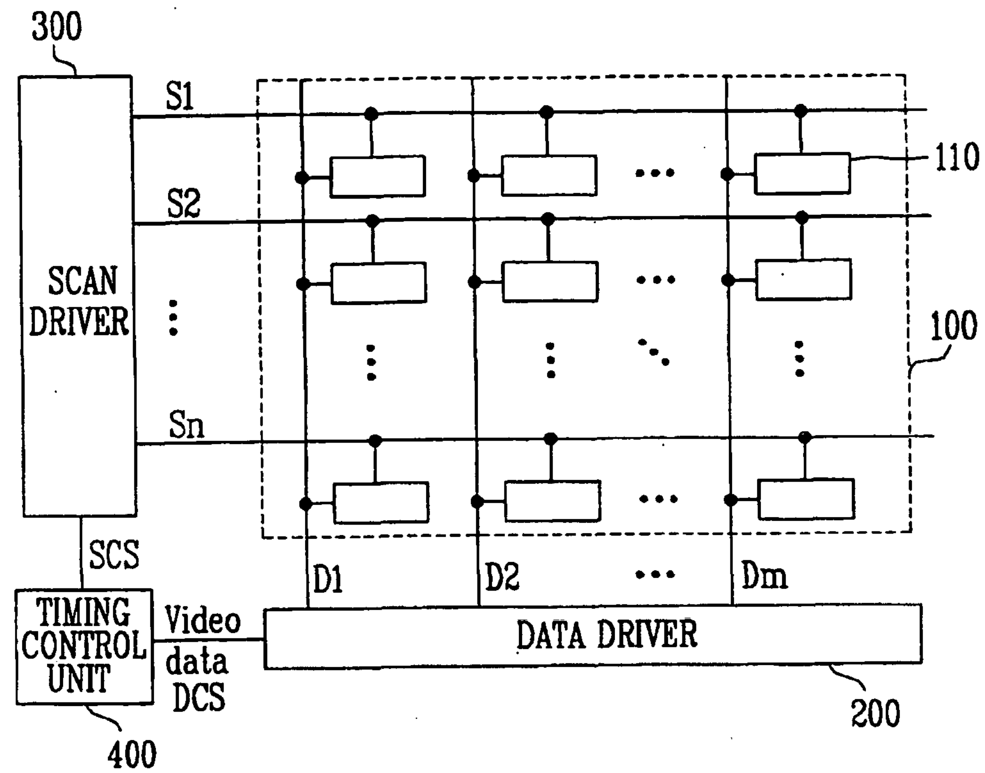

300
SCAN DRIVER
S1
S2
Sn
110
100
SCS
TIMING CONTROL UNIT
Video data DCS
D1
D2
Dm
DATA DRIVER
200
400

FIG. 4

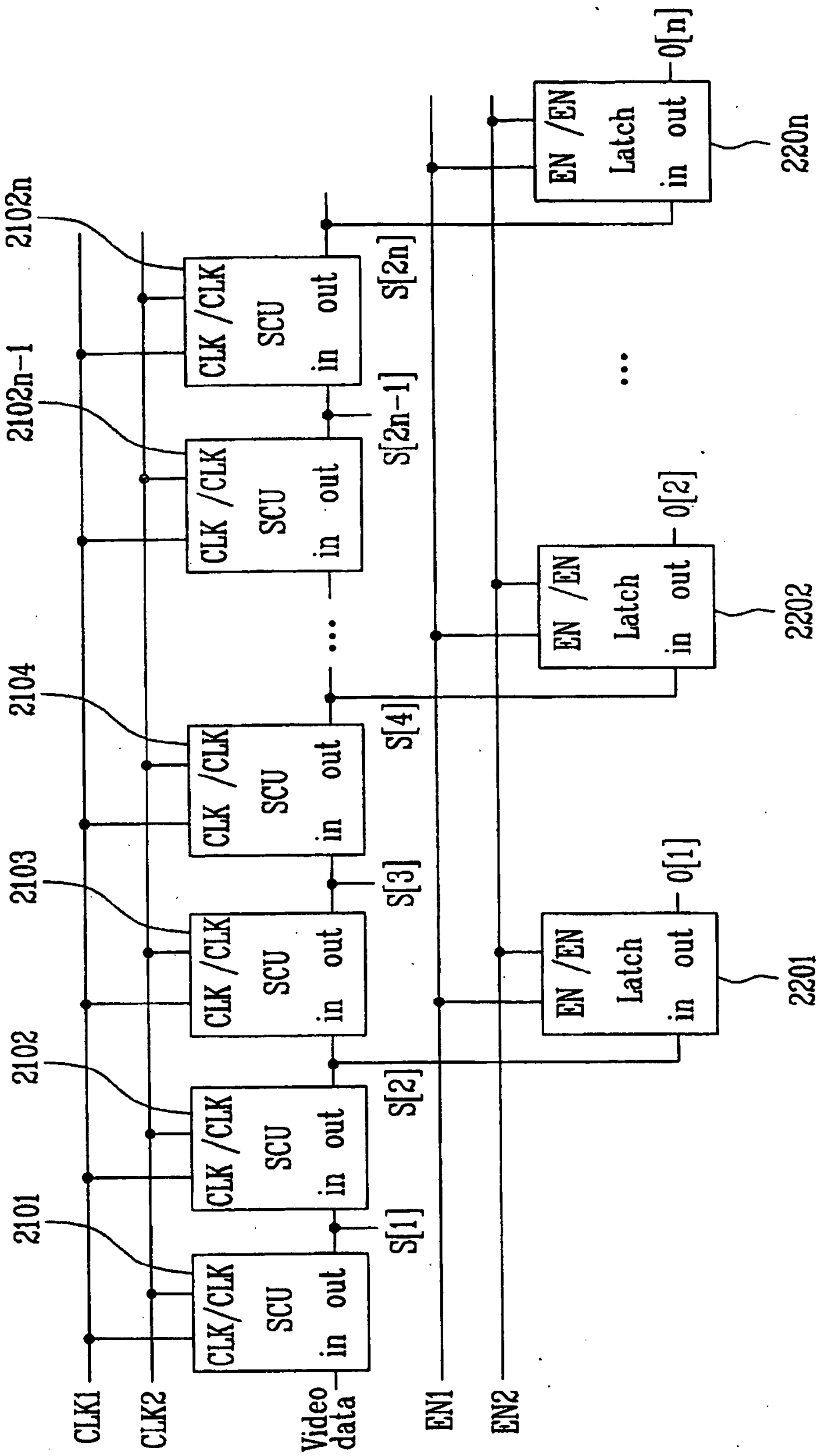

CLK1
CLK2
Video data
EN1
EN2
2101
2102
2103
2104
2102n-1
2102n
CLK/CLK
SCU
in
out
S[1]
S[2]
S[3]
S[4]
S[2n-1]
S[2n]
EN /EN
Latch
O[1]
O[2]
O[n]
2201
2202
220n

FIG. 5

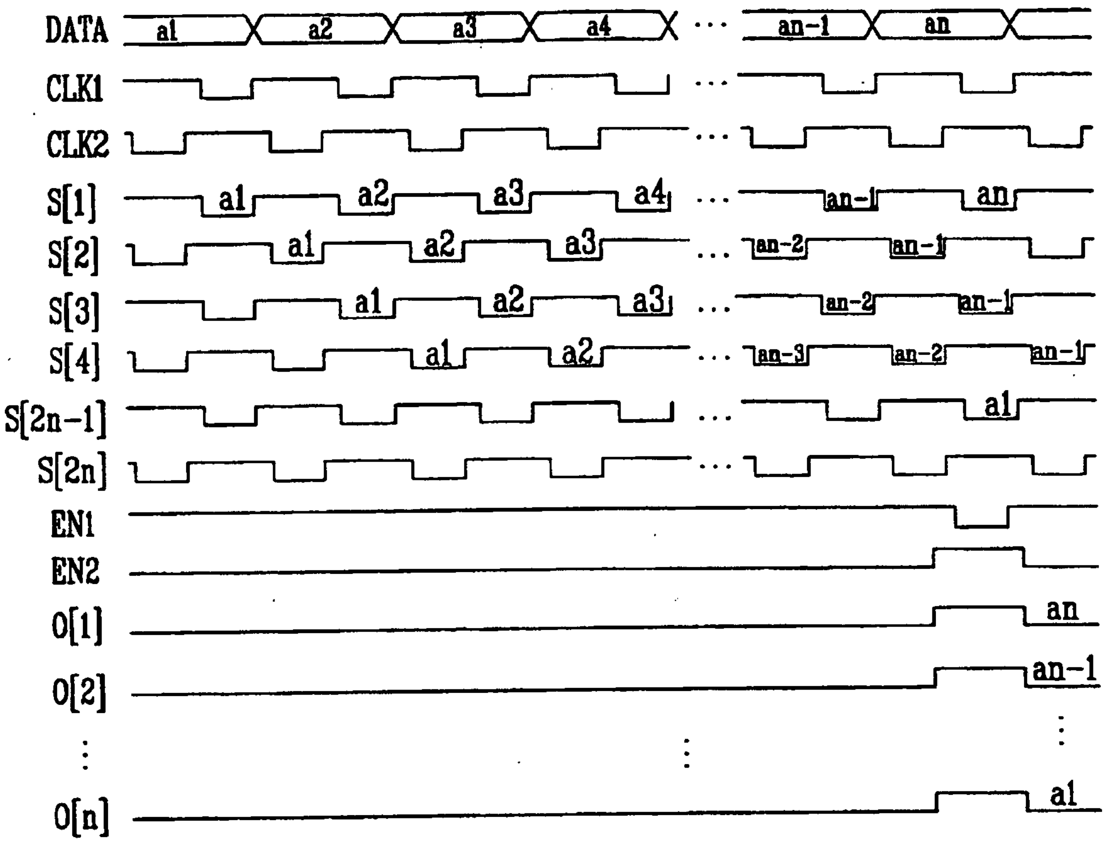
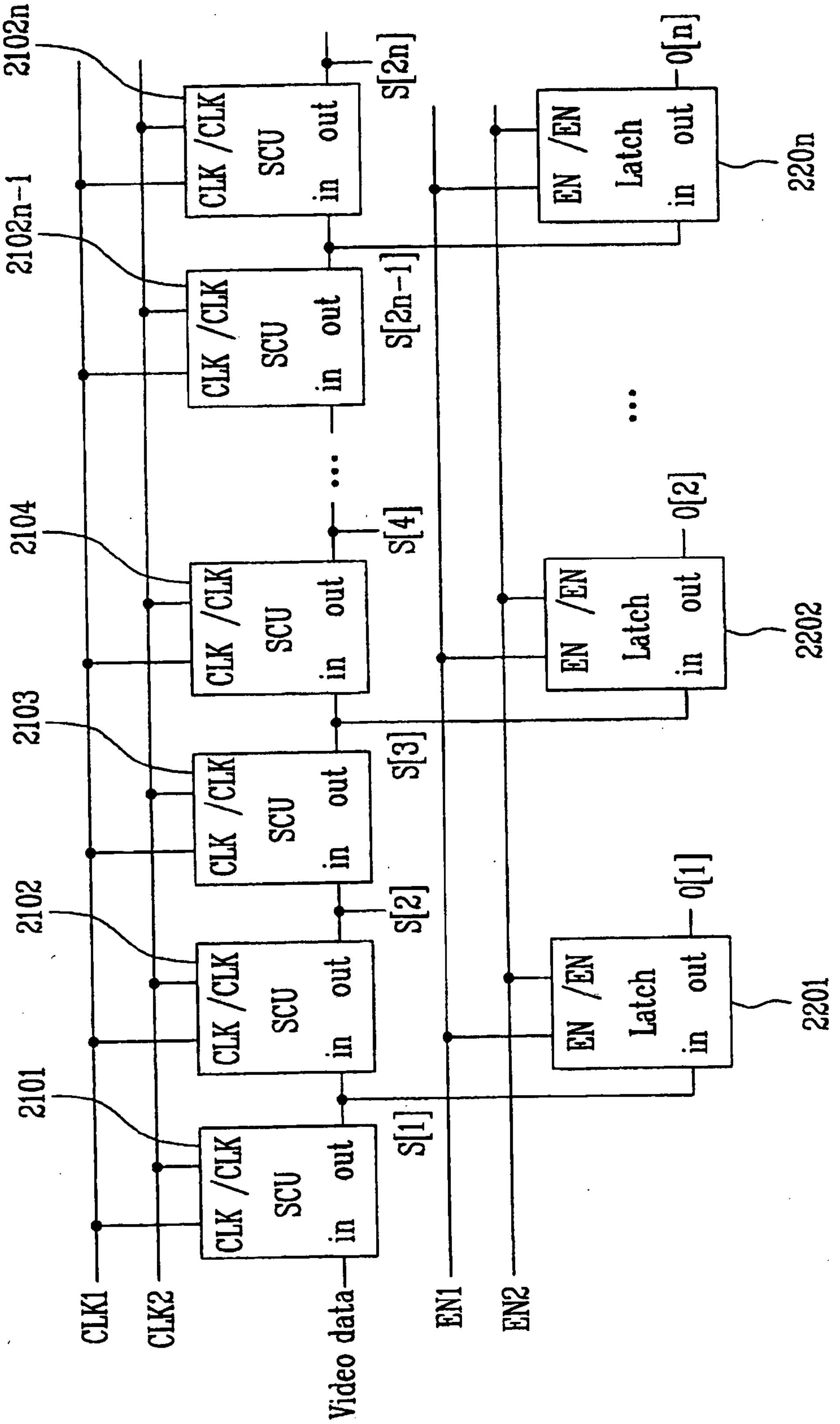

DATA
a1
a2
a3
a4
an-1
an
CLK1
CLK2
S[1]
S[2]
S[3]
S[4]
S[2n-1]
S[2n]
EN1
EN2
O[1]
O[2]
O[n]
an-2
an-3

FIG. 6



CLK1
CLK2
Video data
EN1
EN2
2101
2102
2103
2104
2102n-1
2102n
CLK /CLK
SCU
in out
S[1]
S[2]
S[3]
S[4]
S[2n-1]
S[2n]
EN /EN
Latch
in out
2201
2202
220n
O[1]
O[2]
O[n]

FIG. 7

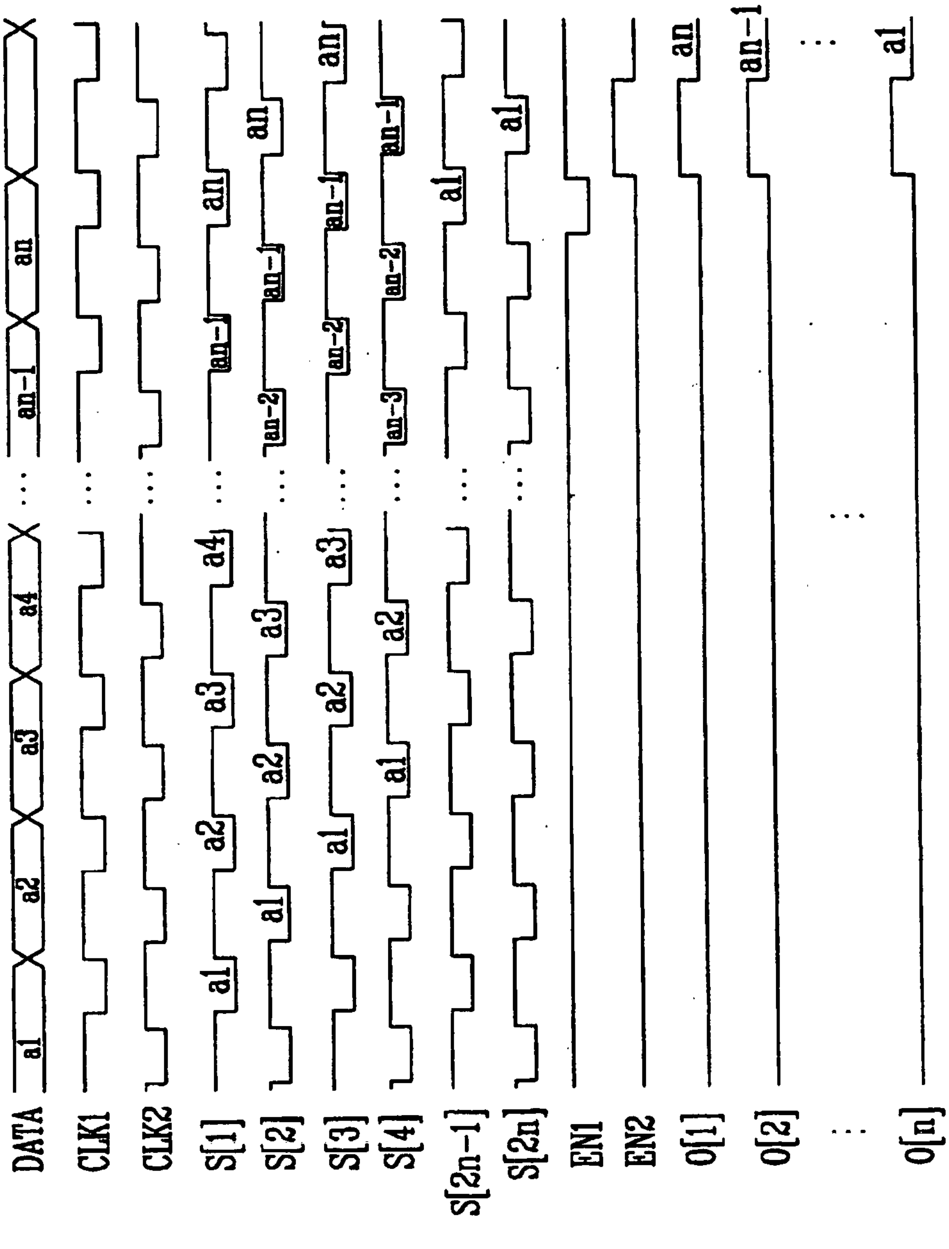

DATA
CLK1
CLK2
S[1]
S[2]
S[3]
S[4]
S[2n-1]
S[2n]
EN1
EN2
O[1]
O[2]
O[n]
a1
a2
a3
a4
an-1
an

FIG. 8

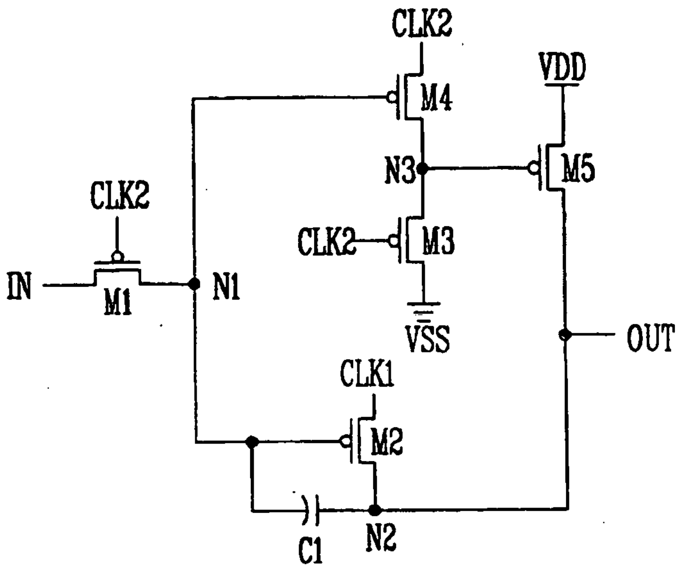

CLK2
VDD
M4
N3
M5
CLK2
CLK2
M3
IN
M1
N1
VSS
OUT
CLK1
M2
C1
N2

FIG. 9

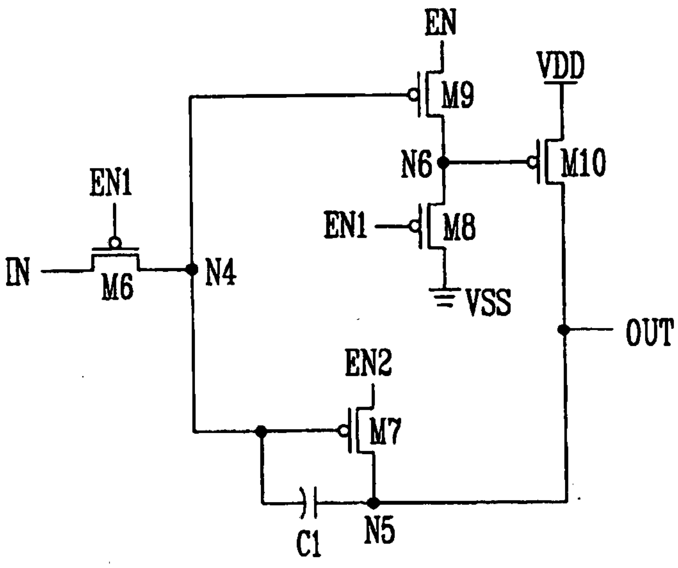

EN
VDD
M9
N6
M10
EN1
EN1
M8
IN
M6
N4
VSS
OUT
EN2
M7
C1
N5

FIG. 10

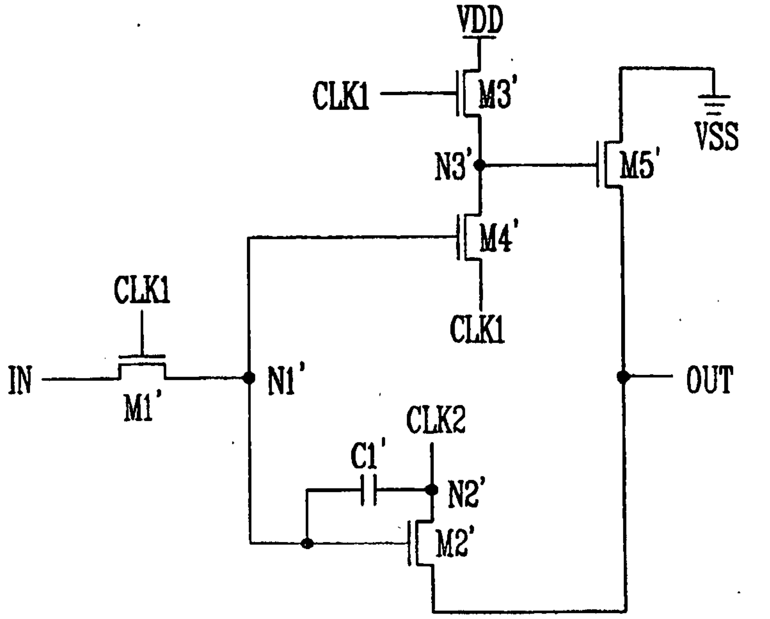

VDD
CLK1
M3'
VSS
N3'
M5'
M4'
CLK1
CLK1
IN
M1'
N1'
OUT
CLK2
C1'
N2'
M2'

FIG. 11

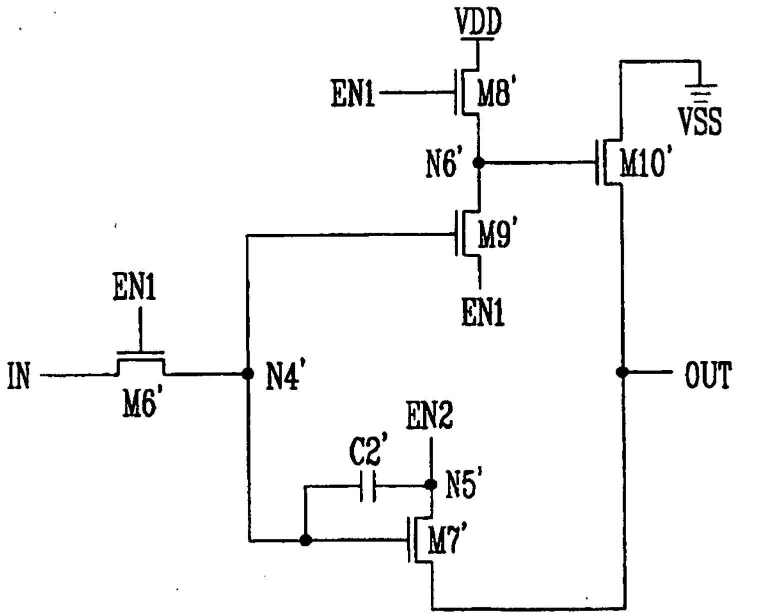

VDD
EN1
M8'
VSS
N6'
M10'
M9'
EN1
EN1
IN
M6'
N4'
OUT
EN2
C2'
N5'
M7'

FIG. 12

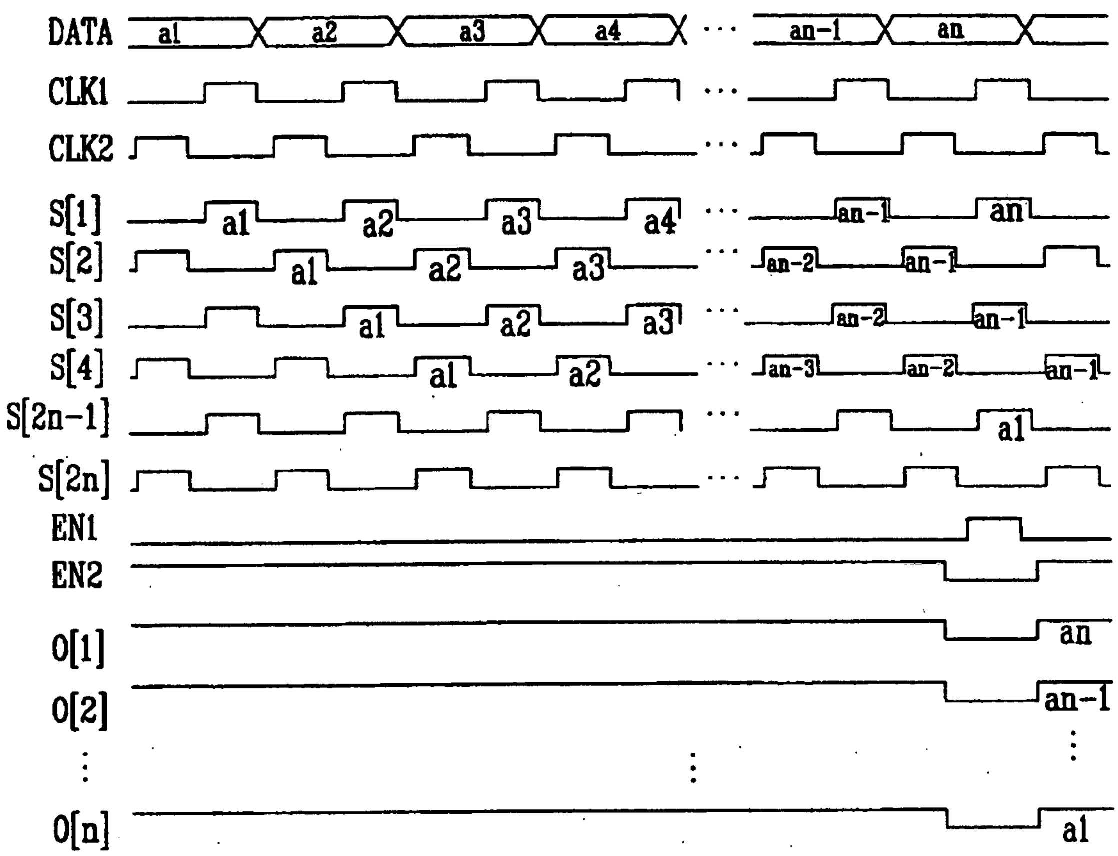
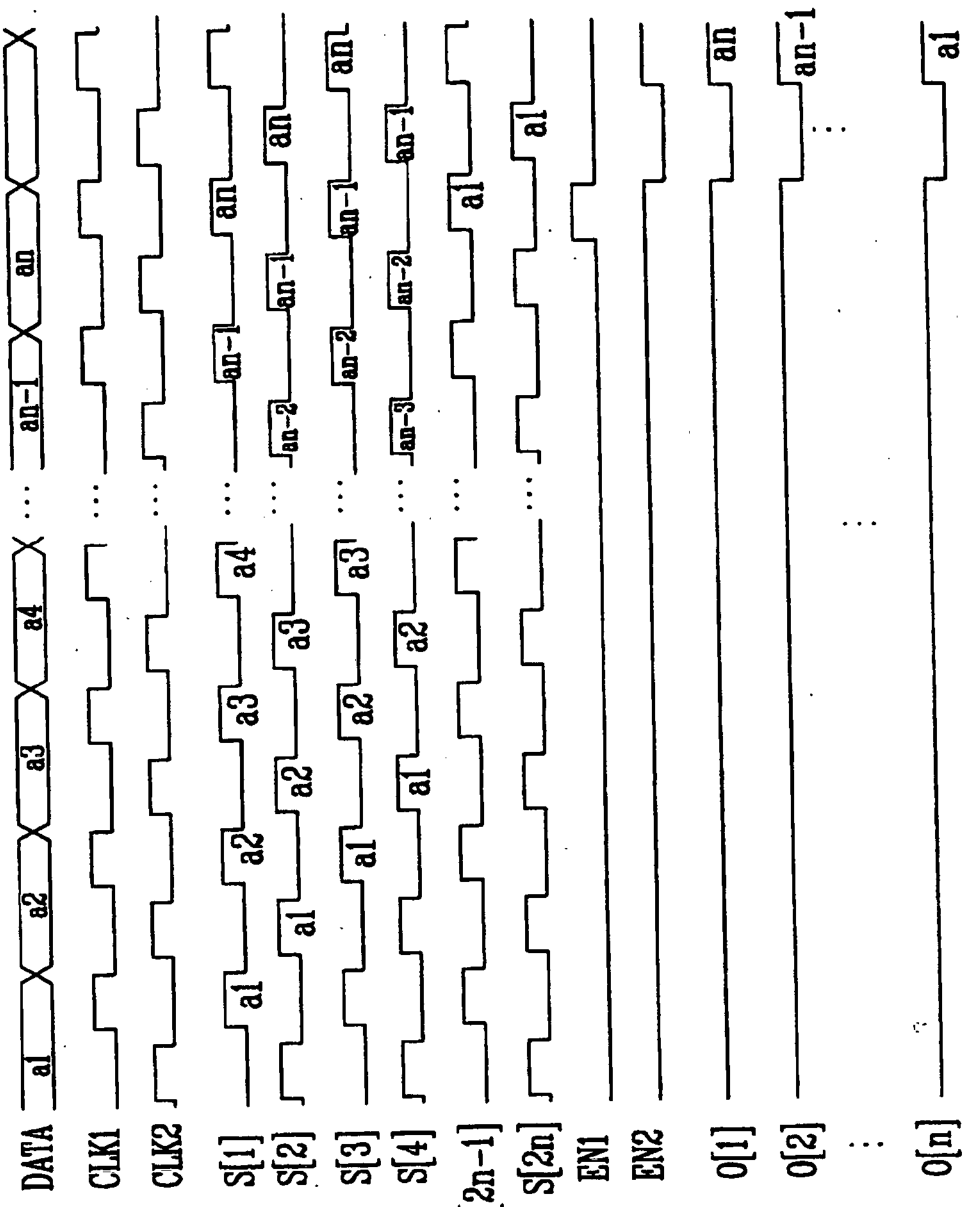

DATA
a1
a2
a3
a4
an-1
an
CLK1
CLK2
S[1]
S[2]
S[3]
S[4]
S[2n-1]
S[2n]
EN1
EN2
O[1]
O[2]
O[n]
an-2
an-3

FIG. 13


DATA
CLK1
CLK2
S[1]
S[2]
S[3]
S[4]
S[2n-1]
S[2n]
EN1
EN2
O[1]
O[2]
O[n]
a1
a2
a3
a4
an-1
an

REFERENCES CITED IN THE DESCRIPTION

Patent documents cited in the description

- US 6784864 B **[0010]**

专利名称(译)	数据驱动电路和使用它的电致发光显示器		
公开(公告)号	EP1783739B1	公开(公告)日	2013-09-11
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[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
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发明人	SHIN, DONG YONG, SAMSUNG SDI CO, LTD.		
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优先权	1020050106171 2005-11-07 KR		
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外部链接	Espacenet		

摘要(译)

数据驱动电路可以包括移位寄存器单元，该移位寄存器单元还可以包括串联连接的多个第一级，其可以接收数据信号并且可以输出数据信号，其中每个第一级可以接收从前一级输出的数据信号。锁存单元，包括多个第二级，其中每个第二级可以连接到不同的预定第一级，其中每个第二级接收从预定第一级输出的数据信号，其中第二级的数量可以是基本上是第一级的数量的一半，并且连接到锁存单元的D / A转换器可以接收数字数据信号并输出模拟数据信号。

FIG. 1
(RELATED ART)

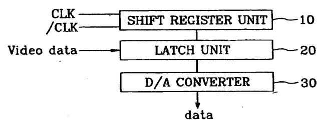

FIG. 2
(RELATED ART)