(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 399 254 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
31.08.2016 Bulletin 2016/35

(21) Application number: **10704705.2**

(22) Date of filing: **12.02.2010**

(51) Int Cl.:
G09G 3/32 *(2006.01)* ***H01L 27/32*** *(2006.01)*

(86) International application number:
PCT/US2010/024050

(87) International publication number:
WO 2010/096341 (26.08.2010 Gazette 2010/34)

(54) CHIPLET DRIVER PAIRS FOR TWO-DIMENSIONAL DISPLAY

CHIPLET-TREIBERPAARE FÜR EIN ZWEIDIMENSIONALES DISPLAY

PAIRES D'EXCITATEURS DE MICROPUCES POUR AFFICHAGE BIDIMENSIONNEL

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

(30) Priority: **17.02.2009 US 372132**

(43) Date of publication of application:
28.12.2011 Bulletin 2011/52

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Description

FIELD OF THE INVENTION

[0001] The present invention relates to display devices having a substrate with distributed, independent chiplets for controlling a pixel array.

BACKGROUND OF THE INVENTION

[0002] Flat-panel display devices are widely used in conjunction with computing devices, in portable devices, and for entertainment devices such as televisions. Such displays typically employ a plurality of pixels distributed over a substrate to display images. Each pixel incorporates several, differently colored light-emitting elements commonly referred to as sub-pixels, typically emitting red, green, and blue light, to represent each image element. As used herein, pixels and sub-pixels are not distinguished and refer to a single light-emitting element. A variety of flat-panel display technologies are known, for example plasma displays, liquid crystal displays, and light-emitting diode (LED) displays.

[0003] Light emitting diodes (LEDs) incorporating thin films of light-emitting materials forming light-emitting elements have many advantages in a flat-panel display device and are useful in optical systems. U.S. Patent No. 6,384,529 to Tang et al. shows an organic LED (OLED) color display that includes an array of organic LED light-emitting elements. Alternatively, inorganic materials can be employed and can include phosphorescent crystals or quantum dots in a polycrystalline semiconductor matrix. Other thin films of organic or inorganic materials can also be employed to control charge injection, transport, or blocking to the light-emitting-thin-film materials, and are known in the art. The materials are placed upon a substrate between electrodes, with an encapsulating cover layer or plate. Light is emitted from a pixel when current passes through the light-emitting material. The frequency of the emitted light is dependent on the nature of the material used. In such a display, light can be emitted through the substrate (a bottom emitter) or through the encapsulating cover (a top emitter), or both.

[0004] LED devices can comprise a patterned light-emissive layer wherein different materials are employed in the pattern to emit different colors of light when current passes through the materials. Alternatively, one can employ a single emissive layer, for example, a white-light emitter, together with color filters for forming a full-color display, as is taught in U.S. Patent No. 6,987,355 by Cok. It is also known to employ a white sub-pixel that does not include a color filter, for example, as taught in U.S. Patent No. 6,919,681 by Cok et al. A design has been taught employing an unpatterned white emitter together with a four-color pixel including red, green, and blue color filters and sub-pixels and an unfiltered white sub-pixel to improve the efficiency of the device (see, e.g. U.S. Patent No. 7,230,594 to Miller, et al).

[0005] Two different methods for controlling the pixels in a flat-panel display device are generally known: active-matrix control and passive-matrix control. In a passive-matrix device, the substrate does not include any active electronic elements (e.g. transistors). An array of row electrodes and an orthogonal array of column electrodes in a separate layer are formed over the substrate; the overlapping intersections between the row and column electrodes form the electrodes of a light-emitting diode. External driver chips then sequentially supply current to each row (or column) while the orthogonal column (or row) supplies a suitable voltage to illuminate each light-emitting diode in the row (or column). Therefore, a passive-matrix design employs 2n connections to produce n^2 separately controllable light-emitting elements. However, a passive-matrix drive device is limited in the number of rows (or columns) that can be included in the device since the sequential nature of the row (or column) driving creates flicker. If too many rows are included, the flicker can become perceptible. Moreover, the currents necessary to drive an entire row (or column) in a display can be problematic the power required for the non-imaging pre-charge and discharge steps of PM driving become dominant as the area of the PM display grows. These problems limit the physical size of a passive-matrix display.

[0006] In an active-matrix device, active control elements are formed of thin films of semiconductor material, for example amorphous or poly-crystalline silicon, coated over the flat-panel substrate. Typically, each sub-pixel is controlled by one control element and each control element includes at least one transistor. For example, in a simple active-matrix organic light-emitting (OLED) display, each control element includes two transistors (a select transistor and a power transistor) and one capacitor for storing a charge specifying the luminance of the sub-pixel. Each light-emitting element typically employs an independent control electrode and an electrode electrically connected in common. Control of the light-emitting elements is typically provided through a data signal line, a select signal line, a power connection and a ground connection. Active-matrix elements are not necessarily limited to displays and can be distributed over a substrate and employed in other applications requiring spatially distributed control. The same number of external control lines (except for power and ground) can be employed in an active-matrix device as in a passive-matrix device. However, in an active- matrix device, each light-emitting element has a separate driving connection from a control circuit and is active even when not selected for data deposition so that flicker is eliminated.

[0007] One common, prior-art method of forming active-matrix control elements typically deposits thin films of semiconductor materials, such as silicon, onto a glass substrate and then forms the semiconductor materials into transistors

and capacitors through photolithographic processes. The thin-film silicon can be either amorphous or polycrystalline. Thin-film transistors (TFTs) made from amorphous or polycrystalline silicon are relatively large and have lower performance compared to conventional transistors made in crystalline silicon wafers. Moreover, such thin-film devices typically exhibit local or large-area non-uniformity across the glass substrate that results in non-uniformity in the electrical performance and visual appearance of displays employing such materials. In such active-matrix designs, each light-emitting element requires a separate connection to a driving circuit.

[0008] Employing an alternative control technique, Matsumura et al., in U.S. Patent Application Publication No. 2006/0055864, describe crystalline silicon substrates used for driving LCD displays. The application describes a method for selectively transferring and affixing pixel-control devices made from first semiconductor substrates onto a second planar display substrate. Wiring interconnections within the pixel-control device and connections from busses and control electrodes to the pixel-control device are shown.

[0009] Document US 2004/0239586 A1 discloses a flat panel display which includes a flexible substrate; a passive matrix display having an array of pixels formed on a side of the flexible substrate, and row and column electrodes formed on the same side of the flexible substrate and connected to the pixels for providing data and selection signals to the pixel elements; a plurality of electrical contacts formed on the same side of the substrate and electrically connected to the row and column electrodes; and discrete data and selection drivers located on the same side of the flexible substrate around the periphery of the passive matrix display and electrically connected to the electrical contacts for driving the pixels of the passive matrix display.

[0010] Document US 2002/0053881 discloses a flat display apparatus having proved luminance, contrast and response of display, and applicable for assembling a large flat display apparatus free from the discontinuity of display and having improved luminance, contrast and response of display. The flat display apparatus includes a plurality of signal electrodes divided into at least three regions; a plurality of scanning electrodes intersecting to the plurality of signal electrodes; and a plurality of displaying signal supplying circuits for independently supplying display signals to the signal electrodes in each divided region. The flat display apparatus may include a display panel in which a plurality of signal electrodes and a plurality of scanning electrodes are intersected.; The signal electrodes are divided into two or more regions, and a plurality of feeding portions for supplying signal to the signal electrodes are provided on a rear surface of the display panel.

[0011] Since a conventional passive-matrix display design is limited in size and number of light-emitting elements, and an active-matrix design using TFTs has lower electrical performance, there is a need for an improved control method for display devices employing LEDs that overcomes these problems.

SUMMARY OF THE INVENTION

[0012] In accordance with the present invention, a display device according to claim 1 is provided.

[0013] The present invention has the advantage that, by providing a display device having a plurality of pixels associated into two-dimensional arrays, each two-dimensional array having distributed, separate row and column chiplet drivers, performance is improved and the number of components and connections is reduced. Further, by having separate row and column driver chiplets, each chiplet can be made with the lowest cost semiconductor fabrication process available for each chiplet.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

FIG. 1A is a cross-section of a chiplet having two connections to the bottom electrodes of light-emitting diodes according to an embodiment of the present invention;

FIG. 1B is a cross- section of a chiplet having two connections to the top electrodes of light-emitting diodes according to an embodiment of the present invention;

FIG. 2 is a schematic of an array of pixels in a pixel group driven by a row driver chiplet and a column driver chiplet according to a simplified illustration of an example;

FIG. 3 is a schematic of an array of pixels in a pixel group driven by two row driver chiplets and two column driver chiplets according to an embodiment of the present invention;

FIG. 4 is a schematic of an array of pixels in a pixel group driven by three row driver chiplets and three column driver chiplets according to an embodiment of the present invention;

FIG. 5 is a schematic of a display device having a pixel array divided into mutually exclusive pixel groups, each group including a row driver chiplet and a column driver chiplet according to a simplified illustration of an example;

FIGS. 6A and 6B are schematics of chiplets having at least one pixel connection portion and at least one circuitry portion according to alternative embodiments of the present invention;

FIGS. 7A-7C are illustrations of various connections between chiplet connection pads and row electrodes according

to various embodiments of the present invention;
FIG. 8 is a schematic of a display device having multiple chiplets connected to a common, parallel-connected buss routed to avoid the chiplet devices according to another embodiment of the present invention;
FIG. 9 is a schematic of a display device having multiple, serially-connected chiplets connected by a buss according to another embodiment of the present invention;
FIG. 10A is a cross section of a chiplet having different connection pads according to another embodiment of the present invention;
FIG. 10B is a top view of FIG. 10A in an embodiment of the present invention;
FIG. 11 is a schematic of multiple pixel groups with chiplet drivers according to an embodiment of the present invention;
FIG. 12 is a partial schematic of multiple pixel groups with chiplet drivers according to another example and
FIG. 13 is a partial schematic of multiple pixel groups with chiplet drivers according to yet another example.

[0015] Because the various layers and elements in the drawings have greatly different sizes, the drawings are not to scale.

DETAILED DESCRIPTION OF THE INVENTION

[0016] Referring to FIGS. 3 and 1A, in one embodiment of the present invention, a display device includes a substrate 10 and a first layer having an array of row electrodes 16 formed in rows across the substrate 10 in a first direction and a second layer having an array of column electrodes 12 formed in columns across the substrate 10 in a second direction different from the first direction. Pixel 30 locations are formed over the substrate 10, where the row and column electrodes 16, 12 overlap. One or more layers 14 of light-emitting material are formed between the row and column electrodes 16, 12 to form a two-dimensional array of pixels 30 in the pixel locations. A plurality of row driver chiplets 20A, 20C and a separate plurality of column driver chiplets 20B, 20D are distributed relative to the substrate 10, each row driver chiplet 20A, 20C exclusively connected to and controlling an independent set of row electrodes 16 and each column driver chiplet 20B, 20D exclusively connected to and controlling an independent set of column electrodes 12. The chiplets are distributed relative to the pixel array so that, as intended herein, the chiplets are located within the pixel array, for example above, below, or adjacent to the light-emitting elements in the light-emitting area of the display and are not located exclusively around the periphery of the two-dimensional pixel array. For example, the chiplets can be distributed over the substrate and located in a layer beneath the pixels, between the pixels and the substrate. Alternatively, the chiplets can be located over the substrate adjacent to and interspersed between the pixels in a common layer, or in layers above or below the pixels.

[0017] Referring to FIG. 1A, light-emitting diodes 15 include one or more layers 14 of light-emitting formed between the row and column electrodes 16, 12 to form a plurality of pixels 30, each pixel 30 located where the row and column electrodes 16, 12 overlap. Pixels can be subpixels that emit different colors of light (e.g. red, green, blue, or white) to form a full-color display in response to a current passed through the one or more layers 14 of light-emitting material by the row and column electrodes 16, 12. In this disclosure, pixels, sub-pixels, and light-emitting elements all refer to a light-emitting diode 15. However, pixels can also include light-controlling or switching material controlled by electrodes and are included in the present invention.

[0018] A plurality of chiplets 20, both row driver chiplets 20A and column driver chiplets 20B, are located over the substrate 10, the number of chiplets 20 being less than the number of pixels 30. Each chiplet has a substrate 28 that is independent and separate from the display device substrate 10. As used herein, distributed relative to the substrate 10 means that the chiplets 20 are not located solely around the periphery of the pixel array but are located within the display area, that is, beneath, above, or between pixels in the light-emitting area of the display.

[0019] The pixels 30 in the array can be subdivided into mutually exclusive pixel groups 32, each pixel group 32 typically having a rectangular arrangement of pixels 30. Each pixel group has a separate array of group row electrodes and a separate array of group column electrodes that are electrically independent from the group row electrodes and group column electrodes of any other pixel group. Each pixel group has one or more separate group row driver chiplets and one or more separate group column driver chiplets located over the substrate, each group row driver chiplet exclusively connected to and controlling pixel group row electrodes and each group column driver chiplet exclusively connected to and controlling pixel group column electrodes. By exclusively connected to and controlling is meant that each group column electrode is connected to only one group column driver chiplet. Likewise, each group row electrode is connected to only one group row driver chiplet. FIGS. 2, 3 and 4 illustrate a single pixel group 32; FIGS. 5, 8, 9, and 11 illustrate multiple pixel groups. In an alternative embodiment, a row driver chiplet can be connected to two or more independent sets of row electrodes or a column driver chiplet can be connected to two or more independent sets of column electrodes. A chiplet thus drives the row or column electrodes of two or more pixel groups.

[0020] Each chiplet 20 can include circuitry 22 for controlling the pixels 30 to which the chiplet 20 is connected through

connection pads 24. The circuitry 22 can include storage elements 26 that store a value representing a desired luminance for each pixel 30 to which the chiplet 20 is connected in a row or column, the chiplet 20 using such value to control either the row electrodes 16 or the column electrodes 12 connected to the pixel 30 to activate the pixel 30 to emit light. For example, if a row driver chiplet 20A is connected to 8 rows and a column driver chiplet 20B is connected to 8 columns, eight storage elements 26 can be employed to store luminance information for the 8 pixels connected to the row or column driver chiplet in one row or column. When a row or column is activated by an external controller, luminance information can be supplied to the corresponding chiplet 20. In one embodiment of the present invention, two storage elements 26 can be employed for each row or column connected to a chiplet, so that luminance information can be stored in one of the storage elements 26 while the other storage element 26 is employed to display luminance information. In yet another embodiment of the present invention, one or two storage elements 26 can be employed for each light-emitting pixel 30 to which the chiplet 20 is connected.

[0021] A planarization layer 18 can be employed to form a smooth surface over which the row and column electrodes 16, 12, and the light-emitting layer 14 can be formed. As shown in FIG. 1A, the connection pads 24 of the chiplet 20 can connect to the bottom electrode of the light-emitting diode 15, here shown as the column electrode 12 and indicated with cross section line 1A in FIG. 2. Alternatively, as shown in FIG. 1B, the connection pads 24 of the chiplet 20 can connect to the top electrode of the light-emitting diode, here shown as the row electrode 16 and indicated with cross section line 1B in FIG. 2. In this way, the connection pads of a chiplet 20 can connect to either row electrodes 16 or column electrodes 12. In FIG. 2 the connection pads of chiplet 20B are distinguished as column connection pads 24B connected to column electrodes 12. The connection pads of chiplet 20A are distinguished as row connection pads 24A connected to row electrodes 16. FIG. 2 is a simplified figure drawn for illustrative purposes as an example and omits the row and column electrodes 16, 12 that can be formed directly above the chiplets 20.

[0022] Fig. 3 according to an embodiment illustrates the use of two row driver chiplets 20A, 20C and two column driver chiplets 20B, 20D within a pixel group 32. As shown in FIG. 3 the row and column connection pads 24A and 24B are carefully laid out on the substrate 10 to avoid electrical shorts between the row and column electrodes 16, 12, by providing enough space between the row connection pads 24A and the column electrodes 12 and by providing enough space between the column connection pads 24B and the row electrodes 16. In an exemplary embodiment shown in FIG. 4, three row driver chiplets 20A. 20C, 20E and three column driver chiplets 20B, 20D, 20F are employed. (The chiplets are shown in dotted lines above the electrodes for clarity, rather than below; also in FIG. 11.) The column connection pads 24B can be covered with row electrodes 16 to increase the overlapping area defining the pixel 30, thereby increasing the aperture ratio of the display device and the lifetime of the display. Depending on the tolerances of the manufacturing process used to construct the present invention, the column electrodes 12 can be increased in size so long as there is not an electrical short between the column electrodes 12 and the row connection pads 24A and row electrodes 16, thereby improving the device aperture ratio.

[0023] Referring to FIG. 4, an embodiment of a display device of the present invention can include multiple chiplets (20A-20D) distributed over the pixel group 32 formed by the intersections of row and column electrodes 16, 12. Each chiplet 20 is connected to a mutually exclusive subset of row electrodes 16 and column electrodes 12. As shown in FIG. 4, chiplet 20A is connected to the top 6 row electrodes 16 in the pixel group 32. Chiplet 20C is connected to the central 6 row electrodes 16 in the pixel group 32. Chiplet 20E is connected to the bottom 6 row electrodes 16 in the pixel group 32. Chiplet 20B is connected to the left-most 6 column electrodes 12 in the pixel group 32. Chiplet 20D is connected to the central 6 column electrodes 12 in the pixel group 32. Chiplet 20F is connected to the right-most 6 column electrodes 12 in the pixel group 32. Hence, the pixel group 32 has 18 by 18 or 324 elements controlled by six chiplets with 6 connection pads each. A careful examination of FIG. 4 shows that each chiplet controls a separate group of row or column electrodes 16, 12.

[0024] FIG. 5 is a more detailed illustration of an example with four pixel arrays 32A, 32B, 32C, 32D, having only two chiplets per pixel array. These pixel arrays are pixel groups formed by the intersection of row and column electrodes. The pixels in pixel array 32A are driven by group row electrodes 16A and group column electrodes 12A. The group row electrodes 16A are driven by row driver chiplet 20A and the group column electrodes 12A are driven by column driver chiplet 20B. The pixels in pixel array 32B are driven by group row electrodes 16B and group column electrodes 12B. The group row electrodes 16B are driven by row driver chiplet 20E and the group column electrodes 12B are driven by column driver chiplet 20F. The pixels in pixel array 32C are driven by group row electrodes 16C and group column electrodes 12C. The group row electrodes 16C are driven by row driver chiplet 20C and the group column electrodes 12C are driven by column driver chiplet 20D. The pixels in pixel array 32D are driven by group row electrodes 16D and group column electrodes 12D. The group row electrodes 16D are driven by row driver chiplet 20G and the group column electrodes 12D are driven by column driver chiplet 20H. None of the group electrodes in one pixel group are electrically connected to the group electrodes in another pixel group. For simplicity, the row and column driver chiplets in each pixel group are illustrated as overlapping. In a practical embodiment, the chiplets would not overlap but, as shown in FIG. 7A, have connection pads 24 connected to the electrodes with routed wires 52. The chiplets can have a long dimension D1 and a short dimension D2 and the long dimension D1 can be parallel to the first direction or the second direction (FIG.

10B) of the row or column electrodes, respectively.

[0025] The present invention provides reduced costs over the prior art. For example, if a conventional, active-matrix backplane were employed to drive the 324 pixels 30 of FIG. 4, a relatively low-performance and expensive thin-film semiconductor backplane would be necessary. If an alternative chiplet design described in commonly assigned, above-cited U.S. Patent Application No. 12/191,462 were employed, 12 pixels 30 can be driven by each chiplet so that 27 chiplets would be required. In contrast, the present invention requires only six chiplets.

[0026] The row driver chiplets need not have the same circuitry as the column driver chiplets, the same number of connection pads, or the same layout of connection pads. Moreover, the number of rows that the row driver chiplets drive need not be the same as the number of columns that the column driver chiplets drive. Although the pixel arrays are illustrated as square (the number of row electrodes is the same as the number of column electrodes) the pixel groups (or the entire pixel array) or the pixels, need not be square. Hence, the number of row driver chiplets need not be the same as the number of column driver chiplets. Moreover, the row driver and column driver chiplets can be located in a wide variety of locations, so long as they are electrically connected to the corresponding row or column electrodes. For example, in FIG. 4, the column driver chiplets can be moved along columns and the row driver chiplets can be moved along rows, as desired. Locations are generally selected to provide routing paths for electrical connections to chiplets and to space the chiplets from each other at a required positional tolerance suitable for the manufacturing process employed. Moreover, the technology, processes, or construction of row driver chiplets can be different from the technology, processes, or construction of column driver chiplets. By construction is meant the process limitations, materials, and manufacturing processes employed to construct the row and column driver chiplets. For example, one chiplet can employ digital designs, processes, and materials and the other can employ analog. Alternatively, one chiplet can employ relatively high-voltage designs, processes, and materials and the other relatively low-voltage. Again, one chiplet can employ semiconductor substrate materials or doping (e.g. n- or p-doping) and the other different materials or doping. The chiplets can also employ different circuit schematics. The chiplet controlling the independent drive direction requires circuitry to receive image data, requires one or more memory locations for image data per output, and controls relatively small currents and functions better when implemented with smaller line-width semiconductor processes. The chiplet controlling the common drive direction does not receive image data or require image data memory, but is required to switch relatively large currents and therefore functions better when implemented with wider line-width semiconductor processes.

[0027] In a further embodiment of the present invention, the chiplet connection pads 24 are not directly connected to a row or column electrode. Such connections can cause the chiplets 20 to be larger than necessary. Referring to FIG. 7A in another embodiment of the present invention, the chiplets 20 can be aligned in any orientation with respect to the pixel groups 32 and substrate 10, including aligning an edge of a chiplet 20 with a row or column electrode 16 or 12. Indeed, different chiplets 20 can be differently aligned. As shown in FIG. 7A, a long dimension of a chiplet 20 is aligned with row electrodes 16. Moreover, a display device can include a plurality of row driver chiplets and a separate plurality of column driver chiplets distributed over the substrate, each chiplet having a long dimension and a short dimension, the long dimension of the row driver chiplet orthogonal to the long dimension of the column driver chiplet. Such an arrangement facilitates the routing of busses in a single layer, for example a metal layer.

[0028] Connection pads 24 are connected with wiring 52 to the row electrodes 16. Vias 50 (also shown in FIG. 1B) can be employed to connect from one wiring layer to another and are formed between, for example, the column electrodes 12 to avoid electrical shorts with the column electrodes 12. Since considerable wiring 52 can be necessary to electrically connect the connection pads 24 to the row and column electrodes 16, 12, a top emitter configuration can be preferred, in which the top electrode (e.g. 16 in FIG. 1A and 1B) is transparent and the bottom electrode (e.g. 12 in FIG. 1A and 1B) can be reflective. The substrate 10 can also be opaque.

[0029] Referring to FIG. 6A, the chiplets 20 can have a pixel connection portion 21A at one end of the chiplet 20 and a circuitry portion 21B connected to a buss at the other end. Referring to FIG. 6B and 7B, the chiplets 20 can have circuitry connection portions 21B at each end of the chiplet 20 connected to a buss 42 through a buss connection pad 25 and a pixel connection portion 21 B in the middle. Alternatively, no separate portions can be employed. FIG. 7C illustrates the case wherein the connection pads 24 are larger than the electrodes 12, 16 or wires 52 and a via 50 is employed to connect the connection pad 24 to the row electrode 16. Referring to FIG. 10A, additional connection pads 25 for connecting to a buss 42 can also be provided in the chiplet 20 and can be located at a circuitry portion of a chiplet or at either end of a chiplet 20, or in the center of the chiplet 20. Internal chiplet connections 44 can be employed to route buss connections from one end of a chiplet 20 to another end. Referring to FIGS. 10A and 10B, each chiplet can have a first group of connection pads 24 connected to the row or column electrodes and second group of connection pads 25 connected to a control buss, wherein the first and second groups of connection pads are spatially separated. As shown in FIGS. 10A and 10B, each chiplet also can have a third group of connection pads 25 in the center of the chiplet connected to a control buss; the first, second, and third groups of connection pads are spatially separated. In an alternative embodiment of the present invention, connection pads 24 for the row and column electrodes can be grouped into spatially separated groups (FIGS. 10A, 10B).

[0030] Chiplets can have a single row (e.g. FIG. 7B), or multiple rows (e.g. 2, FIG. 7C), of connection pads 24 along a long axis of the chiplet. Circuitry in the row driver chiplets can be different from the circuitry in the column driver chiplets. In particular, row drivers can employ very simple circuits with lower data rates but can switch large currents compared to a column driver. Moreover, the number of rows controlled by the row driver chiplet can be different from the number of columns driven by the column driver chiplet. Hence different circuits can be used in the different drivers, or even different manufacturing processes or technologies employed to make the different drivers.

[0031] Referring to FIG. 8 in another embodiment of the present invention, the chiplets 20 can be connected to an external controller 40 through a buss 42. The buss 42 can be a serial, parallel, or point-to-point buss and can be digital or analog. A serial buss, shown in FIG. 9, is one in which data is retransmitted from one chiplet to the next on electrically separated electrical connections; a parallel buss, shown in FIG. 8, is one in which data is simultaneously broadcast to all of the chiplets on an electrically common electrical connection. The buss 42 is connected to the chiplets to provide signals, such as power, ground, data, or select signals. More than one buss 42 separately connected to one or more controllers 40 can be employed. In FIG. 8, a chiplet arrangement corresponding to that shown in FIG. 3 is illustrated. This arrangement has the advantage of providing areas on the device substrate 10 that are not occupied with chiplets 10 and that can then be used for routing busses 42. For example, as shown in FIG. 8, the pixel connection areas of pixel arrays 32A, 32B, 32C, and 32D are only partially occupied with chiplets (e.g. 20A, 20B, 20C, and 20D in pixel array 32A). The remainder of the area within the pixel arrays can be employed for routing buss 42 wires. Hence, in some embodiments of the present invention, the busses can have a serpentine path. FIG. 8 illustrates an embodiment in which the buss 42 is connected in parallel to all of the chiplets. In an alternative embodiment shown in FIG. 9, buss 42 connections can be routed serially through row driver chiplets (e.g. 20A, 20C in pixel array 32A) and through column driver chiplets (e.g. 20B, 20D in pixel array 32A). Such buss arrangements can be useful when only a single metal layer is provided in the device for electrical connections, thereby reducing processing steps and improving manufacturing efficiency. Thus, a control buss can be located in a third layer separate from the first and second layers used for the row and column electrodes. Spaced-apart connection pads can have a pitch 23 (FIG. 10B) formed on the chiplets and openings formed through a planarization layer to expose the connection pads. The control buss can have a first portion that extends through the openings to the connection pads, and a separate second portion having a width greater than the pitch of the connection pads. Thus, the electrical resistance of the control buss can be lower in the areas between chiplets.

[0032] Referring to FIG. 11, in a further embodiment of the present invention, a plurality of two-dimensional pixel arrays 32A-D of pixels can be located over a common substrate 10, each two-dimensional pixel array 32A-D having an electrically independent separate set of group row electrodes, an electrically independent separate set of group column electrodes, and chiplets 20. Hence, the structure described above (e.g. FIG. 3) can be replicated on a larger substrate 10. Each two-dimensional array structure can operate independently to reduce electrode impedance, precharge and discharge power consumption, and flicker. The structures can be connected to a common buss 42 (as shown). Thus, according to an embodiment of the present invention, a display device can include a substrate, a first layer having a plurality of electrically independent arrays of row electrodes formed in rows across the substrate in a first direction and a second layer having a corresponding plurality of electrically independent arrays of column electrodes formed in columns across the substrate in a second direction different from the first direction wherein the first and second electrodes overlap to form pixel locations, one or more layers of light-emitting material formed between the row and column electrodes to form a plurality of electrically independent two-dimensional arrays of pixels, the pixels being located in the pixel locations, a plurality of driver chiplets and a separate plurality of column driver chiplets for each electrically independent array distributed relative to the corresponding two-dimensional array of pixels, the chiplet layer having for each array located over the substrate a plurality of row driver chiplets and a separate plurality of column driver chiplets, each row driver chiplet exclusively connected to and controlling an independent set of row electrodes for the corresponding array and each column driver chiplet exclusively connected to and controlling an independent set of column electrodes for the corresponding array.

[0033] Referring to FIG. 12, a partial schematic of an example employs chiplets having one row of connection pads arranged over a substrate. The pixels 30 are illustrated rather than the electrodes. The row driver chiplets 20A drive pixels. Half of the pixels 30A are driven by one column driver chiplet 20B and half of the pixels 30B are driven by another column driver chiplet 20D. Bus 42A is connected in parallel to all of the row driver chiplets in a row and buss 42B is connected to both row and column driver chiplets, passing through the row driver chiplets 20A and over the column driver chiplets 20B, 20D. Buss 42C passes through only the column driver chiplets. This arrangement has the advantage of locating the busses in a single layer.

[0034] Referring to FIG. 13, a partial schematic of an example employs chiplets having two rows of connection pads arranged over a substrate. As in FIG. 12, the pixels 30 are illustrated rather than the electrodes and the busses 42A, 42B, 42C are likewise connected. In this example, the chiplets have two rows of connection pads. Each chiplet can drive multiple separate pixel groups and, as in FIG. 12, the pixels in a pixel group can be divided among different combinations of row and column drivers. This arrangement also has the advantage of locating the busses in a single layer.

[0035] In both FIGS. 12 and 13, the single layer of wiring is, at least partly, enabled by an electrical connection connected to a row driver chiplet and passing through a column driver chiplet. Alternatively, the electrical connection can be connected to a column driver chiplet and passing through a row driver chiplet. By 'connected to' is meant that the wire makes an electrical connection through a connection pad on a chiplet to circuitry within the chiplet. In contrast, an electrical connection passing through the chiplet is connected to a connection pad at one location on the chiplet, passes through circuitry in the chiplet, and reemerges from a separate connection pad at a different location and different connection pad on the chiplet and connects to another chiplet. In this fashion, signals (e.g. clock, reset, power, ground) can be connected to all of the chiplets in an array of chiplets without conflicting with other signals connected in an orthogonal direction in the same wiring layer. For example, in FIGS. 12 and 13, buss 42A is routed in one direction and buss 42B is routed in an orthogonal direction in the same wiring layer. Buss 42A passes over buss 42B where buss 42B pass through a chiplet so that both busses 42A and 42B can be formed in the same wiring layer.

[0036] An additional advantage of these designs is that the wires can be patterned using low-cost methods since there is ample area available for the wiring. In the previously referenced chiplet design of commonly-assigned, above-cited U.S. Patent Application No. 12/191,462. the spacing of the pads on the chiplets was typically 20 um, requiring wiring alignment accuracy to within 5 um. This required that the back-plane wires and insulators be patterned with expensive fabrication equipment. In the present design, it is possible to use patterning methods to form the wiring and insulator layers that have much wider limits of variations - on the order of the size of a pixel. For example systems developed for printed circuit board fabrication use low-cost photo-masks and proximity exposure tools capable of making 25 um lines and 25 um spaces. These are much lower cost than TFT photo-masks and the TFT stepper exposure tools. This results in a back-plane fabrication process requiring less capital expense, less operating expense, and reduced manufacturing cycle time.

[0037] Referring to FIG. 11, in operation, a controller 40 receives and processes an information signal according to the needs of the display device and transmits the processed signal through one or more busses 42 to each chiplet 20 (shown above the row and column electrodes for clarity) in the device. The processed signal includes luminance information for each light-emitting pixel element 30 corresponding to the associated row and column driver chiplets 20. The luminance information can be stored in a storage element 26 corresponding to each light-emitting pixel element 30. The chiplets then sequentially activate the row and column electrodes to which they are connected. When both the row and column electrode for a pixel is activated, current can flow through the pixel defined by the row and column electrode to emit light. Typically, an entire group of row electrodes or group of column electrodes within a pixel group is activated simultaneously by activating all of the group column electrodes and one row electrode at once (or *vice versa*). The column electrodes are controlled to provide the individual luminance desired for each pixel in the row. Then a second row is selected and the process repeats until all of the rows are activated and all of the pixels emit light. The process can then repeat. Separate pixel groups can function independently. Note that the designation of "row" and "column" is arbitrary and the functions of row and column electrodes can be reversed. Although FIG. 11 illustrates an embodiment in which every chiplet 20 is directly connected to a buss 42, an alternative embodiment can include a serial buss connection arrangement such as that illustrated in FIG. 9.

[0038] Although the sequential activation of separate rows (or columns) in a display device can induce flicker, employing multiple, independently controlled pixel groups 32 reduces the number of rows or columns in each separately controlled pixel group 32. Since the pixel groups 32 are simultaneously activated, flicker can be greatly reduced. Moreover, because the group row electrodes and group column electrodes are connected only within a pixel group 32, the group row electrodes and group column electrodes are short, reducing the electrode capacitance and resistance and the need for high-power driving circuitry in the chiplets 20, and the power consumption of the display is reduced. Hence, the portion of time that each pixel row (or column) emits light is increased, flicker is decreased, and current densities decreased at a desired luminance.

[0039] The busses 42 can supply a variety of signals, including timing (e.g. clock) signals, data signals, select signals, power connections, or ground connections. The signals can be analog or digital, for example digital addresses or data values. Analog data values can be supplied as charge. The storage elements 26 can be digital (for example including flip-flops) or analog (for example including capacitors for storing charge).

[0040] In various embodiments of the present invention, the row driver or column driver chiplets 20 distributed over the substrate 10 can be identical. However, a unique identifying value, i.e. an ID, can be associated with each chiplet 20. The ID can be assigned before or, preferably, after the chiplet 20 is located over the substrate 10 and the ID can reflect the relative position of the chiplet 20 on the substrate 10, that is, the ID can be an address. For example, the ID can be assigned by passing a count signal from one chiplet 20 to the next in a row or column. Separate row or column ID values can be used.

[0041] The controller 40 can be implemented as a chiplet and affixed to the substrate 10. The controller 40 can be located on the periphery of the substrate 10. or can be external to the substrate 10 and include a conventional integrated circuit.

[0042] According to various embodiments of the present invention, the chiplets 20 can be constructed in a variety of

ways, for example with one or two rows of connection pads 24 along a long dimension of a chiplet 20 (FIGS. 7B. 7C). The interconnection busses 42 and wires 52 can be formed from various materials and can use various methods for deposition on the device substrate. For example, the interconnection busses 42 and wires 52 can be metal, either evaporated or sputtered, for example aluminum or aluminum alloys. Alternatively, the interconnection busses 42 and wires 52 can be made of cured conductive inks or metal oxides. In one cost-advantaged embodiment, the interconnection busses 42 and wires 52 are formed in a single layer.

[0043] The present invention is particularly useful for multi-pixel device embodiments employing a large device substrate, e.g. glass, plastic, or foil, with a plurality of chiplets 20 arranged in a regular arrangement over the device substrate 10. Each chiplet 20 can control a plurality of pixels 30 formed over the device substrate 10 according to the circuitry in the chiplet 20 and in response to control signals. Individual pixel groups or multiple pixel groups can be located on tiled elements, which can be assembled to form the entire display.

[0044] According to the present invention, chiplets 20 provide distributed pixel control elements over a substrate 10. A chiplet 20 is a relatively small integrated circuit compared to the device substrate 10 and includes circuit 22 including wires, connection pads, passive components such as resistors or capacitors, or active components such as transistors or diodes, formed on an independent substrate 28. Chiplets 20 are separately manufactured from the display substrate 10 and then applied to the display substrate 10. The chiplets 20 are preferably manufactured using silicon or silicon on insulator (SOI) wafers using known processes for fabricating semiconductor devices. Each chiplet 20 is then separated prior to attachment to the device substrate 10. The crystalline base of each chiplet 20 can therefore be considered a substrate 28 separate from the device substrate 10 and over which the chiplet circuitry 22 is disposed. The plurality of chiplets 20 therefore has a corresponding plurality of substrates 28 separate from the device substrate 10 and each other. In particular, the independent substrates 28 are separate from the substrate 10 on which the pixels 30 are formed and the areas of the independent, chiplet substrates 28, taken together, are smaller than the device substrate 10. Chiplets 20 can have a crystalline substrate 28 to provide higher performance active components than are found in, for example, thin-film amorphous or polycrystalline silicon devices. Chiplets 20 can have a thickness preferably of 100 um or less, and more preferably 20 um or less. This facilitates formation of the adhesive and planarization layer 18 over the chiplet 20 that can then be applied using conventional spin-coating techniques. According to one embodiment of the present invention, chiplets 20 formed on crystalline silicon substrates are arranged in a geometric array and adhered to a device substrate (e.g. 10) with adhesion or planarization materials. Connection pads 24 on the surface of the chiplets 20 are employed to connect each chiplet 20 to signal wires, power busses and row or column electrodes (16, 12) to drive pixels 30. Chiplets 20 can control at least four pixels 30.

[0045] Since the chiplets 20 are formed in a semiconductor substrate, the circuitry of the chiplet can be formed using modem lithography tools. With such tools, feature sizes of 0.5 microns or less are readily available. For example, modem semiconductor fabrication lines can achieve line widths of 90 nm or 45 nm and can be employed in making the chiplets of the present invention. The chiplet 20, however, also requires connection pads 24 for making electrical connection to the wiring layer provided over the chiplets once assembled onto the display substrate 10. The connection pads 24 are sized based on the feature size of the lithography tools used on the display substrate 10 (for example 5 um) and the alignment of the chiplets 20 to the wiring layer (for example +/- 5um). Therefore, the connection pads 24 can be, for example, 15 um wide with 5 um spaces between the pads. The pads will therefore generally be significantly larger than the transistor circuitry formed in the chiplet 20.

[0046] The pads can generally be formed in a metallization layer on the chiplet over the transistors. It is desirable to make the chiplet with as small a surface area as possible to enable a low manufacturing cost.

[0047] By employing chiplets with independent substrates (e.g. including crystalline silicon) having circuitry with higher performance than circuits formed directly on the substrate (e.g. amorphous or polycrystalline silicon), a device with higher performance is provided. Since crystalline silicon has not only higher performance but also much smaller active elements (e.g. transistors), the circuitry size is reduced. A useful chiplet can also be formed using micro-electromechanical (MEMS) structures, for example as described in "A novel use of MEMS switches in driving AMOLED", by Yoon, Lee, Yang, and Jang, Digest of Technical Papers of the Society for Information Display, 2008, 3.4, p. 13.

[0048] The device substrate 10 can include glass and the wiring layers made of evaporated or sputtered metal or metal alloys, e.g. aluminum or silver, formed over a planarization layer (e.g. resin) patterned with photolithographic techniques known in the art. The chiplets 20 can be formed using conventional techniques well established in the integrated circuit industry.

[0049] The present invention can be employed in devices having a multi-pixel infrastructure. In particular, the present invention can be practiced with LED devices, either organic or inorganic, and is particularly useful in information-display devices. In a preferred embodiment, the present invention is employed in a flat-panel OLED device composed of small-molecule or polymeric OLEDs as disclosed in, but not limited to U.S. Patent No. 4,769,292, to Tang et al., and U.S. Patent No. 5,061,569, to VanSlyke et al. Inorganic devices, for example, employing quantum dots formed in a polycrystalline semiconductor matrix (for example, as taught in U.S. Patent Application Publication No. 2007/0057263 by Kahen), and employing organic or inorganic charge-control layers, or hybrid organic/inorganic devices can be employed. Many

combinations and variations of organic or inorganic light-emitting displays can be used to fabricate such a device, including active-matrix displays having either a top- or a bottom-emitter architecture.

PARTS LIST

[0050]

D1	long dimension
D2	short dimension
10	substrate
12	column electrode
12A, 12B	column electrode group
12C, 12D	column electrode group
14	light-emitting layer
15	light-emitting diode
16	row electrode
16A, 16B	row electrode group
16C, 16D	row electrode group
18	planarization layer
20	chiplet
20A, 20C, 20E, 20G	row driver chiplet
20B, 20D, 20F, 20H	column driver chiplet
21 A	pixel connection portion
21 B	control circuit connection portion
22	circuitry
23	connection pad pitch
24	connection pad
24A	row connection pad
24B	column connection pad
25	buss connection pad
26	storage element
28	chiplet substrate
30, 30A, 30B	pixel
32	pixel group
32A, 32B, 32C, 32D,	pixel array
40	controller
42, 42A, 42B, 42C	buss
44	internal chiplet connection
50	via a
52	wire

Claims

1. A display device, comprising:

(a) a substrate (10);
(b) a first layer having an array of row electrodes (16) formed in rows across the substrate in a first direction and a second layer having an array of column electrodes (12) formed in columns across the substrate in a second direction different from the first direction wherein the row and column electrodes (16, 12) overlap to form pixel locations (30);
(c) one or more layers of light-emitting material (14) formed between the row and column electrodes (16, 12) to form a two-dimensional array of pixels (30), the pixels (30) being located in the pixel locations (30);
(d) a plurality of row driver chiplets (20A, 20C, 20E, 20G) and a separate plurality of column driver chiplets (20B, 20D, 20F, 20H) distributed relative to the two-dimensional array of pixels (30) and formed over the substrate directly beneath the row and column electrodes, each row driver chiplet (20A, 20C, 20E, 20G) exclusively connected to and controlling an independent set of row electrodes (16) and each column driver chiplet (20B, 20D, 20F, 20H) exclusively connected to and controlling an independent set of column electrodes (12);

(e) circuitry (22) in each row driver chiplet (20A, 20C, 20E, 20G) for controlling the row electrodes (16); and
(f) circuitry (22) in each column driver chiplet (20B, 20D, 20F, 20H) for controlling the column electrodes (12),

wherein the circuitry (22) in each row driver chiplet (20A, 20C, 20E, 20G) is configured for lower data rates than the circuitry (22) in each column driver chiplet (20B, 20D, 20F, 20H).

2. The display device of claim 1, wherein each chiplet (20) has a storage element (26) for at least each pixel (30) to which it is connected in a row or column, the storage element (26) storing a value representing a desired luminance for each pixel (30) and the chiplet (20) using such value to control the row electrodes (16) or column electrodes (12) connected to the pixel (30).

3. The display device of claim 1, further comprising connection pads on each row driver chiplet (20A, 20C, 20E, 20G)or column driver chiplet (20B, 20D, 20F, 20H), each connection pad connected to a separate row electrode or column electrode, respectively.

4. The display device of claim 3, wherein the number, location, or layout of the connection pads (24) for the row driver chiplet (20A, 20C, 20E, 20G) is different from the number, location, or layout of the connection pads (24) for the column driver chiplet (20B, 20D, 20F, 20H).

5. The display device of claim 3, wherein the connection pads (24) form a single or double row, and/or wherein the row electrodes (16) have a row pitch, the column electrodes (12) have a column pitch, and the chiplets (20) have connection pad pitch (23), and wherein the connection pad pitch (23) is the same as the row pitch or column pitch.

6. The display device of claim 1, including one or more serial or parallel buss connections (42) electrically connected to each chiplet (20), and preferably wherein a buss (42) provides a power or ground electrical connection or a buss (42) transmits a data signal or a control signal.

7. The display device of claim 1, further including a control buss (42) and wherein each chiplet (20) has a first group of connection pads (24) connected to the row and column electrodes and second group of connection pads (25) connected to the control buss (24), wherein the first and second groups of connection pads (24, 25) are spatially separated.

8. The display device of claim 7, wherein each chiplet (20) has a third group of connection pads (25) connected to the control buss (24), wherein the first, second, and third groups of connection pads are spatially separated.

9. The display device of claim 7, wherein each chiplet (20) further includes a third group of connection pads connected to the row and column electrodes (16, 12) wherein the first, second, and third groups of connection pads are spatially separated.

10. The display device of claim 1, wherein the chiplet has a long dimension (D1) and a short dimension (D2) and wherein the long dimension (D1) is parallel to the first or second direction (D2).

11. The display device of claim 1, further including a third layer separate from the first and second layers and a control buss (42) located in the third layer.

12. The display device of claim 11, further comprising spaced- apart connection pads (24) having a pitch (23) formed on the chiplets (20) and openings formed to expose the connection pads and wherein the control buss (42) has a first portion that extends through the openings to the connection pads (24), and a separate second portion having a width greater than the pitch of the connection pads.

13. The display device of claim 1, wherein the row driver chiplets (20A, 20C, 20E, 20G) and the column drive chiplets (20B, 20D, 20F, 20H) have a different size, or wherein the number of row driver chiplets (20A, 20C, 20E, 20G) is different from the number of column driver chiplets (20B, 20D, 20F, 20H), or wherein the number of rows (16) controlled by the row driver chiplet (20A, 20C, 20E, 20G) is different from the number of columns (12) driven by the column driver chiplet (20B, 20D, 20F, 20H).

14. The display device of claim 1, wherein the circuitry construction in the row driver chiplet (20A, 20C, 20E, 20G) is different from the circuitry construction for the column driver chiplet (20B, 20D, 20F, 20H).

15. The display device of claim 1, further comprising an electrical connection connected to a row driver chiplet (20A, 20C, 20E, 20G) and passing through a column driver chiplet (20B, 20D, 20F, 20H) or further comprising an electrical connection connected to a column driver chiplet and passing through a row driver chiplet.

Patentansprüche

1. Anzeigeeinrichtung, die umfasst:

(a) ein Substrat (10);
(b) eine erste Schicht mit einer Anordnung von Reihenelektroden (16), die in Reihen über das Substrat in einer ersten Richtung ausgebildet sind, und einer zweiten Schicht mit einer Anordnung von Spaltenelektroden (12), die in Spalten über das Substrat in einer sich von der ersten Richtung unterscheidenden zweiten Richtung ausgebildet sind, wobei die Reihen- und Spaltenelektroden (16, 12) überlappen, um Pixelpositionen (30) zu bilden;
(c) eine oder mehrere Schicht(en) aus einem Licht emittierende Material (14), die zwischen den Reihen- und Spaltenelektroden (16, 12) ausgebildet ist/sind, um eine zweidimensionale Anordnung von Pixeln (30) zu bilden, wobei die Pixel (30) an den Pixelpositionen (30) angeordnet sind.
(D) eine Mehrzahl von Reihentreiber-Chiplets (20A, 20C, 20E, 20G) und eine separate Mehrzahl von Spaltentreiber-Chiplets (20B, 20D, 20F, 20H), die relativ zu der zweidimensionalen Anordnung von Pixeln (30) verteilt und über dem Substrat unmittelbar unterhalb der Reihen- und Spaltenelektroden ausgebildet sind, wobei jedes Reihentreiber-Chiplet (20A, 20C, 20E, 20G) ausschließlich mit einem unabhängigen Satz von Reihenelektroden (16) verbunden ist und diesen steuert und jedes Spaltentreiber-Chiplet (20B, 20D, 20F, 20H) ausschließlich mit einem unabhängigen Satz von Spaltenelektroden (12) verbunden ist und diesen steuert;
(e) einen Schaltkreis (22) in jedem Reihentreiber-Chiplet (20A, 20C, 20E, 20G) zum Steuern der Reihenelektroden (16); und
(f) einen Schaltkreis (22) in jedem Spaltentreiber-Chiplet (20B, 20D, 20F, 20H) zum Steuern der Spaltenelektroden (12),

wobei der Schaltkreis (22) in jedem Reihentreiber-Chiplet (20A, 20C, 20E, 20G) für geringere Datenraten konfiguriert ist als der Schaltkreis (22) in jedem Spaltentreiber-Chiplet (20B, 20D, 20F, 20H).

2. Anzeigeeinrichtung nach Anspruch 1, bei der jedes Chiplet (20) ein Speicherelement (26) für mindestens jeden Pixel (30) hat, mit dem es in einer Reihe oder Spalte verbunden ist, wobei das Speicherelement (26) einen Wert speichert, der eine gewünschte Helligkeit für jeden Pixel (30) repräsentiert und das Chiplet (20) einen derartigen Wert verwendet, um die mit dem Pixel (30) verbundenen Reihenelektroden (16) oder Spaltenelektroden (12) zu steuern.

3. Anzeigeeinrichtung nach Anspruch 1, die ferner Verbindungspads an jedem Reihentreiber-Chiplet (20A, 20C, 20E, 20G) oder jedem Spaltentreiber-Chiplet (20B, 20D, 20F, 20H) umfasst, wobei jedes Verbindungspad mit einer separaten Reihenelektrode bzw. Spaltenelektrode verbunden ist.

4. Anzeigeeinrichtung nach Anspruch 3, bei der sich die Anzahl, die Position oder das Layout der Verbindungspads (24) für das Reihentreiber-Chiplet (20A, 20C, 20E, 20G) von der Anzahl, der Position oder dem Layout der Verbindungspads (24) für das Spaltentreiber-Chiplet (20B, 20D, 20F, 20H) unterscheidet.

5. Anzeigeeinrichtung nach Anspruch 3, bei der die Verbindungspads (24) eine einzige oder eine Doppelreihe bilden und/oder bei der die Reihenelektroden (16) einen Reihenabstand haben, die Spaltenelektroden (12) einen Spaltenabstand haben und die Chiplets (20) einen Verbindungspadabstand (23) haben, und bei der der Verbindungspadabstand (23) der gleiche ist wie der Reihenabstand oder der Spaltenabstand.

6. Anzeigeeinrichtung nach Anspruch 1, die einen oder mehrere serielle(n) oder parallele(n) Busanschluss/Busanschlüsse (42) umfasst, der/die elektrisch mit jedem Chiplet (20) verbunden ist/sind, wobei vorzugsweise ein Bus (42) eine elektrische Energie- oder Erdungsverbindung bereitstellt oder ein Bus (42) ein Datensignal oder ein Steuersignal überträgt.

7. Anzeigeeinrichtung nach Anspruch 1, die ferner einen Steuerungsbus (42) umfasst, und wobei jedes Chiplet (20) eine mit den Reihen- und Spaltenelektroden verbundene erste Gruppe von Verbindungspads (24) und eine mit dem

Steuerungsbus (42) verbundene zweite Gruppe von Verbindungspads (25) hat, wobei die ersten und zweiten Gruppen von Verbindungspads (24, 25) räumlich voneinander getrennt sind.

8. Anzeigeeinrichtung nach Anspruch 7, bei der jedes Chiplet (20) eine mit dem Steuerungsbus (42) verbundene dritte Gruppe von Verbindungspads (25) hat, wobei die ersten, zweiten und dritten Gruppen von Verbindungspads räumlich voneinander getrennt sind.

9. Anzeigeeinrichtung nach Anspruch 7, bei der jedes Chiplet (20) ferner eine mit den Reihen- und Spaltenelektroden (16, 12) verbundene dritte Gruppe von Verbindungspads hat, wobei die ersten, zweiten und dritten Gruppen von Verbindungspads räumlich voneinander getrennt sind.

10. Anzeigeeinrichtung nach Anspruch 1, bei der das Chiplet eine lange Dimension (D1) und eine kurze Dimension (D2) hat und wobei die lange Dimension (D1) parallel zu der ersten oder zweiten Richtung (D2) ist.

11. Anzeigeeinrichtung nach Anspruch 1, die ferner eine von den ersten und zweiten Schichten getrennte dritte Schicht und einen in der dritten Schicht angeordneten Steuerungsbus (42) umfasst.

12. Anzeigeeinrichtung nach Anspruch 11, die ferner auf den Chiplets (20) ausgebildete, voneinander beanstandete Verbindungspads (24) mit einem Abstand (23) und Öffnungen umfasst, die ausgebildet sind, um die Verbindungspads freizulegen, und wobei der Steuerungsbus (42) einen ersten Abschnitt, der sich durch die Öffnungen zu den Verbindungspads (24) erstreckt, und einen separaten zweiten Abschnitt hat, der eine Breite hat, die größer ist als der Abstand der Verbindungspads.

13. Anzeigeeinrichtung nach Anspruch 1, bei der die Reihentreiber-Chiplets (20A, 20C, 20E, 20G) und die Spaltentreiber-Chiplets (20B, 20D, 20F, 20H) eine unterschiedliche Größe haben, oder wobei sich die Anzahl der Reihentreiber-Chiplets (20A, 20C, 20E, 20G) von der Anzahl der Spaltentreiber-Chiplets (20B, 20D, 20F, 20H) unterscheidet, oder wobei sich die Anzahl der von den Reihentreiber-Chiplets (20A, 20C, 20E, 20G) gesteuerten Reihen (16) von der Anzahl der von den Spaltentreiber-Chiplets (20B, 20D, 20F, 20H) gesteuerten Spalten (12) unterscheidet.

14. Anzeigeeinrichtung nach Anspruch 1, bei der sich die Schaltkreiskonstruktion in dem Reihentreiber-Chiplet (20A, 20C, 20E, 20G) von der Schaltkreiskonstruktion für das Spaltentreiber-Chiplet (20B, 20D, 20F, 20H) unterscheidet.

15. Anzeigeeinrichtung nach Anspruch 1, die ferner eine elektrische Verbindung umfasst, die mit einem Reihentreiber-Chiplet (20A, 20C, 20E, 20G) verbunden ist und durch ein Spaltentreiber-Chiplet (20B, 20D, 20F, 20H) hindurch führt, oder ferner eine elektrische Verbindung umfasst, die mit einem Reihentreiber-Chiplet verbunden ist und durch ein Spaltentreiber-Chiplet hindurch führt.

Revendications

1. Dispositif d'affichage, comprenant :

(a) un substrat (10) ;
(b) une première couche ayant une matrice d'électrodes de rangées (16) formées en rangées au travers du substrat dans un premier sens et une deuxième couche ayant une matrice d'électrodes de colonnes (12) formées en colonnes au travers du substrat dans un deuxième sens différent du premier sens dans lequel les électrodes de rangées et de colonnes (16, 12) se chevauchent pour former des emplacements de pixels (30) ;
(c) une ou plusieurs couche(s) de matériau électroluminescent (14) formée(s) entre les électrodes de rangées et de colonnes (16, 12) pour former une matrice bidimensionnelle de pixels (30), les pixels (30) étant situés dans les emplacements de pixels (30) ;
(d) une pluralité de micropuces d'excitation (20A, 20C, 20E, 20G) de rangées et une pluralité séparée de micropuces d'excitation (20B, 20D, 20F, 20H) de colonnes distribuées par rapport à la matrice bidimensionnelle de pixels (30) et formées pardessus le substrat directement en-dessous des électrodes de rangées et de colonnes, chaque micropuce d'excitation (20A, 20C, 20E, 20G) de rangées exclusivement connectée à et commandant un ensemble indépendant d'électrodes de rangées (16) et chaque micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes exclusivement connectée à et commandant un ensemble indépendant d'électrodes de colonnes (12) ;
(e) un ensemble de circuits (22) dans chaque micropuce d'excitation (20A, 20C, 20E, 20G) de rangées pour

commander les électrodes de rangées (16) ; et
(f) un ensemble de circuits (22) dans chaque micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes pour commander les électrodes de colonnes (12),

dans lequel l'ensemble de circuits (22) dans chaque micropuce d'excitation (20A, 20C, 20E, 20G) de rangées est configuré pour un débit de données moindre que l'ensemble de circuits (22) dans chaque micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes.

2. Dispositif d'affichage selon la revendication 1, dans lequel chaque micropuce (20) a un élément de stockage (26) pour au moins chaque pixel (30) auquel elle est connectée dans une rangée ou une colonne, l'élément de stockage (26) stockant une valeur représentant une luminance désirée pour chaque pixel (30) et la micropuce (20) utilisant une telle valeur pour commander les électrodes de rangées (16) ou les électrodes de colonnes (12) connectées au pixel (30).

3. Dispositif d'affichage selon la revendication 1, comprenant en outre des plots de connexion sur chaque micropuce d'excitation (20A, 20C, 20E, 20G de rangées) ou micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes, chaque plot de connexion connecté à une électrode de rangée ou une électrode de colonnes séparée, respectivement.

4. Dispositif d'affichage selon la revendication 3, dans lequel le nombre, l'emplacement ou la disposition des plots de connexion (24) pour la micropuce d'excitation (20A, 20C, 20E, 20G) de rangées sont différents du nombre, de l'emplacement ou de la disposition des plots de connexion (24) pour la micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes.

5. Dispositif d'affichage selon la revendication 3, dans lequel les plots de connexion (24) forment une rangée unique ou double, et/ou dans lequel les électrodes de rangées (16) ont un pas de rangées, les électrodes de colonnes (12) ont un pas de colonnes, et les micropuces (20) ont un pas (23) de plots de connexion, et dans lequel le pas (23) de plots de connexion est le même que le pas de rangées ou le pas de colonnes.

6. Dispositif d'affichage selon la revendication 1, incluant une ou plusieurs connexion(s) de bus en série ou en parallèle électriquement connectées à chaque micropuce (20), et préférablement dans lequel un bus (42) fournit une connexion électrique d'alimentation ou de terre ou bien un bus (42) transmet un signal de données ou un signal de commande.

7. Dispositif d'affichage selon la revendication 1, incluant en outre un bus (42) de commande et dans lequel chaque micropuce (20) a un premier groupe de plots de connexion (24) connectés aux électrodes de rangées et de colonnes et un deuxième groupe de plots de connexion (25) connectés au bus (42) de commande, dans lequel les premier et deuxième groupes de plots de connexion (24, 25) sont spatialement séparés.

8. Dispositif d'affichage selon la revendication 7, dans lequel chaque micropuce (20) a un troisième groupe de plots de connexion (25) connectés au bus (42) de commande, dans lequel les premier, deuxième et troisième groupe de plots de connexion sont spatialement séparés.

9. Dispositif d'affichage selon la revendication 7, dans lequel chaque micropuce (20) inclut en outre un troisième groupe de plots de connexion connectés aux électrodes de rangées et de colonnes (16, 12) dans lequel les premier, deuxième et troisième groupe de plots de connexion sont spatialement séparés.

10. Dispositif d'affichage selon la revendication 1, dans lequel la micropuce a une dimension longue (D1) et une dimension courte (D2) et dans lequel la dimension longue (D1) est parallèle au premier ou au deuxième sens (D2).

11. Dispositif d'affichage selon la revendication 1, incluant en outre une troisième couche séparée des première et deuxième couches et un bus (42) de commande situé dans la troisième couche.

12. Dispositif d'affichage selon la revendication 11, comprenant en outre des plots de connexion (24) espacés ayant un pas (23) formés sur les micropuces (20) et des ouvertures formées pour exposer les plots de connexion et dans lequel le bus (42) de commande a une première partie qui s'étend à travers les ouvertures jusqu'aux plots de connexion (24), et une deuxième partie séparée ayant une largeur plus grande que le pas des plots de connexion.

13. Dispositif d'affichage selon la revendication 1, dans lequel les micropuces d'excitation (20A, 20C, 20E, 20G) de

rangées et les micropuces d'excitation (20B, 20D, 20F, 20H) de colonnes ont une taille différente, ou dans lequel le nombre de micropuces d'excitation (20A, 20C, 20E, 20G) de rangées est différent du nombre de micropuces d'excitation (20B, 20D, 20F, 20H) de colonnes, ou dans lequel le nombre de rangées (16) commandées par la micropuce d'excitation (20A, 20C, 20E, 20G) de rangées est différent du nombre de colonnes (12) excitées par la micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes.

14. Dispositif d'affichage selon la revendication 1, dans lequel la construction d'ensemble de circuits dans la micropuce d'excitation (20A, 20C, 20E, 20G) de rangées est différente de la construction d'ensemble de circuits pour la micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes.

15. Dispositif d'affichage selon la revendication 1, comprenant en outre une connexion électrique connectée à une micropuce d'excitation (20A, 20C, 20E, 20G) de rangées et passant à travers une micropuce d'excitation (20B, 20D, 20F, 20H) de colonnes ou comprenant en outre une connexion électrique connectée à une micropuce d'excitation de colonnes et passant à travers une micropuce d'excitation de rangées.

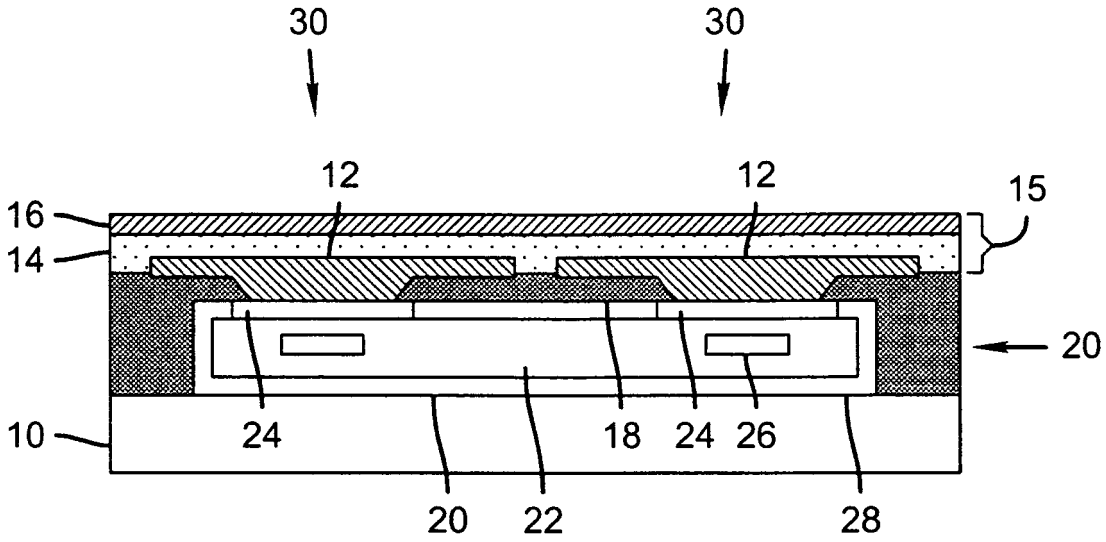
30
30
12
12
15
16
14
20
10
24
18
24
26
20
22
28

FIG. 1A

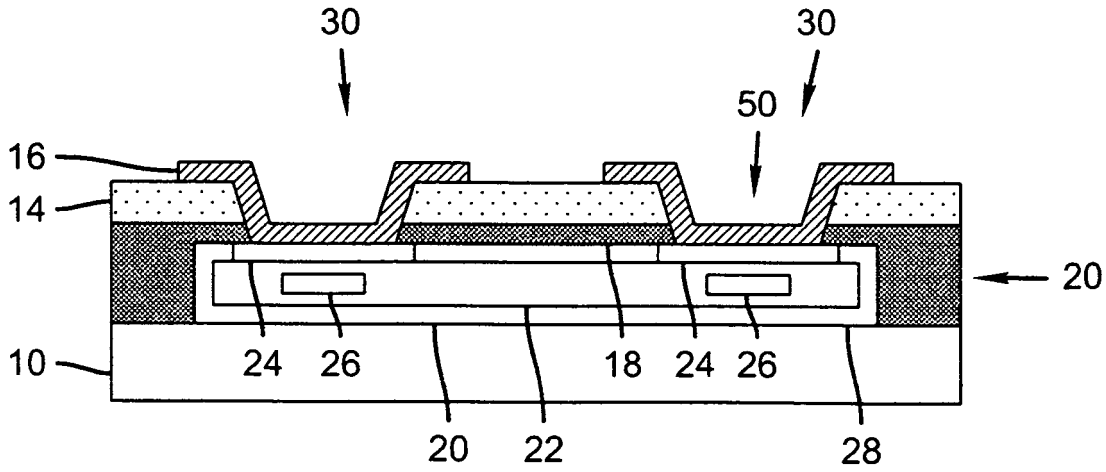
30
30
50
16
14
20
10
24
26
18
24
26
20
22
28

FIG. 1B

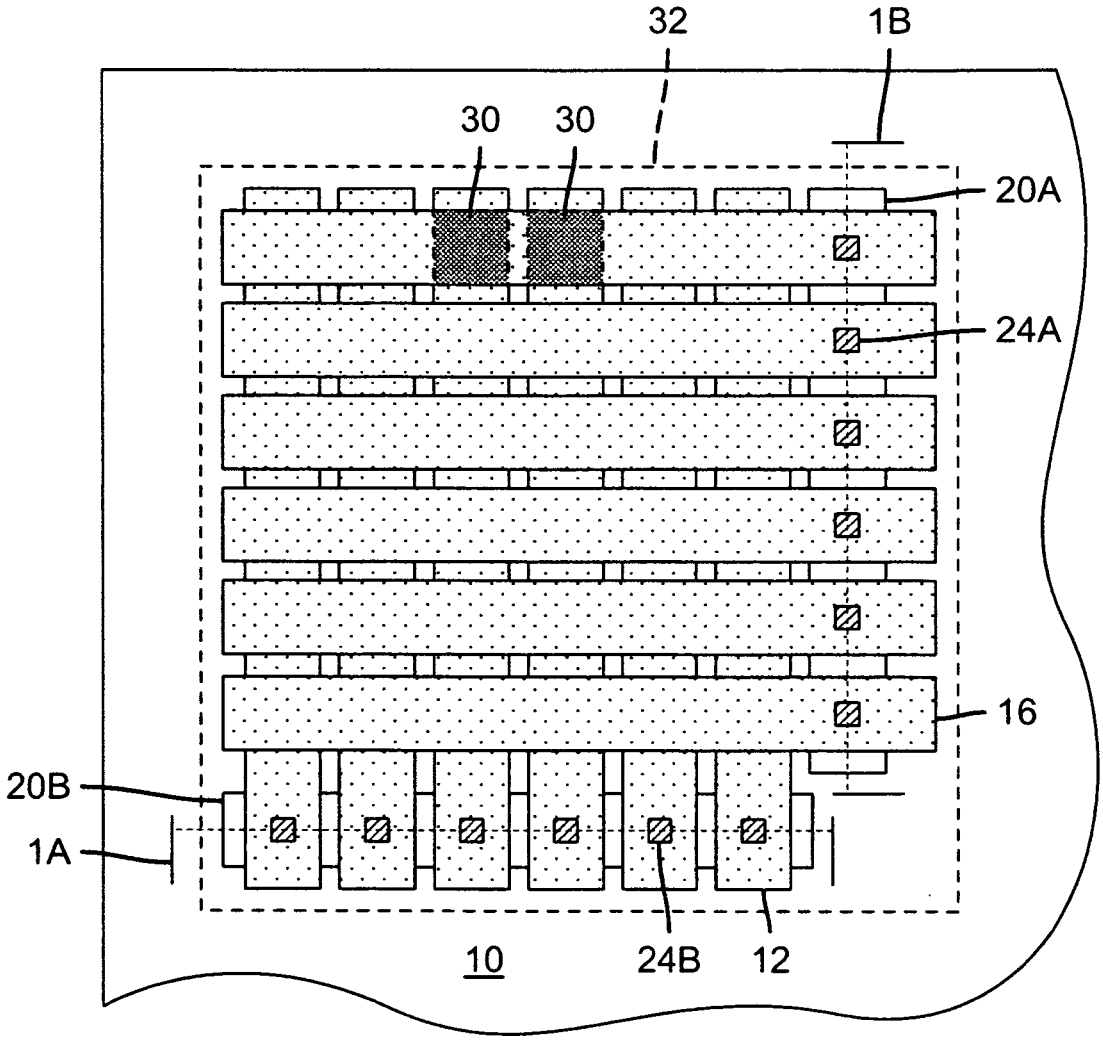

FIG. 2

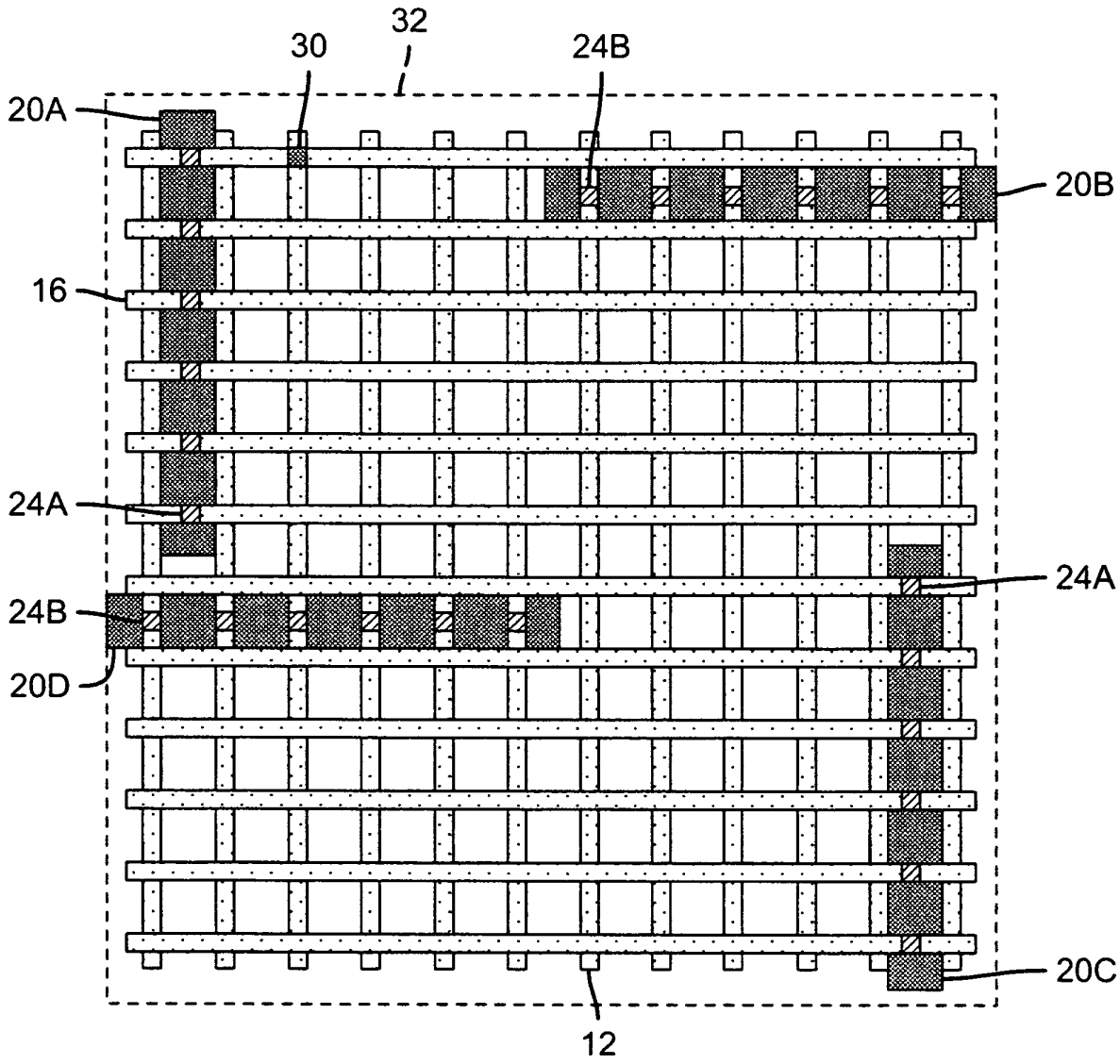

FIG. 3

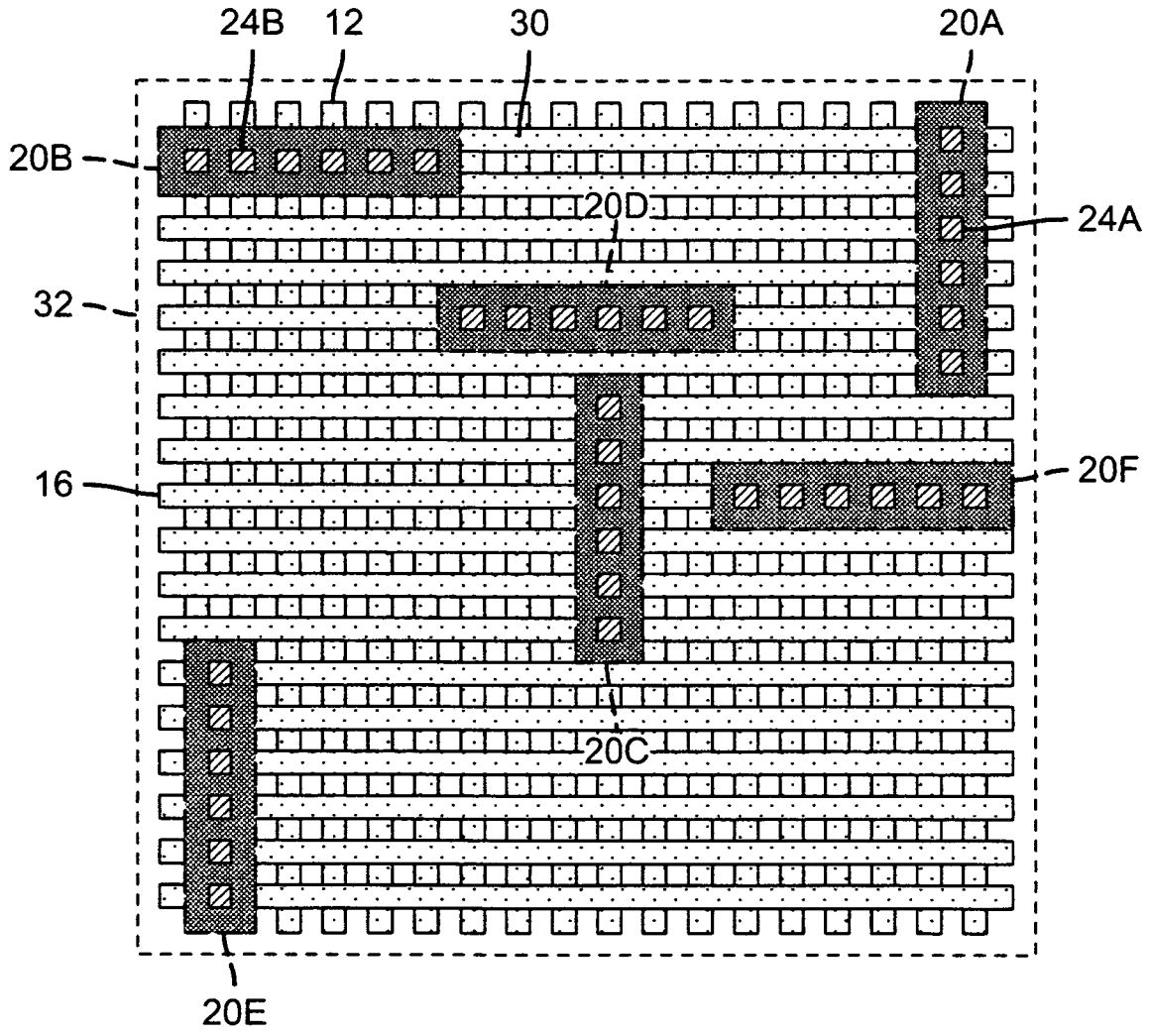

FIG. 4

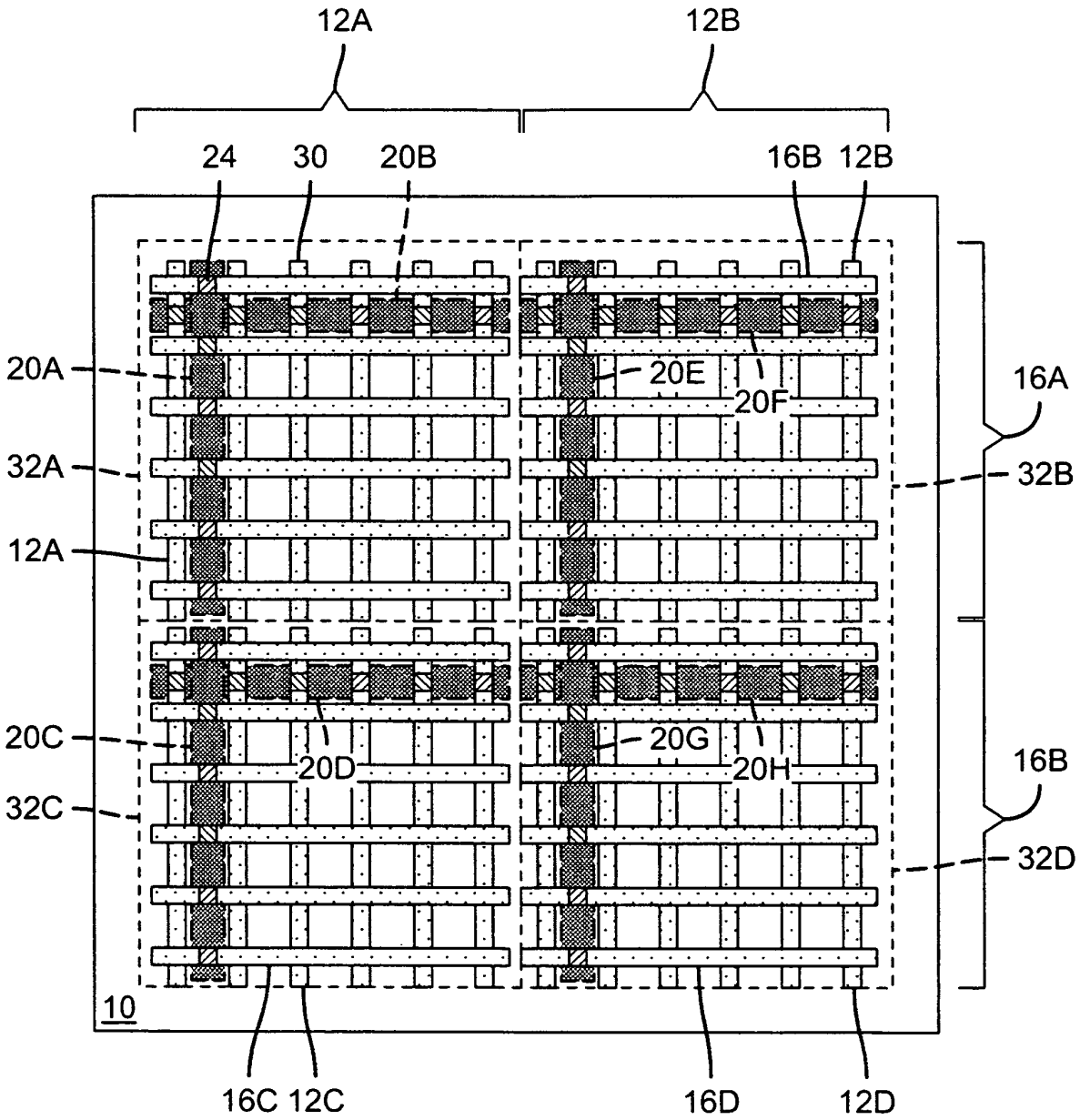
12A
12B
24
30
20B
16B
12B
20A
20E
20F
16A
32A
32B
12A
20C
20D
20G
20H
16B
32C
32D
10
16C
12C
16D
12D

FIG. 5

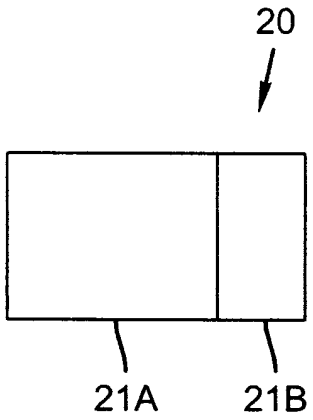

FIG. 6A

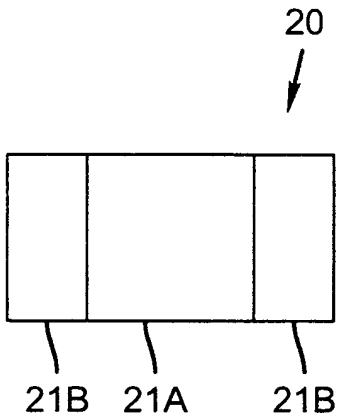

FIG. 6B

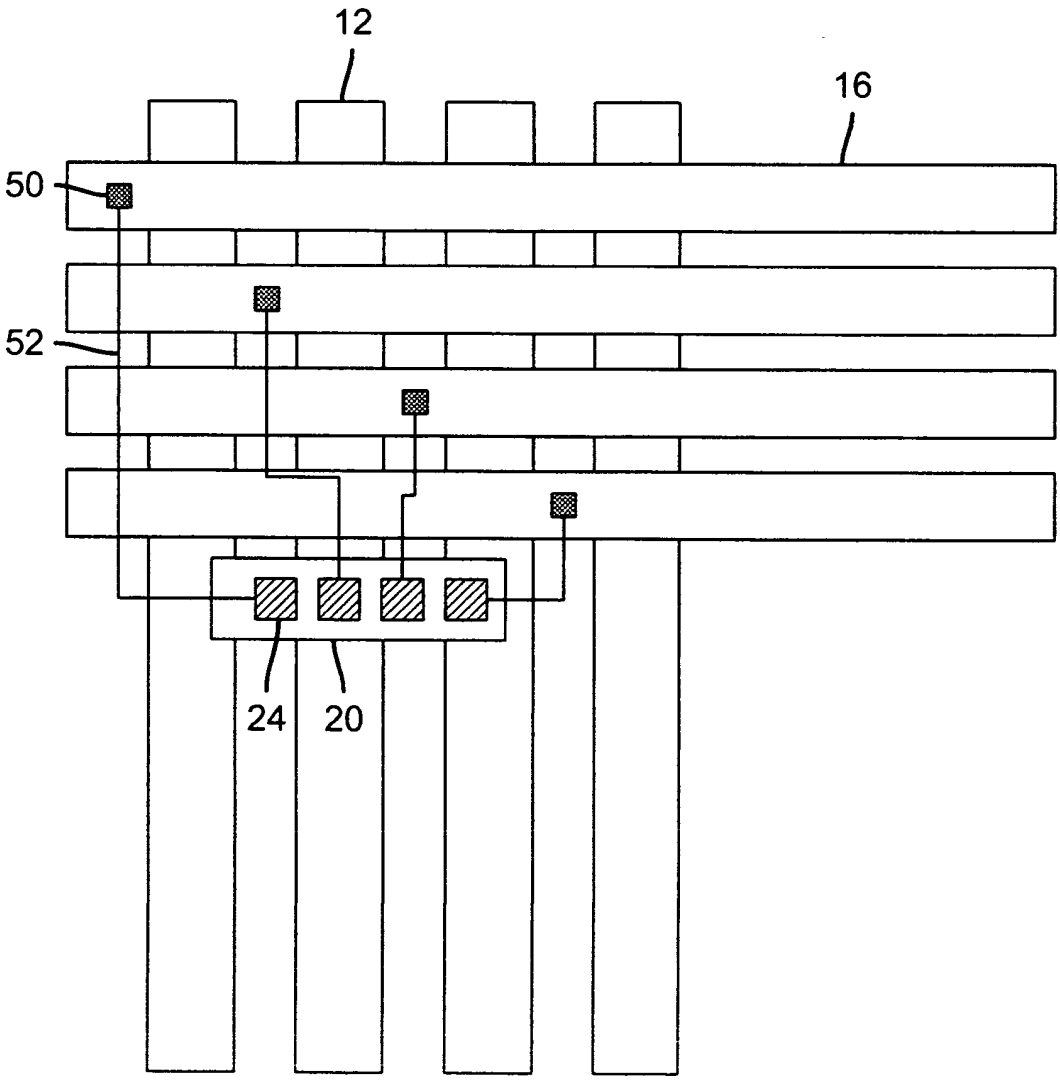

FIG. 7A

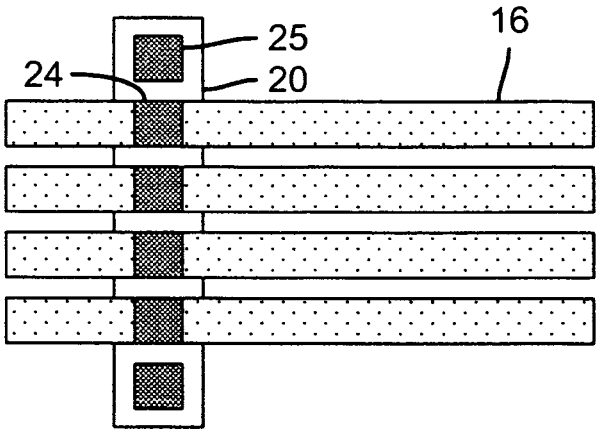

FIG. 7B

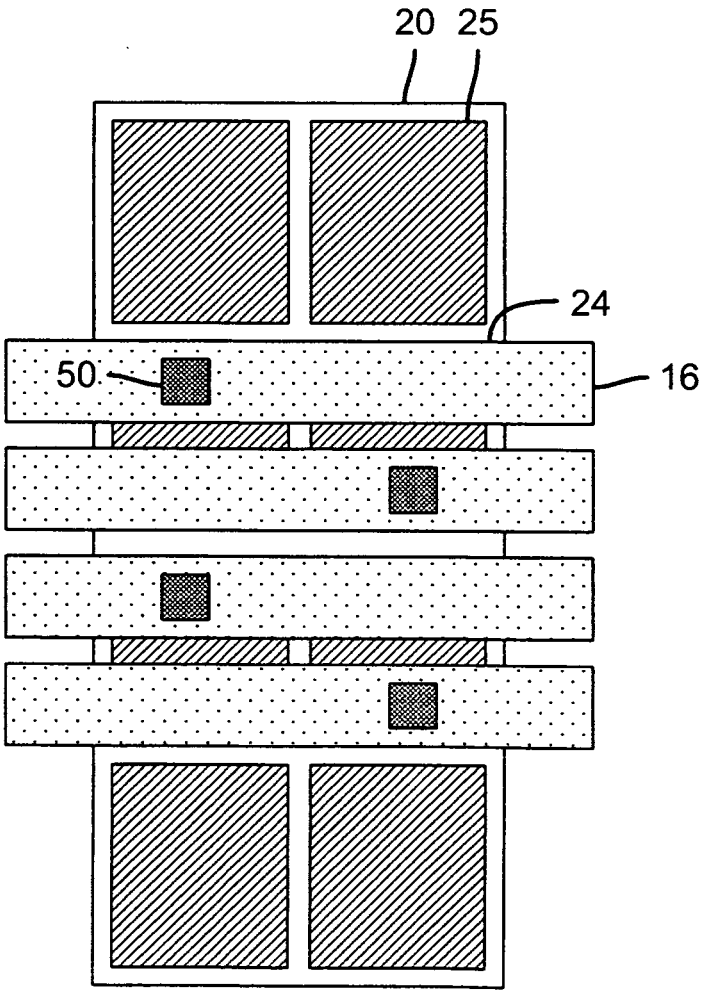

FIG. 7C

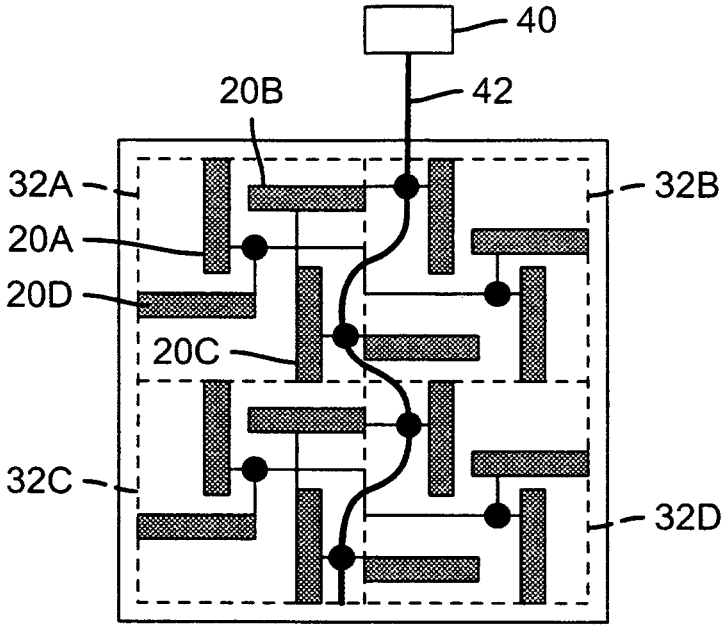

FIG. 8

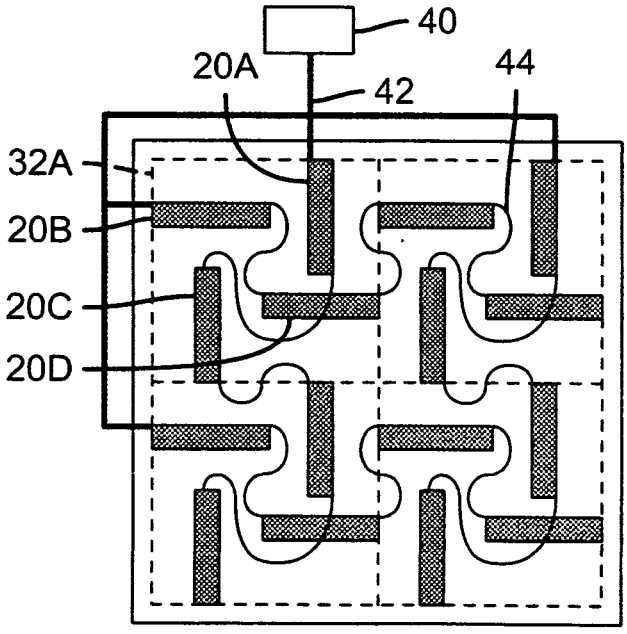

FIG. 9

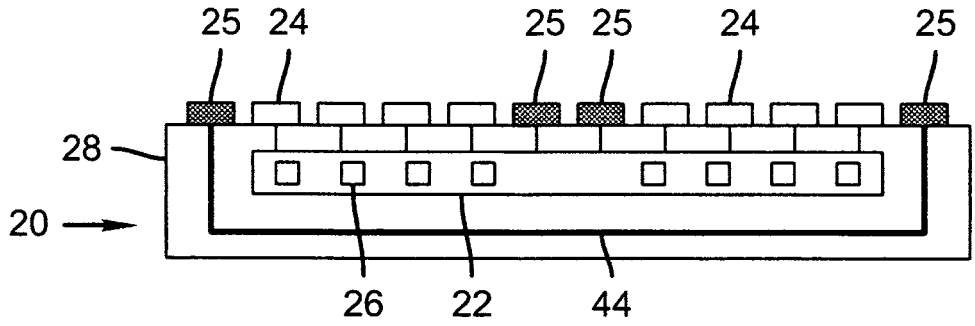

FIG. 10A

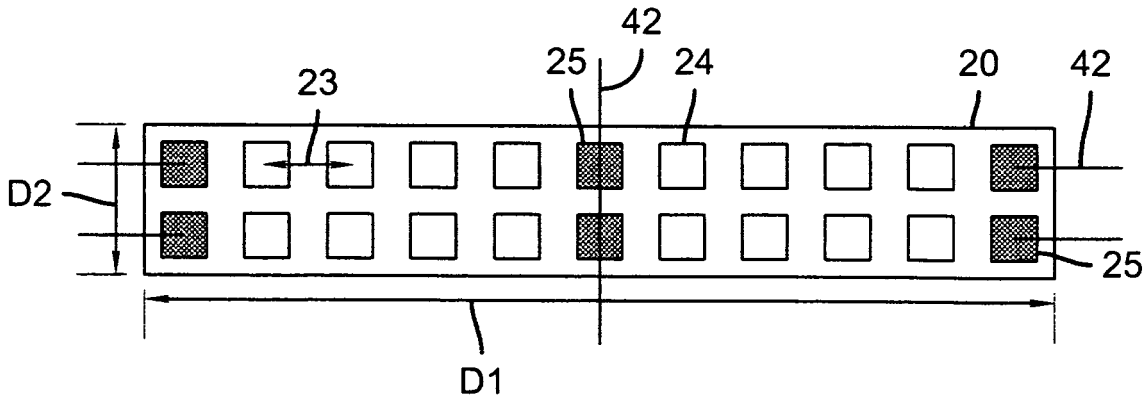

FIG. 10B

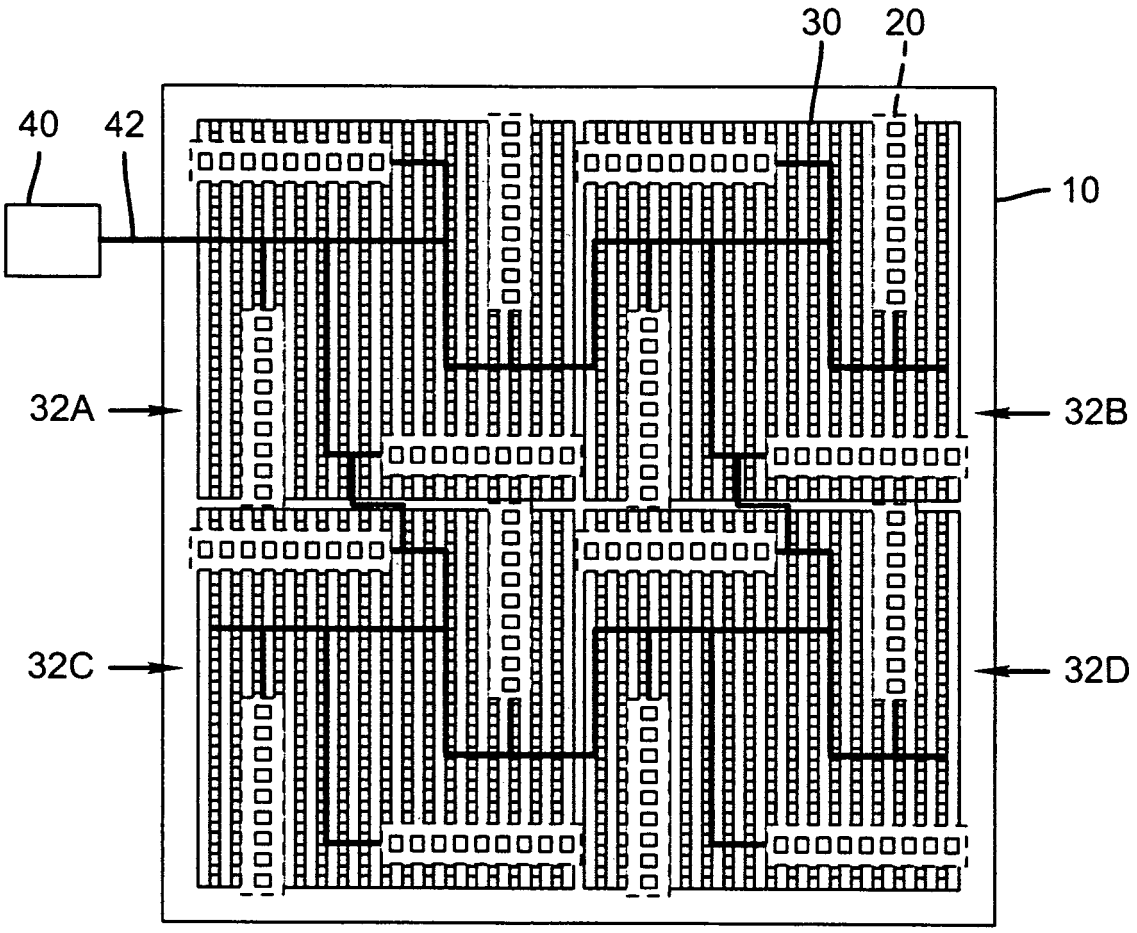

FIG. 11

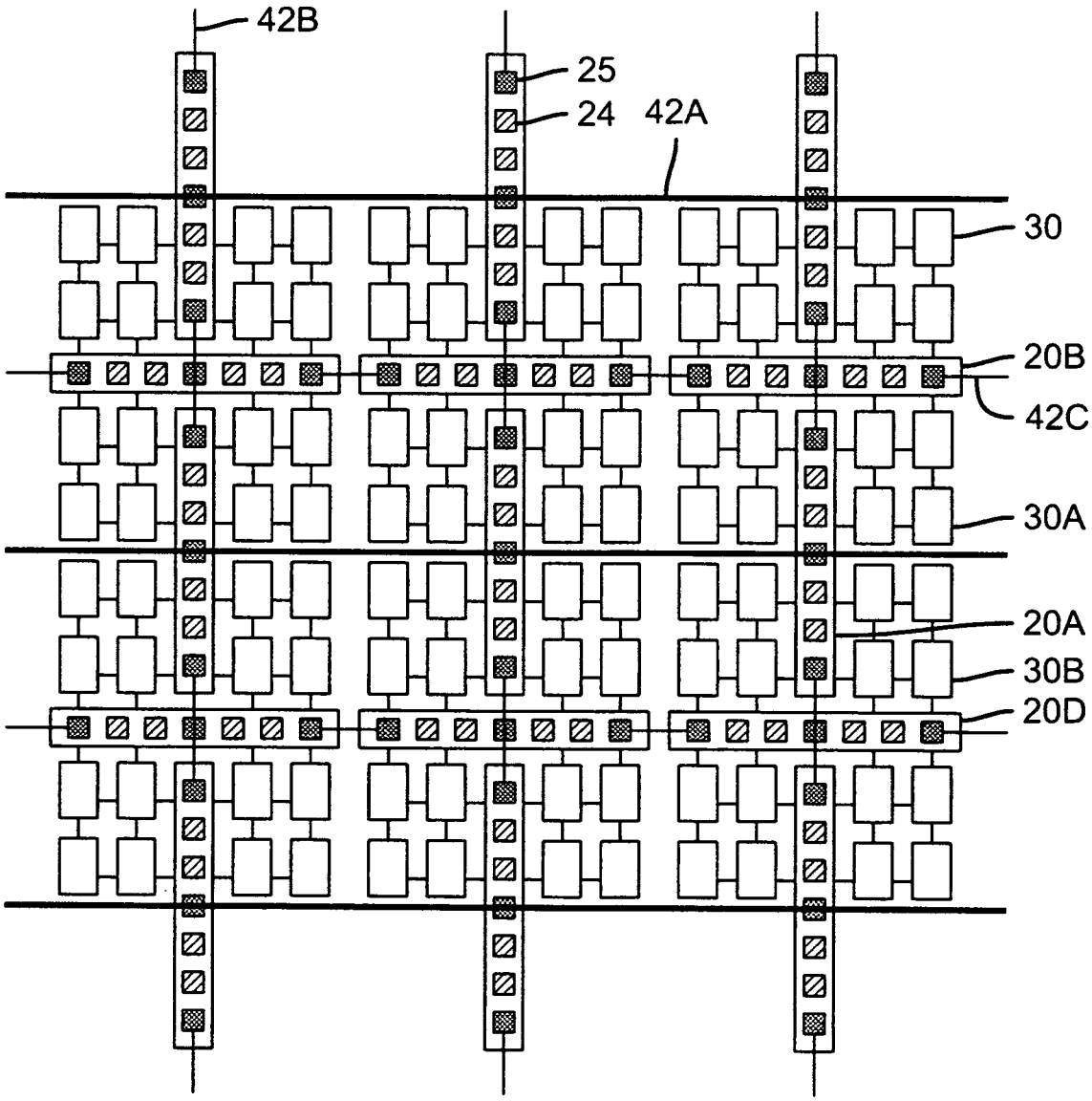

FIG. 12

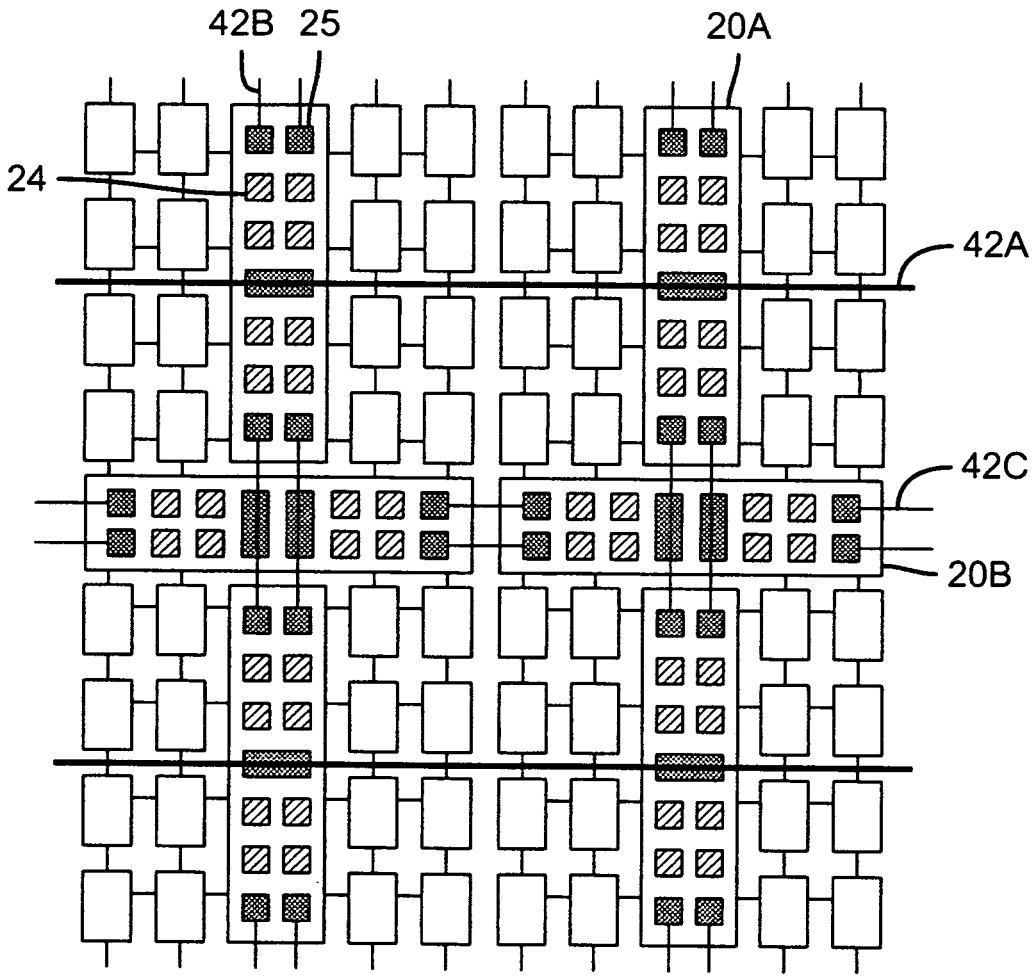

FIG. 13

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	用于二维显示的Chiplet驱动器对		
公开(公告)号	EP2399254B1	公开(公告)日	2016-08-31
申请号	EP2010704705	申请日	2010-02-12
[标]申请(专利权)人(译)	全球OLED TECH		
申请(专利权)人(译)	全球OLED科技有限责任公司		
当前申请(专利权)人(译)	全球OLED科技有限责任公司		
[标]发明人	HAMER JOHN W COK RONALD S		
发明人	HAMER, JOHN, W. COK, RONALD, S.		
IPC分类号	G09G3/32 H01L27/32		
CPC分类号	G09G3/3208 G09G3/3266 G09G3/3275 G09G2300/0426 G09G2300/0465 G09G2310/0218 G09G2310/0221 G09G2320/0247 H01L27/3255 H01L27/3281		
优先权	12/372132 2009-02-17 US		
其他公开文献	EP2399254A1		
外部链接	Espacenet		

摘要(译)

一种显示装置，包括基板;具有形成于行跨越基板在第一方向上的行电极阵列和具有与所述第一方向不同的形成在列跨越基板在第二方向上的列电极的阵列的第二层的第一层，其中所述行和列电极重叠以形成像素位置;行和列电极之间形成光发射材料的一个或多个层以形成像素，像素位于所述像素位置的二维阵列;和多个行驱动器芯片的和独立的多个列驱动器芯片的相对于像素的二维阵列分布，每个行驱动器芯片只连接到并控制一组独立的行电极和各列驱动器芯片独自地连接到和控制一组独立的列电极。

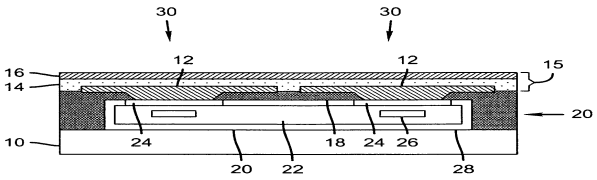

FIG. 1A

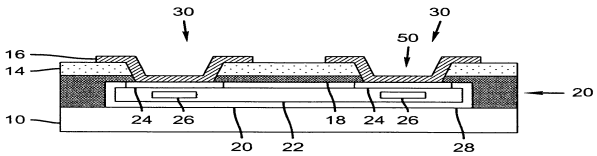

FIG. 1B