(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 796 071 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
13.06.2007 Bulletin 2007/24

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **06256141.0**

(22) Date of filing: **30.11.2006**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK YU

(30) Priority: **30.11.2005 KR 20050116001**

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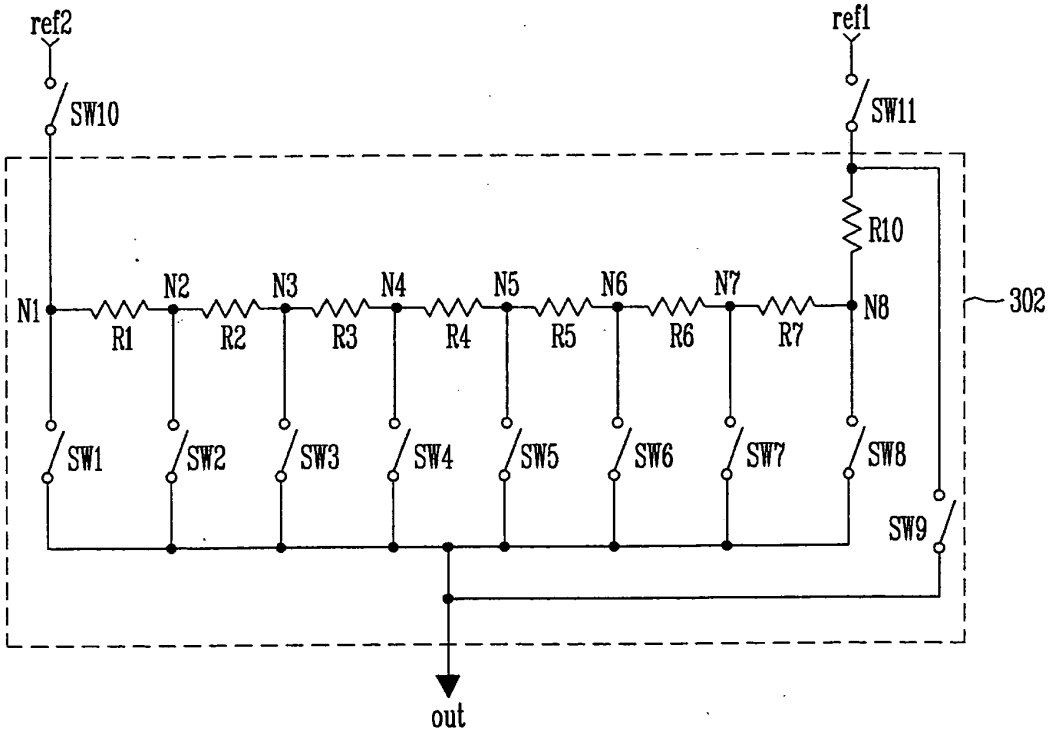
(54) Data driver, organic light emitting display, and method of driving the same

(57) A data driver, including a first digital-to-analog converter configured to select two reference voltages of a plurality of reference voltages depending on upper bits of data, and a second digital-to-analog converter configured to divide the two reference voltages into a plurality of voltages and supply any one voltage of the two reference voltages and the divided voltages to an output terminal as a data signal depending on lower bits of the data, wherein the second digital-to-analog converter is configured to supply an intermediate gray scale voltage to the output terminal prior to supplying the data signal, the intermediate gray scale voltage having a voltage between the two reference voltages.

FIG. 5



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a data driver, an organic light emitting display, and a method of driving the same. More particularly, the present invention relates to a data driver having an enhanced driving speed, an organic light emitting display, and a method of driving the same.

2. Description of the Related Art

[0002] Various flat panel display devices having reduced weight and volume compared to cathode ray tubes (CRTs) have been developed. Such flat panel display devices include, e.g., liquid crystal displays, field emission displays, plasma display panels, light emitting display, etc. These exemplary displays operate differently to display an image.

[0003] For example, an organic light emitting display may display an image by using an organic light emitting diode that generates light by recombining electrons and holes. During operation, an organic light emitting display supplies a current corresponding to a data signal to organic light emitting diodes by employing driving thin film transistors formed at each pixel so light may be emitted from the organic light emitting diodes. Such an organic light emitting display offers certain advantages, such as low power consumption and a rapid response speed.

[0004] An organic light emitting display generates data signals by using data supplied from an external source. Such an organic light emitting display supplies the generated data signals to pixels and displays an image of desired brightness. A data driver for converting the data supplied from the external source into the data signals has been considered.

[0005] Such a data driver may include a data signal generator for converting the external data into the data signals. The data signal generator may include a digital-to-analog converter (hereinafter, referred to as "DAC"). The DAC may be positioned in each channel and may convert the data into the data signals. For example, the data signal generator may include first DACs generating voltages depending on the values of the upper bits of the data and second DACs for generating voltages depending on the values of the lower bits of the data.

[0006] FIG. 1 illustrates a circuit diagram of a conventional second DAC. Referring to FIG. 1, the second DAC 2 receives a first reference voltage (ref1) and a second reference voltage (ref2) from a first DAC (not illustrated). The first DAC receives a plurality of reference voltages from an external source. The first DAC selects the first reference voltage (ref1) and the second reference voltage (ref2) among the plurality of reference voltages received depending on a value of the upper bits of the data. The first DAC supplies the selected first and second reference voltages (ref1) and (ref2) to the second DAC 2 via a tenth switch SW10 and an eleventh switch SW11, as illustrated in FIG. 1. The tenth switch SW10 or the eleventh switch SW11 may be turned on depending on the value of the upper bits of the data. For the sake of discussion, assume that the first reference voltage (ref1) is lower than the second reference voltage (ref2).

[0007] The illustrated second DAC 2 includes a plurality of voltage dividing resistors R1 to R7 for dividing the voltage values of the first reference voltage (ref1) and the second reference voltage (ref2). The second DAC 2 also includes a plurality of switches SW1 to SW8 for supplying voltages divided from the voltage dividing resistors R1 to R7 to an output terminal (out).

[0008] A tenth resistor R10 is arranged between the eleventh switch SW11 and the seventh resistor R7. The tenth resistor R10 compensates for the switch resistances of the tenth switch SW10 and the eleventh switch SW11, so that the second DAC 2 evenly divides the reference voltages via the voltage dividing resistors R1 to R7. That is, the resistance of the tenth resistor R10 is calculated by summing the switch resistance value (i.e., a turn-on resistance value) of the tenth switch SW10 and the switch resistance value of the eleventh switch SW11. The tenth resistor R10 has a resistance approximate to the resistance of the seventh resistor R7.

[0009] The voltage dividing resistors R1 to R7 are arranged in series. The voltage dividing resistors R1 to R7 evenly divide the first reference voltage (ref1) and the second reference voltage (ref2). In this regard, the resistance of each of the voltage dividing resistors R1 to R7 are identical. Further, although FIG. 1 illustrates seven voltage dividing resistors R1 to R7, and assumes that the number of bits of the lower bits of the data is 3, the number of voltage dividing resistors may be different depending on the number of bits of the lower bits of the data.

[0010] The switches SW1 to SW8 are arranged to supply the voltages divided by the voltage dividing resistors R1 to R7 to the output terminal (out). In particular, the first switch SW1 is arranged between a first node N1 and the output terminal (out) to supply the second reference voltage (ref2) to the output terminal (out). The second switch SW2 is arranged between a second node N2 and the output terminal (out) to supply the voltage value of the second node N2 to the output terminal (out). The third switch SW3 is arranged between a third node N3 and the output terminal (out) to supply the voltage value of the third node N3 to the output terminal (out). The fourth switch SW4 is arranged between a fourth node N4 and the output terminal (out) to supply the voltage value of the fourth node N4 to the output terminal (out). The fifth switch SW5 is arranged between a fifth node N5 and the output terminal (out) to supply the voltage value of the fifth node N5 to the output terminal (out). The sixth switch SW6 is arranged between a sixth node N6 and the output terminal (out) to supply the voltage value of the sixth node N6 to the output terminal (out). The seventh switch SW7

is arranged between a seventh node N7 and the output terminal (out) to supply the voltage value of the seventh node N7 to the output terminal (out). The eighth switch SW8 is arranged between an eighth node N8 and the output terminal (out) to supply the first reference voltage (ref1) to the output terminal (out).

[0011] One of the switches SW1 to SW8 may be turned on depending on the lower bits of the data. That is, any one of the switches SW1 to SW8 may be turned on depending on the value of the lower bits of the data, and a predetermined voltage may be supplied to the output terminal (out). The predetermined voltage supplied to the output terminal (out) may be supplied to pixels as a data signal.

[0012] However, in the organic light emitting display illustrated in FIG. 1, the predetermined voltage supplied to the output terminal (out) of the second DAC 2 is generated based on a reference voltage being supplied through at least one voltage dividing resistor and one switch. Therefore, the driving speed of the second DAC 2 is significantly reduced. In other words, since the predetermined voltage is generated via the voltage dividing resistors R1 to R7, a period of time is required before voltages corresponding to the data signals may be supplied to the pixels. This additional time period may result in a driving speed that is undesirably low.

[0013] Additionally, it is preferable that the voltages corresponding to the data signals be charged in the pixels within one horizontal period. However, in the case that voltages corresponding to data signals are supplied via the voltage dividing resistors R1 to R7, as illustrated in FIG. 1, a problem arises since sufficient voltages may not be charged in the pixels within the required period of time, e.g., one horizontal period.

SUMMARY OF THE INVENTION

[0014] The present invention is therefore directed to a data driver, an organic light emitting display, and a method of driving the same that substantially overcome one or more of the problems due to the limitations and disadvantages of the related art.

[0015] It is therefore a feature of embodiments of the present invention to provide a data driver and an organic light emitting display that include a circuit arrangement which enhance driving speed.

[0016] It is therefore another feature of embodiments of the present invention to provide a data driver and an organic light emitting display that include a circuit arrangement which may enhance precision of a gray scale.

[0017] According to a first aspect of the invention, there is provided a data driver according to Claim 1. Preferred features of this aspect are set out in claims 2 to 13.

[0018] According to a second aspect of the invention, there is provided an organic light emitting display according to claim 14.

[0019] According to a third aspect of the invention, there is provided a method of driving an organic light emitting display according to Claim 15. Preferred features of this aspect are set out in claims 16 to 20.

BRIEF DESCRIPTION OF THE DRAWINGS

[0020] The above and other features and advantages of the present invention will become more apparent to those of ordinary skill in the art by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

[0021] FIG. 1 illustrates a circuit diagram of a conventional second DAC;

[0022] FIG. 2 illustrates a circuit diagram of an organic light emitting display according to an embodiment of the present invention;

[0023] FIG. 3 illustrates a block diagram of an data driving circuit as illustrated in FIG. 2;

[0024] FIG. 4 illustrates a block diagram of an data signal generator as illustrated in FIG. 3;

[0025] FIG. 5 illustrates a circuit diagram of a first embodiment of a second DAC as illustrated in FIG. 4;

[0026] FIG. 6 illustrates an exemplary timing diagram of an operation of the second DAC as illustrated in FIG. 5;

[0027] FIG. 7 illustrates a graph of an exemplary output voltage of the second DAC as illustrated in FIG. 5;

[0028] FIG. 8 illustrates a circuit diagram of a second embodiment of a second DAC as illustrated in FIG. 4;

[0029] FIG. 9 illustrates an exemplary timing diagram of an operation of the second DAC as illustrated in FIG. 8;

[0030] FIG. 10 illustrates a graph of an exemplary output voltage of the second DAC as illustrated in FIG. 8;

[0031] FIG. 11 illustrates a circuit diagram of a third embodiment of a second DAC as illustrated in FIG. 4;

[0032] FIG. 12 illustrates an exemplary timing diagram of an operation of the second DAC as illustrated in FIG. 11; and

[0033] FIG. 13 illustrates a circuit diagram of a fourth embodiment of a second DAC as illustrated in FIG. 4.

DETAILED DESCRIPTION OF THE INVENTION

[0034] The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the present invention are illustrated. The present invention may, however, be embodied in different forms and should not be construed as limited to the exemplary embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

[0035] Hereinafter, embodiments according to the present invention, which can be easily carried out by those skilled in the art, will be described with reference to FIGS. 2 through 13.

[0036] FIG. 2 illustrates a circuit diagram of an organic light emitting display according to an embodiment of the

present invention. Referring to FIG. 2, the organic light emitting display includes a pixel unit 230. The pixel unit 230 includes pixels 240 arranged on regions where scan lines S1 to Sn intersect with data lines D1 to Dm. The organic light emitting display also includes a scan driver 210 for driving scan lines S1 to Sn, a data driver 220 for driving data lines D1 to Dm, and a timing controller 250 for controlling the scan driver 210 and the data driver 220. The data driver 220 includes at least one data driving circuit 222.

[0037] The scan driver 210. generates scan signals in response to scan driving control signals SCS from the timing controller 250. The scan driver 210 supplies the generated scan signals to the scan lines S1 to Sn in sequence. The scan driver 210 also generates light emitting control signals in response to the scan driving control signals SCS from the timing controller 250. The scan driver 210 supplies the generated light emitting control signals to the light emitting control lines E1 to En in sequence.

The data driver 220 generates data signals in response to data driving control signals DCS from the timing controller 250. The data driver 220 supplies the generated data signals to the data lines D1 to Dm in sequence. The data driving circuit 222 converts data supplied from an external source into data signals and supplies them to the data lines D1 to Dm. A detailed description of the data driving circuit 222 will be provided later.

[0038] The timing controller 250 generates data driving control signals DCS and scan driving control signals SCS based on synchronization signals supplied from an external source. Data driving control signals DCS and scan driving control signals SCS generated from the timing controller 250 are supplied to the data driver 220 and to the scan driver 210, respectively. The timing controller 250 rearranges the data supplied from the external source and supplies the data to the data driver 220.

[0039] The pixel unit 230 receives a first power source ELVDD and a second power source ELVSS from an external source. The first power source ELVDD and the second power source ELVSS supplied to the pixel unit 230 are respectively supplied to the pixels 240. The pixels 240 display images corresponding to data signals supplied from the data driving circuit 222.

[0040] FIG. 3 illustrates a block diagram of an exemplary data driving circuit as illustrated in FIG. 2. For the sake of discussion, FIG. 3 will be described assuming that the data diving circuit 222 includes "i" channels. Referring to FIG. 3, the data driving circuit 222 includes a shift register unit 223 for supplying sampling signals in sequence, a sampling latch unit 224 for storing data in sequence in response to the sampling signals, a holding latch unit 225 for temporarily storing data stored in the sampling latch unit 224 and for supplying the stored data to a level shifter 226, a level shifter 226 for raising a voltage level of the data, a data signal generator 227 for generating data signals corresponding to bit values of the data, and a buffer unit for supplying data signals to data lines D1 to Di.

[0041] The shift register unit 223 receives a source shift clock SSC and a source start pulse SSP from the timing controller 250. The shift register unit 223 receiving the source shift clock SSC and the source start pulse SSP generates "i" sampling signals in sequence, while allowing the source start pulse SSP to be shifted depending on the source shift clock SSC. The shift register unit 223 includes "i" shift registers 2231 to 223i.

[0042] The sampling latch unit 224 stores data in sequence depending on the sampling signals supplied in sequence from the shift register unit 223. The sampling latch unit 224 includes "i" sampling latches 2241 to 224i for storing i data. Each size of the sampling latches 2241 to 224i is set to store k bit data. For the sake of discussion, this exemplary sampling latch unit 224 will be described assuming that k bit is 6 bits.

[0043] The holding latch unit 225 receives and stores the data from the sampling latch unit 224 in response to a source output enable SOE signal. The holding latch unit 225 supplies the stored data to a level shifter 226. The holding latch unit 225 includes "i" holding latches 2251 to 225i. Each of the holding latches 2251 to 225i is configured to store k bit data.

[0044] The level shifter 226 raises a voltage level of the data supplied from the holding latch unit 225. The level shifter 226 supplies the data with a raised voltage level to the data signal generator 227. In this regard, the data driver 220 receives data having a low voltage level and raises the voltage level of the data to a high voltage level by employing the level shifter 226.

[0045] In other implementations, the data driver may not include the level shifter 226. For example, circuit components necessary to raise the voltage level of the data from a low voltage level to a high voltage level may be arranged external to the data driver 220. Accordingly, the holding latch unit 225 may be directly connected to the data signal generator 227. However, such an arrangement may increase manufacturing expenses.

[0046] The data signal generator 227 generates data signals corresponding to bit values (or gray scale values) of the data. The data signal generator 227 supplies the generated data signals to a buffer unit 228. The data signal generator 227 receives a plurality of reference voltages (refs) from a gamma voltage unit 229. The data signal generator generates data signals by using the received reference voltages (refs). The data signal generator 227 will be described in greater detail later.

[0047] The gamma voltage unit 229 supplies the plurality of reference voltages (refs) to the data signal generator 227. The gamma voltage unit 229 may be arranged inside or outside of the data driving circuit 222.

[0048] The buffer unit 228 supplies data signals supplied from the data signal generator 227 to data lines D1 to Di.

[0049] FIG. 4 illustrates a block diagram of an exemplary data signal generator as illustrated in FIG. 3. Referring to FIG. 4, the data signal generator 227 includes

a first DAC 300 and a second DAC 302 in each channel 2271 to 227i. For the sake of discussion, this exemplary data signal generator will be described assuming that nine reference voltages (refs) are supplied from the gamma voltage unit 229.

[0050] The first DAC 300 selects a first reference voltage (ref1) and a second reference voltage (ref2) of the reference voltages (refs) depending on, e.g., a value of upper bits of the data supplied from the level shifter 226. In another implementation, previously discussed above, the first DAC 300 may receive the data directly from the holding latch unit 225.

[0051] The first DAC 300 supplies the first reference voltage (ref1) and the second reference voltage (ref2) to the second DAC 302. That is, the first DAC 300 extracts two reference voltages of the nine reference voltages (refs) depending on the bit values of, for example, an upper 3 bits of the data. The first DAC 300 supplies the extracted two reference voltages to the second DAC 302 as the first reference voltage (ref1) and the second reference voltage (ref2). Hereinafter, for the sake of discussion, assume that the first reference voltage (ref1) is set to be lower than the second reference voltage (ref2).

[0052] The second DAC 302 divides the first reference voltage (ref1) and the second reference voltage (ref2) into a plurality of voltages. The second DAC 302 supplies any one of the first reference voltage (ref1), the second reference voltage (ref2) and the divided voltages to the output terminal (out) as a data signal, depending on the value of the lower 3 bits of the data.

[0053] FIG. 5 illustrates a circuit diagram of a second DAC according to a first embodiment of the present invention. A tenth switch SW10 and an eleventh switch SW11 of the first DAC 300 is also illustrated in FIG. 5. The tenth switch SW10 and the eleventh switch SW11 may be turned on to supply the first reference voltage (ref1) and the second reference voltage (ref2) to the second DAC 302.

[0054] Referring to FIG. 5, the second DAC 302 includes a plurality of voltage dividing resistors R1 to R7 for dividing the first reference voltage (ref1) and the second reference voltage (ref2), and a plurality of switches SW1 to SW8 for supplying the voltages divided from the voltage dividing resistors R1 to R7 to the output terminal (out). The second DAC 302 also includes a tenth resistor R10 and a switch SW9.

[0055] The voltage dividing resistors R1 to R7 are arranged in series between inputs for receiving the first reference voltage (ref1) and the second reference voltage (ref2). In this regard, the voltage dividing resistors R1 to R7 divides the voltage values of the first reference voltage (ref1) and the second reference voltage (ref2). Additionally, the voltage dividing resistors R1 to R7 have identical resistance values. While this embodiment of the second DAC may include seven voltage dividing resistors R1 to R7, on the assumption that the number of the lower bits of the data is 3 bits, embodiments of the present invention are not limited thereto. That is, the number of voltage dividing resistors may be different.

[0056] The switches SW1 to SW8 are connected to a node of the voltage dividing resistors R1 to R7 so as to supply the voltages divided by the voltage dividing resistors R1 to R7 to the output terminal (out).

[0057] The first switch SW1 is arranged between a first node N1 and the output terminal (out) and supplies the second reference voltage (ref2) to the output terminal (out). The second switch SW2 is arranged between a second node N2 and the output terminal (out) and supplies the voltage value of the second node N2 to the output terminal (out). The third switch SW3 is arranged between a third node N3 and the output terminal (out) and supplies the voltage value of the third node N3 to the output terminal (out). The fourth switch SW4 is arranged between a fourth node N4 and the output terminal (out) and supplies the voltage value of the fourth node N4 to the output terminal (out). The fifth switch SW5 is arranged between a fifth node N5 and the output terminal (out) and supplies the voltage value of the fifth node N5 to the output terminal (out). The sixth switch SW6 is arranged between a sixth node N6 and the output terminal (out) and supplies the voltage value of the sixth node N6 to the output terminal (out). The seventh switch SW7 is arranged between a seventh node N7 and the output terminal (out) and supplies the voltage value of the seventh node N7 to the output terminal (out). The eighth switch SW8 is arranged between an eighth node N8 and the output terminal (out) and supplies the first reference voltage (ref1) to the output terminal (out).

[0058] Any one of the switches SW1 to SW8 may be turned on depending on the lower 3 bits of the data. That is, any one of the switches SW1 to SW8 may be turned on depending on value of the lower 3 bits of the data, and a predetermined voltage value may be supplied to the output terminal (out). The voltage supplied to the output terminal (out) is supplied to the pixels 240 as a data signal via the buffer unit 228.

[0059] As discussed above, the second DAC 302 includes the tenth resistor R10 that is arranged between the eleventh switch SW11 and the seventh voltage dividing resistor R7. The tenth resistor R10 compensates for the switch resistances of the tenth switch SW10 and the eleventh switch SW11 so that the second DAC 302 evenly divide the reference voltages by employing the voltage dividing resistors R1 to R7. That is, the resistance of the tenth resistor R10 is calculated by summing the switch resistance value (i.e., a turn-on resistance value) of the tenth switch SW10 and the switch resistance value of the eleventh switch SW11. The tenth resistor R10 has a resistance approximate to the seventh resistor R7.

[0060] The second DAC 302 also includes the ninth switch SW9 that is arranged between the eleventh switch SW11 and the output terminal (out). The ninth switch SW9 is turned on before the data signal is supplied to the output terminal (out) so as to initially charge the pixels 240 with the voltage value of the reference voltage (ref1). That is, the first reference voltage (ref1) is supplied via

the ninth switch SW9 to the pixels 240 without passing through the voltage dividing resistors R1 to R7, and the tenth resistor R10, thereby making it possible to reduce the charging time of the pixels 240.

[0061] FIG. 6 illustrates an exemplary timing diagram of an operation of the second DAC as illustrated in FIG. 5. Referring to FIG. 5 and FIG. 6, during a first period T1 of a horizontal period 1H, the ninth switch SW9 is turned on. If the ninth switch SW9 is turned on, the first reference voltage (ref1) is supplied to the pixels 240 via the output terminal of the second DAC 302 and the buffer unit 228. That is, the first reference voltage (ref1) is supplied during the first period T1 to the pixels 240 without passing through the voltage dividing resistors R1 to R7 and the tenth resistor R10 of the second DAC 302. Thus, the first reference voltage (ref1) is charged in the pixels 240 at a rapid charging speed during the first period T1, as illustrated in FIG. 7. Accordingly, the charging speed of the pixels 240 is significantly enhanced.

[0062] During a second period T2 of the horizontal period 1H, the ninth switch SW9 is turned off, and any one of the switches SW1 to SW8 may be turned on. The turned-on switch supplies a predetermined voltage to the output terminal (out) of the second DAC 302. The predetermined voltage outputted is supplied to the pixels 240 as a data signal.

[0063] The first reference voltage (ref1) is supplied to the pixels 240 during the first period T1, and the voltage corresponding to the data signal is charged during the second period T2. Thus, even though during the second period T2, the voltage is supplied to the output terminal (out) via the voltage dividing resistors R1 to R7, and the charging speed of the pixels 240 may not be as rapid as the charging speed of the pixels 240 during the first period T1, when the first reference voltage (ref1) is supplied to the output terminal (out) via the ninth switch SW9, a voltage corresponding to a data signal is charged in the pixels 240 more rapidly due to the voltage previously charged in the pixels 240 during the first period T1. In this regard, the voltage corresponding to the data signal is charged in the pixels 240 within the horizontal period 1H.

[0064] In the second DAC 302 as illustrated in FIG. 5, it may be somewhat difficult to supply an intermediate gray scale voltage to the output terminal (out) prior to supplying the data signal. The intermediate gray scale voltage is a voltage between the first reference voltage (ref1) and the second reference voltage (ref2). That is, when supplying the intermediate gray scale voltage via the voltage dividing resistors R1 to R7, the total resistance thereof may be significant, and can prevent a necessary voltage being charged in the pixels 240. Accordingly, when generating a voltage corresponding to a data signal by employing the voltage dividing resistors R1 to R7, it is desirable to enhance the precision of the gray scale levels of the data signal generated in the intermediate portions of the voltage dividing resistors R1 to R7.

[0065] FIG. 8 illustrates a circuit diagram of a second DAC according to a second embodiment of the present invention. In FIG. 8 the same elements illustrated in FIG. 5 have been designated by the same reference numerals, and a detailed description thereof will not be repeated. Referring to FIG. 8, the second DAC 302 includes a capacitor C. The first electrode of the capacitor C is connected to the tenth node N10. The tenth node N10 is a common node between the ninth switch SW9 and the output terminal (out). The second electrode of the capacitor C receives a variation voltage W. In an exemplary operation, the capacitor C changes the voltage of the output terminal (out) to an intermediate gray scale voltage of the first reference voltage (ref1) and the second reference voltage (ref2). That is, after the ninth switch SW9 is turned on to supply the first reference voltage (ref1) to the output terminal (out), the capacitor C supplies the intermediate gray scale voltage to the output terminal (out). The intermediate gray scale voltage is between the first reference voltage (ref1) and the second reference voltage (ref2). Accordingly, the intermediate gray scale voltage is rapidly charged in the pixels 240.

[0066] FIG. 9 illustrates an exemplary timing diagram of an operation of the second DAC as illustrated in FIG. 8. Referring to FIG. 8 and FIG. 9, during a first period T10 of a horizontal period 1H, the ninth switch SW9 is turned on. If the ninth switch SW9 is turned on, the first reference voltage (ref1) is supplied to the pixels 240 via the output terminal (out) of the second DAC 302 and the buffer unit 228. That is, the first reference voltage (ref1) is supplied during the first period T10 to the pixels 240 without passing through the voltage dividing resistors R1 to R7 and the tenth resistor R10 of the second DAC 302. Thus, the first reference voltage (ref1) is charged in the pixels 240 at an increased charging speed during the first period T10, as illustrated in FIG. 10. Accordingly, the charging speed of the pixels 240 is significantly enhanced. Also, during the first period T10, the variation voltage W having a first voltage value V1 is supplied to the second electrode of the capacitor C.

[0067] During a second period T11, the ninth switch SW9 is turned off, and the variation voltage W having a second voltage value V2 is supplied to the second electrode of the capacitor C. For the sake of discussion, the second voltage V2 is higher than the first voltage V1. The second voltage V2 is set so that the voltage of the output terminal (out) of the second DAC 302 increases from the first reference voltage (ref1) to the intermediate gray scale voltage. In particular, the second voltage V2 is set so that the charge in the pixels 240 increases from the first reference voltage (ref1) to the intermediate gray scale voltage. Accordingly, the intermediate gray scale voltage is charged in the pixels 240.

[0068] After the voltage of the output terminal (out) is increased to the intermediate gray scale voltage, any one of the switches SW1 to SW8 may be turned on. The turned-on switch supplies a predetermined voltage to the output terminal (out). The predetermined voltage is supplied to the pixels 240 as a data signal via the buffer unit 228. In this regard, the second DAC 302 of this embod-

iment enhances the precision of the intermediate gray scale by changing the voltage of the output terminal (out) to the intermediate gray scale voltage using the capacitor C.

[0069] As discussed, if the intermediate gray scale voltage is selected as a voltage corresponding to a data signal, the intermediate gray scale voltage is stably charged in the pixels 240. Further, if, for example, the second node N2 voltage or the seventh node N7 voltage is selected, the desired voltage is stably charged in the pixels 240. In other words, the voltage value of the second node N2 or the seventh node N7 is supplied via one resistor (R1 or R7) to the output terminal (out), and the voltage corresponding to the data signal is rapidly charged in the pixels 240.

[0070] FIG. 11 illustrates a circuit diagram of a third exemplary embodiment of a second DAC as illustrated in FIG. 4. In FIG. 11, the same elements illustrated in FIG. 8 have been designated by the same reference numerals, and a detailed description thereof will not be repeated. Referring to FIG. 11, the connection arrangement of the ninth switch SW9 and the tenth resistor R10 is different from the second DAC 302 illustrated in FIG. 8. For example, the ninth switch SW9 provides a connection path for the second reference voltage (ref2) to the output terminal (out). The tenth resistor R10 is arranged between the tenth switch SW10 and the first voltage dividing resistor R1. In an exemplary operation, the ninth switch SW9 is turned on, and the second reference voltage (ref2) is supplied to the output terminal (out) of the second DAC 302.

[0071] FIG. 12 illustrates an exemplary timing diagram of an operation of the second DAC as illustrated in FIG. 11. Referring to FIG. 11 and FIG. 12, during a first period T20 of a horizontal period 1H, the ninth switch SW9 is turned on. If the ninth switch SW9 is turned on, the second reference voltage (ref2) is supplied to the pixels 240 via the output terminal (out) of the second DAC 302 and the buffer unit 228. That is, the second reference voltage (ref2) is supplied during the first period T20 to the pixels 240 without passing through the voltage dividing resistors R1 to R7 and the tenth resistor R10 of the second DAC 302. Thus, the second reference voltage (ref2) is charged in the pixels 240 at a rapid charging speed during the first period T20. Accordingly, the charging speed of the pixels 240 is significantly enhanced. Also, during the first period T20, the variation voltage W having a second voltage value V2 is supplied to the second electrode of the capacitor C.

[0072] During a second period T21, the ninth switch SW9 is turned off and the variation voltage W having a first voltage value V1 is supplied to the second electrode of the capacitor C. For the sake of discussion, the first voltage V1 is lower than the second voltage V2. The first voltage V1 is set so that the voltage of the output terminal (out) of the second DAC 302 decreases from the second reference voltage (ref2) to the intermediate gray scale voltage. For example, the first voltage V1 is set so that the voltage of the output terminal (out) decreases from the second reference voltage (ref2) to the voltage of, for example, the fourth node N4 or the fifth node N5.

[0073] Accordingly, if the voltage of the output terminal (out) decreases to the intermediate gray scale voltage by employing the capacitor C, the voltage value of the intermediate gray scale value is rapidly charged in the pixels 240. That is, the second DAC 302 of this embodiment enhances the precision of the intermediate gray scale by changing the voltage value of the output terminal (out) to the intermediate gray scale voltage employing the capacitor C.

[0074] After the voltage of the output terminal (out) is decreased to the intermediate gray scale voltage, any one of the switches SW1 to SW8 may be turned on. The turned-on switch supplies a predetermined voltage to the output terminal (out), and is supplied to the pixels 240 as a data signal via the buffer unit 228.

[0075] In the above discussed embodiments, switches S1 to SW11 are implemented employing at least one transistor. For example, the switches SW1 to SW11 may be implemented employing two transistors, such as NMOS, PMOS transistors connected in a transmission gate arrangement, as illustrated in FIG. 13 of a fourth embodiment of a second DAC.

[0076] A data driver, an organic light emitting display, and a method of driving the same according to embodiments of the present invention may include switches arranged between inputs for receiving two gray scale voltages supplied to the second DAC and the output terminal (out). The charging speed of the pixels may be significantly enhanced by supplying a gray scale voltage of the two gray scale voltages to the pixels via the switches. Also, embodiments of the present invention may increase the voltage of the output terminal to the intermediate gray scale voltage by using, for example, a capacitor connected to the switches, thereby making it possible to enhance the precision of the gray scale. Also, embodiments of the present invention may control the charge of the capacitor C and the voltage supplied to the second electrode of the capacitor C, thereby making it possible to control the level of the voltage supplied to the output terminal (out), and overcome any deviation of the manufacturing process, etc.

[0077] Embodiments of the present invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. Accordingly, it will be understood by those of ordinary skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. A data driver, comprising:

a first digital-to-analog converter configured to select two reference voltages of a plurality of reference voltages depending on upper bits of data; and
a second digital-to-analog converter configured to divide the two reference voltages into a plurality of voltages and to supply any one voltage of the two reference voltages and the divided voltages to an output terminal as a data signal depending on lower bits of the data,

wherein the second digital-to-analog converter is configured to supply an intermediate gray scale voltage to the output terminal prior to supplying the data signal, the intermediate gray scale voltage having a voltage between the two reference voltages.

2. A data driver according to claim 1, wherein the first digital-to-analog converter includes a tenth switch and an eleventh switch that are each configured to be turned on to supply a respective one of two reference voltages of the plurality of reference voltages.

3. A data driver according to claim 2, wherein the second digital-to-analog converter includes:

a plurality of voltage dividing resistors arranged between the tenth switch and the eleventh switch of the first digital-to-analog converter to divide the two reference voltages;
first switches arranged between nodes of the voltage dividing resistors and the output terminal and configured to be turned on depending on lower bits of the data;
a second switch arranged between the tenth switch and the output terminal or the eleventh switch and the output terminal; and
a first electrode of a capacitor connected to the second switch and the output terminal.

4. A data driver according to claim 3, wherein the eleventh switch is connected to a first reference voltage of the two reference voltages, and the tenth switch is connected to a second reference voltage having a voltage higher than the first reference voltage.

5. A data driver according to claim 4, wherein the second switch is arranged directly between the eleventh switch and the output terminal.

6. A data driver according to claim 4, wherein the second switch is arranged directly between the tenth switch and the output terminal.

7. A data driver according to any one of claims 3 to 6, wherein a second electrode of the capacitor is configured to receive a variation voltage, and the capacitor is configured to be charged to a voltage level substantially equal to an intermediate gray scale voltage.

8. A data driver according to any one of claims 3 to 7, wherein the second digital-to-analog converter further includes a compensation resistor arranged between the tenth switch and the voltage dividing resistors to compensate for the resistance values of the tenth switch and the eleventh switch.

9. A data driver according to any one of claims 3 to 8, wherein the second digital-to-analog converter further includes a compensation resistor arranged between the eleventh switch and the voltage dividing resistors to compensate for the resistance values of the tenth switch and the eleventh switch.

10. A data driver according to claim 9, wherein the compensation resistor has a resistance value substantially equal to any one of the voltage dividing resistors.

11. A data driver according to claim 1, wherein the second digital-to-analog converter includes:

voltage dividing resistors configured to divide the two reference voltages;
first switches configured to supply any one voltage of the voltage values divided by the voltage dividing resistors depending on lower bits of the data;
a second switch configured to supply any one voltage of the two reference voltages to the output terminal without passing through the voltage dividing resistors; and
a capacitor having a first electrode connected to the second switch and the output terminal, and having a second electrode connected to a variation voltage.

12. A data driver according to any one of claims 1 to 11, wherein the data driver includes:

a shift register configured to supply sampling signals in sequence;
a sampling latch unit configured to sample data in response to the sampling signals;
a holding latch unit configured to store data from the sampling latch unit; and
a data signal generator configured to receive the data from the holding latch unit and generate the data signal,

wherein each channel of the data signal generator is provided with the first digital-to-analog converter and the second digital-to-analog converter.

13. A data driver according to claim 12, wherein the data

driver further includes:

a level shifter arranged between the holding latch unit and the data signal generator and configured to raise a voltage level of the data; and
a buffer unit configured to receive the data signal from the data signal generator.

14. An organic light emitting display, comprising:

a pixel unit including a plurality of pixels connected to scan lines and data lines;
a scan driver configured to drive the scan lines; and
a data driver configured to drive the data lines, wherein the data driver is according to any one of claims 1 to 13..

15. A method of driving an organic light emitting display, comprising:

selecting two reference voltages of a plurality of reference voltages depending on upper bits of data;
dividing the two reference voltages into a plurality of voltages;
supplying any one of the two reference voltages to an output terminal during a first period of a horizontal period;
supplying an intermediate gray scale voltage between the two reference voltages to the output terminal at the beginning of a second period of the horizontal period; and
supplying any one of the divided voltages and the two reference voltages to the output terminal as a data signal depending on lower bits of the data during the remainder of the second period.

16. A method according to claim 15, wherein, in supplying any one of the two reference voltages to the output terminal, the reference voltage is not passed through voltage dividers.

17. A method according to claim 15 or 16, wherein supplying the intermediate gray scale voltage includes supplying a variation voltage to a capacitor connected to the output terminal.

18. A method according to claim 17, wherein supplying the variation voltage to the capacitor includes setting a voltage of the variation voltage so that the voltage of the output terminal during the first period is changed to the intermediate gray scale voltage at the beginning of the second period.

19. A method according to claim 17 or 18, wherein:

the variation voltage includes a first voltage during the first period and a second voltage during the second period, and the two reference voltages include a first reference voltage and a second reference voltage, the second reference voltage being higher than the first reference voltage,
supplying any one of the two reference voltages includes supplying the first reference voltage to the output terminal without passing through voltage dividers, and
supplying the variation voltage to the capacitor includes setting the second voltage to be higher than the first voltage during the second period so as to increase the voltage of the output terminal to the intermediate gray scale voltage.

20. A method according to claim 17 or 18, wherein:

the variation voltage includes a first voltage during the first period and a second voltage during the second period, and the two reference voltages include a first reference voltage and a second reference voltage, the second reference voltage being higher than the first reference voltage,
supplying any one of the two reference voltages includes supplying the second reference voltage to the output terminal without passing through voltage dividers, and
supplying the variation voltage to the capacitor includes setting the second voltage to be lower than the first voltage during the second period so as to decrease the voltage of the output terminal to the intermediate gray scale voltage.

FIG. 1
(RELATED ART)

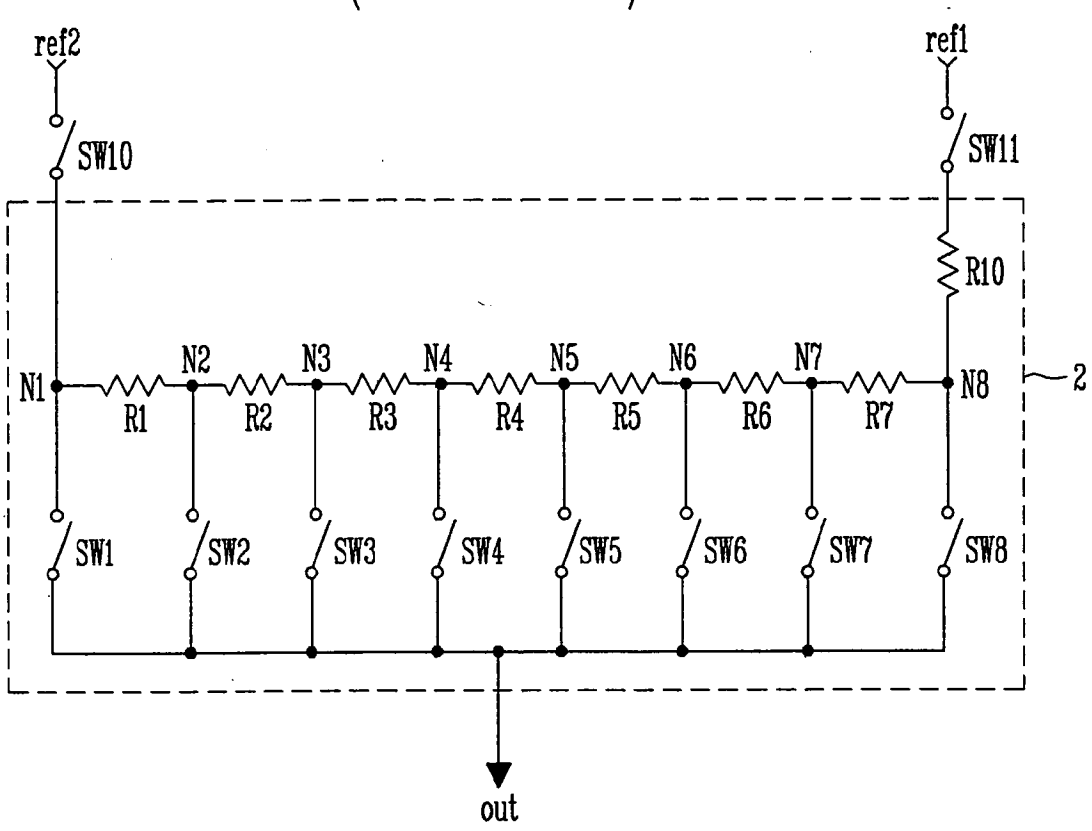


FIG. 2

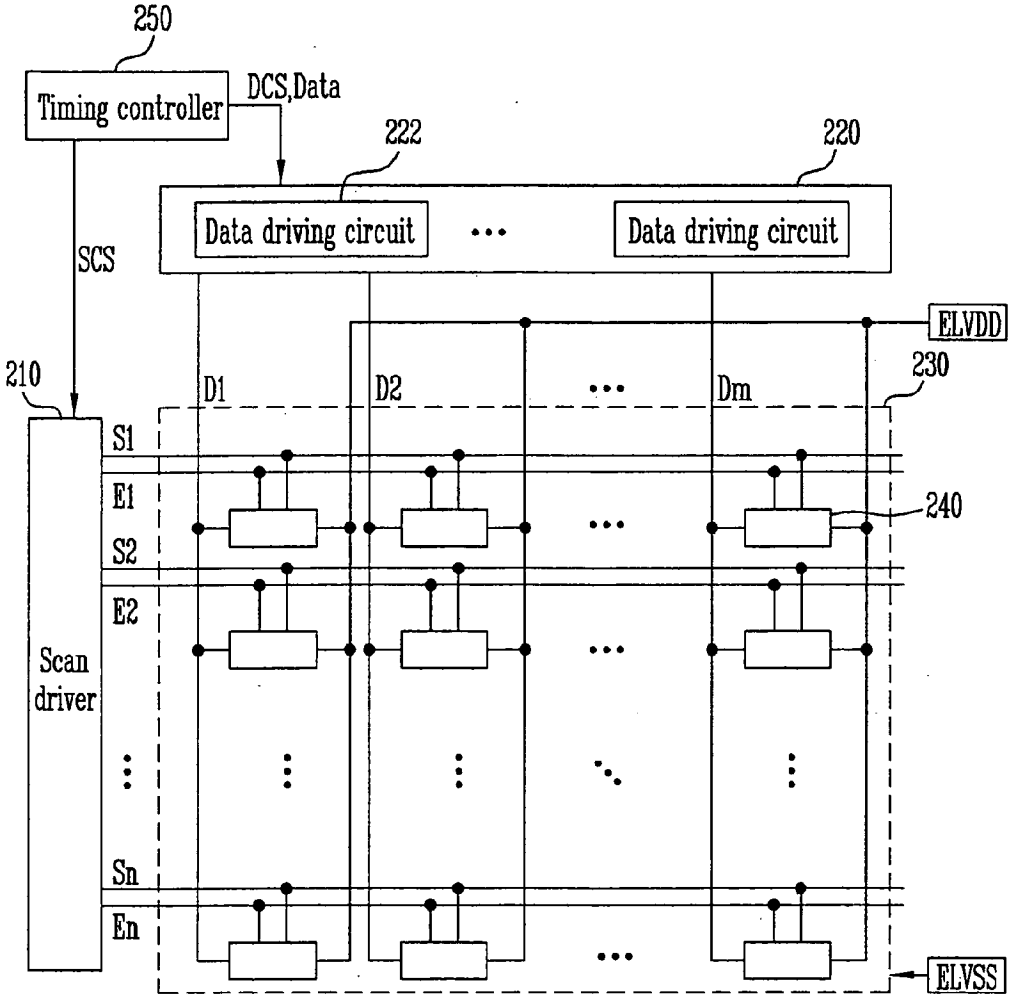

250
Timing controller
DCS,Data
222
220
Data driving circuit
Data driving circuit
SCS
ELVDD
210
230
D1
D2
Dm
S1
E1
240
S2
E2
Scan driver
Sn
En
ELVSS

FIG. 3

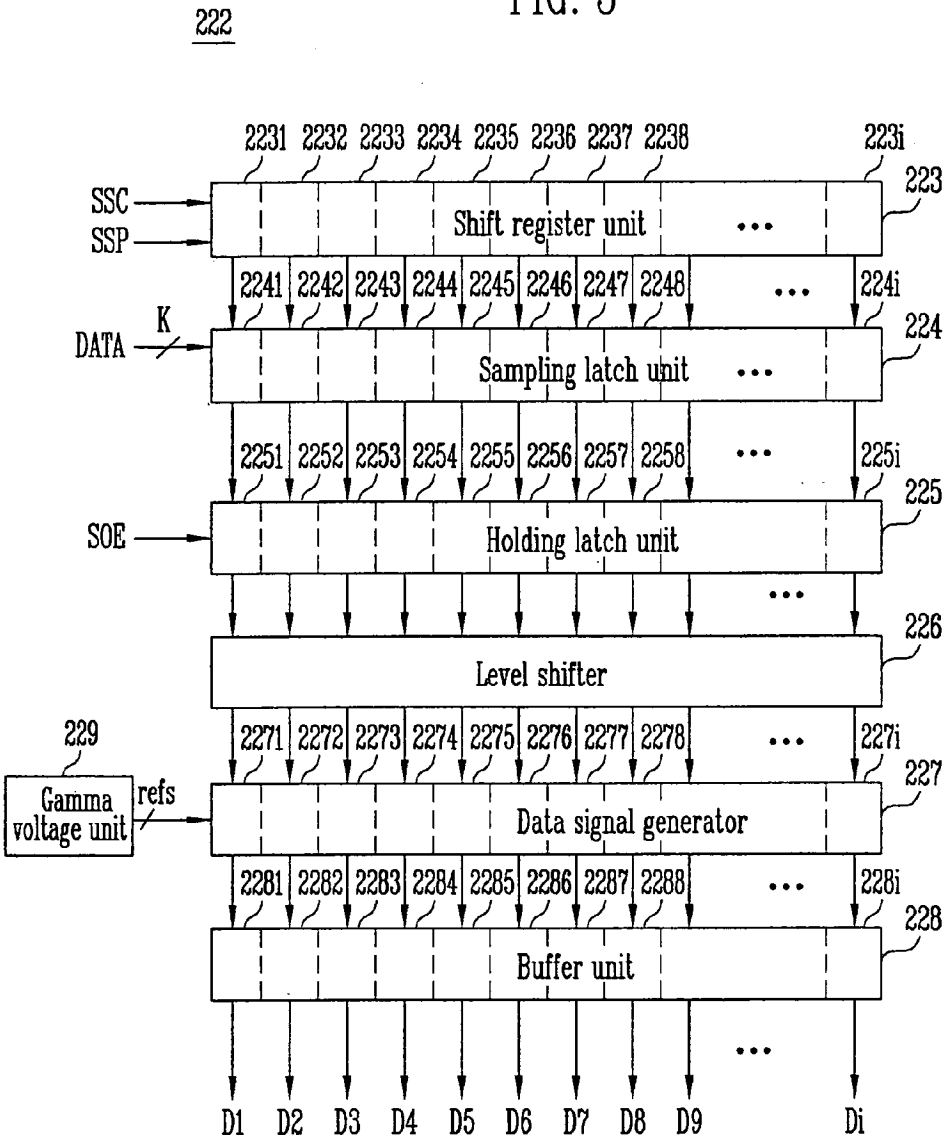

222
2231 2232 2233 2234 2235 2236 2237 2238
223i
223
SSC
SSP
Shift register unit
2241 2242 2243 2244 2245 2246 2247 2248
224i
K
DATA
224
Sampling latch unit
2251 2252 2253 2254 2255 2256 2257 2258
225i
225
SOE
Holding latch unit
226
Level shifter
229
2271 2272 2273 2274 2275 2276 2277 2278
227i
227
Gamma voltage unit
refs
Data signal generator
2281 2282 2283 2284 2285 2286 2287 2288
228i
228
Buffer unit
D1 D2 D3 D4 D5 D6 D7 D8 D9 Di

FIG. 4

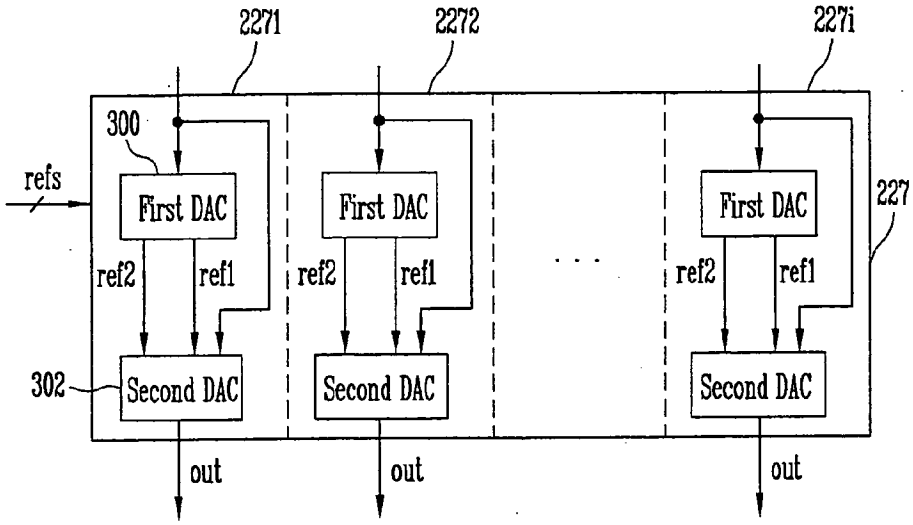

2271
2272
227i
300
refs
First DAC
First DAC
First DAC
227
ref2
ref1
ref2
ref1
ref2
ref1
302
Second DAC
Second DAC
Second DAC
out
out
out

FIG. 5

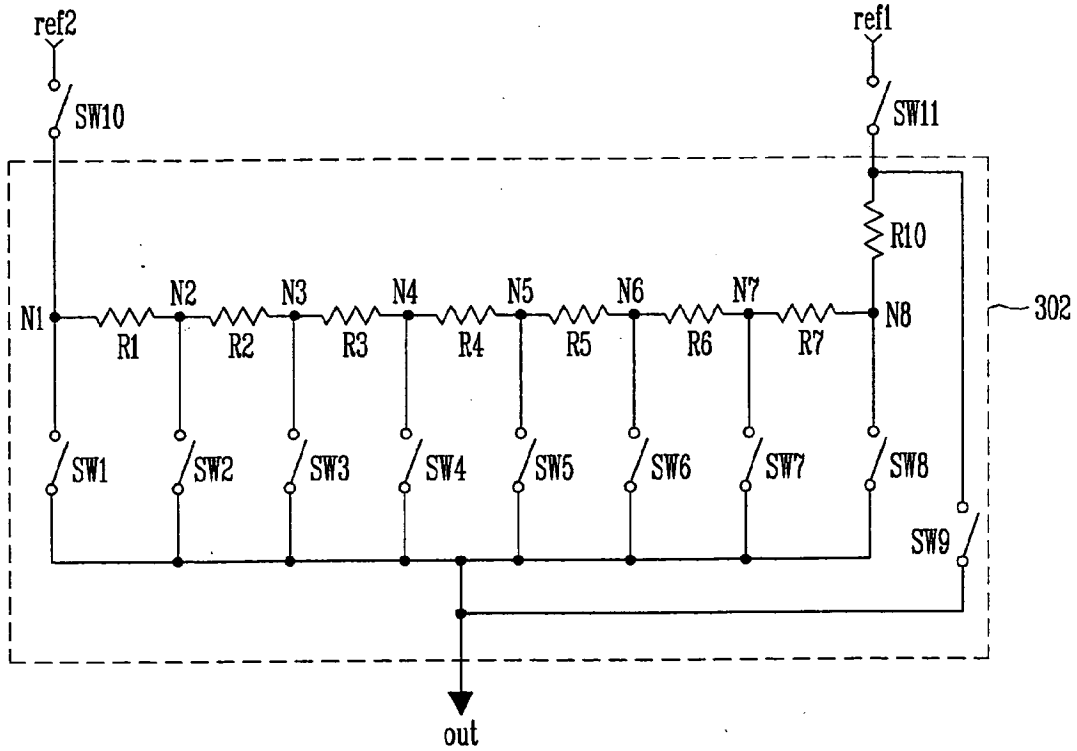

ref2
ref1
SW10
SW11
R10
N1
N2
N3
N4
N5
N6
N7
N8
302
R1
R2
R3
R4
R5
R6
R7
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
out

FIG. 6

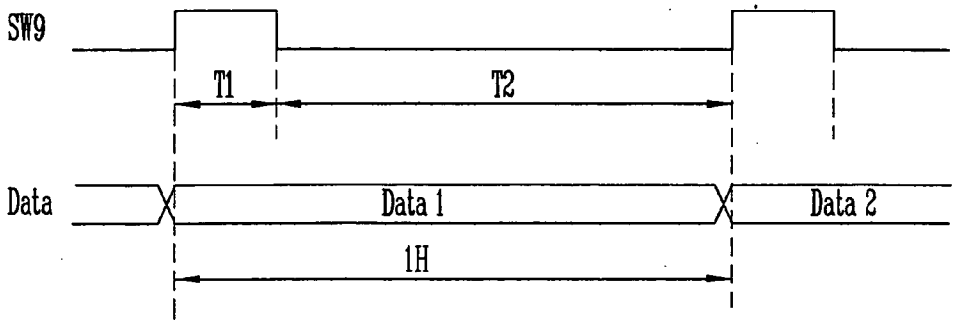

SW9
T1
T2
Data
Data 1
Data 2
1H

FIG. 7

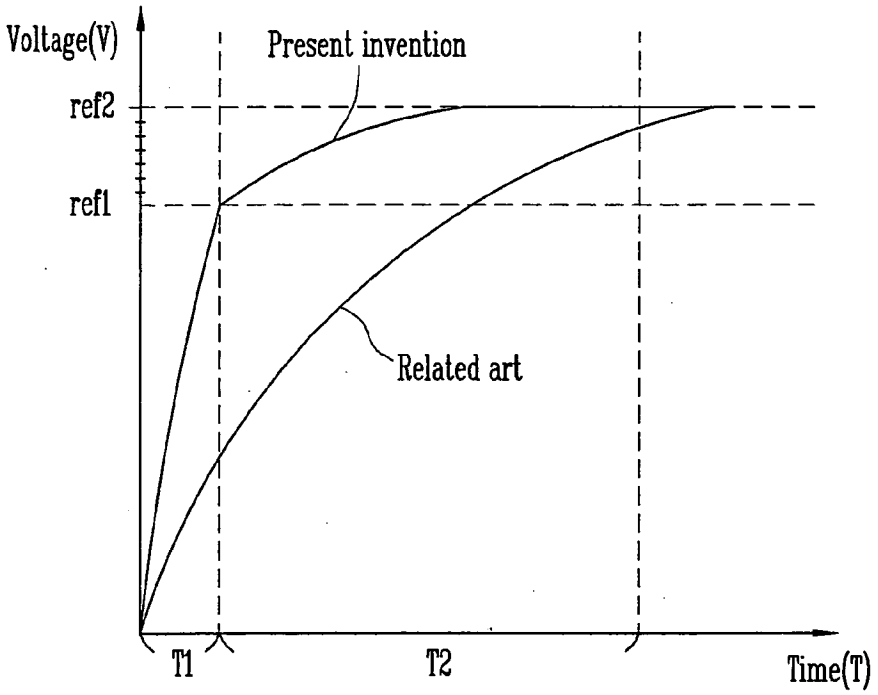

Voltage(V)
Present invention
ref2
ref1
Related art
T1
T2
Time(T)

FIG. 8

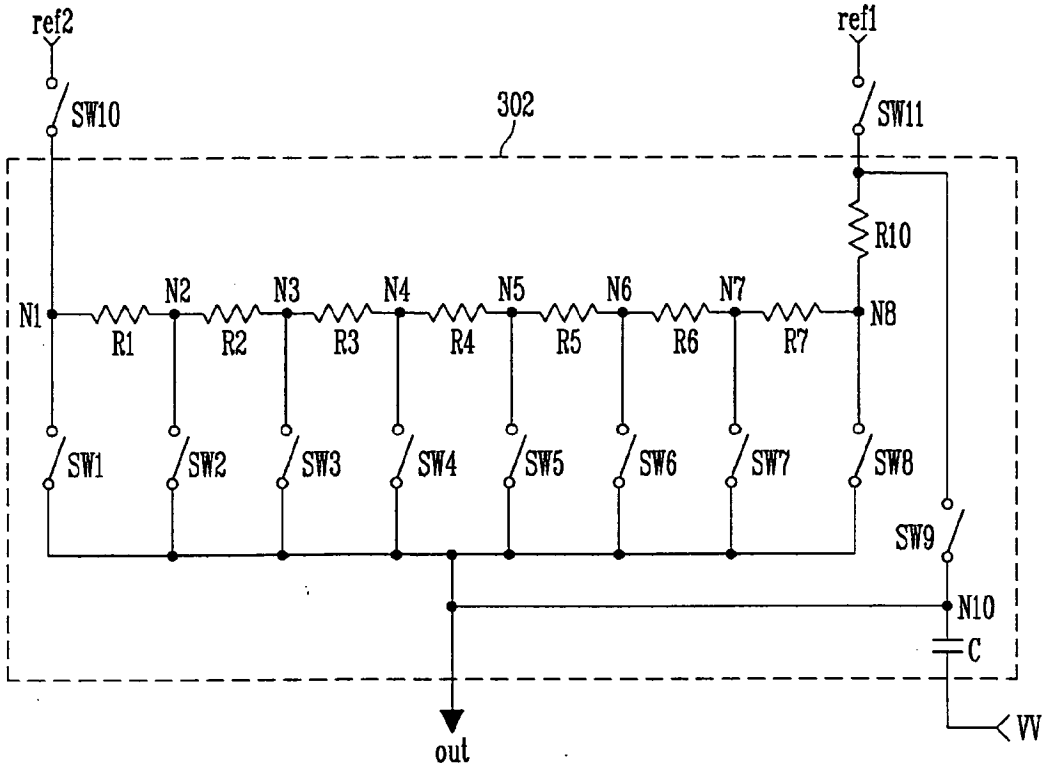

ref2
ref1
SW10
302
SW11
R10
N1
N2
N3
N4
N5
N6
N7
N8
R1
R2
R3
R4
R5
R6
R7
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
N10
C
VV
out

FIG. 9

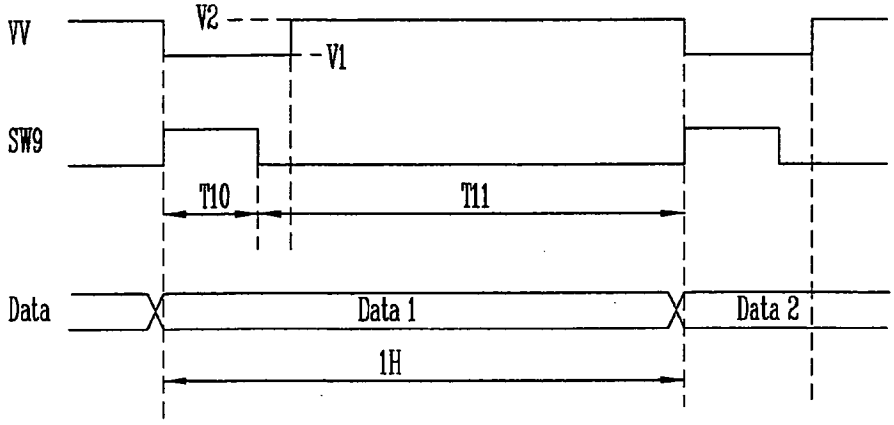

VV
V2
V1
SW9
T10
T11
Data
Data 1
Data 2
1H

FIG. 10

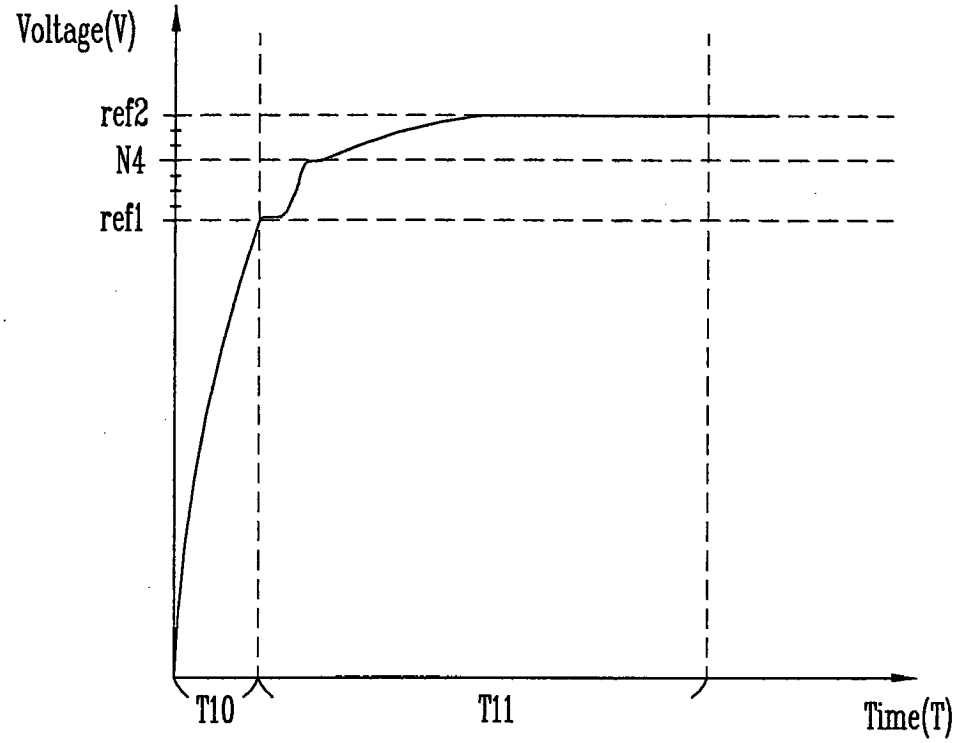


FIG. 11

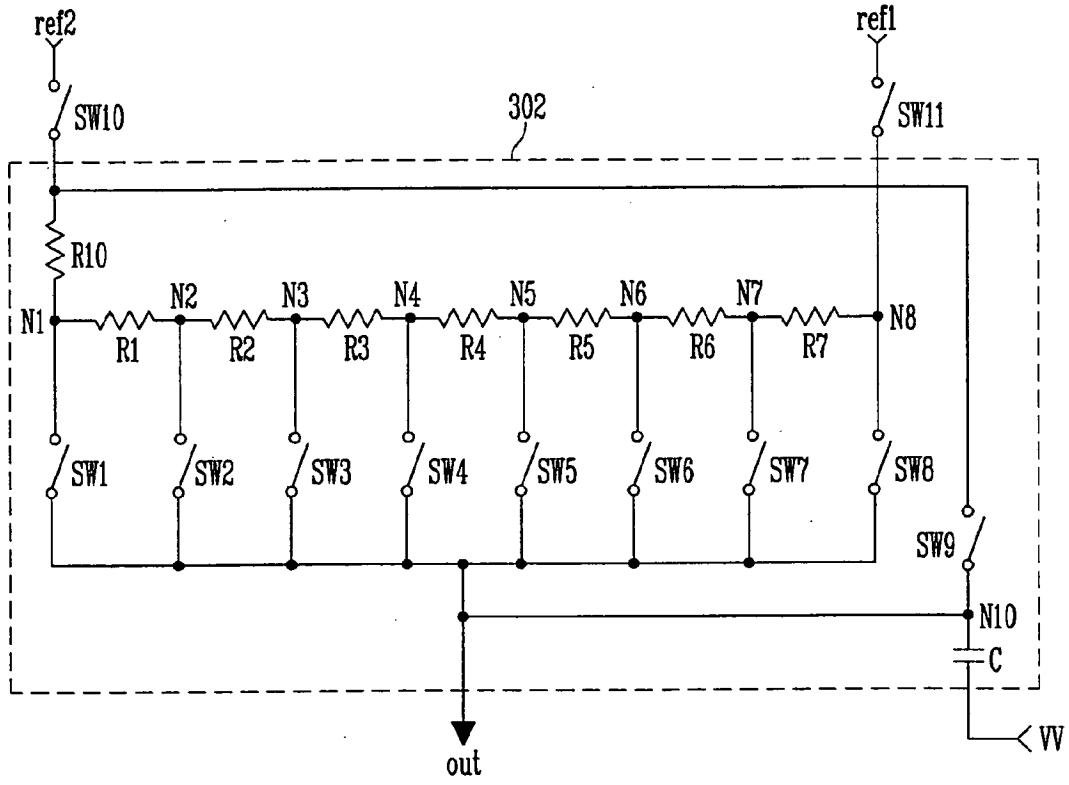

ref2
ref1
SW10
302
SW11
R10
N1
N2
N3
N4
N5
N6
N7
N8
R1
R2
R3
R4
R5
R6
R7
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
N10
C
VV
out

FIG. 12

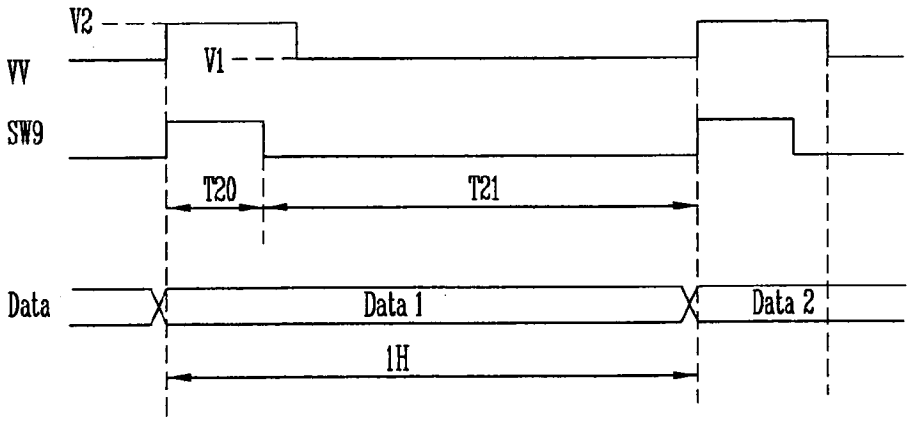
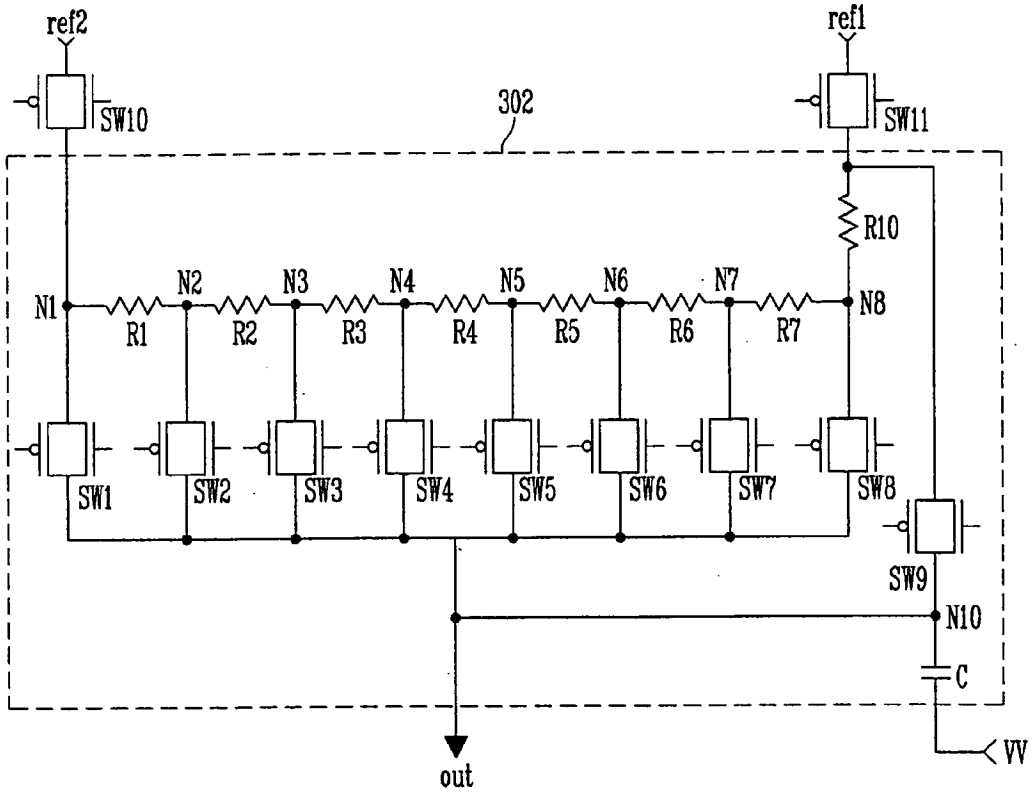

V2
V1
VV
SW9
T20
T21
Data
Data 1
Data 2
1H

FIG. 13


ref2
ref1
SW10
302
SW11
R10
N1
N2
N3
N4
N5
N6
N7
N8
R1
R2
R3
R4
R5
R6
R7
SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
N10
C
VV
out

专利名称(译)	数据驱动器，有机发光显示器及其驱动方法		
公开(公告)号	EP1796071A2	公开(公告)日	2007-06-13
申请号	EP2006256141	申请日	2006-11-30
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	CHOI SANG MOO		
发明人	CHOI, SANG-MOO		
IPC分类号	G09G3/32 H03M1/76 G09G3/20 H03M1/68		
CPC分类号	G09G3/3225 G09G3/2011 G09G3/3291 G09G2300/0861 G09G2310/0248 G09G2310/027 G09G2320/0252 H03M1/682 H03M1/765		
优先权	1020050116001 2005-11-30 KR		
其他公开文献	EP1796071B1 EP1796071A3		
外部链接	Espacenet		

摘要(译)

一种数据驱动器，包括：第一数模转换器，被配置为根据数据的高位选择多个参考电压的两个参考电压;以及第二数模转换器，被配置为将两个参考电压分成a多个电压并将两个参考电压和分压电压中的任何一个电压作为数据信号提供给输出端，取决于数据的低位，其中第二数模转换器配置为提供中间灰度级在提供数据信号之前，输出端子的电压，中间灰度电压具有两个参考电压之间的电压。

FIG. 5