(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 207 557 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
12.10.2005 Bulletin 2005/41

(43) Date of publication A2:
22.05.2002 Bulletin 2002/21

(21) Application number: **01308327.4**

(22) Date of filing: **28.09.2001**

(51) Int Cl.[7]: **H01L 27/00**, H01L 51/40

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **28.09.2000 JP 2000296582**
20.09.2001 JP 2001287328

(71) Applicant: **SANYO ELECTRIC CO., LTD.**
Moriguchi-shi, Osaka (JP)

(72) Inventors:
- **Yamada, Tsutomu**
  Motosu-gun, Gifu (JP)
- **Yoneda, Kiyoshi**
  Motosu-gun, Gifu (JP)

(74) Representative:
Cross, Rupert Edward Blount et al
BOULT WADE TENNANT,
Verulam Gardens
70 Gray's Inn Road
London WC1X 8BT (GB)

(54) Method of attaching layer material and forming layer in predetermined pattern on substrate using mask

(57) Upon formation of a layer such as an emissive layer of an organic EL element by attaching an emissive material onto a substrate (10), an evaporation mask (100) including an opening (110) corresponding to the layer formed to have a plurality of individual patterns and having an area, for example, smaller than the substrate is disposed between the substrate (10) and a material source (200). A relative position between the mask (100) and the material source (200), and the substrate (10) is slid by a predetermined pitch corresponding to the size of a pixel of the substrate (10), thereby forming a material layer (such as the emissive layer 64) in a predetermined region of the substrate. As a result, the material layer can be formed on the substrate through, for example, evaporation with a high accuracy.

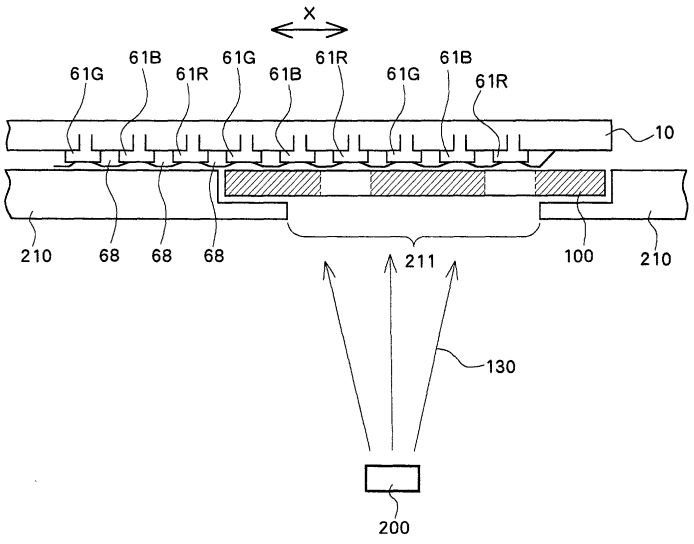

Fig. 4

EP 1 207 557 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 30 8327

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 06, 22 September 2000 (2000-09-22) -& JP 2000 068053 A (MATSUSHITA ELECTRIC IND CO LTD), 3 March 2000 (2000-03-03) * abstract * * paragraph [0026] - paragraph [0028] * * paragraph [0031] - paragraph [0033]; figures 1,2 *	1,5,6,16	H01L27/00 H01L51/40
A		7-10, 13-15	

X	US 6 093 445 A (NAWATE ET AL) 25 July 2000 (2000-07-25) * abstract; figures 1,2 * * column 1, line 64 - line 67 * * column 3, line 55 *	1,2,15	

X	US 4 303 489 A (MORRISON, JR. ET AL) 1 December 1981 (1981-12-01) * abstract * * column 2, line 57 - column 3, line 11 *	1	
	-----		TECHNICAL FIELDS SEARCHED (Int.Cl.7)
P,X	EP 1 128 449 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD) 29 August 2001 (2001-08-29) * paragraphs [0022], [0108], [0111] *	1,5,16	H01L C23C H05B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	19 August 2005	Bakos, T

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 30 8327

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

19-08-2005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 2000068053 A	03-03-2000	NONE	
US 6093445 A	25-07-2000	JP 3018172 B2	13-03-2000
		JP 2000058453 A	25-02-2000
US 4303489 A	01-12-1981	NONE	
EP 1128449 A	29-08-2001	CN 1311523 A	05-09-2001
		EP 1128449 A2	29-08-2001
		JP 2001345176 A	14-12-2001
		TW 495809 B	21-07-2002
		US 2001017409 A1	30-08-2001

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

专利名称(译)	使用掩模在基板上附着预定图案的层材料和形成层的方法		
公开(公告)号	EP1207557A3	公开(公告)日	2005-10-12
申请号	EP2001308327	申请日	2001-09-28
[标]申请(专利权)人(译)	三洋电机株式会社		
申请(专利权)人(译)	SANYO ELECTRIC CO.，LTD.		
当前申请(专利权)人(译)	SANYO ELECTRIC CO.，LTD.		
[标]发明人	YAMADA TSUTOMU YONEDA KIYOSHI		
发明人	YAMADA, TSUTOMU YONEDA, KIYOSHI		
IPC分类号	H05B33/10 C23C14/04 G09F9/00 G09F9/30 H01L27/32 H01L51/00 H01L51/30 H01L51/40 H01L51/50 H01L51/56 H05B33/12 H01L27/00		
CPC分类号	H01L51/0013 C23C14/042 H01L27/3211 H01L51/001 H01L51/0011 H01L51/0059 H01L51/0062 H01L51/0081 H01L51/56		
优先权	2000296582 2000-09-28 JP 2001287328 2001-09-20 JP		
其他公开文献	EP1207557A2		
外部链接	Espacenet		

摘要(译)

在通过将发光材料附着到基板（10）上形成诸如有机EL元件的发光层的层时，蒸发掩模（100）包括与形成为具有多个单独的层对应的开口（110）在基板（10）和材料源（200）之间设置例如小于基板的区域。掩模（100）和材料源（200）之间的相对位置以及基板（10）以与基板（10）的像素的尺寸相对应的预定间距滑动，从而形成材料层（诸如此类）。作为发光层64）在基板的预定区域中。结果，可以通过例如高精度的蒸发在基板上形成材料层。

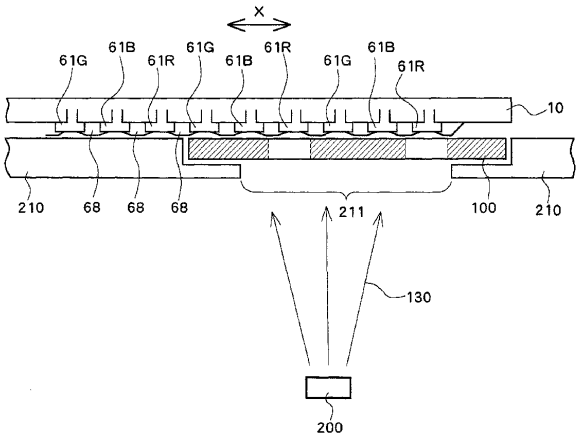

Fig. 4