(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 May 2009 (07.05.2009)

PCT

(10) International Publication Number
WO 2009/055920 A1

(51) International Patent Classification:
H01L 51/50 (2006.01) *H01L 27/32* (2006.01)
H01L 23/52 (2006.01)

(21) International Application Number:
PCT/CA2008/001914

(22) International Filing Date: 28 October 2008 (28.10.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2,610,148 29 October 2007 (29.10.2007) CA

(71) Applicant *(for all designated States except US)*: **IGNIS INNOVATION INC.** [CA/CA]; 22 Frederick Street, Suite 1020, Kitchener, Ontario N2H 6M6 (CA).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **NATHAN, Arokia** [CA/GB]; 189 Huntingdon Road, Cambridge CB3 0DL (GB). **CHAJI, G., Reza** [CA/CA]; 507-196 Westmount Road North, Waterloo, Ontario N2L 3G5 (CA).

(74) Agents: **HARRIS, John, D.** et al.; Gowling Lafleur Henderson LLP, Suite 2600, 160 Elgin Street, Ottawa, Ontario K1P 1C3 (CA).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(54) Title: HIGH APERTURE RATIO PIXEL LAYOUT FOR DISPLAY DEVICE

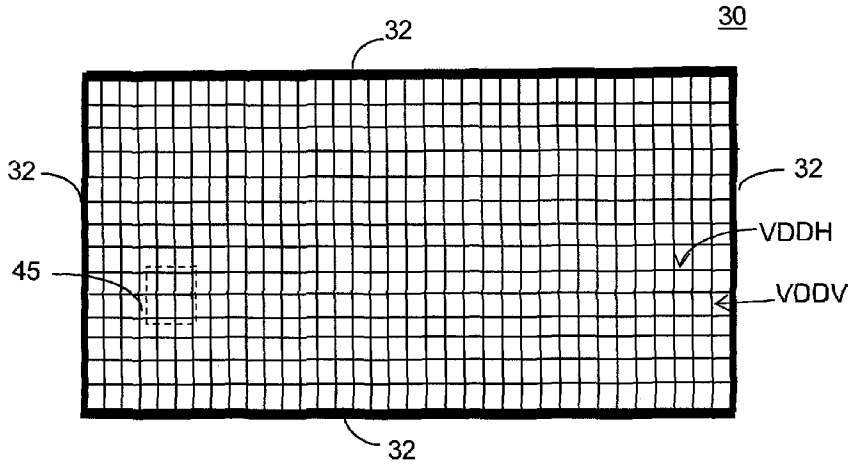

FIG. 3

(57) Abstract: A display device, pixel layout and method of forming the same is provided. The display device includes: a plurality of pixels formed in a pixel array area; and a power supply grid for distributing power to the pixels. Each pixel has a light emitting device and a plurality of transistors. The power supply grid includes a first group of power supply lines and a second group of power supply lines. The first group of power supply lines extend across the pixel array area. The second group of power supply lines extends across the pixel array area and electrically contacts the first group of power supply lines in the pixel array area. Each pixel is coupled to at least one power supply line in the first group of power supply lines and the second group of power supply lines.

WO 2009/055920 A1

High Aperture Ratio Pixel Layout For Display Device

FIELD OF INVENTION

[0001] The present invention relates to a display device, and more specifically to a display device having a plurality of pixels with high aperture ratio.

BACKGROUND OF THE INVENTION

[0002] Active-matrix organic light-emitting diode (AMOLED) displays have become more attractive due to their advantages, such as, low temperature fabrication, its low cost fabrication, and a high resolution with a wide viewing angle.

[0003] Figure 1 illustrates a power supply line distribution in a conventional AMOLED display panel. The panel display device 10 of Figure 1 includes a plurality of pixels arranged in rows and columns. In the panel, each column (or row) has its own power supply line 12 or shares it with its adjacent column (or row). The power supply lines 12 are extended vertically and connected to panel power supply bars 14 disposed horizontally in two sides of the panel. The panel power supply bars 14 provide driving voltages to the power supply lines 12. Each pixel operates using power provided through the corresponding power supply line 12.

[0004] Figure 2 illustrates an example of a RGBW pixel layout of Figure 1. A region 25 contains a pixel 20 having four pixel components 22a (White), 22b (Red), 22c (Blue), and 22d (Green). Each pixel component operates using power provided through the corresponding power supply line 12.

[0005] In Figure 2, the column of the pixel 20 shares two power supply lines 12 with its adjacent columns. Thus it is not required to dispose a power supply line for each column. However, in a large-area display with high current density, the power supply line 12 should be wide. As a result, the aperture ratio is compromised reducing the panel lifetime.

SUMMARY OF THE INVENTION

[0006] It is an object of the invention to provide a display device that obviates or mitigates at least one of the disadvantages of existing systems.

[0007] According to an aspect of the present invention there is provided a display device includes: a plurality of pixels formed in a pixel array area; and a power supply grid for distributing power to the pixels. Each pixel has a light emitting device and a plurality of transistors. The power supply grid includes a first group of power supply lines and a second group of power supply lines. The first group of power supply lines extends across the pixel array area. The second group of power supply lines extends across the pixel array area and electrically contacts the first group of power supply lines in the pixel array area. Each pixel is coupled to at least one power supply line in the first group of power supply lines and the second group of power supply lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

Figure 1 is a schematic diagram illustrating a conventional power supply line distribution layout for an AMOLED display panel;

Figure 2 is a schematic diagram illustrating a RGBW pixel layout for the panel of Figure 1;

Figure 3 is a schematic diagram illustrating an example of a power supply grid layout for a display panel, in accordance with an embodiment of the present invention;

Figure 4 is a schematic diagram illustrating an example of a RGBW pixel layout for the panel of Figure 3.

Figure 5 is a schematic diagram illustrating an example of a pixel circuit for the pixel layout of Figure 4;

Figure 6 is a plan view illustrating a RGBW pixel layout with the power supply grid and the pixel circuit of Figure 5;

Figure 7 is a vertical cross section view of the RGBW pixel of Figure 6; and

Figure 8 is a horizontal cross section view of the RGBW pixel of Figure 6.

DETAILED DESCRIPTION

[0009] Embodiments of the present invention are described using a panel having a pixel with an OLED, e.g., AMOLED display panels, OLED flat panels. However, any display device driven by a power supply line for supplying power to a light emitting device (or layer) falls within the scope of the embodiments.

[0010] In the embodiments, relative terms, such as "horizontal" and "vertical" are used to describe the geographical relationship among elements. However, it will be appreciated by one of ordinary skill in the art that the terms "horizontal" and "vertical" are examples only, and may encompass two different directions which are determined, for example, by the requirement of a pixel layout.

[0011] Referring to Figure 3, a power supply grid layout for a panel in accordance with an embodiment of the present invention is described. The panel display device 30 of Figure 3 contains a power supply grid that can reduce the width of each power supply line, thereby reducing the IR-drop and increasing the aperture ratio.

[0012] The power supply grid includes a plurality of power supply lines VDDVs extended in a first direction (e.g., vertically) across a pixel array area and a plurality of power supply lines VDDHs extended in a second direction (e.g., horizontally) across the pixel array area. The power supply lines VDDV and VDDH are electrically connected at their cross points in the pixel array area. The power supply lines VDDVs and VDDHs may be formed by different metals, ITO, or any other conductor used in the panel.

[0013] In Figure 3, the panel has a rectangular shape. However, the panel may have a shape different from that of Figure 3, as would be appreciated by one of ordinary skill in the art. In Figure 3, "VDDH" extends in a direction perpendicular to "VDDV". However, Each of "VDDH " and "VDDV" may extend in a direction different from that shown in Figure 3. It would be appreciated by one of ordinary skill in the art that the number of VDDVs and VDDHs may vary based on the pixel layout and current densities.

[0014] The power supply lines VDDVs and VDDHs are connected to a panel VDD ring 32 disposed in the periphery of the panel. In Figure 3, the VDD ring 32 is formed so as to surround the rectangle-shaped panel. The VDD ring 32 has main wires that provide a driving voltage to each power supply line VDDV, VDDH.

[0015] The panel may be a bottom emission type display or a top emission type display, including bottom and top emission displays for RGB and RGBW. The panel includes a plurality of pixels arranged in row and column. The VDD power is distributed to the pixels in the panel uniformly, through the power supply lines VDDVs and VDDHs.

[0016] The power supply grid provides a better (lower) resistance and distribution. There is no need to use wide metals for VDDH and VDDV. The width of each power supply line VDDH, VDDV can be small while the effective resistance is low.

[0017] The power supply lines VDDVs and VDDHs distribute VDD voltage and current across the panel uniformly, which results in minimizing IR drop across the panel (especially when the panel of Figure 3 is a large panel with high luminance).

[0018] Figure 4 illustrates an example of a RGBW pixel layout for the panel of Figure 3. In Figure 4, "VDDHi" (i=n-1, n, n+1) represents a power supply line corresponding to VDDH of Figure 3; "VDDVj" (j=m-1, m, m+1) represents a power supply line corresponding to VDDV of Figure 3. In Figure 4, a pixel region 45 contains a pixel 40 having four pixel components (circuits) 42a, 42b, 42c, and 42d for "White", "Red", "Blue", and "Green", respectively. The power supply line VDDVj and the power supply line VDDHi are electrically connected at a contact point 44. For example, VDDHn-1 is connected to VDDVm-1, VDDVm, and VDDVm+1, where each of VDDVm-1, VDDVm and VDDVm+1 is further connected to VDDHn and VDDHn+1.

[0019] Each of the "White", "Red", "Blue", and "Green" pixel components 42a-42d is connected to a plurality of power supply lines and uses VDD voltage/current from them. For example, VDDHn-1 is directly connected to a transistor for the White pixel component 42a where VDDHn-1 is connected to VDDVm-1 and VDDVm. VDDHn may be directly coupled

to the White pixel component 42a, the Red pixel component 42c, the Blue pixel component 42c, and the Green pixel component 42d. VDDHi may be shared with another pixel (not shown in Figure 4). Similary VDDVj may be shared with another pixel (not shown in Figure 4).

[0020] The power supply lines VDDHi and VDDVj distribute VDD power to the pixels uniformly. The width of each power supply lines VDDHi and VDDVj can be smaller than that of Figure 1, and the effective resistance of each power supply line VDDHi, VDDVj is low.

[0021] In this example, each pixel component is defined by two power supply lines VDDVs extending in a first direction and two power supply lines VDDHs extending in a second direction perpendicular to the first direction. However, the number of VDDVs and VDDHs varies based on the pixel layout and current densities.

[0022] Figure 5 illustrates an example of a pixel circuit for the RGBW pixel layout of the Figure 4. The pixel circuit 50 of Figure 5 includes a switch transistor 52, a drive transistor 54, a storage capacitor 56, and an OLED 58. The pixel circuit 50 corresponds to, for example, the pixel component 42d ("Green") of Figure 4.

[0023] The transistors 52 and 54 are thin film transistors (TFTTs). Each transistor has a gate terminal and first and second terminals (e.g., source/drain). The gate terminal of the switch transistor 52 is connected to a select line (address line) 62. The first and second terminals of the switch transistor 52 is connected between a data line (Vdata) 60 and the gate terminal of the drive transistor 54. The first and second terminals of the drive transistor 54 is connected to the power supply line VDDHn and the OLED 58. The storage capacitor 56 is connected to the gate terminal of the drive transistor 54 and the OLED 58. The power supply line VDDHn is connected to the power supply lines VDDVm and VDDVm+1 that are connected to the power supply line VDDVn+1.

[0024] Figure 6 illustrates a plan view of a RGBW pixel layout with the power supply grid and the pixel circuit of Figure 5. Figure 7 illustrates a vertical cross section view of the

RGBW pixel of Figure 6. Figure 8 illustrates a horizontal cross section view of the RGBW pixel of Figure 6.

[0025] Referring to Figures 5-8, the power supply lines VDDH and VDDV are fitted between the distances between OLED banks 72 so that the aperture ratio is not affected. The panel using the pixel of Figure 6 provides for front screen luminance of , for example, 500 cd/m2 after polarizer imposing large current density at peak luminance. In the panel of Figure 6, large TFTs are used to reduce the aging of the TFT. However, the aperture ratio is higher than 58%. Moreover, the resistance of between the VDD contact (44 of Figure 4) and each pixel is negligible since each contact carry only small current for each pixel while the power supply lines VDDHs and VDDVs carry the entire current for the panel.

[0026] One or more currently preferred embodiments have been described by way of example. It will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A display device comprising:

a plurality of pixels formed in a pixel array area, each having a light emitting device and a plurality of transistors; and

a power supply grid for distributing power to the pixels, the power supply grid including a first group of power supply lines and a second group of power supply lines, the first group of power supply lines extending across the pixel array area, the second group of power supply lines extending across the pixel array area and electrically contacting the first group of power supply lines in the pixel array area, each pixel being coupled to at least one power supply line in the first group of power supply lines and the second group of power supply lines.

2. A display device as claimed in claim 1, wherein the power supply grid distributes uniform current to the pixels.

3. A display device as claimed in claim 1, wherein the power supply grid distributes uniform voltage to the pixels.

4. A display device as claimed in claim 1, wherein the power supply grid comprises:

a coupler coupled to the first group of power supply lines and the second group of power supply lines.

5. A display device as claimed in claim 4, wherein the coupler comprises:

a power supply ring structure disposed on the periphery of the pixel array, coupled to the first group of power supply lines and the second group of power supply lines.

6. A display device as claimed in claim 1, wherein the light emitting device is an organic light emitting diode (OLED).

7. A display device as claimed in claim 6, wherein the first group of power supply lines are formed between OLED banks.

8. A display device as claimed in claim 7, wherein the second group of power supply lines are formed between OLED banks.

9. A display device as claimed in claim 1, wherein a power supply line in the first group of power lines is directly coupled to adjacent pixels.

10. A display device as claimed in claim 1, wherein a power supply line in the first group of power lines is formed between two adjacent pixels

11. A display device as claimed in claim 1, wherein the pixel array has a RGB top emission or bottom emission structure.

12. A display device as claimed in claim 1, wherein the pixel array has a RGBW top emission or bottom emission structure.

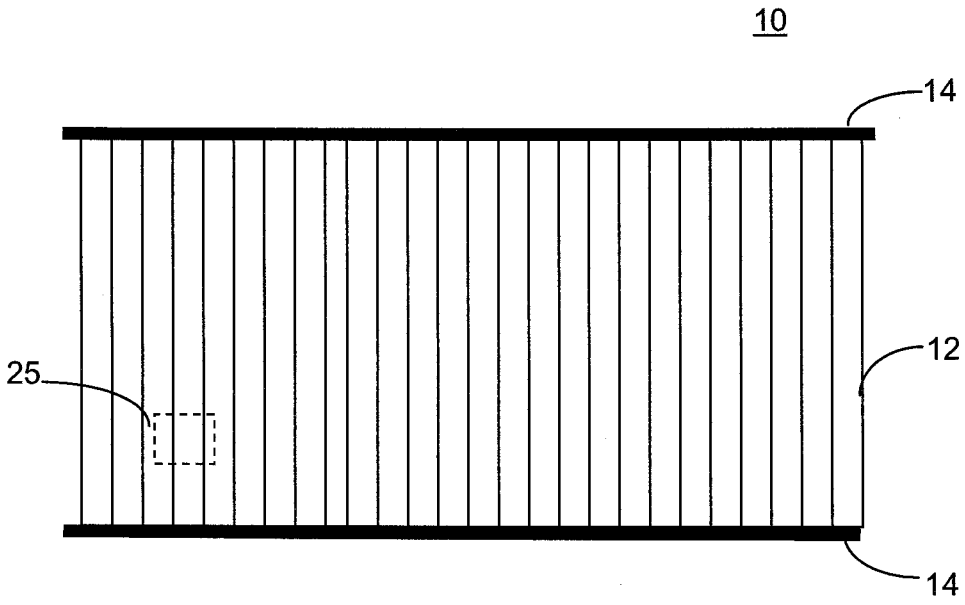

FIG. 1

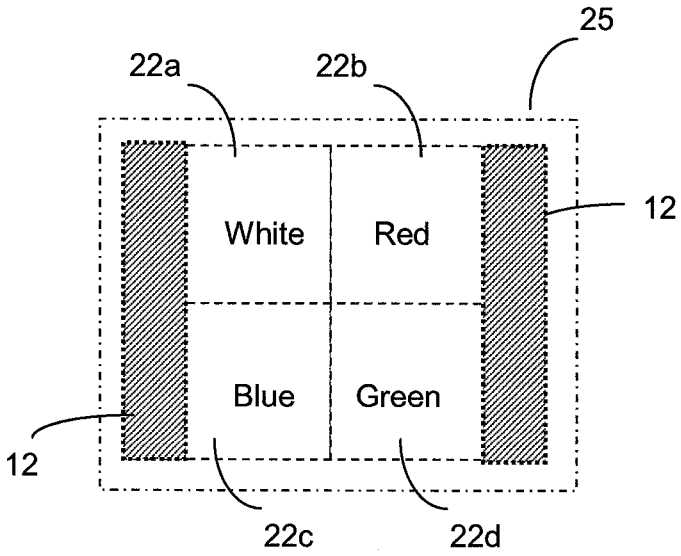

FIG. 2

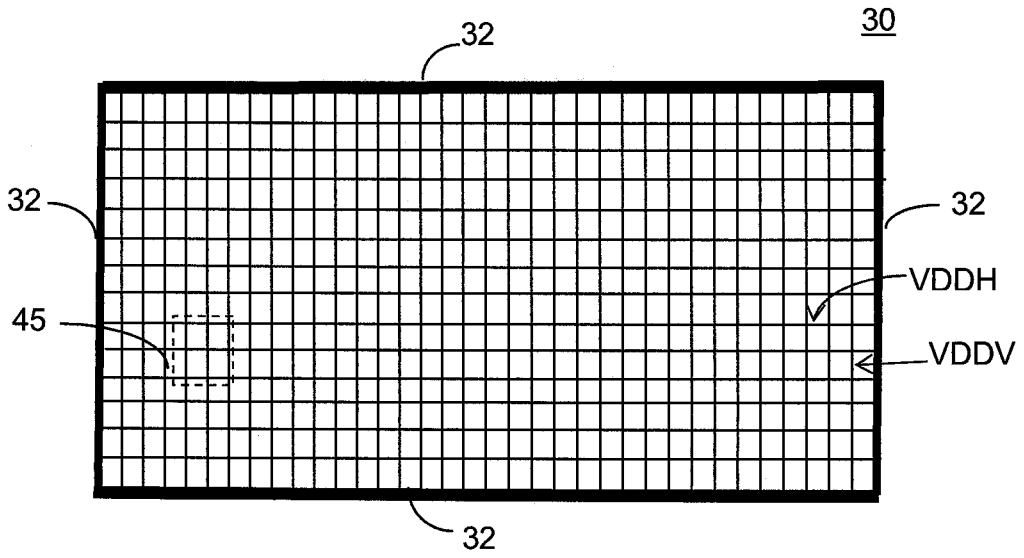
30
32
32
32
32
45
VDDH
VDDV

FIG. 3

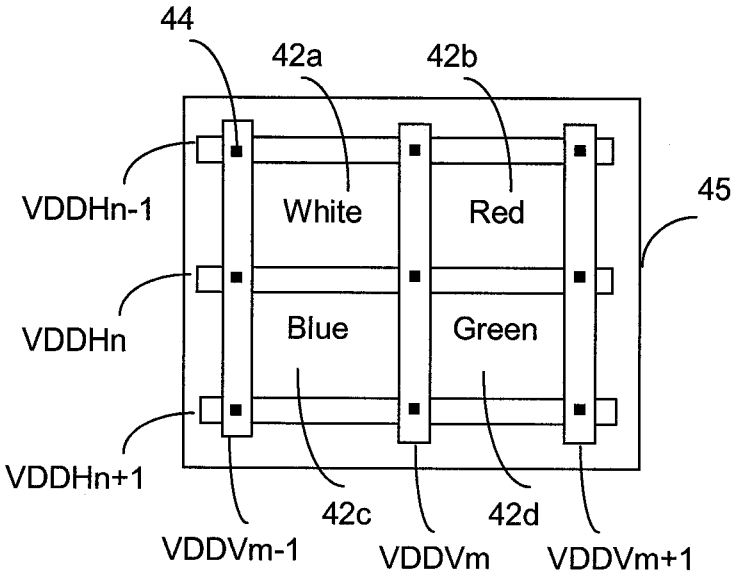
44
42a
42b
VDDHn-1
White
Red
45
VDDHn
Blue
Green
VDDHn+1
42c
42d
VDDVm-1
VDDVm
VDDVm+1

FIG. 4

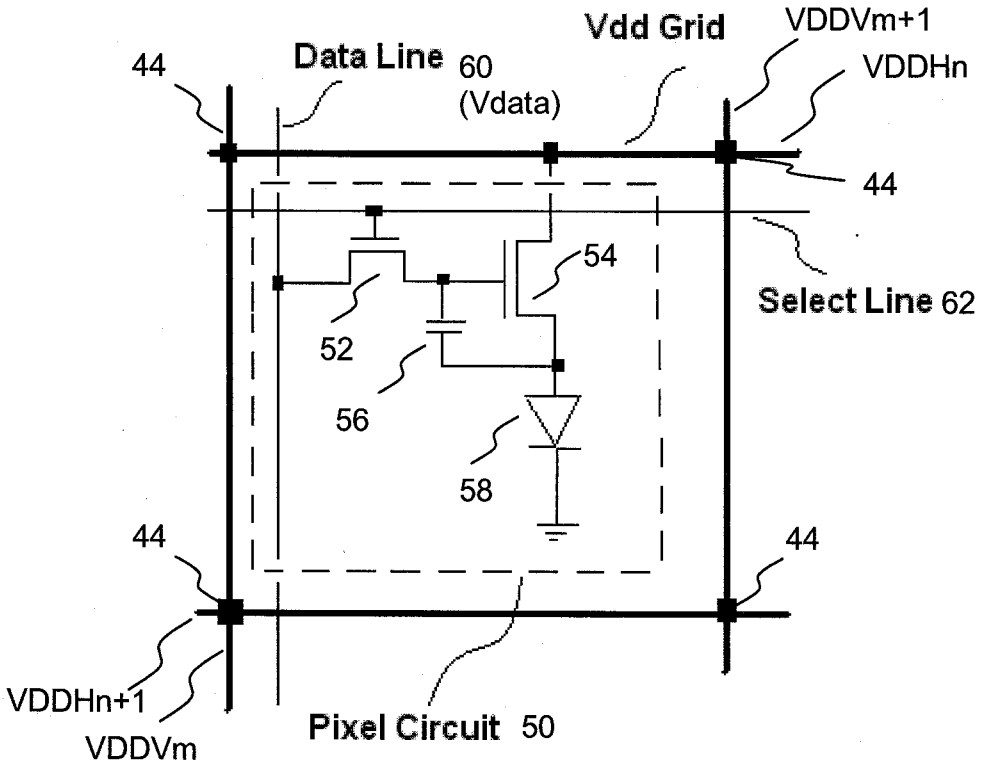
Vdd Grid
VDDVm+1
VDDHn
44
Data Line 60
(Vdata)
44
54
Select Line 62
52
56
58
44
44
VDDHn+1
VDDVm
Pixel Circuit 50

FIG. 5

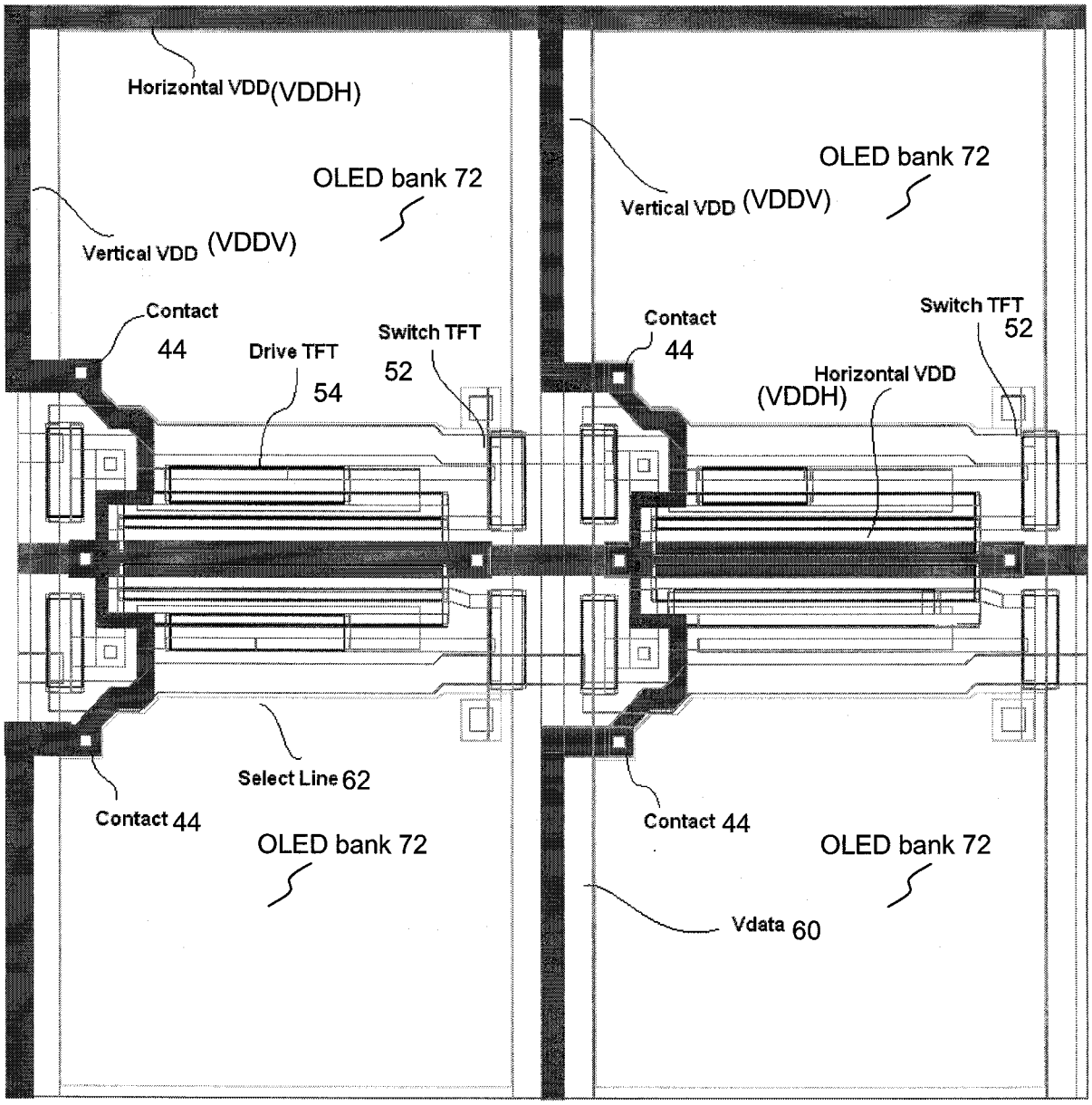
Horizontal VDD (VDDH)
OLED bank 72
Vertical VDD (VDDV)
Contact 44
Drive TFT 54
Switch TFT 52
Select Line 62
Contact 44
OLED bank 72
Vertical VDD (VDDV)
OLED bank 72
Contact 44
Switch TFT 52
Horizontal VDD (VDDH)
Contact 44
OLED bank 72
Vdata 60

FIG. 6

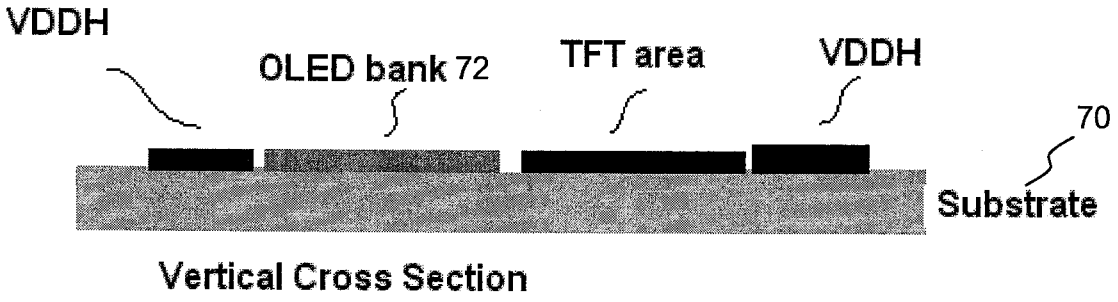
VDDH
OLED bank 72
TFT area
VDDH
70
Substrate
Vertical Cross Section

FIG. 7

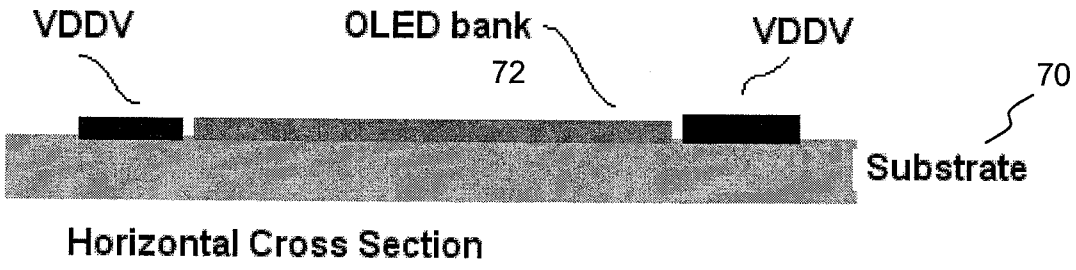
VDDV
OLED bank
72
VDDV
70
Substrate
Horizontal Cross Section

FIG.8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2008/001914

A. CLASSIFICATION OF SUBJECT MATTER
IPC: ***H01L 51/50*** (2006.01) , ***H01L 23/52*** (2006.01) , ***H01L 27/32*** (2006.01)
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L (2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)
Databases: Canadian Patents Database, WEST, Delphion, Google Patents, IEEE XPLORE
Keywords: grid, power, supply, pixel, uniform, current, voltage, ring, OLED, organic, RGB, RGBW, top emission, bottom emission

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/0182672 A1 (Hoppenbrouwers et al.) 9 August 2007 (09-08-2007) * Abstract; Fig 1, 3, 4, 6, 7; par [0002] - [0004] and [0021] - [0037] *	1 - 12
A	US 6,380,688 B1 (Bae et al.) 30 April 2002 (30-04-2002) * Whole Document *	
A	US 6,229,508 B1 (Kane) 8 May 2001 (08-05-2001) * Whole Document *	
A	US 7,242,398 B2 (Nathan et al.) 10 July 2007 (10-07-2007) * Whole Document *	
A	US 7,248,236 B2 (Nathan et al.) 24 July 2007 (24-07-2007) * Whole Document *	
A	US 2007/0247398 A1 (Nathan et al.) 25 October 2007 (25-10-2007) * Whole Document *	

[ ] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 December 2008 (15-12-2008)	14 January 2009 (14-01-2009)

Name and mailing address of the ISA/CA	Authorized officer
Canadian Intellectual Property Office Place du Portage I, C114 - 1st Floor, Box PCT 50 Victoria Street Gatineau, Quebec K1A 0C9 Facsimile No.: 001-819-953-2476	Raghid Shreih 819- 994-2694

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CA2008/001914

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US 2007182672A1	09-08-2007	CN 1930603A	14-03-2007
		EP 1728236A1	06-12-2006
		JP 2007528513T	11-10-2007
		WO 2005088593A1	22-09-2005
US 6380688B1	30-04-2002	KR 20010017933A	05-03-2001
US 6229508B1	08-05-2001	EP 0905673A1	31-03-1999
		EP 0905673B1	26-11-2008
		JP 3767877B2	19-04-2006
		JP 4045285B2	13-02-2008
		JP 11219146A	10-08-1999
		JP 2006146257A	08-06-2006
		US 6618030B2	09-09-2003
		US 2001024186A1	27-09-2001
US 7242398B2	10-07-2007	CA 2438603A1	29-08-2002
		CA 2438603C	09-10-2007
		EP 1362375A1	19-11-2003
		JP 2004531753T	14-10-2004
		US 2004124763A1	01-07-2004
		WO 02067329A1	29-08-2002
US 7248236B2	24-07-2007	CA 2438581A1	29-08-2002
		CA 2438581C	29-11-2005
		EP 1362374A2	19-11-2003
		JP 2004531752T	14-10-2004
		US 2004130516A1	08-07-2004
		WO 02067328A2	29-08-2002
		WO 02067328A3	07-11-2002
US 2007247398A1	25-10-2007	CA 2490858A1	07-06-2006
		CA 2526436A1	28-02-2006
		CA 2526436C	09-10-2007
		CA 2544090A1	06-06-2007
		CA 2583708A1	07-07-2007
		CN 101116128A	30-01-2008
		EP 1859431A1	28-11-2007
		JP 2008523425T	03-07-2008
		US 2006176250A1	10-08-2006
		WO 2006060902A1	15-06-2006
		WO 2007118332A1	25-10-2007

专利名称(译)	用于显示设备的高孔径比像素布局		
公开(公告)号	EP2206173A1	公开(公告)日	2010-07-14
申请号	EP2008845948	申请日	2008-10-28
[标]申请(专利权)人(译)	伊格尼斯创新公司		
申请(专利权)人(译)	IGNIS创新INC.		
当前申请(专利权)人(译)	IGNIS创新INC.		
[标]发明人	NATHAN AROKIA CHAJI G REZA		
发明人	NATHAN, AROKIA CHAJI, G., REZA		
IPC分类号	H01L51/50 H01L23/52 H01L27/32 G09G3/3225		
CPC分类号	G09G3/3225 G09G2300/0426 G09G2300/0452 G09G2330/02 H01L27/3276		
优先权	2610148 2007-10-29 CA		
外部链接	Espacenet		

摘要(译)

提供了一种显示装置，像素布局及其形成方法。该显示装置包括：形成在像素阵列区域中的多个像素;以及用于向像素分配电力的电源网格。每个像素具有发光器件和多个晶体管。供电网包括第一组电源线和第二组电源线。第一组电源线在像素阵列区域上延伸。第二组电源线在像素阵列区域上延伸并且电连接像素阵列区域中的第一组电源线。每个像素耦合到第一组电源线和第二组电源线中的至少一个电源线。