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(71) Applicant: **LG Display Co., Ltd.**
SEOUL, 07336 (KR)

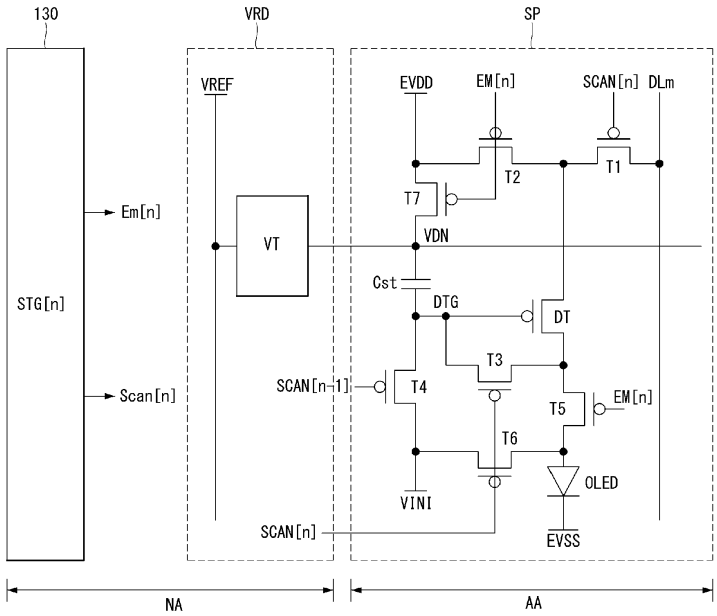
(72) Inventors:
- **KIM, Jaesung**
  10845 Gyeonggi-do (KR)
- **YOO, Juhnsuk**
  10845 Gyeonggi-do (KR)
- **KIM, Jungchul**
  10845 Gyeonggi-do (KR)
- **KONG, Chungsik**
  10845 Gyeonggi-do (KR)
- **SHIN, Mihee**
  10845 Gyeonggi-do (KR)

(74) Representative: **Ter Meer Steinmeister & Partner**
Patentanwälte mbB
Nymphenburger Straße 4
80335 München (DE)

(54) ELECTROLUMINESCENT DISPLAY DEVICE AND DRIVING METHOD THEREOF

(57) There is provided an electroluminescence display device comprising a display panel having a display area (AA) where images are displayed and a non-display area (NA) where images are not displayed, a subpixel (SP) located in the display area, and a voltage transfer part (VRD) that is located in the non-display area and transfers a reference voltage (VREF) to the subpixel in response to a signal applied from outside the display panel or a signal generated on the display panel.

Fig. 6



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Description

[0001] This application claims the benefit of Korean Patent Application No. 10-2017-0111225, filed on August 31, 2017, and No. 10-2017-0135720, filed on October 19, 2017.

BACKGROUND

Field

[0002] The present disclosure relates to an electroluminescence display and a driving method thereof.

Related Art

[0003] The market for displays which act as an intermediary between users and information is growing with the development of information technology. Thus, different types of display devices such as electroluminescence displays, liquid crystal displays, and quantum dot displays are increasingly used.

[0004] A display device comprises a display panel comprising a plurality of subpixels and a driving unit that drives the display panel. The driving unit comprises a gate driver that supplies gate signals to the display panel and a data driver that supplies data signals to the display panel.

[0005] In the case of an electroluminescence display, for example, when gate signals, data signals, etc. are supplied to the subpixels, the light-emitting elements of selected subpixels emit light to thereby display an image. The light-emitting elements may be implemented based on organic or inorganic materials.

[0006] The electroluminescence display has many advantages because it displays an image based on light generated by the light-emitting elements in the subpixels, so there is a need for improvements in the accuracy of pixel circuits that control the light emission of the subpixels. For example, the accuracy of the pixel circuits may be improved by compensating for time-varying characteristics (or variation with time), such as the threshold voltage of the transistors included in the pixel circuits.

[0007] The time-varying characteristics of the electroluminescence display can be compensated for in various ways. However, some of the commonly proposed compensation methods do not take drops in the voltage applied to the subpixels into consideration, which result in picture quality issues such as vertical luminance non-uniformity or crosstalk on the display panel.

[0008] Therefore, attempts are being made to seek solutions for improving the accuracy of the pixel circuits and gate driver in order to transfer accurate signals to the subpixels.

SUMMARY

[0009] The inventors of the present specification recognized the aforementioned problems and devised a display panel for minimizing voltage drops on voltage-supply lines and invented a display device using the same.

[0010] An aspect of the present disclosure is to provide a pixel circuit electroluminescence display that can solve/address picture quality issues such as vertical luminance non-uniformity or crosstalk on the display panel by compensating for time-varying characteristics, with voltage drops on voltage supply lines taken into consideration, and an electroluminescence display comprising the same.

[0011] Another aspect of the present disclosure is to provide an electroluminescence display that can achieve a high resolution by efficiently designing a gate driver providing gate signals applied to subpixels and a circuit providing a reference voltage.

[0012] Another aspect of the present disclosure is to provide an electroluminescence display is to provide a driving method of an electroluminescence display that includes the step of providing a reference voltage according to a method of driving subpixels so as to eliminate or minimize the effect of voltage drops on a drive current applied to organic light-emitting elements.

[0013] Technical problems to be solved or addressed by the present disclosure are not limited to the above-mentioned technical problems, and other technical problems not mentioned herein may be clearly understood by those skilled in the art from description below.

[0014] The objectives are solved by the features of the independent claims. Advantageous embodiments are derived from the respective dependent claims.

[0015] According to an aspect of the present disclosure, there is provided an electroluminescence display device comprising a display panel having a display area where images are displayed and a non-display area where images are not displayed, a subpixel located in the display area, and a voltage transfer part that is located in the non-display area and transfers a reference voltage to a voltage transfer node of the subpixel in response to a signal applied from

outside the display panel or a signal generated on the display panel.

[0016] According to an aspect of the present disclosure, there is provided an electroluminescence display device comprising a display panel having a display area where images are displayed and a non-display area where images are not displayed, a subpixel located in the display area, and a voltage transfer part that is located in the non-display area and transfers a reference voltage to the subpixel. The method comprising an initial step for initializing the subpixel, and a sampling step for compensating for the threshold voltage of a driving transistor of the subpixel. Wherein, during the sampling step, the voltage transfer part operates in response to a signal applied from outside the display panel or a signal generated on the display panel.

[0017] According to an aspect of the present disclosure, there is provided an electroluminescence display device comprising a display panel having a display area where images are displayed and a non-display area where images are not displayed, a subpixel located in the display area, a gate driver located in the non-display area, and a voltage transfer transistor that is located in the non-display area and transfers a reference voltage to the subpixel. And a gate of the voltage transfer transistor is connected to the gate driver.

[0018] According to an aspect of the present disclosure, there is provided a driving method of an electroluminescence display device comprising a display panel having a display area and a non-display area, a subpixel located in the display area and comprising an organic light-emitting diode, and a voltage transfer part located in the non-display area. The method comprising a first initial step for initializing a gate of a driving transistor included in the subpixel, a sampling and second initial step for compensating for the threshold voltage of the driving transistor and initializing an anode of the organic light-emitting diode. Wherein, during the first initial step and the sampling and second initial step, the voltage transfer part provides a reference voltage to the subpixel.

[0019] Other detailed matters of the embodiments are included in the detailed description and the drawings.

[0020] According to the present disclosure, a circuit for transferring a reference voltage to subpixels may be included in a non-display area, and this can simplify the pixel circuits and therefore offers advantages for high integration, thereby preventing a decrease in aperture ratio when making a large-screen or high-resolution display panel.

[0021] According to the present disclosure, a circuit for transferring a reference voltage to subpixels may be included in the gate driver, and this can improve the efficiency of the gate driver.

[0022] According to the present disclosure, a drive circuit for compensating for time-varying characteristics (or variation with time) may be implemented, with drops in power-supply voltage taken into consideration, and this can solve picture quality problems such as vertical luminance non-uniformity or crosstalk on the display panel.

[0023] The objects to be achieved by the present disclosure, the aspects, and the effects of the present disclosure described above do not specify essential features of the claims, and, thus, the scope of the claims is not limited to the disclosure of the present disclosure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] The accompany drawings, which are included to provide a further understanding of the disclosure and are incorporated on and constitute a part of this specification illustrate embodiments of the disclosure and together with the description serve to explain the principles of the disclosure.

FIG. 1 is a schematic block diagram of an electroluminescence display according to an embodiment of the present disclosure;

FIG. 2 is a schematic block diagram of a subpixel illustrated in FIG. 1;

FIG. 3 is an illustration of the configuration of a gate driver illustrated in FIG. 1;

FIG. 4 is a circuit diagram of a subpixel which explains an electroluminescence display according to a test example;

FIG. 5 is a waveform diagram explaining some of the drive characteristics of the subpixel circuit of FIG. 4;

FIG. 6 is a block diagram of a display panel which schematically illustrates an electroluminescence display according to an embodiment of the present disclosure;

FIG. 7 is a waveform diagram explaining the drive characteristics of the subpixel of FIG. 6.

FIG. 8 is a view showing in more detail the configuration of an Nth voltage transfer part according to the first embodiment of the present disclosure;

FIGs. 9 to 16 are views explaining in more detail the driving method according to the configuration of FIG. 8;

FIG. 17 is a diagram of the configuration of a display panel which schematically explains an electroluminescence display according to a second embodiment of the present disclosure;

FIG. 18 is a waveform diagram explaining some of the drive characteristics of the subpixel circuit of FIG. 17;

FIG. 19 is a diagram of the configuration of a display panel which schematically explains an electroluminescence display according to a third embodiment of the present disclosure;

FIG. 20 is a waveform diagram explaining some of the drive characteristics of the subpixel circuit of FIG. 19;

FIG. 21 is a circuit diagram showing the configuration of a voltage transfer part and a gate driver according to a first

modification of one of the first to third embodiments of the present disclosure;
FIG. 22 is a circuit diagram showing a voltage transfer part and a subpixel according to a fourth embodiment of the present disclosure;
FIG. 23A is a view showing an operation during a first initial period of FIG. 22;
FIG. 23B is a waveform diagram showing the operation of FIG. 23A;
FIG. 24A is a view showing an operation during a sampling and second initial period of FIG. 22;
FIG. 24B is a waveform diagram showing the operation of FIG. 24A;
FIG. 25A is a view showing an operation during a holding period of FIG. 22;
FIG. 25B is a waveform diagram showing the operation of FIG. 25A;
FIG. 26A is a view showing an operation during an emission period of FIG. 22;
FIG. 26B is a waveform diagram showing the operation of FIG. 26A;
FIG. 27 is a circuit diagram showing the configuration of a voltage transfer part and a gate driver according to a second modification of one of the first to fourth embodiments of the present disclosure;
FIG. 28 is a circuit diagram showing a voltage transfer part and a subpixel according to a fifth embodiment of the present disclosure; and
FIG. 29 is a waveform diagram showing an operation of FIG. 28.

DESCRIPTION OF EMBODIMENTS

[0025] Reference will now be made in detail embodiments of the disclosure of which are illustrated in the accompanying drawings.

[0026] Hereinafter, the embodiments of the present disclosure will be described with the attached drawings.

[0027] An electroluminescence display to be described below in this specification may be implemented as a television, a video player, a personal computer (PC), a home theater system, a smartphone, a virtual reality device (VR), and so on. The electroluminescence display below will be described by taking an organic electroluminescence display based on organic light-emitting diodes (light-emitting elements) as an example. Also, the electroluminescence display to be described in this specification may be implemented based on inorganic light-emitting diodes.

[0028] Moreover, the electroluminescence display to be described below in this specification may be implemented based on either a p-type transistor or n-type transistor or both of them. Source and drain are interchangeable between the p-type and n-type transistors, but a gate is not interchangeable. Hence, the source and drain may be termed first and second electrodes so as not to limit them to specific positions. Also, in the present specification, pixel circuits and a gate driver formed on a substrate of a display panel may be implemented as n-type or p-type transistors. For example, the transistors may be implemented as MOSFET (metal oxide semiconductor field effect transistor) transistors. A transistor is a three-electrode device with gate, source, and drain. The source is an electrode that provides carriers to the transistor. The carriers in the transistor flow from the source. The drain is an electrode where the carriers leave the transistor. That is, carriers in a transistor flow from the source to the drain. In the case of an n-type transistor, the carriers are electrons, and thus the source voltage is lower than the drain voltage so that the electrons flow from the source to the drain. In the n-type transistor, since the electrons flow from the source to the drain, current flows from the drain to the source. In the case of a p-type transistor, the carriers are holes, and thus the source voltage is higher than the drain voltage so that the holes flow from the source to the drain. In the p-type transistor, since the holes flow from the source to the drain, current flows from the source to the drain. It should be noted that the source and drain of a transistor are not fixed in position, but the source and drain of the transistor are interchangeable depending on the applied voltage.

[0029] As used herein, "gate-on voltage" may refer to the voltage of a gate signal at which a transistor can be turned on, and "gate-off voltage" may refer to the voltage of a gate signal at which a transistor may be turned off. In a p-type transistor, the gate-on voltage may be a gate-low voltage (or logic-low voltage VL), and the gate-off voltage may be a gate-high voltage (or logic-high voltage VH). In an n-type transistor, the gate-on voltage may be a gate-high voltage, and the gate-off voltage may be a gate-low voltage.

<First Embodiment>

[0030] FIG. 1 is a schematic block diagram of an electroluminescence display according to an embodiment of the present disclosure. FIG. 2 is a schematic block diagram of a subpixel illustrated in FIG. 1. FIG. 3 is an illustration of the configuration of a gate driver illustrated in FIG. 1. All the components of the electroluminescence display (or display device) according to all embodiments of the present disclosure are operatively coupled and configured.

[0031] As illustrated in FIG. 1, the electroluminescence display comprises an image processor 110, a timing controller 120, a data driver 140, a scan driver 130, a display panel 150, and a power supply part 180.

[0032] The image processor 110 outputs drive signals for driving various kinds of devices, along with externally supplied image data. The drive signals outputted from the image processor 110 may comprise a data enable signal, a vertical

synchronization signal, a horizontal synchronization signal, and a clock signal.

[0033] The timing controller 120 receives drive signals, etc., along with image data, from the image processor 110. The timing controller 120 outputs a gate timing control signal GDC for controlling the operation timing of the gate driver 130 and a data timing control signal DDC for controlling the operation timing of the data driver 140, based on the drive signals.

[0034] The data driver 140 outputs data voltages in response to a data timing control signal DDC supplied from the timing controller 120. The data driver 140 samples and latches a digital data signal DATA supplied from the timing controller 120 and converts it into an analog data voltage based on a gamma reference voltage. The data driver 140 outputs data voltages DATA through data lines DL1 to DLm where m is positive integer. The data driver 140 may be provided in the form of an IC (integrated circuit).

[0035] The gate driver 130 outputs gate signals in response to a gate timing control signal GDC supplied from the timing controller 120. The gate driver 130 outputs gate signals through gate lines GL1 to GLn where n is a positive integer. The gate driver 130 may be provided in the form of an IC (integrated circuit). The gate driver 130 may be divided into a first gate driver and a second gate driver arranged at opposite sides of the display area AA.

[0036] The power supply part 180 outputs a first power supply voltage and a low-level voltage. The first power supply voltage and low-level voltage outputted from the power supply part 180 are supplied to the display panel 150. The first power supply voltage is supplied to the display panel 150 via a first power line EVDD, and the low-level voltage is supplied to the display panel 150 via a second power line EVSS. The voltages outputted from the power supply part 180 may be used by the data driver 140 or the gate driver 130.

[0037] The display panel 150 displays an image in response to data voltages and gate signals respectively supplied from the data driver 140 and gate driver 130 and power supplied from the power supply part 180. The display panel 150 comprises a plurality of subpixels SPs that work to display an image. The subpixels SPs can be arranged in a matrix configuration.

[0038] The subpixels SPs may comprise red subpixels, green subpixels, and blue subpixels, or may comprise white subpixels, red subpixels, green subpixels, and blue subpixels. The subpixels SPs may have one or more different light-emission areas depending on the light-emission characteristics.

[0039] FIG. 2 is a block diagram of each subpixel SP of FIG. 1 and a signal inputted into the subpixel SP. Referring to FIG. 2, a single subpixel SP is connected to a gate line GL, a data line DL, a first power line EVDD, a second power line EVSS, an initial line VINI, and a reference voltage line VREF. The numbers of transistors and capacitors in the subpixel SP and the driving method thereof are determined by the configuration of the pixel. In this case, the gate line GL may comprise a plurality of gate lines that transfer gate signals. Accordingly, the gate driver may provide a single pixel circuit with one or more gate signals.

[0040] As illustrated in FIG. 3, the display panel 150 comprises a display area AA that displays an image based on subpixels SPs and a non-display area NA where signal lines or drive circuits are situated, that displays no image.

[0041] The gate driver 130 is provided in the form of a gate-in-panel in the non-display area NA of the display panel 150. The gate driver 130 may be placed on either one or both of the left and right sides of the display panel 150. The left side and the right side of the display panel 150 may be defined according to a horizontal alignment of the display panel 150. The left side is arranged opposite to the right side. The left side is a first side of the display panel 150 and the right side is a second side of the display panel 150 being arranged opposite to the first side. The gate driver 130 may include a plurality of stages. For example, the first stage of the gate driver 130 outputs a first gate signal (or a first scan signal) for driving a first gate line (or a first scan line) on the display panel 150.

[0042] Meanwhile, the electroluminescence display device has many advantages, including being spotlighted as a next-generation display device, because it displays an image based on light generated by the organic light-emitting diodes in the subpixels. However, the electroluminescence display has time-varying characteristics (variation with time), such as the threshold voltage of the elements (e.g., driving transistors, etc.) included in the subpixels, which need to be compensated for.

[0043] Consequently, various compensation methods for compensating for time-varying characteristics of the electroluminescence display have been suggested. However, some of these compensation methods do not take voltage drops into consideration and therefore have picture quality issues such as vertical luminance non-uniformity or crosstalk, thus bringing about the need for improvement.

[0044] Hereinafter, problems with a test example that bring about picture quality issues, such as vertical luminance non-uniformity or crosstalk on the display panel of the electroluminescence display, will be discussed, and an embodiment of the present specification for solving/addressing these problems will be described. For convenience of explanation, the following description will be given with an example in which all of the transistors included a subpixel are P-type transistors, but the embodiment of the present disclosure is also applicable to N-type transistors.

<Test Example>

[0045] FIG. 4 is a circuit diagram of a subpixel which explains an electroluminescence display according to a test example. FIG. 5 is a waveform diagram explaining some of the drive characteristics of the subpixel circuit of FIG. 4.

[0046] As illustrated in FIGs. 4 and 5, an nth subpixel according to the test example is a subpixel connected to an nth scan line and an mth data line, and the nth subpixel comprises first to sixth transistors T1 to T6, a driving transistor DT, a capacitor Cst, and an organic light-emitting diode OLED. Such a configuration of a subpixel circuit is referred to as 7T1C subpixel circuit.

[0047] The first to sixth transistors T1 to T6 and the driving transistor DT are configured as P-type transistors. The third transistor T3 and the fourth transistor T4 may be provided in the form of dual transistors (i.e., two transistors are connected in series, with gates connected together to form a pair). The third transistor T3 and the fourth transistor T4 may be single transistors.

[0048] For an nth subpixel according to a test example, internal circuit-based compensation is done as a first initial period INI and a sampling and second initial period SAM occur while an nth emission control signal Em[n] is not applied (the logic-high voltage is maintained). The operating characteristics during these periods will be described below in brief. The subpixels are arranged as a matrix and may be scanned row-by row.

[0049] During the first initial period INI, the fourth transistor T4 is turned on in response to the logic-low voltage of an (n-1)th scan signal Scan[n-1] applied via an (n-1)th scan line SCAN[n-1]. In this case, the initial voltage Vini, lower than the first power supply voltage applied via the first power supply line EVDD, is applied to the initial line VINI. By this operation, a gate node DTG of the driving transistor DT is initialized based on the initial voltage Vini.

[0050] During the sampling and second initial period SAM, the first transistor T1, third transistor T3, and sixth transistor T6 are turned on in response to the logic-low voltage VL of an nth scan signal Scan[n] applied via an nth scan line SCAN[n]. The nth scan line SCAN[n] is a scan line that transfers the nth scan signal Scan[n] for driving nth subpixels located in the nth scan line SCAN[n].An (n-1)th scan line SCAN[n-1] is a scan line that transfers the (n-1)th scan signal Scan[n-1] for driving (n-1)th subpixels located in the row before the nth scan line SCAN[n].

[0051] A data voltage applied via the mth data line DLm is applied to a first electrode of the driving transistor DT by the turn-on of the first transistor T1. The driving transistor DT is diode-connected by the turn-on of the third transistor T3. The threshold voltage of the driving transistor DT is sampled by the turn-on of the third transistor T3. The data voltage applied to the first electrode of the driving transistor DT is stored in the gate node DTG via the third transistor T3. The organic light-emitting diode OLED is initialized based on the initial voltage Vini by the turn-on of the sixth transistor T6.

[0052] The concept of compensation in a subpixel according to the test example may be represented by the following current equation:

$$Ioled = K(Vsg - |Vth|)^2 = K\{(VDD-(Vdata-|Vth|) - |Vth|\}^2 = K(VDD-Vdata)^2$$

wherein Ioled is the current flowing through the organic light-emitting diode OLED, K is a constant, Vsg is the voltage between the source and gate of the driving transistor DT, Vth is the threshold voltage of the driving transistor DT, VDD is the first power supply voltage applied via the first power supply line EVDD, and Vdata is a data voltage applied via the mth data line DLm.

[0053] However, the subpixel SP according to the test example has defect issues caused by voltage drop (IR drop) in the first power supply voltage since the first power supply voltage applied via the first power supply line EVDD is not taken into consideration. Voltage drops in the first power supply voltage bring about picture quality issues such as vertical luminance uniformity or crosstalk on the display panel, so improvements can be made in the following embodiments.

<First Embodiment>

[0054] FIG. 6 is a block diagram of a display panel which schematically illustrates an electroluminescence display according to an embodiment of the present disclosure. FIG. 7 is a waveform diagram explaining some of the drive characteristics of the subpixel of FIG. 6.

[0055] As illustrated in FIGs. 6 and 7, the electroluminescence display according to the first embodiment comprise an nth voltage transfer part VRD that performs an operation for transferring an externally applied voltage to subpixels so as to compensate for voltage drop in the first power supply voltage applied to the nth subpixels SPs. Here, the term "externally" refers to the outside of the display area AA. The term voltage transfer part VRD is used interchangeable with the term voltage transfer transistor hereinafter, unless otherwise stated. The voltage transfer part VRD may represent at least one voltage transfer transistor that is located in the non-display area NA, wherein a gate of the at least one voltage transfer transistor is connected to the gate driver 130 and wherein the voltage transfer transistor is configured to transfer a reference voltage to a voltage transfer node of the subpixel SP in response to a signal applied from outside

the display panel 150 or a signal generated on the display panel 150.

[0056] The nth voltage transfer part VRD is placed in the non-display area NA. For example, the nth voltage transfer part VRD may be placed between the gate driver 130 disposed in the non-display area NA of the display panel and the subpixels SPs disposed in the display area AA.

[0057] The gate driver 130 comprises an nth stage STG[n] that drives the nth subpixels SPs disposed in the nth scan line SCAN[n]. The nth stage STG[n] outputs the nth emission control signal Em[n] and nth scan signal Scan[n] for driving the nth subpixels. The nth voltage transfer part VRD may be placed to correspond to every scan line as well as the nth scan line SCAN[n]. A plurality of nth voltage transfer parts VRD may be provided. Also, the subpixels SPs may be highly integrated by placing the nth voltage transfer part VRD in the non-display area NA, rather than by placing the nth voltage transfer part VRD in each of the subpixels SPs disposed in the display area AA, and this allows for a high-resolution display panel.

[0058] The nth voltage transfer part VRD acts to transfer a reference voltage applied via a reference voltage line VREF to voltage transfer nodes VDN of the nth subpixels SPs during a specific period. The reference voltage may have a voltage level between the first power supply line EVDD and the second power supply line EVSS or a level equivalent to the first power supply voltage applied via the first power supply line EVDD.

[0059] The nth voltage transfer part VRD comprises at least one voltage transfer transistor VT. The at least one voltage transfer transistor VT is turned on or off in response to an externally applied control signal or a scan signal outputted from the gate driver 130. The externally applied control signal may refer to, but not limited to, a control signal outputted from the timing controller or power supply part, for example.

[0060] In the first embodiment, by way of example, the nth voltage transfer part VRD is placed separately and independently from the gate driver 130. However, the nth voltage transfer part VRD may be included in the gate driver 130. However, the nth voltage transfer part VRD may be included in one of the divided gate drivers according to FIG.3, arranged at the first side or the second side of the display panel 150.

[0061] Placing the nth voltage transfer part VRD in the non-display area NA as in the first embodiment may offer advantages in terms of process over placing circuits for reference voltage application in the nth subpixels SPs. The advantages in terms of process are as follows. First, voltage can be transferred without placing circuits required for voltage transfer within the subpixels SPs, and the number of electrodes in each subpixel SP or the number of contacts on a wire can be reduced by placing the voltage transfer circuits outside the subpixels. This heavily reduces parasitic effects that may occur when arranging it in the subpixel SP. Second, the space limitations of the subpixels can be avoided, which is advantageous in high integration and prevents a decrease in aperture ratio when making a large-screen or high-resolution display panel.

[0062] An nth subpixel SP according to the first embodiment comprises first to seventh transistors T1 to T7, a driving transistor DT, a capacitor Cst, and an organic light-emitting diode OLED. The nth subpixel SP according to the first embodiment will be illustrated and described with an example in which it is implemented based on a total of 8 transistors, but the embodiment of the present specification is not limited to this example. The configuration and connections of the nth subpixel SP according to the first embodiment of the present disclosure will be described below. Such a configuration may be considered as a 8T1C subpixel circuit.

[0063] The first transistor T1 has a gate connected to the nth scan line SCAN[n], a first electrode connected to the mth data line DLm, and a second electrode connected to a first electrode of the second transistor T2 and a first electrode of the driving transistor DT. The first transistor T1 is turned on in response to the logic-low voltage VL of the Nth scan signal Scan[n] applied via the nth scan line SCAN[n]. When the first transistor T1 is turned on, a data voltage applied via the mth data line DLm is stored in the second electrode of the first transistor T1 (or between the first transistor and the second transistor).

[0064] The second transistor T2 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the second electrode of the first transistor T1, and a second electrode connected to the first power supply line EVDD and a first electrode of the seventh transistor T7. The second transistor T2 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the second transistor T2 is turned on, a data voltage stored in the second electrode of the first transistor T1 is transferred to one electrode of the capacitor Cst through the second transistor T2 and the seventh transistor T7.

[0065] The third transistor T3 has a gate connected to the nth scan line SCAN[n], a first electrode connected to a second electrode of the driving transistor DT, and a second electrode connected to a gate electrode of the driving transistor DT. The third transistor T3 is turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. When the third transistor T3 is turned on, the driving transistor DT is diode-connected.

[0066] The fourth transistor T4 has a gate connected to the (n-1)th scan line SCAN[n-1], a first electrode connected to an initial line VINI, and a second electrode connected to the other electrode of the capacitor Cst, the second electrode of the third transistor T3, and the gate of the driving transistor DT. The fourth transistor T4 is turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. When the fourth

transistor T4 is turned on, the gate node DTG of the driving transistor DT is initialized based on the initial voltage Vini.

[0067] The fifth transistor T5 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the second electrode of the driving transistor DT, and a second electrode connected to the anode of the organic light-emitting diode OLED. The fifth transistor T5 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the fifth transistor T5 is turned on, the organic light-emitting diode OLED emits light in response to a drive current generated through the driving transistor DT.

[0068] The sixth transistor T6 has a gate connected to the nth scan line SCAN[n], a first electrode connected to the initial line VINI, and a second electrode connected to the second electrode of the driving transistor DT and the anode of the organic light-emitting diode OLED. The sixth transistor T6 is turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. When the sixth transistor T6 is turned on, the anode of the organic light-emitting diode OLED is initialized based on the initial voltage Vini.

[0069] The seventh transistor T7 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the first power supply line EVDD and the second electrode of the second transistor T2, and a second electrode connected to one electrode of the capacitor Cst. The seventh transistor T7 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the seventh transistor T7 is turned on, a data voltage stored in the second electrode of the first transistor T1 is transferred to the one electrode of the capacitor Cst through the second transistor T2.

[0070] One electrode of the capacitor Cst is connected to the second electrode of the seventh transistor T7, and the other electrode is connected to the second electrode of the fourth transistor T4. A node connected to the second electrode of the seventh transistor T7 and the one electrode of the capacitor Cst is defined as a voltage transfer node VDN which transfers the reference voltage. The anode of the organic light-emitting diode OLED is connected to the second electrode of the fifth transistor T5, and the cathode thereof is connected to the second power supply line EVSS.

[0071] The nth subpixel SP according to the first embodiment operates in a sequence of a first initial period INI, a sampling and second initial period SAM, a holding period HLD, and an emission period EMI. The first initial period INI is a period in which the gate node DTG of the driving transistor DT is initialized. The sampling and second initial period SAM is a period in which the threshold voltage of the driving transistor DT is sampled and the organic light-emitting diode OLED is initialized. The holding period HLD is a period in which a data voltage applied via the mth data line DLm is held in a particular node. The emission period EMI is a period in which the organic light-emitting diode OLED emits light by a drive current generated based on the data voltage.

[0072] For the Nth subpixel SP according to the first embodiment, internal circuit-based compensation is done as the first initial period INI and the sampling and second initial period SAM occur while the nth emission control signal Em[n] is not applied (the logic-high voltage is maintained). The operating characteristics during these periods will be described below in brief. By way of example, the low-logic voltage is applied in response to the (n-1)th scan signal Scan[n-1] and the Nth scan signal Scan[n] during 1 horizontal time 1H. Also, by way of example, the first initial period INI and the sampling and second initial period SAM each occur during 1 horizontal time 1H.

[0073] During the first initial period INI, the fourth transistor T4 is turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. In this case, the initial voltage Vini, lower than the first power supply voltage applied via the first power supply line EVDD, is applied to the initial line VINI. By this operation, the gate node DTG of the driving transistor DT is initial based on the initial voltage Vini.

[0074] During the sampling and second initial period SAM, the first transistor T1, third transistor T3, and sixth transistor T6 are turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. A data voltage applied via the mth data line DLm is applied to the first electrode of the driving transistor DT by the turn-on of the first transistor T1. By the turn-on of the third transistor T3, the driving transistor DT is diode-connected, and the threshold voltage of the driving transistor DT is sampled. The data voltage applied to the first electrode of the driving transistor DT is stored in the gate node DTG. The organic light-emitting diode OLED is initial based on the initial voltage Vini by the turn-on of the sixth transistor T6.

[0075] During the emission period EMI, the second transistor T2, seventh transistor T7, and fifth transistor T5 are turned on in response to the logic-low voltage VL of the emission control signal Em[n] applied via the nth emission control signal line EM[n]. The first power supply voltage applied via the first power supply line EVDD is applied to the first electrode of the driving transistor DT by the turn-on of the second transistor T2. The first power supply voltage applied via the first power supply line EVDD is applied to the voltage transfer node VDN, which is one electrode of the capacitor Cst, by the turn-on of the seventh transistor T7. In this case, the voltage of the gate node DTG of the driving transistor DT, which is the other electrode of the capacitor Cst, is varied due to coupling by the amount of change from the reference voltage Vref to the first power supply voltage.

[0076] The nth subpixel SP according to the first embodiment is supplied with the reference voltage from the nth voltage transfer part VRD during the first initial period INI and the sampling and second initial period SAM so that voltage drops in the first power supply voltage are taken into consideration. The resulting current in the nth subpixel SP may be

represented by the following current equation:

$$Ioled = K(Vsg - |Vth|)^2 = K\{(VDD-(Vdata-|Vth|+VDD-Vref) - |Vth|\}^2 = K(Vref-Vdata)^2$$

wherein Ioled is the current flowing through the organic light-emitting diode OLED, K is a constant, Vsg is the voltage between the source and the gate of the driving transistor DT, Vth is the threshold voltage of the driving transistor DT, VDD is the first power supply voltage applied via the first power supply line EVDD, Vref is the reference voltage applied via the reference voltage line VREF, and Vdata is a data voltage applied via the mth data line DLm.

[0077] As can be seen from the above equation, Ioled is determined by the difference between the reference voltage and the data voltage. From the equation, it can be seen that, for the nth subpixel SP according to the first embodiment, voltage drops in the first power supply voltage applied via the first power supply line EVDD are compensated for by the reference voltage applied during the first initial period INI and the sampling and second initial period SAM.

[0078] Hereinafter, a more detailed description of the first embodiment will be given below with an example in which the nth voltage transfer part VRD includes two voltage transfer transistors.

[0079] FIG. 8 is a view showing in more detail the configuration of an nth voltage transfer part according to the first embodiment of the present disclosure. FIGs. 9 to 16 are views explaining in more detail the driving method according to the configuration of FIG. 8.

[0080] As illustrated in FIG. 8, the nth voltage transfer part VT comprises a first voltage transfer transistor VTa and a second voltage transfer transistor Vtb. The first voltage transfer transistor VTa is turned on or off in response to the (n-1)th scan signal applied via the (n-1)th scan line SCAN[n-1]. The second voltage transfer transistor Vtb is turned on or off in response to the nth scan signal applied through the nth scan line SCAN[n].

[0081] The first voltage transfer transistor VTa has a gate connected to the (n-1)th scan line SCAN[n-1], a first electrode connected to the reference voltage line VREF, and a second electrode connected to the second electrode of the seventh transistor T7 and the voltage transfer node VDN, which is one electrode of the capacitor Cst. The second voltage transfer transistor VTb has a gate connected to the nth scan line SCAN[n], a first electrode connected to the reference voltage line VREF, and a second electrode connected to the second electrode of the seventh transistor T7 and the voltage transfer node VDN, which is one electrode of the capacitor Cst. That is, the gates of the first voltage transfer transistor VTa and the second voltage transfer transistor VTb are connected to different scan lines, and the first electrodes thereof are connected to each other and the second electrodes thereof are connected to each other.

[0082] Hereinafter, the driving method according to the first embodiment will be described below in conjunction with the nth voltage transfer part VT and the nth subpixel SP. In the description below, the transistors marked by a slash are turned-off transistors, and the other transistors are turned-on transistors.

[0083] FIGs. 9 and 10 are views showing an operation during a first initial period and the resulting drive waveforms according to the configuration of FIG. 8.

[0084] As illustrated in FIGs. 9 and 10, during the first initial period INI, the first voltage transfer transistor VTa is turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. In this case, the reference voltage transferred via the reference voltage line VREF is applied to the nth subpixels via the turned-on first voltage transfer transistor VTa. By this operation, the reference voltage is stored at one electrode of the capacitor Cst.

[0085] Moreover, during the first initial period INI, the fourth transistor T4 is turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. In this case, the initial voltage, lower than the first power supply voltage applied via the first power supply line EVDD, is applied to the initial line VINI. By this operation, the gate node DTG of the driving transistor DT is initialized based on the initial voltage Vini (or residual voltage is released).

[0086] FIGs. 11 and 12 are views showing an operation during a sampling and second initial period and the resulting drive waveforms according to the configuration of FIG. 8.

[0087] As illustrated in FIGs. 11 and 12, during the sampling and second initial period SAM, the second voltage transfer transistor VTb is turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. In this case, the reference voltage transferred via the reference voltage line VREF is applied to the nth subpixels via the turned-on second voltage transfer transistor VTb. By this operation, the reference voltage is continuously stored at one electrode of the capacitor Cst.

[0088] Moreover, during the sampling and second initial period SAM, the first transistor T1, third transistor T3, and sixth transistor T6 are turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. A data voltage applied via the mth data line DLm is applied to the first electrode of the driving transistor DT by the turn-on of the first transistor T1. The driving transistor DT is diode-connected by the turn-on of the third transistor T3. The threshold voltage of the driving transistor DT is sampled by the turn-on of the third transistor T3.

The data voltage applied to the first electrode of the driving transistor DT is stored in the gate node DTG via the third transistor T3. The organic light-emitting diode OLED is initialized based on the initial voltage Vini by the turn-on of the sixth transistor T6.

[0089] FIGs. 13 and 14 are views showing an operation during a holding period and the resulting drive waveforms according to the configuration of FIG. 8.

[0090] As illustrated in FIGs. 13 and 14, during the holding period HLD, the first voltage transfer transistor VTa is turned off in response to the logic-high voltage VH of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. The second voltage transfer transistor VTb is turned off in response to the logic-high voltage VH of the nth scan signal Scan[n] applied via the nth scan line SCAN[n].

[0091] Moreover, during the holding period HLD, the first to seventh transistors T1 to T7 are turned off in response to the logic-high voltage VH of the (n-1)th scan signal Scan[n-1], nth scan signal Scan[n], and nth emission control signal Em[n]. By this operation, the capacitor Cst stores and holds a data voltage based on the voltage difference between the two ends.

[0092] FIGs. 15 and 16 are views showing an operation during an emission period and the resulting drive waveforms according to the configuration of FIG. 8.

[0093] As illustrated in FIGs. 15 and 16, during the emission period EMI, the first voltage transfer transistor VTa and the second voltage transfer transistor VTb are kept turned off, as is during the holding period HLD.

[0094] Moreover, during the emission period EMI, the second transistor T2, fifth transistor T5, and seventh transistor T7 are turned on in response to the logic-low voltage VL of the nth emission control signal Em[n]. By the turn-on of the second transistor T2, fifth transistor T5, and seventh transistor T7, the driving transistor DT are turned on while generating a drive current based on a data voltage obtained by threshold voltage compensation.

[0095] The variations in the voltage of the voltage transfer node, the voltages of the gate node, source node, and drain node of the driving transistor, the threshold voltage Vth of the driving transistor, and the drive current Ioled flowing through the organic light-emitting diode, during the time from the first initial period INI to the emission period EMI, are shown in the following table. In Table 1 below, the first power supply voltage is denoted by VDD, and the reference voltage is denoted by Vref.

[0096] [Table 1]

	First initial period (INI)	Sampling and second initial period (SAM)	Holding period (HLD)	Emission period (EMI)
Voltage transfer node	Vref	Vref	Vref	VDD
Gate node of driving transistor	Vini	Vdata-|Vth|	Same as before	Vdata-|Vth|+ (VDD-Vref)
Source node of driving transistor	-	Vdata	Same as before	VDD
Drain node of driving transistor	-	Vdata-|Vth|	Same as before	-
Drive current	Ioled = $K(Vsg - \|Vth\|)^2 = K\{ VDD-(Vdata-\|Vth\|+VDD-Vref)-\|Vth\|)\}^2 = K(Vref-Vdata)^2$			

[0097] As can be seen from the above description, the first embodiment can prevent or solve picture quality issues such as vertical luminance non-uniformity or crosstalk on the display panel since defect issues caused by voltage drop in the first power supply voltage can be prevented or solved. Moreover, the first embodiment can reduce the number of electrodes in each subpixel or the number of contacts on a wire by placing circuits for transferring reference voltage to the subpixels, and also can offer advantages in high integration and therefore prevents a decrease in aperture ratio when making a large-screen or high-resolution display panel.

<Second Embodiment>

[0098] FIG. 17 is a diagram of the configuration of a display panel which schematically explains an electroluminescence display according to a second embodiment of the present disclosure. FIG. 18 is a waveform diagram explaining some of the drive characteristics of the subpixel circuit of FIG. 17. The second embodiment of the present disclosure is a modification of the first embodiment, so redundancies between the first and second embodiments will be omitted or described briefly.

[0099] As illustrated in FIGs. 17 and 18, the electroluminescence display according to the second embodiment comprise an Nth voltage transfer part VRD that performs an operation for transferring an externally applied voltage to subpixels

so as to compensate for voltage drop in the first power supply voltage applied to the nth subpixels SPs. Here, the term "externally" refers to the outside of the display area AA.

[0100] The nth voltage transfer part VRD is placed in the non-display area NA. The nth voltage transfer part VRD acts to transfer a reference voltage applied via a reference voltage line VREF to voltage transfer nodes VDN of the nth subpixels SPs during a specific period. The nth voltage transfer part VRD comprises one voltage transfer transistor VT.

[0101] The voltage transfer transistor VT has a gate connected to the nth scan line SCAN[n], a first electrode connected to the reference voltage line VREF, and a second electrode connected to the second electrode of the seventh transistor T7 and one electrode of the capacitor Cst. The voltage transfer transistor VT is turned on or off in response to the nth scan signal Scan[n] applied via the nth scan line SCAN[n].

[0102] In the second embodiment, enough time will be given for the first initial period INI and the sampling and second initial period SAM by configuring signals in such a way that the logic-low voltage part of at least 1 horizontal time 1H overlaps between the previous scan signal and the current scan signal. Therefore, the nth voltage transfer part VRD may comprise a single voltage transfer transistor VT by configuring the (n-1)th scan line SCAN[n-1] and the nth scan line SCAN[n] in such a way that their logic-low voltage parts overlap.

[0103] In the second embodiment, the nth voltage transfer part VRD can be kept turned on for at least 2 horizontal times, without changing from the turned-off state to the turned-on state for a specific period of time, since the previous scan signal and the current scan signal overlap when applied. Thus, power supply can be prevented from being cut off when the reference voltage is transferred, or the nodes can be prevented from electrically floating. Moreover, in the second embodiment, the nth voltage transfer part VRD comprises a single voltage transfer transistor VT, thereby simplifying the circuits enough to further reduce the non-display area (or bezel area) of the display panel.

[0104] As opposed to scan signals for 1 horizontal time, scan signals for 2 horizontal times may have a compensation period only when the pulses overlap. Thus, applying the reference voltage to the subpixels during the initial period INI may be necessary depending on whether the scan signals overlap or not. By applying the reference voltage from the initial period INI onward, power supply can be prevented from being cut off when the reference voltage is transferred, or the nodes can be prevented from electrically floating.

[0105] An nth subpixel SP according to the second embodiment comprises first to seventh transistors T1 to T7, a driving transistor DT, a capacitor Cst, and an organic light-emitting diode OLED. In the nth subpixel SP according to the second embodiment, the driving transistor DT and the organic light-emitting diode OLED are simultaneously initial, unlike the first embodiment. The configuration and connections of the nth subpixel SP according to the second embodiment of the present disclosure will be described below.

[0106] The first transistor T1 has a gate connected to the nth scan line SCAN[n], a first electrode connected to the mth data line DLm, and a second electrode connected to a first electrode of the second transistor T2 and a first electrode of the driving transistor DT. The first transistor T1 is turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. When the first transistor T1 is turned on, a data voltage applied via the mth data line DLm is stored in the second electrode of the first transistor T1.

[0107] The second transistor T2 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the second electrode of the first transistor T1, and a second electrode connected to the first power supply line EVDD and a first electrode of the seventh transistor T7. The second transistor T2 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the second transistor T2 is turned on, a data voltage stored in the second electrode of the first transistor T1 is transferred to one electrode of the capacitor Cst through the seventh transistor T7.

[0108] The third transistor T3 has a gate connected to the nth scan line SCAN[n], a first electrode connected to a second electrode of the driving transistor DT, and a second electrode connected to a gate of the driving transistor DT. The third transistor T3 is turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. When the third transistor T3 is turned on, the driving transistor DT is diode-connected.

[0109] The fourth transistor T4 has a gate connected to the (n-1)th scan line SCAN[n-1], a first electrode connected to an initial line VINI, and a second electrode connected to the other electrode of the capacitor Cst, the second electrode of the third transistor T3, and the gate of the driving transistor DT. The fourth transistor T4 is turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. When the fourth transistor T4 is turned on, the gate node DTG of the driving transistor DT is initial based on the initial voltage Vini.

[0110] The fifth transistor T5 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the second electrode of the driving transistor DT, and a second electrode connected to the anode of the organic light-emitting diode OLED. The fifth transistor T5 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the fifth transistor T5 is turned on, the organic light-emitting diode OLED emits light in response to a drive current generated through the driving transistor DT.

[0111] The sixth transistor T6 has a gate connected to the (n-1)th scan line SCAN[n-1], a first electrode connected to the initial line VINI, and a second electrode connected to the second electrode of the driving transistor DT and the anode

of the organic light-emitting diode OLED. The sixth transistor T6 is turned on in response to the logic-low voltage of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. When the sixth transistor T6 is turned on, the anode of the organic light-emitting diode OLED is initialized based on the initial voltage Vini.

[0112] The seventh transistor T7 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the first power supply line EVDD and the second electrode of the second transistor T2, and a second electrode connected to one electrode of the capacitor Cst. The seventh transistor T7 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the seventh transistor T7 is turned on, a data voltage stored in the second electrode of the first transistor T1 is transferred to the one electrode of the capacitor Cst through the second transistor T2.

[0113] One electrode of the capacitor Cst is connected to the second electrode of the seventh transistor T7, and the other electrode is connected to the second electrode of the fourth transistor T4. The anode of the organic light-emitting diode OLED is connected to the second electrode of the fifth transistor T5, and the cathode thereof is connected to the second power supply line EVSS.

[0114] The Nth subpixel SP according to the second embodiment operates in a sequence of an initial period INI, a sampling period SAM, a holding period HLD, and an emission period EMI. The initial period INI is a period in which the gate node DTG of the driving transistor DT and the organic light-emitting diode OLED are simultaneously initialized. The sampling period SAM is a period in which the threshold voltage of the driving transistor DT is sampled. The holding period HLD is a period in which a data voltage applied via the mth data line DLm is held in a particular node. The emission period EMI is a period in which the organic light-emitting diode OLED emits light by a drive current generated based on the data voltage.

[0115] For the nth subpixel SP according to the second embodiment, internal circuit-based compensation is done as the initial period INI and the sampling period SAM occur while the nth emission control signal Em[n] is not applied (the logic-high voltage is maintained). The operating characteristics during these periods will be described below in brief. By way of example, the low-logic voltage is applied in response to the (n-1)th scan signal Scan[n-1] and the nth scan signal Scan[n] during 2 horizontal times 2H, and the two signals overlap during 1 horizontal time 1H.

[0116] During the first initial period INI, the fourth transistor T4 and the sixth transistor T6 are simultaneously turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. In this case, the initial voltage, lower than the first power supply voltage applied via the first power supply line EVDD, is applied to the initial line VINI. By this operation, the gate node DTG of the driving transistor DT and the organic light-emitting diode OLED are initialized based on the initial voltage.

[0117] During the sampling period SAM, the first transistor T1 and the third transistor T3 are turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the Nth scan line SCAN[n]. A data voltage applied via the mth data line DLm is transferred to the nth subpixel SP by the turn-on of the first transistor T1. By the turn-on of the third transistor T3, the driving transistor DT is diode-connected. By the turn-on of the third transistor T3, the threshold voltage of the driving transistor DT is sampled.

[0118] The nth subpixel SP according to the second embodiment is supplied with the reference voltage from the nth voltage transfer part VRD during the initial period INI and the sampling period SAM so that voltage drops in the first power supply voltage are taken into consideration. Accordingly, for the nth subpixel according to the second embodiment as well, voltage drops in the first power supply voltage applied via the first power supply line EVDD may be compensated for by the reference voltage.

[0119] Therefore, the second embodiment may offer the same benefit as the first embodiment since the nth voltage transfer part VRD is capable of applying the reference voltage during the initial period INI and the sampling period SAM. Moreover, in the second embodiment, power supply can be prevented from being cut off when the reference voltage is transferred, or the nodes can be prevented from electrically floating. In addition, in the second embodiment, the nth voltage transfer part VRD comprises a single voltage transfer transistor VT, thereby simplifying the circuits enough to further reduce the non-display area (or bezel area) of the display panel.

<Third Embodiment>

[0120] FIG. 19 is a diagram of the configuration of a display panel which schematically explains an electroluminescence display according to a third embodiment of the present disclosure. FIG. 20 is a waveform diagram explaining some of the drive characteristics of the subpixel circuit of FIG. 19. The third embodiment of the present disclosure is a modification of the first and/or second embodiments, so redundancies between the third embodiment and the first and second embodiments will be omitted or described briefly.

[0121] As illustrated in FIGs. 19 and 20, the electroluminescence display according to the third embodiment comprise an nth voltage transfer part VRD that performs an operation for transferring an externally applied voltage to subpixels so as to compensate for voltage drop in the first power supply voltage applied to the nth subpixels SPs. Here, the term "externally" refers to the outside of the display area AA.

[0122] The nth voltage transfer part VRD is placed in the non-display area NA. The nth voltage transfer part VRD acts to transfer a reference voltage applied via a reference voltage line VREF to voltage transfer nodes VDN of the nth subpixels SPs during a specific period. The nth voltage transfer part VRD comprises one voltage transfer transistor VT.

[0123] The voltage transfer transistor VT has a gate connected to the (n-2)th scan line SCAN[n-1], a first electrode connected to the reference voltage line VREF, and a second electrode connected to the second electrode of the seventh transistor T7 and the voltage transfer node VDN, which is one electrode of the capacitor Cst. The voltage transfer transistor VT is turned on or off in response to the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1].

[0124] In the third embodiment, enough time will be given for the first initial period INI and the sampling and second initial period SAM by configuring signals in such a way that the logic-low voltage part of at least 1 horizontal time 1H overlaps between the previous scan signal and the current scan signal. Therefore, the nth voltage transfer part VRD may comprise a single voltage transfer transistor VT by configuring the (n-1)th scan line SCAN[n-1] and the nth scan line SCAN[n] in such a way that their logic-low voltage parts overlap.

[0125] An nth subpixel SP comprises first to third transistors T1 to T3, fifth to seventh transistors T5 to T7, a driving transistor DT, a capacitor Cst, and an organic light-emitting diode OLED. The nth subpixel SP according to the third embodiment does not comprise the fourth transistor T4, as opposed to that of the second embodiment.

[0126] In the nth subpixel SP according to the third embodiment, unlike the first embodiment, the driving transistor DT is diode-connected and, at the same time, the organic light-emitting diode OLED is initialized. Specifically, in response to the (n-1)th scan signal Scan[n-1], the driving transistor DT is diode-connected, and the organic light-emitting diode OLED is initialized. Moreover, the fifth transistor T5 is turned on in response to the (n+1)th emission control signal Em[n+1] and transfers a drive current generated through the driving transistor DT to the organic light-emitting diode OLED. The configuration and connections of the nth subpixel SP according to the third embodiment of the present disclosure will be described below.

[0127] The first transistor T1 has a gate connected to the nth scan line SCAN[n], a first electrode connected to the mth data line DLm, and a second electrode connected to a first electrode of the second transistor T2 and a first electrode of the driving transistor DT. The first transistor T1 is turned on in response to the logic-low voltage VL of the nth scan signal Scan[n] applied via the nth scan line SCAN[n]. When the first transistor T1 is turned on, a data voltage applied via the mth data line DLm is stored in the second electrode of the first transistor T1.

[0128] The second transistor T2 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the second electrode of the first transistor T1, and a second electrode connected to the first power supply line EVDD and a first electrode of the seventh transistor T7. The second transistor T2 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the second transistor T2 is turned on, a data voltage stored in the second electrode of the first transistor T1 is transferred to one electrode of the capacitor Cst through the seventh transistor T7.

[0129] The third transistor T3 has a gate connected to the (n-1)th scan line SCAN[n-1], a first electrode connected to a second electrode of the driving transistor DT, and a second electrode connected to a gate electrode of the driving transistor DT. The third transistor T3 is turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. When the third transistor T3 is turned on, the driving transistor DT is diode-connected.

[0130] The fifth transistor T5 has a gate connected to the (n+1)th emission control signal line EM[n+1], a first electrode connected to the second electrode of the driving transistor DT, and a second electrode connected to the anode of the organic light-emitting diode OLED. The fifth transistor T5 is turned on in response to the logic-low voltage VL of the (n+1)th emission control signal Em[n+1] applied via the (n+1)th emission control signal line EM[n+1], When the fifth transistor T5 is turned on, the organic light-emitting diode OLED emits light in response to a drive current generated through the driving transistor DT.

[0131] The sixth transistor T6 has a gate connected to the (n-1)th scan line SCAN[n-1], a first electrode connected to the initial line VINI, and a second electrode connected to the second electrode of the driving transistor DT and the anode of the organic light-emitting diode OLED. The sixth transistor T6 is turned on in response to the logic-low voltage of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. When the sixth transistor T6 is turned on, the anode of the organic light-emitting diode OLED is initialized based on the initial voltage Vini.

[0132] The seventh transistor T7 has a gate connected to the nth emission control signal line EM[n], a first electrode connected to the first power supply line EVDD and the second electrode of the second transistor T2, and a second electrode connected to one electrode of the capacitor Cst. The seventh transistor T7 is turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n]. When the seventh transistor T7 is turned on, a data voltage stored in the second electrode of the first transistor T1 is transferred to the one electrode of the capacitor Cst through the second transistor T2.

[0133] One electrode of the capacitor Cst is connected to the second electrode of the seventh transistor T7, and the other electrode is connected to the second electrode of the fourth transistor T4. A node provided at the second electrode of the seventh transistor T7 and the one electrode of the capacitor Cst is defined as a voltage transfer node VDN which

transfers the reference voltage. The anode of the organic light-emitting diode OLED is connected to the second electrode of the fifth transistor T5, and the cathode thereof is connected to the second power supply line EVSS.

[0134] The Nth subpixel SP according to the third embodiment operates in a sequence of an initial and sampling period INI & SAM, a holding period HLD, and an emission period EMI. The initial and sampling period INI and SAM is a period in which the organic light-emitting diode OLED is initialized and the threshold voltage of the driving transistor DT is sampled. The holding period HLD is a period in which a data voltage applied via the mth data line DLm is held in a particular node. The emission period EMI is a period in which the organic light-emitting diode OLED emits light by a drive current generated based on the data voltage. The emission period EMI occurs not by the nth emission signal Em[n] but by the (n+1)th emission signal Em[n+1].

[0135] In the case that the nth subpixel SP is driven in such a way that the previous scan signal and the current scan signal overlap as in the third embodiment, the emission control signal may be applied longer than 3 horizontal times, e.g., up to 4 horizontal times, and then emit light based on the next emission control signal. That is, if the nth subpixel SP, which is at the current stage, emits light based on the (n+1)th emission control signal Em[n+1], which is the next emission control signal, this means that a signal for forming the emission period EMI may be selected freely. This method has the advantage of avoiding space limitations when designing or changing the layout of subpixels (because the degree of freedom for the arrangement of signal lines is high).

[0136] For the nth subpixel SP according to the third embodiment, internal circuit-based compensation is done as the initial and sampling period INI & SAM occurs while the nth emission control signal Em[n] is not applied (the logic-high voltage is maintained). The operating characteristics during these periods will be described below in brief. By way of example, the low-logic voltage is applied in response to the (n-1)th scan signal Scan[n-1] and the nth scan signal Scan[n] during 2 horizontal times 2H, and the two signals overlap during 1 horizontal time 1H.

[0137] During the initial and sampling period INI & SAM, the third transistor T3 and the sixth transistor T6 are simultaneously turned on in response to the logic-low voltage VL of the (n-1)th scan signal Scan[n-1] applied via the (n-1)th scan line SCAN[n-1]. By the turn-on of the third transistor T3 and sixth transistor T6, the threshold voltage of the driving transistor DT is sampled, and the organic light-emitting diode OLED is initialized based on the initial voltage.

[0138] The Nth subpixel SP according to the third embodiment is supplied with the reference voltage from the Nth voltage transfer part VRD during the initial and sampling period INI & SAM so that voltage drops in the first power supply voltage are taken into consideration. Accordingly, for the nth subpixel according to the third embodiment as well, voltage drops in the first power supply voltage applied via the first power supply line EVDD may be compensated for by the reference voltage applied during the initial and sampling period INI & SAM.

[0139] Therefore, the second embodiment may offer the same benefit as the first embodiment since the nth voltage transfer part VRD is capable of applying the reference voltage during the initial and sampling period INI & SAM. Moreover, in the third embodiment, power supply can be prevented from being cut off when the reference voltage is transferred, or the nodes can be prevented from electrically floating. Moreover, in the third embodiment, the nth voltage transfer part VRD comprises a single voltage transfer transistor VT, thereby simplifying the circuits enough to further reduce the non-display area (or bezel area) of the display panel. In addition, the third embodiment can overcome space limitations when designing or changing the layout of subpixels because the degree of freedom for the arrangement of signal lines is high.

[0140] As seen above, the present specification can solve or improve picture quality issues such as vertical luminance non-uniformity or crosstalk on the display panel by compensating for time-varying characteristics, with voltage drops on voltage supply lines taken into consideration. Moreover, the present specification can reduce the number of electrodes in each subpixel or the number of contacts on a wire by placing circuits for transferring reference voltage to the subpixels, and also can offer advantages in high integration, thereby preventing a decrease in aperture ratio when making a large-screen or high-resolution display panel.

[0141] FIG. 21 is a circuit diagram showing the configuration of a voltage transfer part and a gate driver according to a first modification of one of the first to third embodiments of the present specification.

[0142] The nth voltage transfer part VRD according to the first modification of the present disclosure may comprise a single voltage transfer transistor VT. The voltage transfer transistor VT may be controlled by being connected to a component of the gate driver 130. The gate driver illustrated in FIG. 21 illustrates only some of the components for explaining the connections of the voltage transfer transistor VT.

[0143] The gate driver 130 comprises a pull-up transistor Tu, a first boosting capacitor CQ1, and a first auxiliary transistor Tb1. The pull-up transistor Tu outputs a gate-on voltage to the nth scan line SCAN[n] via a scan output node SO. If a transistor connected to the nth scan line SCAN[n] is a p-type transistor, the gate-on voltage is the logic-low voltage, and if a transistor connected to the nth scan line SCAN[n] is an n-type transistor, the gate-on voltage is the logic-high voltage.

[0144] The pull-up transistor Tu has a Q1 node Q1, a first electrode connected to a clock signal line CLKL providing clock signals, and a second electrode connected to the scan output node SO. The pull-up transistor Tu is turned on in response to the logic-low voltage input into the Q1 node Q1 and applies clock signals to the scan output node SO.

[0145] One electrode of the first boosting capacitor CQ1 is connected to the gate of the pull-up transistor Tu, and the

other electrode is connected to the second electrode of the pull-up transistor Tu and the scan output node SO. The first boosting capacitor CQ1 allows the pull-up transistor Tu to stably apply the gate-on voltage to the scan output node SO by boosting the gate of the pull-up transistor Tu when the pull-up transistor Tu is turned on.

[0146] The first auxiliary transistor Tb1 has a gate connected to a logic-low voltage line VLL via which the logic-low voltage is applied, a first electrode connected to the Q1 node Q1, and a second electrode connected to the Q node Q. The first auxiliary transistor Tb1 is always kept turned on since the logic-low voltage is applied to its gate, thereby preventing voltage changes at the Q1 node Q1 from affecting other transistors connected to the Q node Q.

[0147] The voltage transfer transistor VT has a gate connected to the Q1 node Q1, a first electrode connected to the reference voltage line VREF, and a second electrode connected to the voltage transfer node VDN. The voltage transfer transistor VT is turned on in response to the logic-low voltage applied to the Q1 node Q1. In this case, the reference voltage is applied to the voltage transfer node VDN while the pull-up transistor Tu is turned on by the logic-low voltage applied to the Q node Q. Also, the reference voltage is applied to the voltage transfer node VDN while the logic-low voltage is applied to the nth scan line SCAN[n].

<Fourth Embodiment>

[0148] FIG. 22 is a circuit diagram showing a voltage transfer part and a subpixel according to a fourth embodiment of the present disclosure.

[0149] The nth voltage transfer part VRD according to the fourth embodiment may comprise a voltage transfer transistor VT, as illustrated in FIG. 6. FIG. 22 illustrates the connections between the voltage transfer part VRD and the subpixel SP. Moreover, the components of the subpixels SPs are identical to the components of the subpixels SPs explained in FIG. 6 may be omitted or explained briefly.

[0150] The voltage transfer transistor VT has a gate connected to the Q1 node Q1, a first electrode connected to the reference voltage line VREF, and a second electrode connected to the voltage transfer node VDN. The voltage transfer transistor VT is turned on in response to the logic-low voltage applied to the Q1 node Q1 and applies the reference voltage to the voltage transfer node VDN.

[0151] FIGs. 23A to 26B are views showing operations and waveforms of FIG. 22. FIG. 23A is a view showing an operation during a first initial period of FIG. 22. FIG. 23B is a waveform diagram showing the operation of FIG. 23A. FIG. 24A is a view showing an operation during a sampling and second period of FIG. 22. FIG. 24B is a waveform diagram showing the operation of FIG. 24A. FIG. 25A is a view showing an operation during a holding period of FIG. 22. FIG. 25B is a waveform diagram showing the operation of FIG. 25A. FIG. 26A is a view showing an operation during an emission period of FIG. 22. FIG. 26B is a waveform diagram showing the operation of FIG. 26A.

[0152] Referring to FIGs. 23A and 23B, the fourth transistor T4 is turned on in response to the logic-low voltage VL applied via the (n-1)th scan line SCAN[n-1] during the first initial period INI. Since the initial voltage Vini is applied to the gate DTG of the driving transistor DT through the turned-on fourth transistor T4, the gate node DTG of the driving transistor DT is initialized to the initial voltage Vini. Moreover, the voltage transfer transistor VT is turned on in response to the logic-low voltage VL applied to the Q1 node Q1 during the first initial period INI. The reference voltage is applied to the voltage transfer node VDN through the turned-on voltage transfer transistor VT.

[0153] Referring to FIGs. 24A and 24B, the first transistor T1, third transistor T3, driving transistor DT, and sixth transistor T6 are turned on in response to the logic-low voltage VL applied via the nth scan line SCAN[n] during the sampling and second initial period SAM. The gate and drain electrode of the driving transistor are connected together by the turned-on third transistor T3, and a data voltage Vdata is applied to the source electrode of the driving transistor DT through the turned-on first transistor T1, thereby turning on the driving transistor DT. The voltage of the gate node DTG of the driving transistor DT rises up to the difference between the data voltage Vdata and the threshold voltage Vth of the driving transistor DT. Moreover, the Q1 node Q1 is boosted during the sampling and second initial period SAM to apply the logic-low voltage through the nth scan line SCAN[n], and therefore the voltage transfer transistor VT is turned on to apply the reference voltage to the voltage transfer node VDN. In this case, the boosted voltage of the Q1 node Q1 is lower than the logic-low voltage VL and higher than 2VL, which is twice as high as the logic-low voltage. Accordingly, the reference voltage Vref applied to one electrode of the capacitor and the difference Vdata-|Vth| between the data voltage applied to the other electrode of the capacitor Cst are stored as a capacitance. Moreover, the sixth transistor T6 is turned on during the sampling and second initial period SAM to initial the anode of the organic light-emitting diode OLED to the initial voltage Vini.

[0154] As can be seen from FIGs. 24A and 24B, the voltage transfer transistor is turned on during the first initial period in response to the logic-low voltage of the (n-1)th scan signal for driving the (N-1)th subpixels of the (n-1)th scan line and during the sampling and second initial period in response to the nth scan signal for driving the nth subpixels of the Nth scan line, thereby applying the reference voltage to the subpixels. Accordingly, the subpixels applied with the reference voltage supplies the organic light-emitting diodes with a drive current not affected by the first power supply voltage, thereby improving the problem of the picture quality of the electroluminescence display.

[0155] Referring to FIGs. 25A and 25B, the logic-high voltage VH is applied to the Q1 node during the holding period HLD to thereby turn off the voltage transfer transistor VT. Moreover, the (n-1)th scan signal Scan[n-1] and the nth scan signal Scan[n] are the logic-high voltage VH, which causes all transistors constituting the subpixel to be turned off. The holding period HLD varies with the cycle of clock signals from an emission driver outputting the nth emission control signal Em[n] and the cycle of clock signals from the gate driver outputting the Nth scan signal Scan[n]. For example, the holding period HLD may be longer than 1 horizontal time 1H. During the holding period HLD, the capacitor Cst stores and maintains a data voltage based on the voltage difference between the two ends. As the nth scan signal Scan[n] is switched from the logic-low voltage to the logic-high voltage during the holding period HLD, the voltage of the gate node DTG of the driving transistor DT may be slightly varied by a parasitic capacitor of the third transistor T3.

[0156] Referring to FIGs. 26A and 26B, the second transistor T2, seventh transistor T7, and fifth transistor T5 are turned on in response to the logic-low voltage VL of the nth emission control signal Em[n] applied via the nth emission control signal line EM[n] during the emission period EMI. The first power supply voltage VDD is applied to one electrode of the capacitor Cst through the turned-on seventh transistor T7. The first power supply voltage VDD is applied to the first electrode of the driving transistor DT through the turned-on second transistor T2, and the fifth transistor T5 is turned on, thereby turning on the driving transistor DT. The turned-on driving transistor DT provides a drive current to the anode of the organic light-emitting diode, thereby causing the organic light-emitting diode to emit light. In this case, the voltage applied to one electrode of the capacitor Cst is varied, so the voltage of the other electrode of the capacitor Cst is also varied due to coupling. The drive current provided to the anode of the organic light-emitting diode OLED is the same as represented by the equation mentioned with respect to FIG. 3.

[0157] According to the fourth embodiment of the present specification, the voltage transfer transistor VT for applying the reference voltage may be disposed at one electrode of the capacitor Cst. Therefore, a drive circuit for compensating for time-varying characteristics (or variation with time) may be implemented, with drops in power-supply voltage taken into consideration, and this can solve picture quality problems such as vertical luminance non-uniformity or crosstalk on the display panel.

[0158] FIG. 27 is a circuit diagram showing the configuration of a voltage transfer part and a gate driver according to a second modification of one of the first to fourth embodiments of the present specification. FIG. 27 shows a modification of the connections of the voltage transfer part due to an alteration to the configuration of the gate driver 130 of FIG. 21, so any redundancies will be omitted or explained briefly.

[0159] The nth voltage transfer part VRD according to the second modification of the present disclosure may comprise a single voltage transfer transistor VT. The voltage transfer transistor VT may be controlled by being connected to a component of the gate driver 130. The gate driver illustrated in FIG. 27 illustrates only some of the components for explaining the connections of the voltage transfer transistor VT.

[0160] Referring to FIG. 27, the gate driver 130 comprises a pull-up transistor Tu, a first boosting capacitor CQ1, a second boosting capacitor CQ2, a first auxiliary transistor Tb1, and a second auxiliary transistor Tb2. The pull-up transistor Tu outputs a gate-on voltage to the nth scan line SCAN[n] via a scan output node SO.

[0161] The pull-up transistor Tu has a Q1 node Q1, a first electrode connected to a clock signal line CLKL providing clock signals, and a second electrode connected to the scan output node SO. The pull-up transistor Tu is turned on in response to the logic-low voltage input into the Q1 node Q1 and applies clock signals to the scan output node SO.

[0162] One electrode of the first boosting capacitor CQ1 is connected to the gate of the pull-up transistor Tu, and the other electrode is connected to the second electrode of the pull-up transistor Tu and the scan output node SO. The first boosting capacitor CQ1 allows the pull-up transistor Tu to stably apply the gate-on voltage to the scan output node SO by boosting the gate of the pull-up transistor Tu when the pull-up transistor Tu is turned on.

[0163] One electrode of the second boosting capacitor CQ2 is connected to the other electrode of the first bosting capacitor CQ1, and the other electrode is connected to a Q2 node Q2 and the gate of the voltage transfer transistor VT. According to the second modification of the present specification, the gate of the voltage transfer transistor VT is connected to the Q1 node Q1, and the Q1 node Q1 forms a parasitic capacitance as well as the capacitance caused by the first boosting capacitor CQ1. Due to the parasitic capacitance caused by the voltage transfer transistor VT, the boosting efficiency of the Q1 node Q1 may be decreased. According to the second embodiment of the present specification, the gate of the voltage transfer transistor VT may be separated from the Q1 node Q by using the second boosting capacitor CQ2 in the gate driver 130, thereby preventing a decrease in the boosting efficiency of the Q1 node Q1.

[0164] The first auxiliary transistor Tb1 has a gate connected to a logic-low voltage line VLL via which the logic-low voltage is applied, a first electrode connected to the Q1 node Q1, and a second electrode connected to the Q node Q. The first auxiliary transistor Tb1 is always kept turned on since the logic-low voltage is applied to its gate, thereby preventing voltage changes at the Q1 node Q1 from affecting other transistors connected to the Q node Q.

[0165] The second auxiliary transistor Tb2 has a gate connected to the logic-low voltage line VLL via which the logic-low voltage is applied, a first electrode connected to the Q2 node Q2, and a second electrode connected to the Q node Q. The second auxiliary transistor Tb2 is always kept turned on since the logic-low voltage is applied to its gate, thereby preventing voltage changes at the Q2 node Q2 from affecting other transistors connected to the Q node Q. The second

auxiliary transistor Tb2 separates the gate of the voltage transfer transistor VT form the Q1 node Q1, along with the second boosting capacitor CQ2.

[0166] The voltage transfer transistor VT has a gate connected to the Q2 node Q2, a first electrode connected to the reference voltage line VREF, and a second electrode connected to the voltage transfer node VDN. The voltage transfer transistor VT is turned on in response to the logic-low voltage applied to the Q2 node Q2. In this case, the reference voltage is applied to the voltage transfer node VDN while the pull-up transistor Tu is turned on by the logic-low voltage applied to the Q node Q. Also, the reference voltage is applied to the voltage transfer node VDN while the logic-low voltage is applied to the nth scan line SCAN[n].

<Fifth Embodiment>

[0167] FIG. 28 is a circuit diagram showing a voltage transfer part and a subpixel according to a fifth embodiment of the present disclosure.

[0168] The nth voltage transfer part VRD according to the fifth embodiment may comprise a voltage transfer transistor VT, as illustrated in FIG. 27. FIG. 28 illustrates the connections between the voltage transfer part VRD and the subpixel SP. Moreover, the components of the subpixels SPs are identical to the components of the subpixels SPs explained in FIG. 6 may be omitted or explained briefly.

[0169] The voltage transfer transistor VT has a gate connected to the Q2 node Q2, a first electrode connected to the reference voltage line VREF, and a second electrode connected to the voltage transfer node VDN. The voltage transfer transistor VT is turned on in response to the logic-low voltage applied to the Q2 node Q2 and applies the reference voltage to the voltage transfer node VDN.

[0170] FIG. 29 is a view showing an operation of FIG. 28.

[0171] The nth subpixel SP operates in a sequence of a first initial period INI, a sampling and second initial period SAM, a holding period HLD, and an emission period EMI. The operations of the subpixel SP in the respective phases are identical to those shown in FIGs. 23A, 24A, 25A, and 26A according to the first embodiment of the present disclosure, so any redundancies will be omitted or explained briefly.

[0172] During the first initial period INI, the gate node DTG of the driving transistor DT is initial to the initial voltage Vini by the logic-low voltage VL of the (n-1)th scan signal Scan[n-1]. Also, the logic-low voltage VL is applied to the Q1 node Q1 and the Q2 node Q2 in response to the logic-low voltage VL applied to the Q node Q.

[0173] During the sampling and second initial period SAM, the voltage applied to the gate node DTG of the driving transistor DT by the logic-low voltage VL of the nth scan signal Scan[n] rises up to the difference between the data voltage and the threshold voltage of the driving transistor DT. Moreover, in the gate driver 130, the Q1 node Q1 is boosted by the first boosting capacitor CQ1, and the voltage of the Q1 node Q1 drops to 2VL which is lower than the logic-low voltage VL, thereby properly outputting the logic-low voltage VL to the nth scan line SCAN[n]. Accordingly, the efficiency of the gate driver 130 can be improved. In this case, the gate of the voltage transfer transistor VT, as well as the second boosting capacitor CQ2, is connected to the Q2 node Q2, thereby keeping the voltage of the Q2 node Q2 from dropping as much as the voltage at the Q1 node Q1 drops due to the parasitic capacitance of the voltage transfer transistor VT.

[0174] During the holding period HLD, the nth scan signal Scan[n], Q node Q, Q1 node Q1, and Q2 node may be switched to the logic-high voltage VH, and the (n-1)th scan signal Scan[n-1] and the nth emission control signal Em[n] may be kept at the logic-high voltage VH. In this case, the holding period HLD may be maintained for 1 horizontal time 1H or longer. Also, during the holding period HLD, the capacitor Cst stores and maintains a data voltage based on the voltage difference between the two ends. In this case, as the nth scan signal Scan[n] is switched from the logic-low voltage to the logic-high voltage, the voltage of the gate node DTG of the driving transistor DT may be slightly varied by a parasitic capacitor of the third transistor T3.

[0175] During the emission period EMI, the nth emission control signal Em[n] is switched to the logic-low voltage VL, and the driving transistor DT is turned on. The turned-on driving transistor DT provides a drive current to the anode of the organic light-emitting diode OLED, thereby causing the organic light-emitting diode OLED to emit light. The drive current provided to the anode of the organic light-emitting diode OLED is the same as represented by the equation mentioned with respect to FIG. 3.

[0176] According to the fifth embodiment of the present specification, the voltage transfer transistor VT for applying the reference voltage may be disposed at one electrode of the capacitor Cs, and the second boosting capacitor CQ2 and the second auxiliary transistor Tb2 may be disposed at the gate driver 130. Therefore, a drive circuit for compensating for time-varying characteristics (or variation with time) may be implemented, with drops in power-supply voltage taken into consideration, and this can solve picture quality problems such as vertical luminance non-uniformity or crosstalk on the display panel.

[0177] Although the voltage transfer part VRD according to the fourth and fifth embodiments of the present specification has been illustrated and explained separately from the gate driver 130, the present disclosure is not limited thereto and

the voltage transfer part VRD may be included in the gate driver 130. Accordingly, the efficiency of the gate driver may be improved.

[0178] According to the embodiments of the present specification, a circuit for transferring a reference voltage to subpixels may be included in a non-display area, and this can simplify the pixel circuits and therefore offers advantages for high integration, thereby preventing a decrease in aperture ratio when making a large-screen or high-resolution display panel.

[0179] According to the embodiments of the present specification, a circuit for transferring a reference voltage to subpixels may be included in the gate driver, and this can improve the efficiency of the gate driver.

[0180] According to the embodiments of the present specification, a drive circuit for compensating for time-varying characteristics (or variation with time) may be implemented, with drops in power-supply voltage taken into consideration, and this can solve picture quality problems such as vertical luminance non-uniformity or crosstalk on the display panel.

[0181] An electroluminescent display device and a driving method of the electroluminescence display device according to various embodiments of the disclosure will be described as follows.

[0182] According to an aspect of the present disclosure, there is provided an electroluminescence display device comprising a display panel having a display area where images are displayed and a non-display area where images are not displayed, a subpixel located in the display area, and a voltage transfer part that is located in the non-display area and transfers a reference voltage to a voltage transfer node of the subpixel in response to a signal applied from outside the display panel or a signal generated on the display panel.

[0183] According to another aspect of the present disclosure, the display panel may comprise a plurality of scan lines, to each of which a plurality of subpixels are connected, and the voltage transfer part is provided on each scan line in the non-display area.

[0184] According to another aspect of the present disclosure, the voltage transfer part may operate to output the reference voltage during a sampling period for sampling the threshold voltage of a driving transistor of the subpixel.

[0185] According to another aspect of the present disclosure, the voltage transfer part may comprise at least one voltage transfer transistor that is turned on or off in response to an (n-1)th scan signal for driving (n-1)th subpixels on an (n-1)th scan line or an nth scan signal for driving nth subpixels on an nth scan line.

[0186] According to another aspect of the present disclosure, the first voltage transfer transistor may have a gate connected to the (n-1)th scan line, a first electrode connected to a reference voltage line for transferring the reference voltage, and a second electrode connected to the voltage transfer node included in the subpixel, and the second voltage transfer has a gate connected to the nth scan line, a first electrode connected to the reference voltage line, and a second electrode connected to the voltage transfer node.

[0187] According to another aspect of the present disclosure, the voltage transfer part may comprise a voltage transfer transistor that has a gate connected to the nth scan line, a first electrode connected to a reference voltage line for transferring the reference voltage, and a second electrode connected to the voltage transfer node.

[0188] According to another aspect of the present disclosure, the voltage transfer part may comprise a voltage transfer transistor that has a gate connected to the (n-1)th scan line, a first electrode connected to a reference voltage line for transferring the reference voltage, and a second electrode connected to the voltage transfer node.

[0189] According to another aspect of the present disclosure, the subpixel may comprise a first transistor that has a gate connected to an nth scan line and a first electrode connected to a first data line, a second transistor that has a gate connected to an nth emission control signal line, a first electrode connected to a second electrode of the first transistor, and a second electrode connected to a first power supply line, a driving transistor that has a gate connected to a gate node and a first electrode connected to the second electrode of the first transistor and the first electrode of the second transistor, a third transistor that has a gate connected to the nth scan line, a first electrode connected to a second electrode of the driving transistor, and a second electrode connected to the gate of the driving transistor, a fourth transistor that has a gate connected to an (n-1)th scan line, a first electrode connected to an initial line, and a second electrode connected to the second electrode of the third transistor and the gate of the driving transistor, a fifth transistor that has a gate connected to the nth emission control signal line and a first electrode connected to the second electrode of the driving transistor, a sixth transistor that has a gate connected to the nth scan line, a first electrode connected to the initial line, and a second electrode connected to a second electrode of the fifth transistor, a seventh transistor that has a gate connected to the nth emission control signal line, a first electrode connected to the first power supply line, and a second electrode connected to the voltage transfer node, a capacitor that has a first electrode connected to the voltage transfer node, and a second electrode connected to the gate of the driving transistor, and an organic light-emitting diode that has an anode connected to the second electrode of the fifth transistor and a cathode connected to a second power supply line.

[0190] According to another aspect of the present disclosure, the subpixel may comprise a first transistor that has a gate connected to an nth scan line and a first electrode connected to a first data line, a second transistor that has a gate connected to an nth emission control signal line, a first electrode connected to a second electrode of the first transistor, and a second electrode connected to a first power supply line, a driving transistor that has a gate connected to a gate

node and a first electrode connected to the second electrode of the first transistor and the first electrode of the second transistor, a third transistor that has a gate connected to the nth scan line, a first electrode connected to a second electrode of the driving transistor, and a second electrode connected to the gate of the driving transistor, a fourth transistor that has a gate connected to an (n-1)th scan line, a first electrode connected to an initial line, and a second electrode connected to the second electrode of the third transistor and the gate of the driving transistor, a fifth transistor that has a gate connected to the nth emission control signal line and a first electrode connected to the second electrode of the driving transistor, a sixth transistor that has a gate connected to the (n-1)th scan line, a first electrode connected to the initial line, and a second electrode connected to the second electrode of the fifth transistor, a seventh transistor that has a gate connected to the nth emission control signal line, a first electrode connected to the first power supply line, and a second electrode connected to the voltage transfer node, a capacitor that has a first electrode connected to the voltage transfer node, and a second electrode connected to the gate of the driving transistor, and an organic light-emitting diode that has an anode connected to the second electrode of the fifth transistor and a cathode connected to a second power supply line.

[0191] According to another aspect of the present disclosure, the subpixel may comprisea first transistor that has a gate connected to an nth scan line and a first electrode connected to a first data line, a second transistor that has a gate connected to an nth emission control signal line, a first electrode connected to a second electrode of the first transistor, and a second electrode connected to a first power supply line, a driving transistor that has a gate connected to a gate node and a first electrode connected to the second electrode of the first transistor and the first electrode of the second transistor, a third transistor that has a gate connected to the (n-1)th scan line, a first electrode connected to a second electrode of the driving transistor, and a second electrode connected to the gate of the driving transistor, a fifth transistor that has a gate connected to the (n+1)th emission control signal line and a first electrode connected to the second electrode of the driving transistor, a sixth transistor that has a gate connected to the (n-1)th scan line, a first electrode connected to the initial line, and a second electrode connected to a second electrode of the fifth transistor, a seventh transistor that has a gate connected to the nth emission control signal line, a first electrode connected to the first power supply line, and a second electrode connected to the voltage transfer node, a capacitor that has a first electrode connected to the voltage transfer node, and a second electrode connected to the gate of the driving transistor, and an organic light-emitting diode that has an anode connected to the second electrode of the fifth transistor and a cathode connected to a second power supply line.

[0192] According to an aspect of the present disclosure, there is provided an electroluminescence display device comprising a display panel having a display area where images are displayed and a non-display area where images are not displayed, a subpixel located in the display area, and a voltage transfer part that is located in the non-display area and transfers a reference voltage to the subpixel. The method comprising an initial step for initializing the subpixel, and a sampling step for compensating for the threshold voltage of a driving transistor of the subpixel. Wherein, during the sampling step, the voltage transfer part operates in response to a signal applied from outside the display panel or a signal generated on the display panel.

[0193] According to another aspect of the present disclosure, the voltage transfer part may be turned on for a first period based on an (n-1)th scan signal for driving (n-1)th subpixels on an (n-1)th scan line, the voltage transfer part may be turned on during a second period subsequent to the first period based on an nth scan signal for driving nth subpixels on an nth scan line, and the reference voltage may be transferred to the nth subpixels during the first and second periods.

[0194] According to another aspect of the present disclosure, for the nth subpixels on the display panel, the initial step and the sampling step may be performed at different times based on an nth scan signal and an (n-1)th scan signal which overlap during at least 1 horizontal time.

[0195] According to another aspect of the present disclosure, the voltage transfer part may be turned on based on the nth scan signal for driving the nth subpixels so as to transfer the reference voltage to the nth subpixels.

[0196] According to another aspect of the present disclosure, for the nth subpixels on the display panel, the initial step and the sampling step may be performed simultaneously based on an nth scan signal and an (n-1)th scan signal which overlap during at least 1 horizontal time.

[0197] According to another aspect of the present disclosure, the voltage transfer part may be turned on based on the (n-1)th scan signal for driving the (n-1)th subpixels so as to transfer the reference voltage to the nth subpixels.

[0198] According to an aspect of the present disclosure, there is provided an electroluminescence display device comprising a display panel having a display area where images are displayed and a non-display area where images are not displayed, a subpixel located in the display area, a gate driver located in the non-display area, and a voltage transfer transistor that is located in the non-display area and transfers a reference voltage to the subpixel. And a gate of the voltage transfer transistor is connected to the gate driver.

[0199] According to another aspect of the present disclosure, the gate driver may comprise a pull-up transistor, and a first boosting capacitor connected to a gate of the pull-up transistor and a drain of the pull-up transistor. And the gate of the voltage transfer transistor may be connected to the gate of the pull-up transistor.

[0200] According to another aspect of the present disclosure, the gate driver may further comprise a first auxiliary

transistor. And a gate of the first auxiliary transistor may be connected to a line via which a logic-low voltage is applied, and a first electrode of the first auxiliary transistor may be connected to the gate of the pull-up transistor.

[0201] According to another aspect of the present disclosure, the gate driver may comprise a pull-up transistor, a first boosting capacitor connected to a gate of the pull-up transistor and a drain of the pull-up transistor, and a second boosting capacitor whose one electrode may be connected to the drain of the pull-up transistor. And the gate of the pull-up transistor may be connected to the other electrode of the second boosting capacitor.

[0202] According to another aspect of the present disclosure, the gate driver may further comprise a first auxiliary transistor and a second auxiliary transistor. And a gate of the first auxiliary transistor and a gate of the second auxiliary transistor may be connected to a line via which a logic-low voltage is applied, a first electrode of the first auxiliary transistor may be connected to a gate of the pull-up transistor, a first electrode of the second auxiliary transistor may be connected to a gate of the voltage transfer transistor, and a second electrode of the first auxiliary transistor and a second electrode of the second auxiliary transistor may be connected to the same node.

[0203] According to another aspect of the present disclosure, a first electrode of the voltage transfer transistor may be connected to a line via which the reference voltage is applied, and a second electrode of the voltage transfer transistor may be connected to a voltage transfer node included in the subpixel.

[0204] According to an aspect of the present disclosure, there is provided a driving method of an electroluminescence display device comprising a display panel having a display area and a non-display area, a subpixel located in the display area and comprising an organic light-emitting diode, and a voltage transfer part located in the non-display area. The method comprising a first initial step for initializing a gate of a driving transistor included in the subpixel, a sampling and second initial step for compensating for the threshold voltage of the driving transistor and initializing an anode of the organic light-emitting diode. Wherein, during the first initial step and the sampling and second initial step, the voltage transfer part provides a reference voltage to the subpixel.

[0205] According to another aspect of the present disclosure, the voltage transfer part may be turned on in the first initial step in which an (n-1)th scan signal for driving subpixels connected to an (n-1)th scan line is a logic-low voltage and in the sampling and second initial step in which an nth scan signal for driving subpixels connected to an nth scan line is the logic-low voltage.

[0206] According to another aspect of the present disclosure, in the sampling and second initial step, the reference voltage applied through the voltage transfer part may be stored at one electrode of a capacitor included in the subpixel.

[0207] According to another aspect of the present disclosure, a logic-low voltage may be applied to the voltage transfer part in the first initial step, and a voltage lower than the logic-low voltage may be applied to the voltage transfer part in the sampling and second initial step.

Claims

1. An electroluminescence display device comprising:

a display panel (150) having a display area (AA) where images are displayed and a non-display area (NA) where images are not displayed;
a subpixel (SP) located in the display area (AA);
a gate driver (130) located in the non-display area (NA); and
at least one voltage transfer transistor (VT) that is located in the non-display area (NA), wherein a gate of the voltage transfer transistor (VT) is connected to the gate driver (130) and wherein the voltage transfer transistor (VT) is configured to transfer a reference voltage (VREF) to a voltage transfer node (VDN) of the subpixel (SP) in response to a signal applied from outside the display panel (150) or a signal generated on the display panel (150).

2. The electroluminescence display device of claim 1, wherein the gate driver (130) comprises:

a pull-up transistor (Tu); and
a first boosting capacitor (CQ1) connected to a gate of the pull-up transistor (Tu) and a drain of the pull-up transistor (Tu),

wherein the gate of the voltage transfer transistor (VT) is connected to the gate of the pull-up transistor (Tu).

3. The electroluminescence display device of claim 2, wherein the gate driver (130) further comprises a first auxiliary transistor (Tb1),

wherein a gate of the first auxiliary transistor (Tb1) is connected to a line (VLL) via which a logic-low voltage is applied, and a first electrode of the first auxiliary transistor (Tb1) is connected to the gate of the pull-up transistor (Tu).

4. The electroluminescence display device of one of the claims 2 to 3, wherein the gate driver (130) further comprises a second boosting capacitor (CQ2) whose one electrode is connected to the drain of the pull-up transistor (Tu),

wherein the gate of the voltage transfer transistor (VT) is connected to the other electrode of the second boosting capacitor (CQ2).

5. The electroluminescence display device of one of the claims 3 or 4, wherein the gate driver (130) further comprises a second auxiliary transistor (Tb2),

wherein a gate of the second auxiliary transistor (Tb2) is connected to a line (VLL) via which a logic-low voltage is applied,
wherein a first electrode of the second auxiliary transistor (Tb2) is connected to a gate of the voltage transfer transistor (VT), and
wherein a second electrode of the first auxiliary transistor (Tb1) and a second electrode of the second auxiliary transistor (Tb2) are connected to the same node.

6. The electroluminescence display device of one of the preceding claims, wherein a first electrode of the voltage transfer transistor (VT) is connected to a line via which the reference voltage is applied, and a second electrode of the voltage transfer transistor (VT) is connected to the voltage transfer node (VDN) included in the subpixel (SP).

7. The electroluminescence display device of one of the preceding claims, wherein the display panel (150) comprises a plurality of scan lines (GL1, ..., GLn), to each of which a plurality of subpixels (SP) is connected, and the voltage transfer transistor (VT) is provided on each scan line (GL1, ..., GLn) in the non-display area (NA).

8. The electroluminescence display device of one of the preceding claims, wherein the voltage transfer transistor (VT) is configured to output the reference voltage (VREF) during a sampling period (SAM) for sampling the threshold voltage of a driving transistor (DT) of the subpixel (SP).

9. The electroluminescence display device of one of the preceding claims, wherein the voltage transfer transistor (VT) is turned on or off in response to an (n-1)th scan signal for driving (n-1)th subpixels (SP) on an (n-1)th scan line (SCAN[n-1]) or an nth scan signal (SCAN[n]) for driving nth subpixels (SP) on an nth scan line (SCAN[n]).

10. The electroluminescence display device of one of the claims, wherein the at least one voltage transfer transistor (VT) is a first voltage transfer transistor (VTa) and the gate of the first voltage transfer transistor (VTa) is connected to an (n-1)th scan line (SCAN[n-1]), a first electrode is connected to a reference voltage line (VREF) for transferring the reference voltage, and a second electrode is connected to the voltage transfer node (VDN) included in the subpixel (SP); and
a second voltage transfer transistor (VTb) that has a gate connected to an nth scan line (SCAN[n]), a first electrode connected to the reference voltage line (VREF), and a second electrode connected to the voltage transfer node (VDN).

11. The electroluminescence display device of one of the preceding claims, wherein the subpixel (SP) comprises:

a first transistor (T1) that has a gate connected to an nth scan line (SCAN[n]) and a first electrode connected to a first data line (DLm);
a second transistor (T2) that has a gate connected to an nth emission control signal line (EM[n]), a first electrode connected to a second electrode of the first transistor (T1), and a second electrode connected to a first power supply line (EVDD);
a driving transistor (DT) that has a gate connected to a gate node (DTG) and a first electrode connected to the second electrode of the first transistor (T1) and the first electrode of the second transistor (T2);
a third transistor (T3) that has a gate connected to the nth scan line (SCAN[n]) or the (n-1)th scan line (SCAN[n-1]), a first electrode connected to a second electrode of the driving transistor (DT), and a second electrode connected to the gate electrode of the driving transistor (DT);
preferably, a fourth transistor (T4) that has a gate connected to an (n-1)th scan line (SCAN[n-1]), a first electrode connected to an initial line (VINI), and a second electrode connected to the second electrode of the third transistor

(T3) and the gate of the driving transistor (DT);
a fifth transistor (T5) that has a gate connected to the nth emission control signal line or the (n-1)th emission control signal line and a first electrode connected to the second electrode of the driving transistor (DT);
a sixth transistor (T6) that has a gate connected to the nth scan line (SCAN[n]) or the (n-1)th scan line (SCAN[n-1]), a first electrode connected to the initial line (VINI), and a second electrode connected to a second electrode of the fifth transistor (T5);
a seventh transistor (T7) that has a gate connected to the nth emission control signal line (EM[n]), a first electrode connected to the first power supply line (EVDD), and a second electrode connected to the voltage transfer node (VDN);
a capacitor (Cst) that has a first electrode connected to the voltage transfer node (VDN), and a second electrode connected to the gate of the driving transistor (DT); and
an organic light-emitting diode (OLED) that has an anode connected to the second electrode of the fifth transistor (T5) and a cathode connected to a second power supply line (EVSS).

12. A driving method of an electroluminescence display device according to one of the preceding claims that comprises:

a display panel (150) having a display area (AA) where images are displayed and a non-display area (NA) where images are not displayed;
a subpixel located in the display area (AA);
a gate driver (130) located in the non-display area (AA); and
at least one voltage transfer transistor (VT) that is located in the non-display area (NA), wherein a gate of the voltage transfer transistor (VT) is connected to the gate driver (130) and wherein the voltage transfer transistor (VT) is configured to transfer a reference voltage (VREF) to a voltage transfer node (VDN) of the subpixel (SP), the method comprising:

an initial step for initializing the subpixel (SP); and
a sampling step for compensating for the threshold voltage of a driving transistor (DT) of the subpixel (SP),

wherein, during the sampling step, the voltage transfer transistor (VT) is configured to operate in response to a signal applied from outside the display panel (150) or a signal generated on the display panel (150).

13. The method of claim 12, wherein the voltage transfer transistor (VT) is turned on for a first period based on an (n-1)th scan signal for driving (n-1)th subpixels (SP) on an (n-1)th scan line (SCAN[n-1]), the voltage transfer transistor (VT) is turned on during a second period subsequent to the first period based on an nth scan signal for driving nth subpixels on an nth scan line (SCAN[n]), and the reference voltage (VREF) is transferred to the nth subpixels (SP) during the first and second periods.

14. The method of claim 12 or 13, wherein, for the nth subpixels (SP) on the display panel (150), the initial step and the sampling step are performed at different times based on an nth scan signal and an (n-1)th scan signal which overlap during at least 1 horizontal time.

15. The method of one of the claims 12 to 14, wherein the voltage transfer transistor (VT) is turned on based on the nth scan signal for driving the nth subpixels so as to transfer the reference voltage (VREF) to the nth subpixels (SP).

Fig. 1

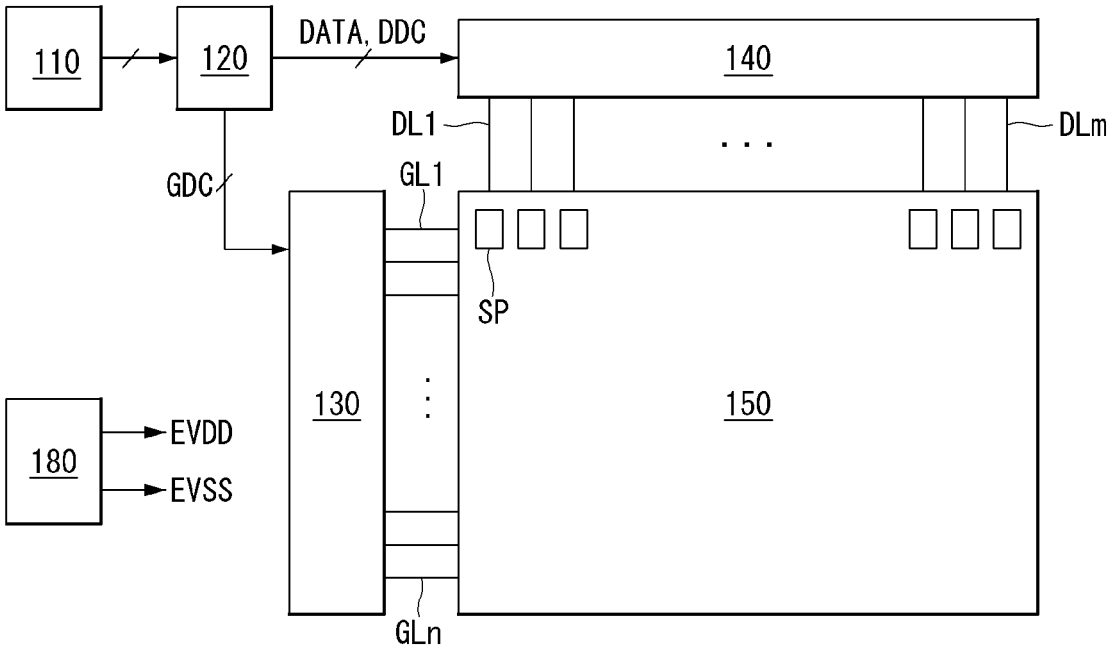
110
120
DATA, DDC
140
DL1
DLm
GDC
GL1
SP
130
150
180
EVDD
EVSS
GLn

Fig. 2

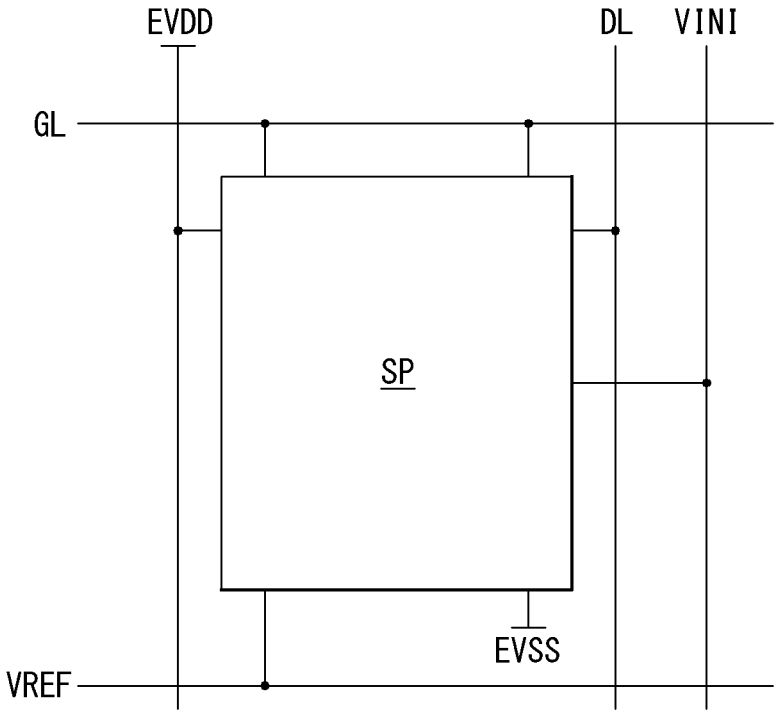
EVDD
DL
VINI
GL
SP
EVSS
VREF

Fig. 3

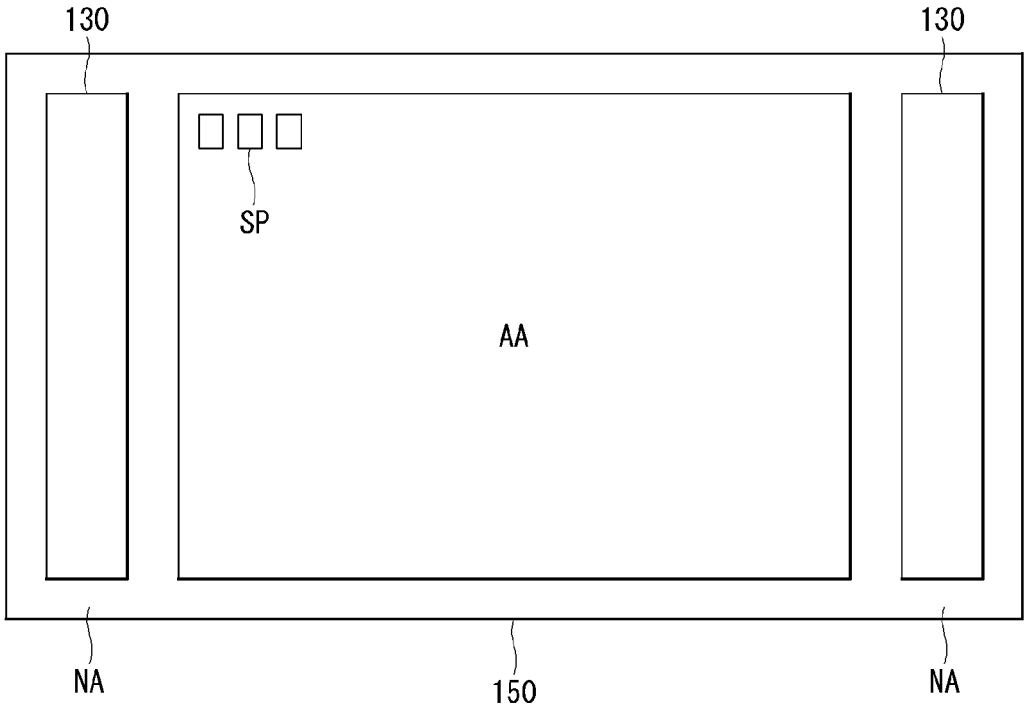
130
130
SP
AA
NA
150
NA

Fig. 4

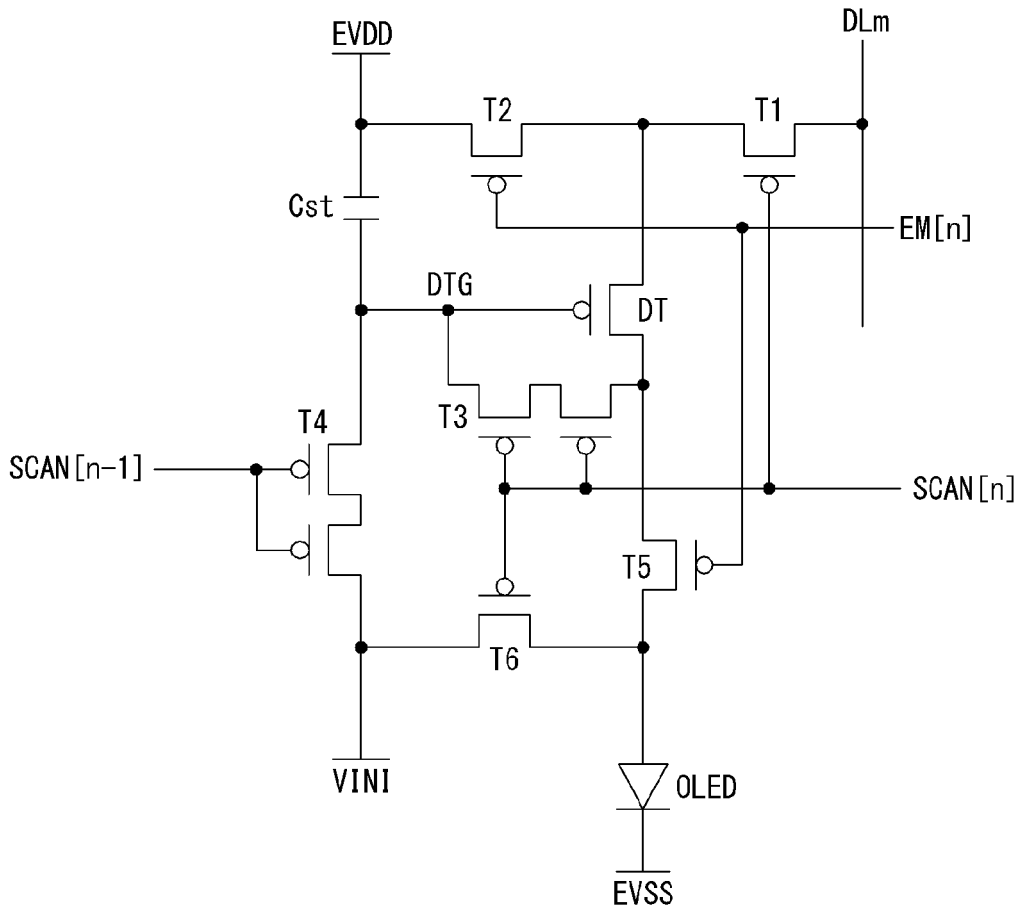
EVDD
DLm
T2
T1
Cst
EM[n]
DTG
DT
T3
T4
SCAN[n-1]
SCAN[n]
T5
T6
VINI
OLED
EVSS

Fig. 5

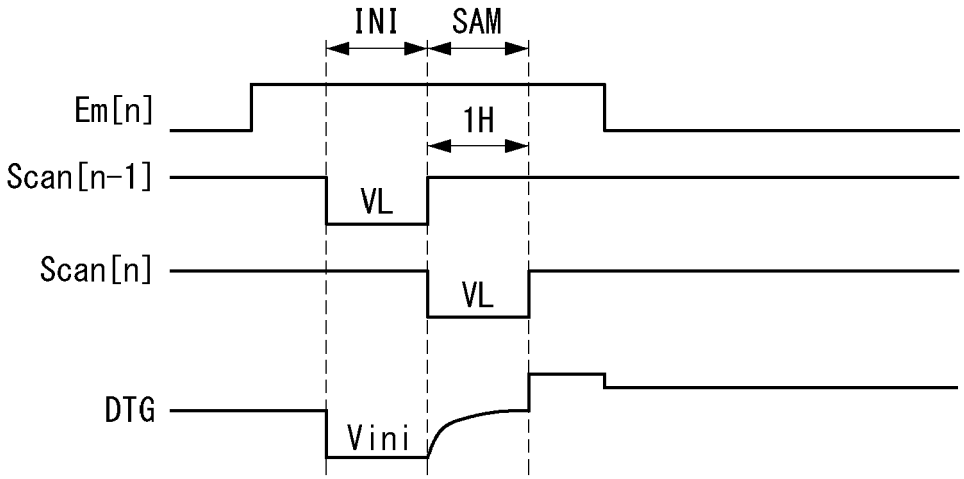
INI
SAM
Em[n]
1H
Scan[n-1]
VL
Scan[n]
VL
DTG
Vini

Fig. 6

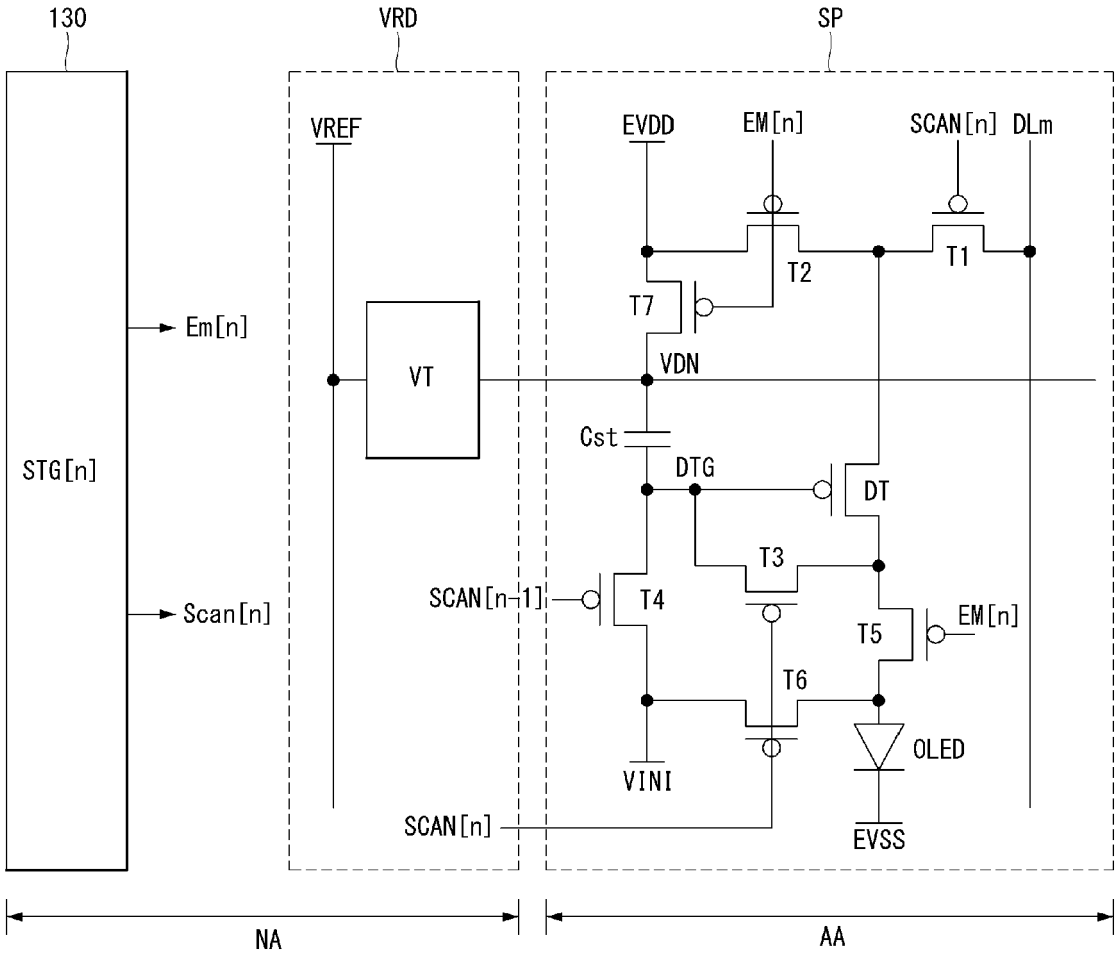
130
VRD
SP
VREF
EVDD
EM[n]
SCAN[n]
DLm
T1
T2
T7
VDN
VT
Em[n]
STG[n]
Cst
DTG
DT
T3
SCAN[n-1]
T4
T5
EM[n]
Scan[n]
T6
OLED
VINI
SCAN[n]
EVSS
NA
AA

Fig. 7

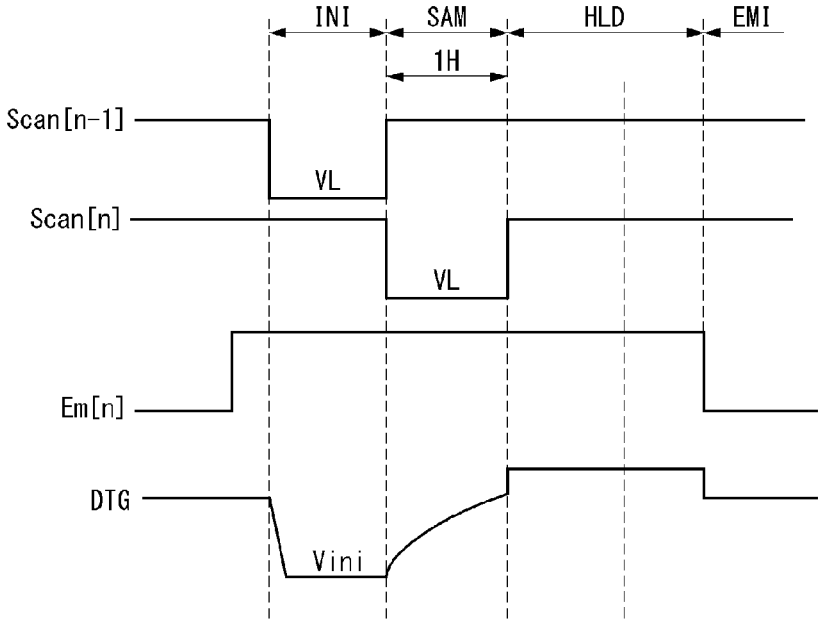
INI
SAM
HLD
EMI
1H
Scan[n-1]
VL
Scan[n]
VL
Em[n]
DTG
Vini

Fig. 8

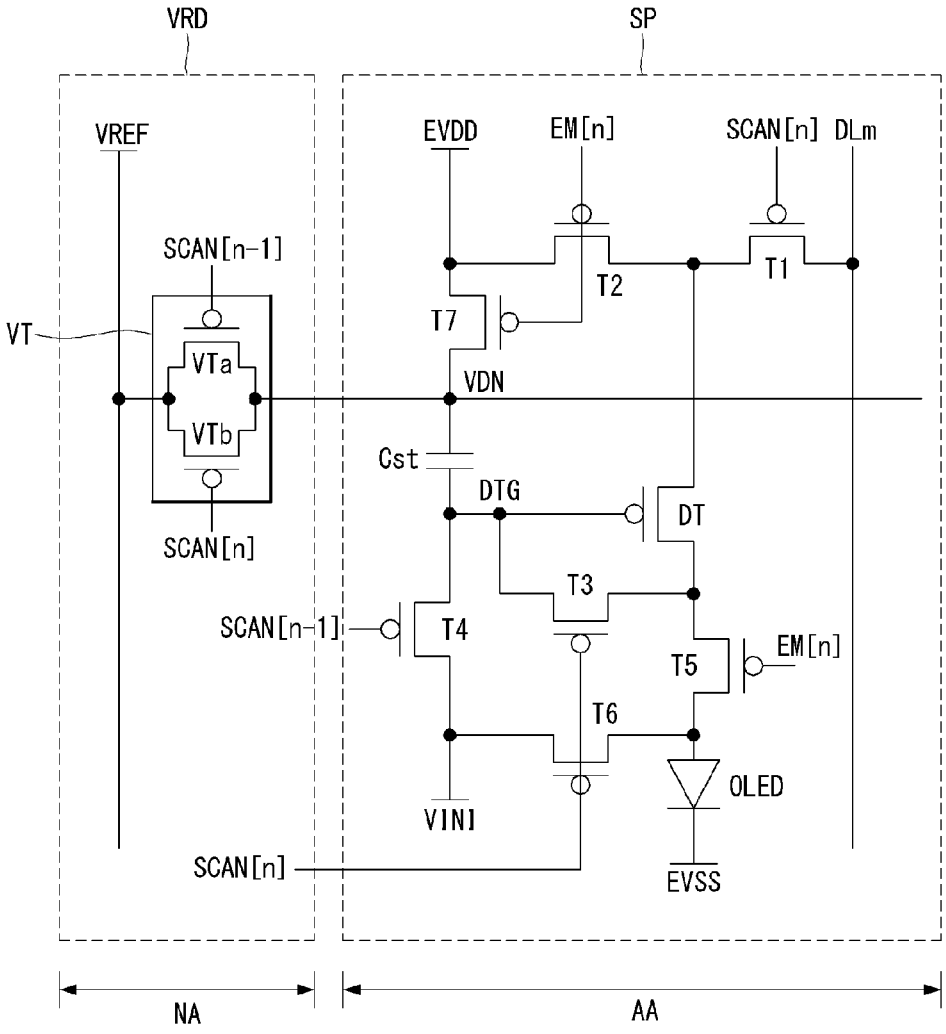
VRD
SP
VREF
EVDD
EM[n]
SCAN[n]
DLm
SCAN[n-1]
T2
T1
T7
VT
VTa
VDN
VTb
Cst
DTG
DT
SCAN[n]
T3
SCAN[n-1]
T4
EM[n]
T5
T6
OLED
VINI
SCAN[n]
EVSS
NA
AA

Fig. 9

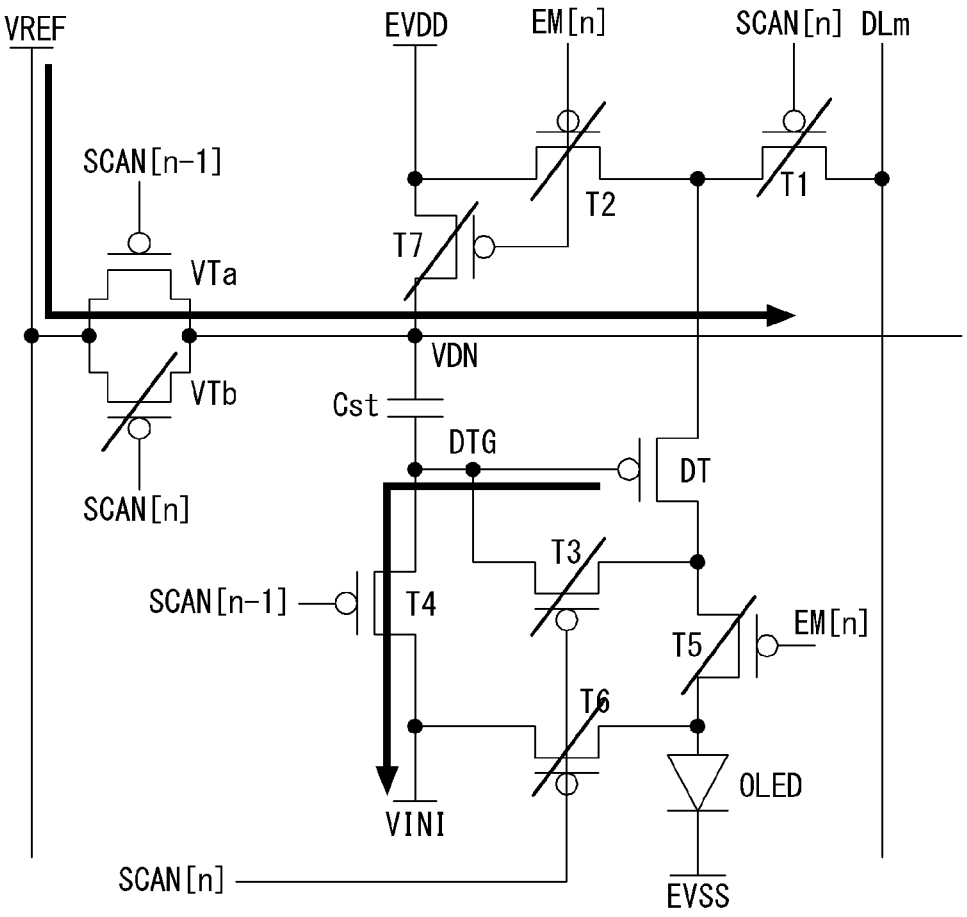
VREF
EVDD
EM[n]
SCAN[n]
DLm
SCAN[n-1]
T2
T1
T7
VTa
VDN
VTb
Cst
DTG
DT
SCAN[n]
T3
SCAN[n-1]
T4
EM[n]
T5
T6
OLED
VINI
SCAN[n]
EVSS

Fig. 10

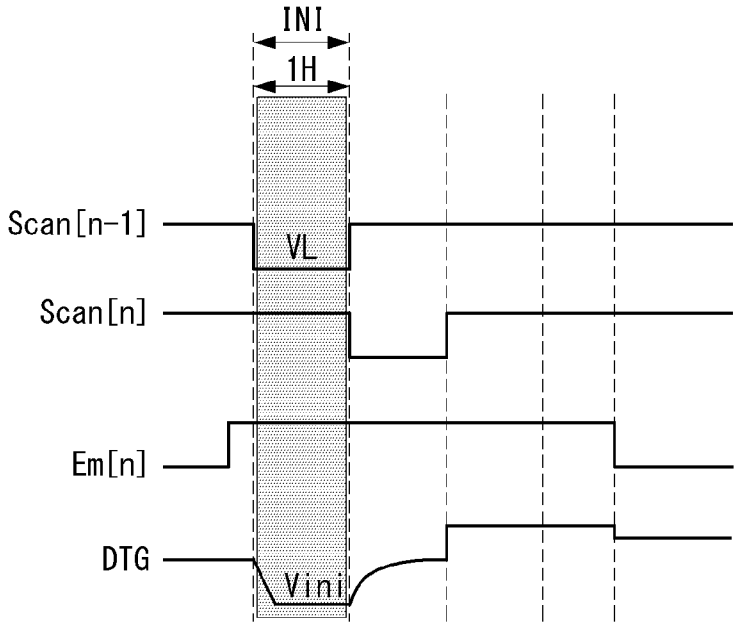
INI
1H
Scan[n-1]
VL
Scan[n]
Em[n]
DTG
Vini

Fig. 11

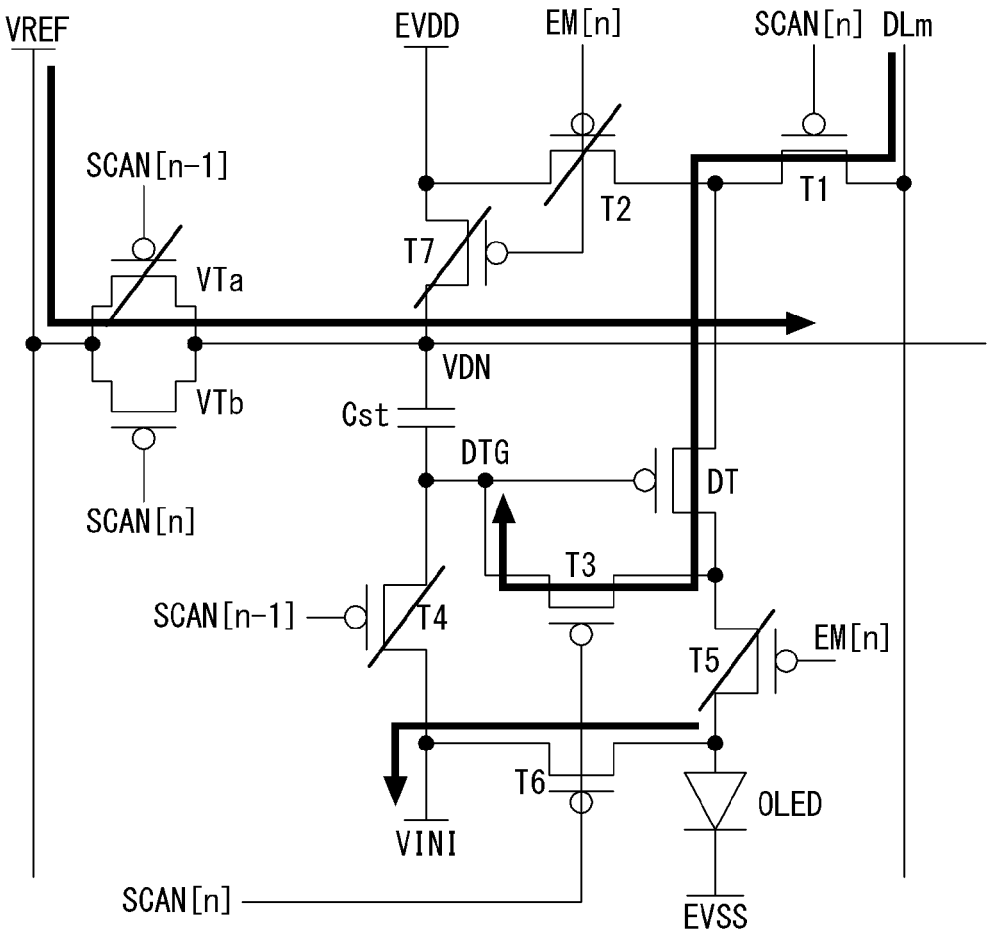
VREF
EVDD
EM[n]
SCAN[n]
DLm
SCAN[n-1]
T2
T1
T7
VTa
VDN
VTb
Cst
DTG
DT
SCAN[n]
T3
SCAN[n-1]
T4
T5
EM[n]
T6
OLED
VINI
SCAN[n]
EVSS

Fig. 12

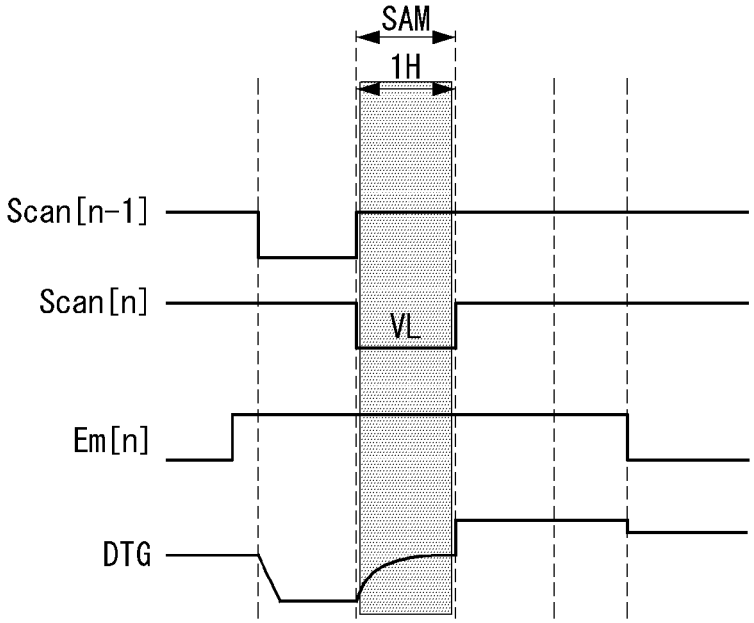
SAM
1H
Scan[n-1]
Scan[n]
VL
Em[n]
DTG

Fig. 13

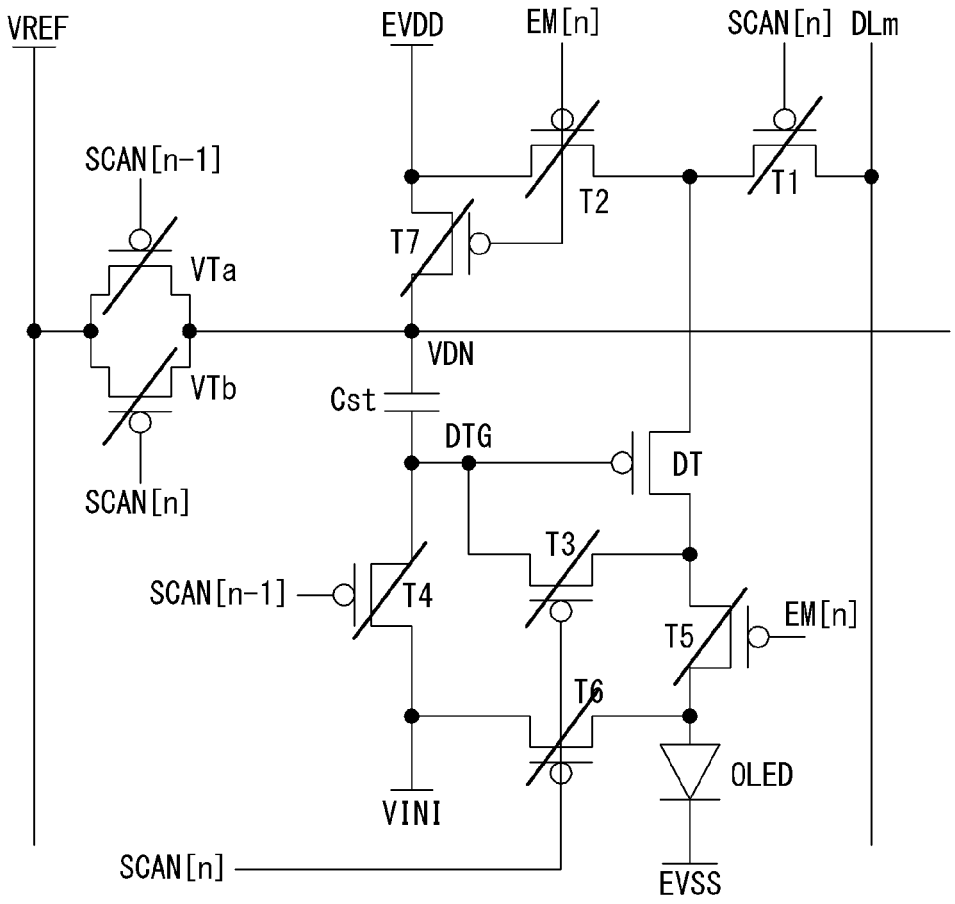
VREF
EVDD
EM[n]
SCAN[n]
DLm
SCAN[n-1]
T2
T1
T7
VTa
VDN
VTb
Cst
DTG
DT
SCAN[n]
T3
SCAN[n-1]
T4
EM[n]
T5
T6
OLED
VINI
SCAN[n]
EVSS

Fig. 14

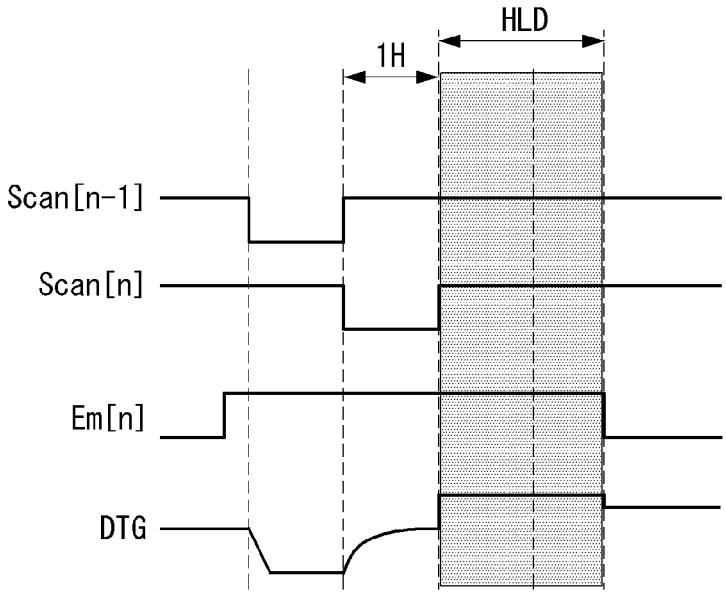
HLD
1H
Scan[n-1]
Scan[n]
Em[n]
DTG

Fig. 15

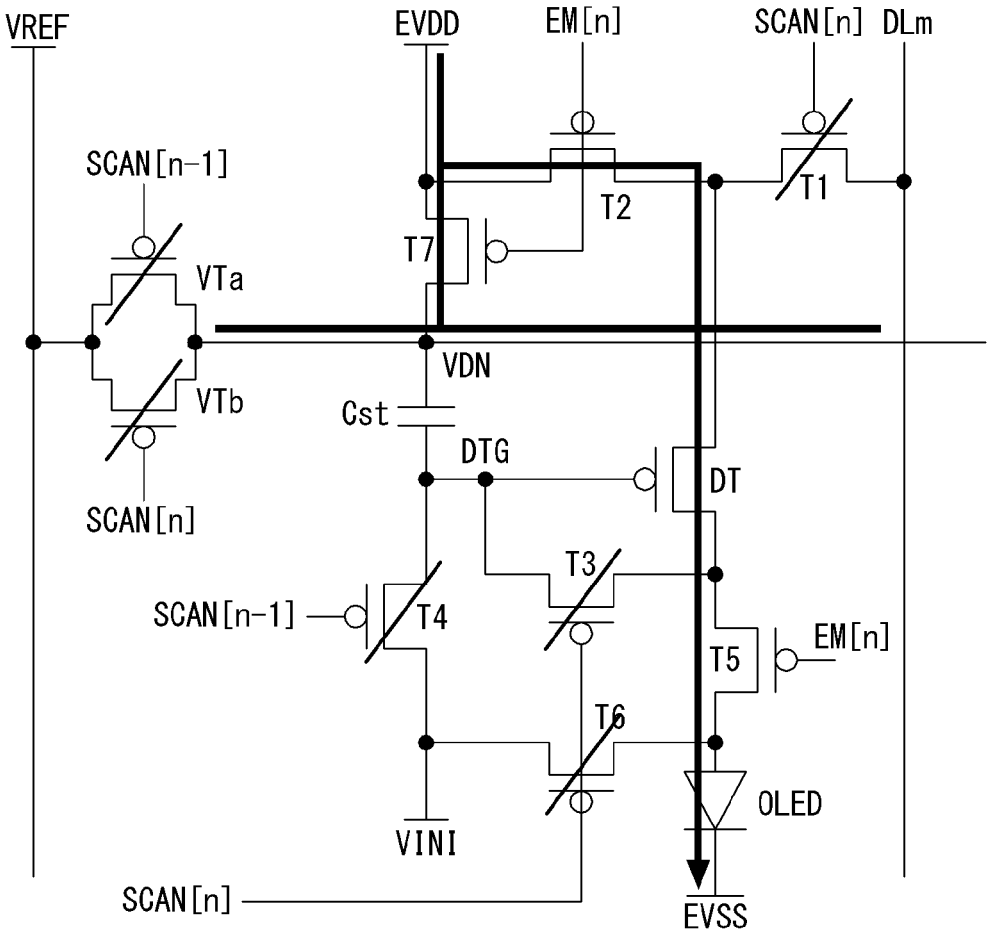
VREF
EVDD
EM[n]
SCAN[n]
DLm
SCAN[n-1]
T1
T2
T7
VTa
VDN
VTb
Cst
DTG
DT
SCAN[n]
T3
SCAN[n-1]
T4
EM[n]
T5
T6
OLED
VINI
SCAN[n]
EVSS

Fig. 16

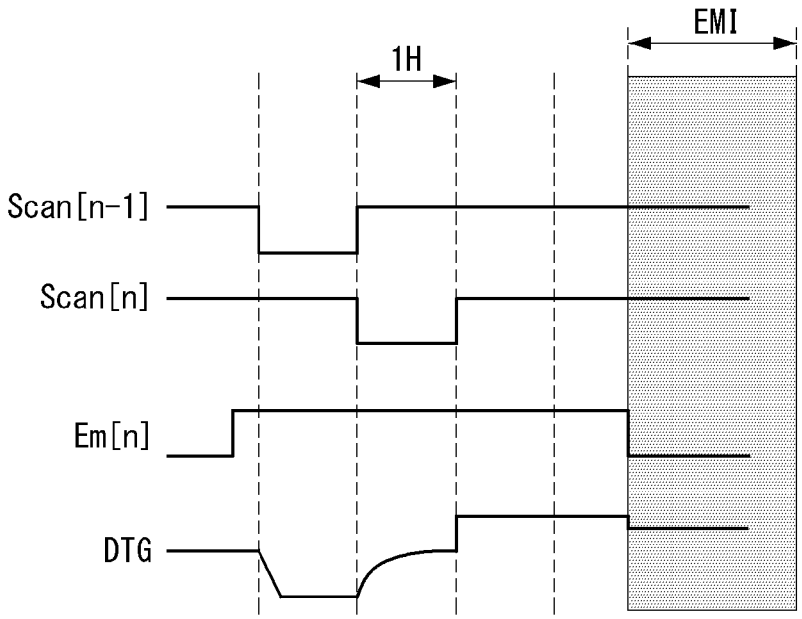
EMI
1H
Scan[n-1]
Scan[n]
Em[n]
DTG

Fig. 17

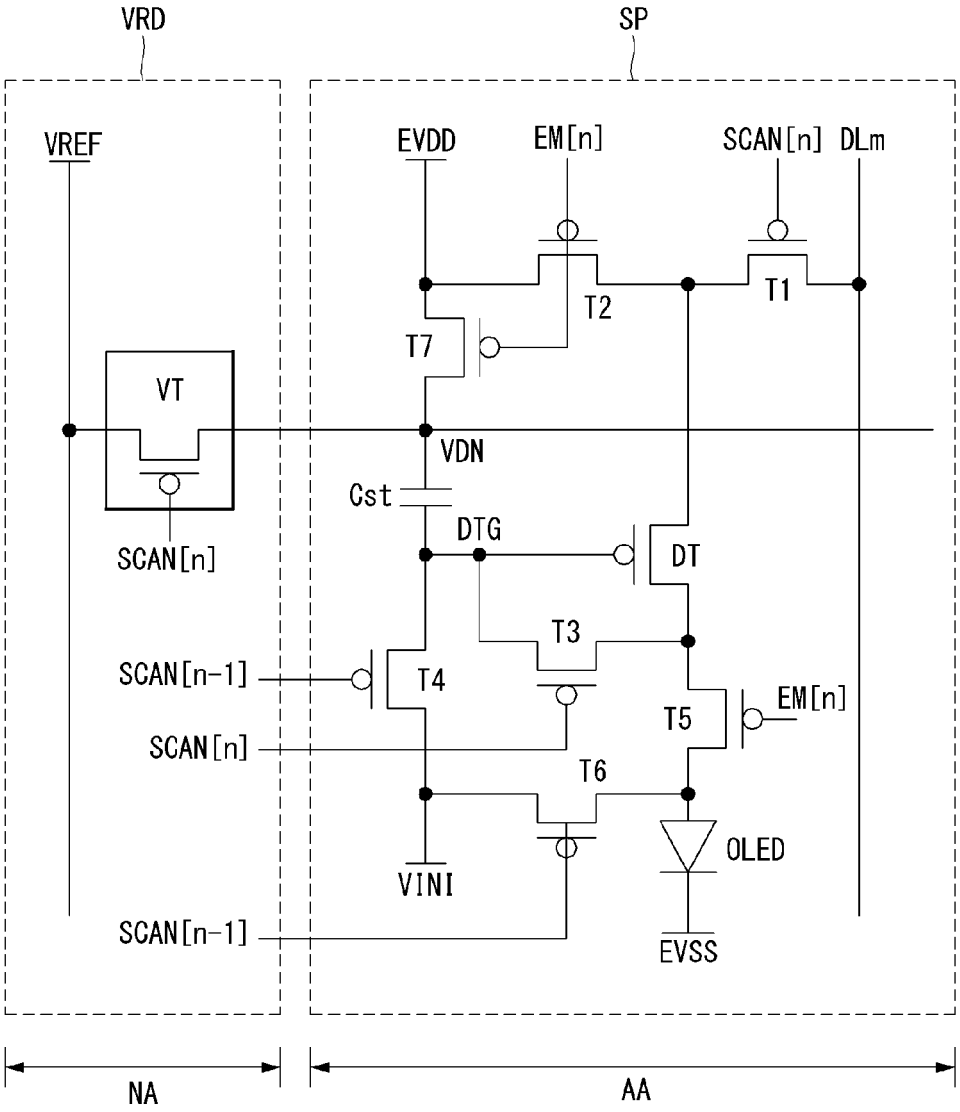
VRD
SP
VREF
EVDD
EM[n]
SCAN[n]
DLm
T1
T2
T7
VT
VDN
Cst
DTG
DT
SCAN[n]
T3
SCAN[n-1]
T4
EM[n]
T5
SCAN[n]
T6
OLED
VINI
SCAN[n-1]
EVSS
NA
AA

Fig. 18

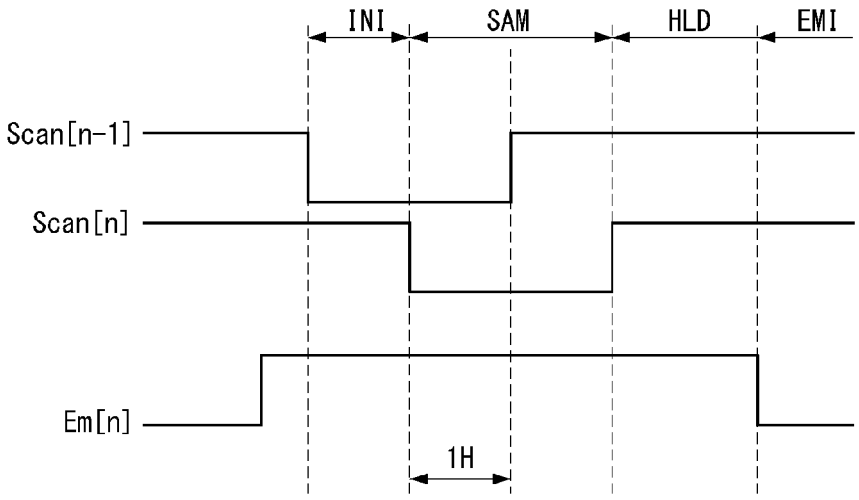
INI
SAM
HLD
EMI
Scan[n-1]
Scan[n]
Em[n]
1H

Fig. 19

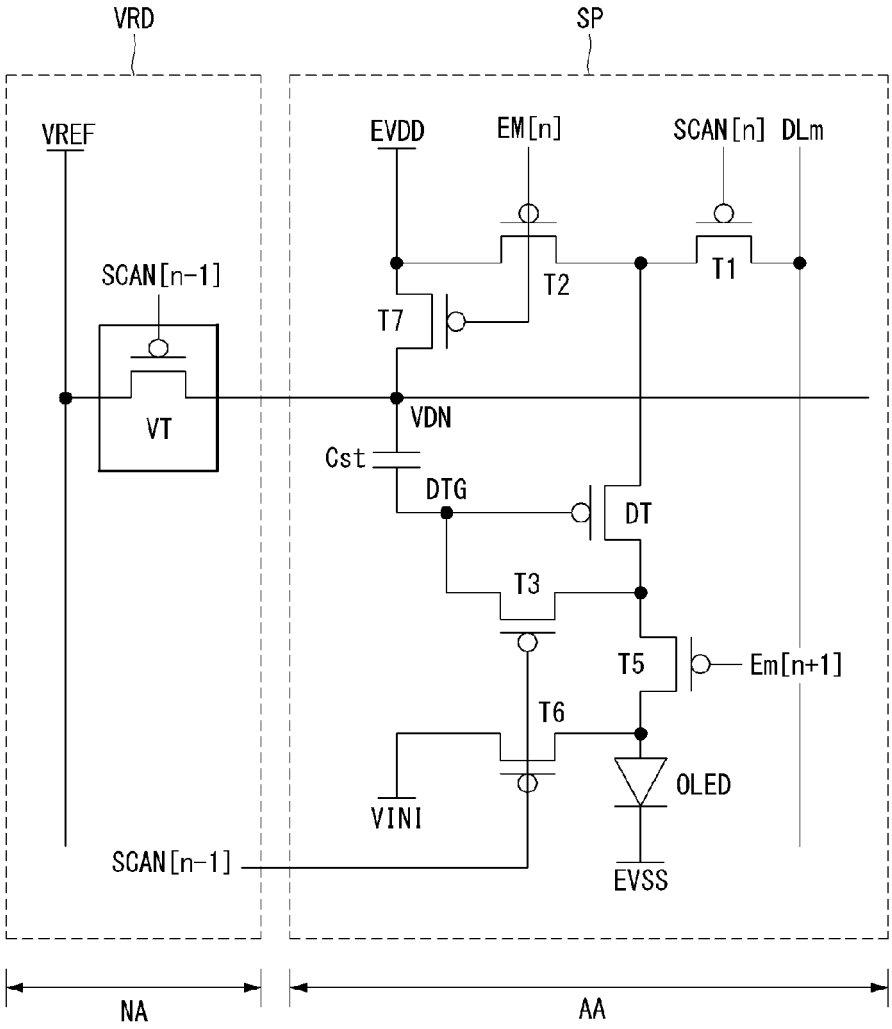
VRD
SP
VREF
EVDD
EM[n]
SCAN[n]
DLm
SCAN[n-1]
T2
T1
T7
VT
VDN
Cst
DTG
DT
T3
T5
Em[n+1]
T6
OLED
VINI
SCAN[n-1]
EVSS
NA
AA

Fig. 20

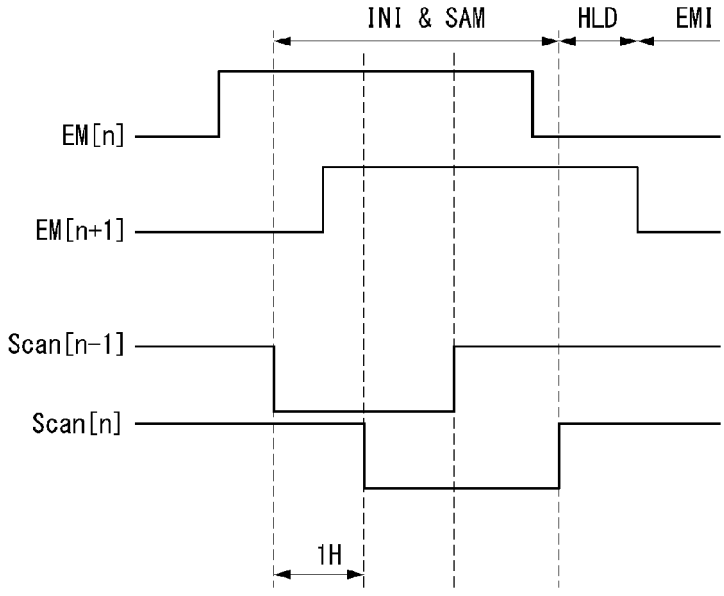
INI & SAM
HLD
EMI
EM[n]
EM[n+1]
Scan[n-1]
Scan[n]
1H

Fig. 21

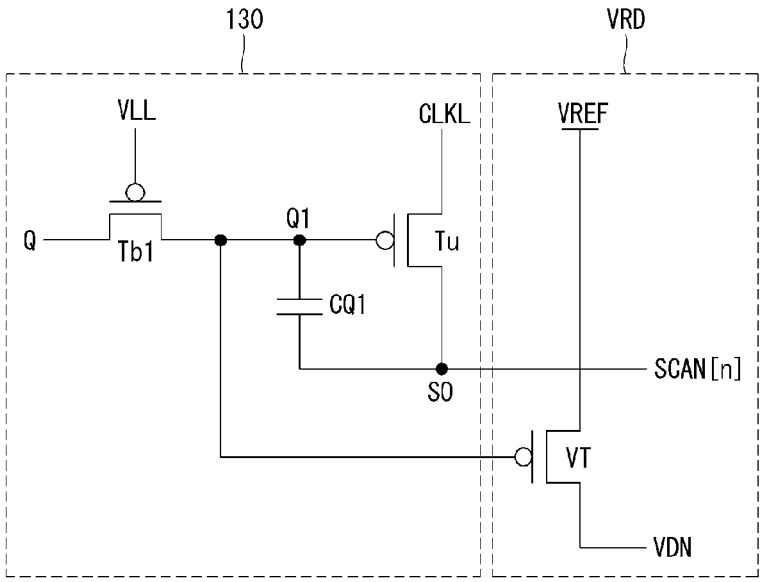
130
VRD
VLL
CLKL
VREF
Q
Tb1
Q1
Tu
CQ1
SCAN[n]
SO
VT
VDN

Fig. 22

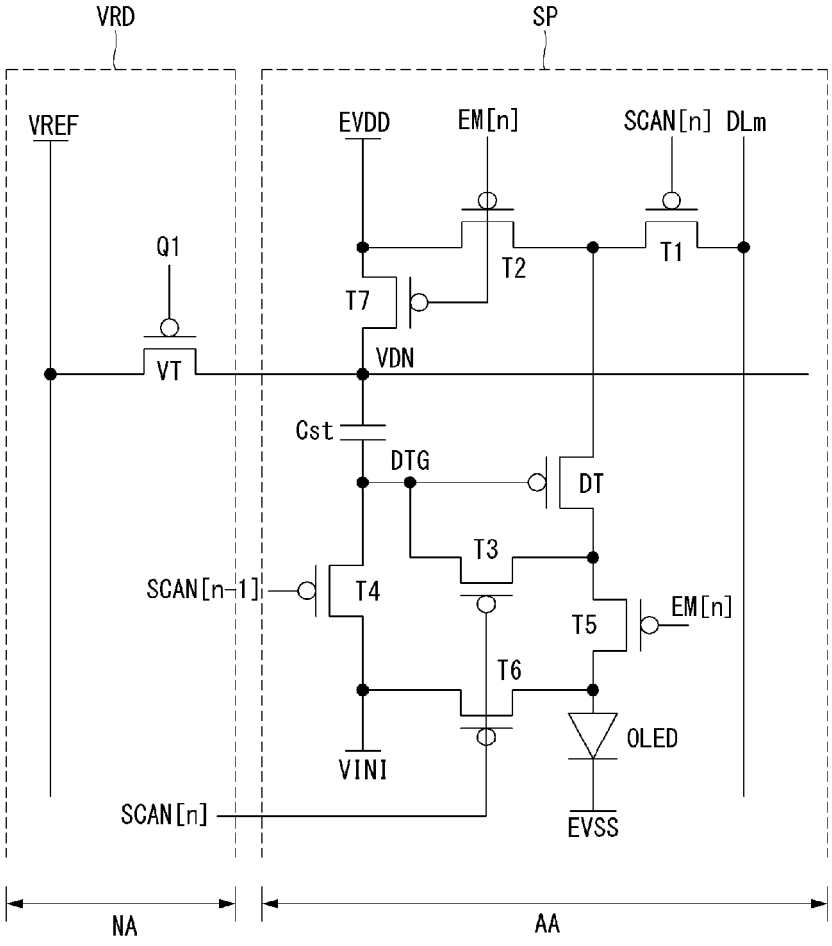
VRD
SP
VREF
EVDD
EM[n]
SCAN[n]
DLm
Q1
T2
T1
T7
VT
VDN
Cst
DTG
DT
T3
SCAN[n-1]
T4
T5
EM[n]
T6
OLED
VINI
SCAN[n]
EVSS
NA
AA

Fig. 23A

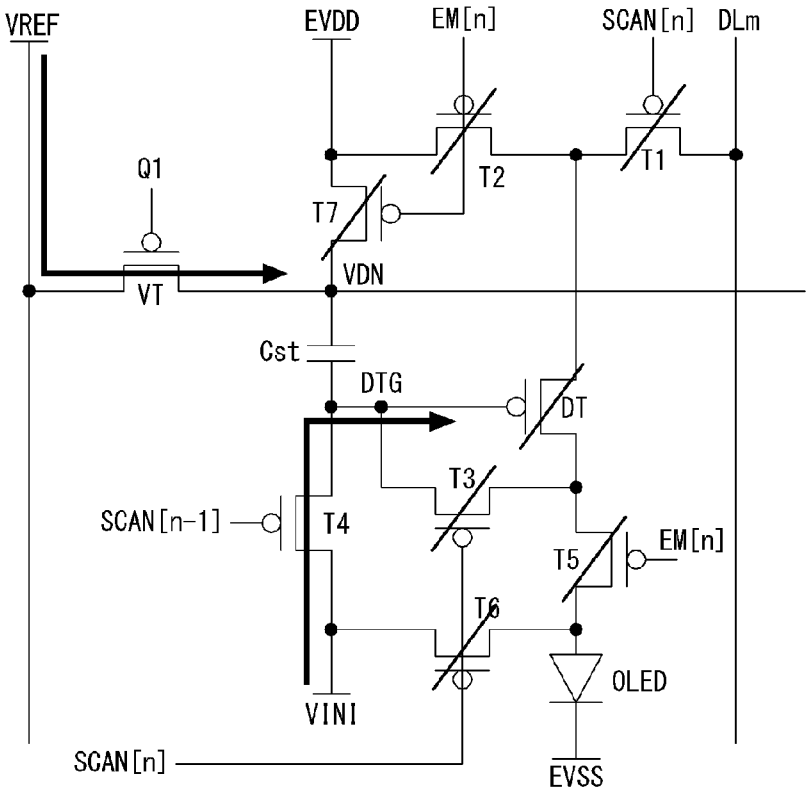

Fig. 23B

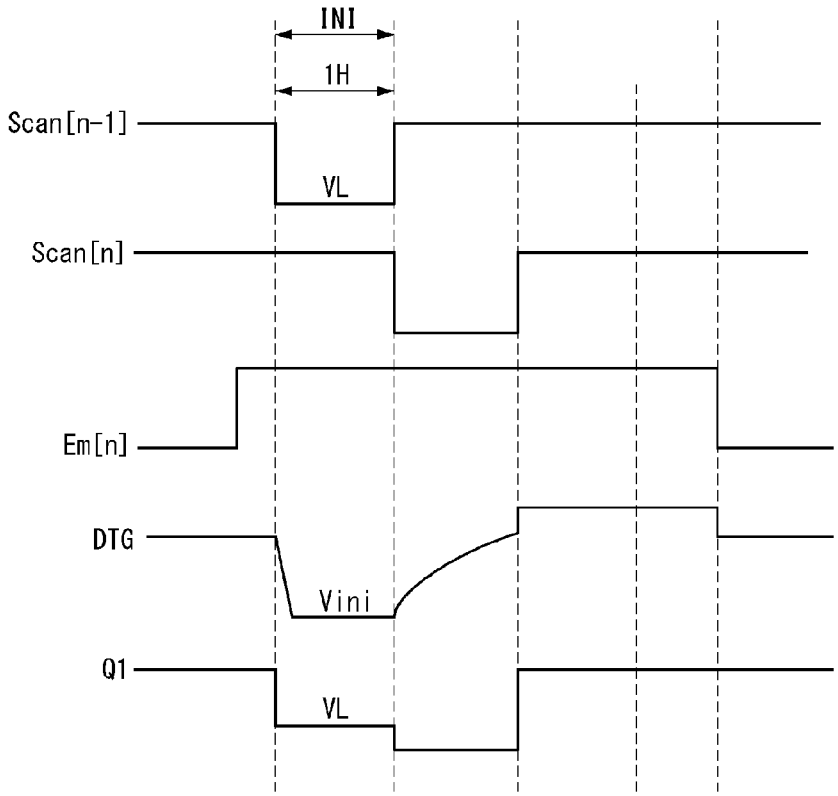

Fig. 24A

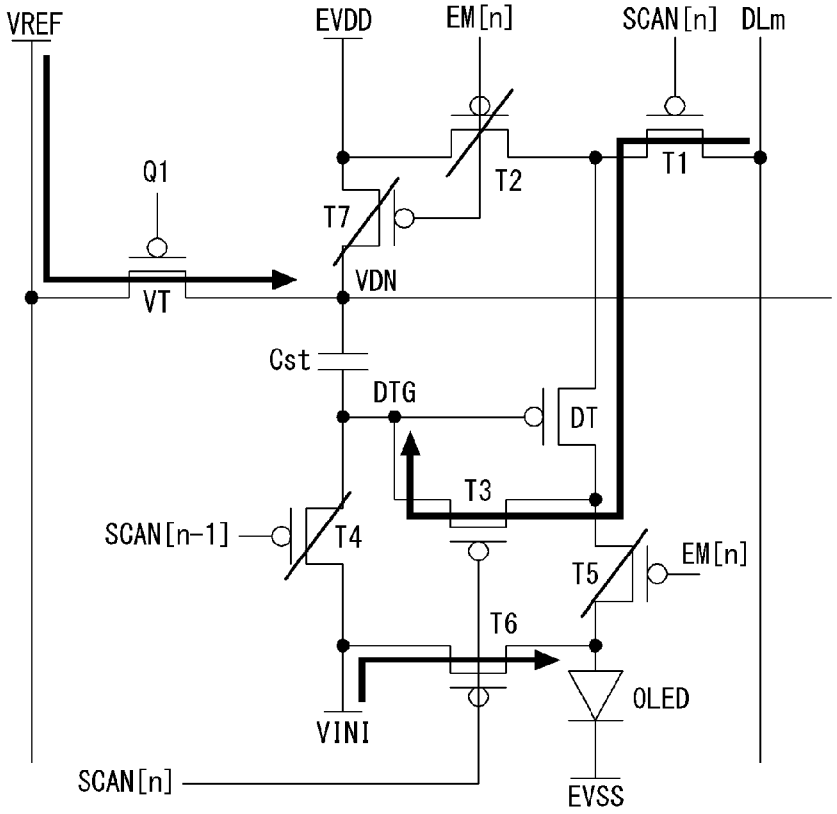

Fig. 24B

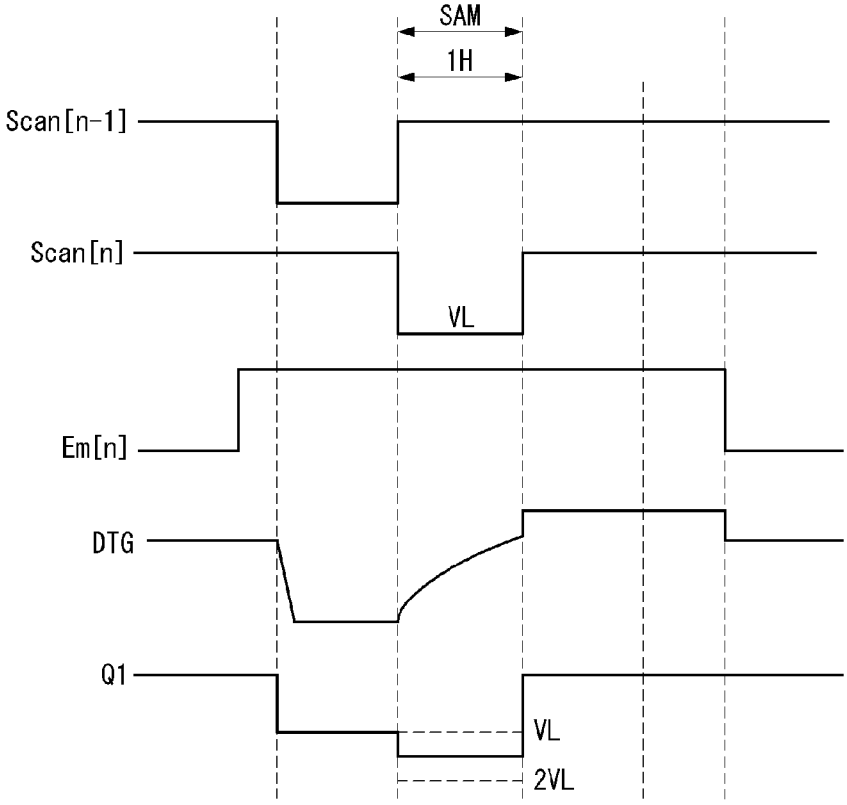

Fig. 25A

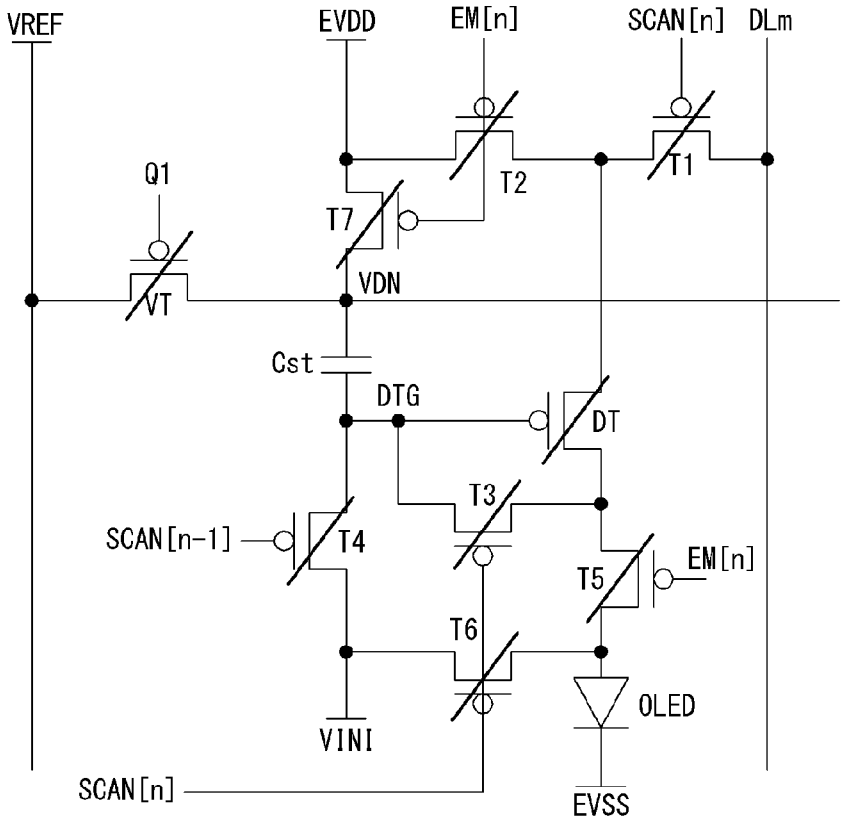

Fig. 25B

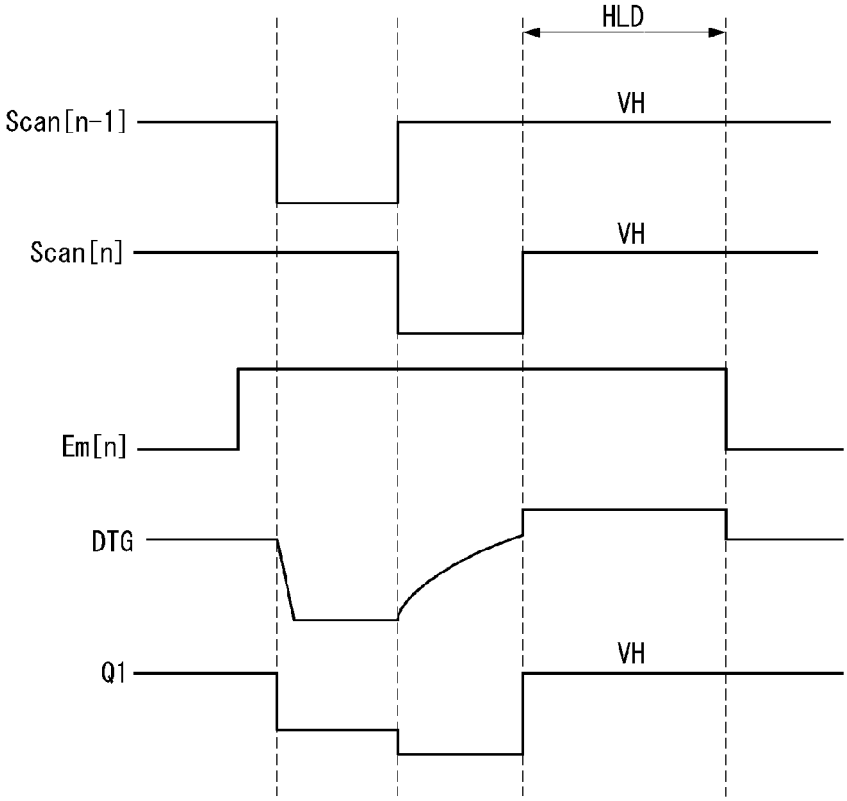

Fig. 26A

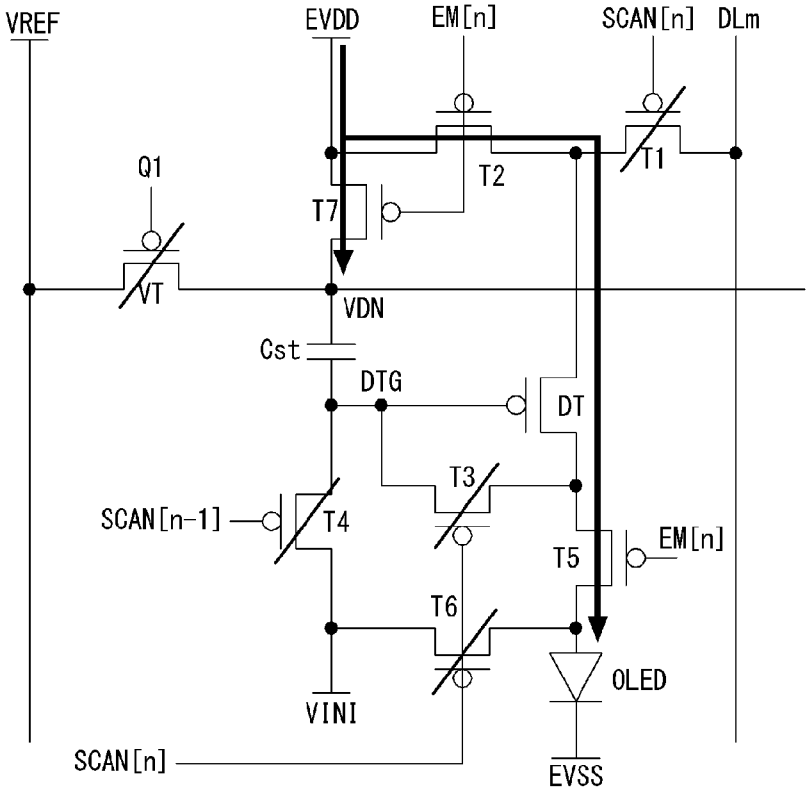

Fig. 26B

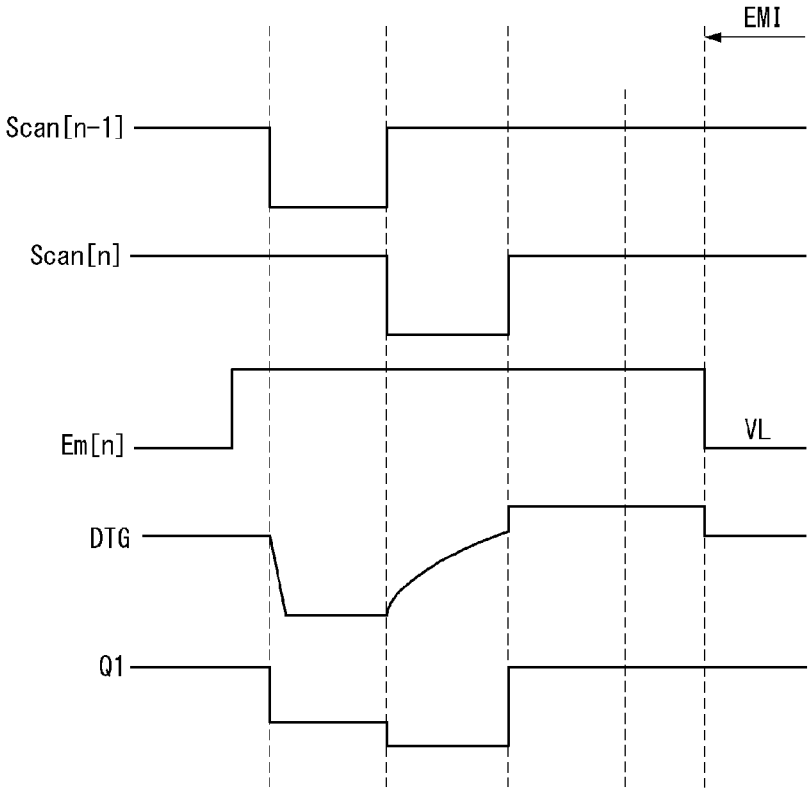

Fig. 27

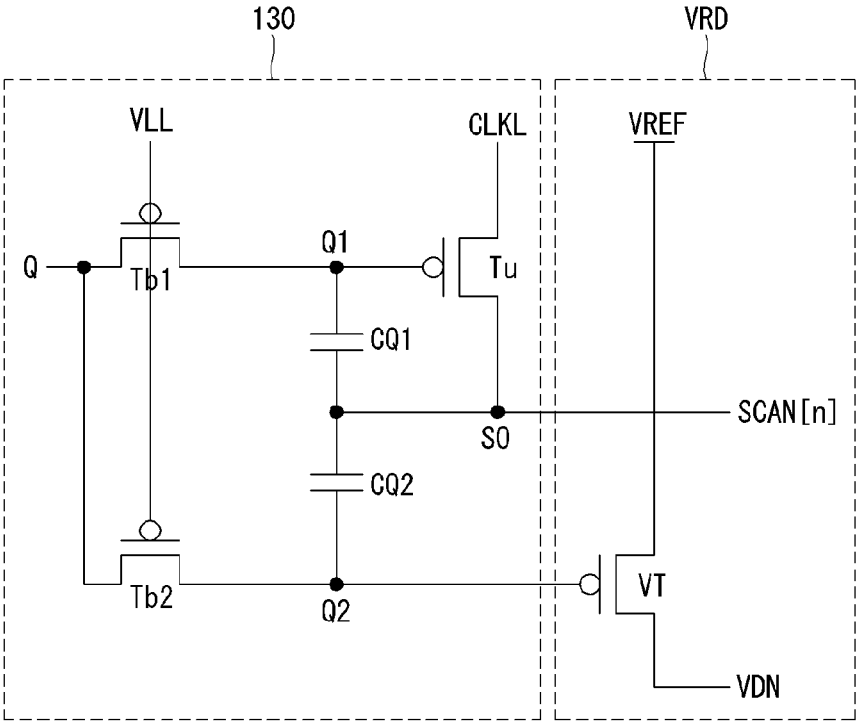
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Fig. 28

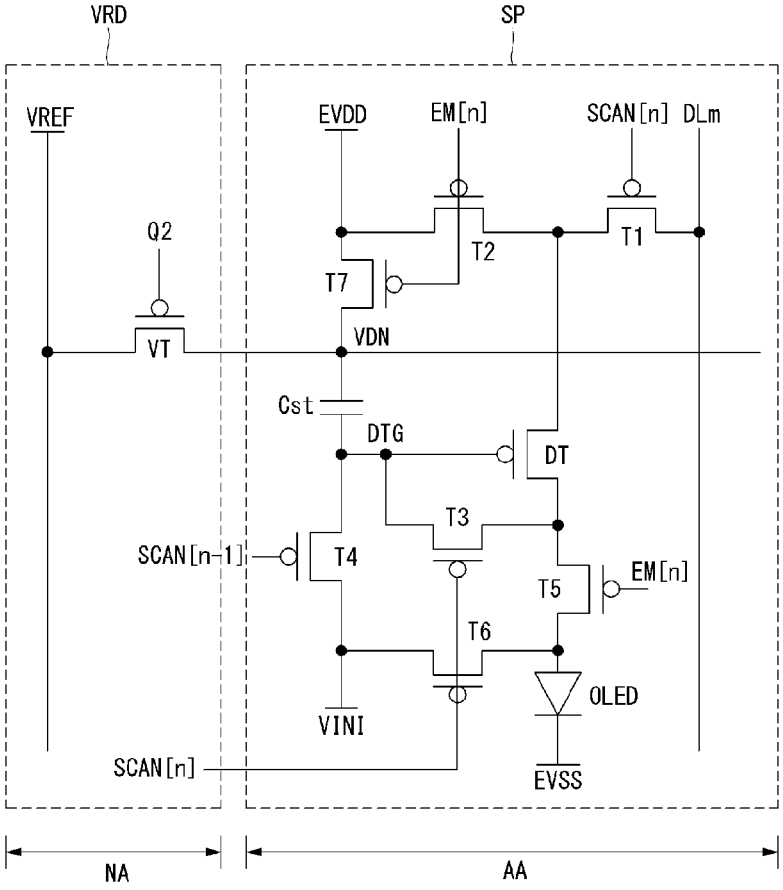
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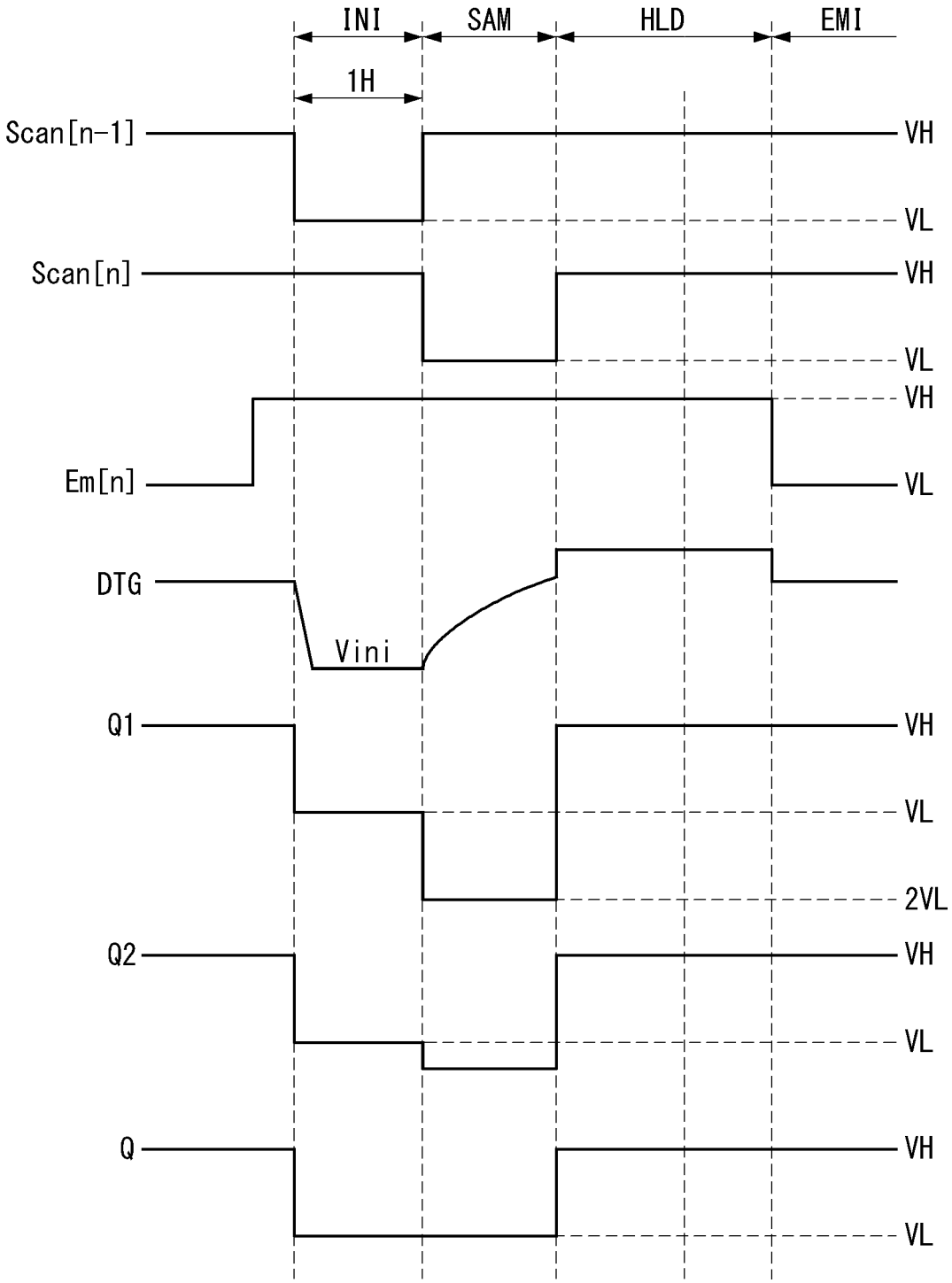
Fig. 29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EUROPEAN SEARCH REPORT

Application Number
EP 18 19 1531

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X A	US 2013/328753 A1 (TSUGE HITOSHI [JP]) 12 December 2013 (2013-12-12) * paragraphs [0001], [0033], [0092] - [0099]; figures 1,2,3A,9 * -----	1-10, 12-15 11	INV. G09G3/3233 ADD. G09G3/3266
X A	US 2016/104423 A1 (PARK KYONG TAE [KR] ET AL) 14 April 2016 (2016-04-14) * paragraphs [0052], [0067], [0079] - [0081]; figures 1,2,3,6,7 * -----	1-10, 12-15 11	
X	US 2017/213506 A1 (SHIBUSAWA MAKOTO [JP] ET AL) 27 July 2017 (2017-07-27) * paragraph [0064]; figures 1,2,6,7 * -----	1	
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TECHNICAL FIELDS SEARCHED (IPC)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	14 January 2019	Pichon, Jean-Michel

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14-01-2019

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专利名称(译)	电致发光显示装置及其驱动方法		
公开(公告)号	EP3451321A1	公开(公告)日	2019-03-06
申请号	EP2018191531	申请日	2018-08-29
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KIM JAESUNG YOO JUHNSUK KIM JUNGCHUL KONG CHUNGSIK SHIN MIHEE		
发明人	KIM, JAESUNG YOO, JUHNSUK KIM, JUNGCHUL KONG, CHUNGSIK SHIN, MIHEE		
IPC分类号	G09G3/3233 G09G3/3266		
CPC分类号	G09G3/3266 G09G3/3233 G09G3/3258 G09G3/3291 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2300/0876 G09G2310/0251 G09G2310/06 G09G2320/0233 G09G2320/045 G09G2330/025 H01L27/3265 H01L27/3276 H01L51/5206 H01L51/5221		
审查员(译)	PICHON , JEAN-MICHEL		
优先权	1020170111225 2017-08-31 KR 1020170135720 2017-10-19 KR		
外部链接	Espacenet		

摘要(译)

提供一种电致发光显示装置，包括：显示区域，其具有显示图像的显示区域（AA）;以及不显示图像的非显示区域（NA）;位于显示区域中的子像素（SP），以及电压传输部分（VRD）位于非显示区域中，并响应于从显示面板外部施加的信号或在显示面板上产生的信号将参考电压（VREF）传输到子像素。

Fig. 6