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(54) **Hermetically sealed isolated OLED pixels**

(57) A novel thin film encapsulated OLED panel architecture (50) and a method for making the panels with improved shelf life is disclosed. The OLED panel (50) consists of a plurality of OLED pixels; each OLED pixel is individually hermetically sealed and isolated from its neighboring pixels. The organic stack (53) of the OLED pixel is contained within its own hermetically sealed structure, achieved by making the structure on a barrier coated substrate (55) and using a first barrier material as the

grid (52) and a second barrier (56) for encapsulating the entire OLED pixel. The first barrier material (52) provides the edge seal while the second barrier (56) disposed over the pixel provides protection from top down moisture diffusion. By isolating and hermetically sealing individual pixels; any damage such as moisture and oxygen ingress due to defects or particles, delamination, cracking etc. can be effectively contained within the pixel thereby protecting other pixels in the panel.

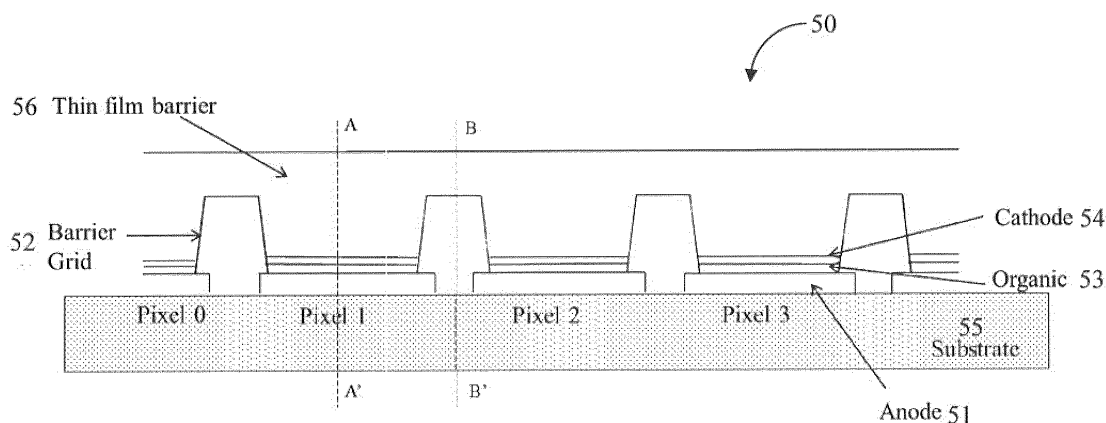


Figure 5

Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit under 35 U.S.C. 119(e) of a U.S. provisional patent application of Siddharth Harikrishna Mohan et al., entitled "Hermetically Sealed Isolated OLED Pixels", Serial No. 61/970,937, filed March 27, 2014, the entire contents of said application being incorporated herein by reference.

JOINT RESEARCH

[0002] The claimed invention was made by, on behalf of, and/or in connection with one or more of the following parties to a joint university corporation research agreement: Regents of the University of Michigan, Princeton University, The University of Southern California, and the Universal Display Corporation. The agreement was in effect on or before the effective filing date of the claimed invention, and the claimed invention was made as a result of activities undertaken within the scope of the agreement.

FIELD OF THE INVENTION

[0003] The present invention relates generally to the fabrication of high efficiency OLED devices and more specifically, to the fabrication of OLED panels wherein each OLED pixel of the panel is individually hermetically sealed and isolated from its neighboring pixels.

BACKGROUND

[0004] Organic light-emitting diode (OLED) displays and lighting panels need reliable protection from atmospheric gases, in particular moisture and oxygen. Conventionally protection is provided by encapsulating the OLEDs and a desiccant between two glass plates, which are sealed around the edge with an adhesive. This traditional encapsulation method makes the display rigid and hence cannot be used for encapsulating flexible OLEDs. To make OLED displays and lighting panels flexible and lightweight, thin film encapsulation must be used instead of rigid glass plates. Flexible OLED display and lighting panels fabricated on polymeric substrates such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN), require moisture protection on both the top side and bottom side of the device as the substrates have poor moisture barrier properties. For example, the water vapor transmission rate (WVTR) of 100 μm thick PET is approximately 3.9 and 17 $\text{g}/\text{m}^2/\text{day}$ at 37.8 C and 40 C respectively. The most widely quoted value for required water vapor transmission rate (WVTR) for an OLED lifetime of 10000 h is 10^{-6} $\text{g}/\text{m}^2/\text{day}$. Similarly, required oxygen transmission rate (OTR) for similar lifetimes has been reported as anywhere from to 10^{-5} $\text{cm}^3/\text{m}^2/\text{day}$ to 10^{-3} $\text{cm}^3/\text{m}^2/\text{day}$ (Lewis and Weaver).

[0005] Thin film encapsulation has been demonstrated for encapsulating substrates and electronics devices. Patent number US 6,548,912 B1 teaches the use of 'multiple' barrier stacks/dyads to encapsulate moisture sensitive devices (such as OLEDs) and substrates. Each barrier stack or "dyad" consists of an inorganic material/polymer layer pair. Patent number US 7,015,640 B2 discloses the use of a graded composition diffusion barrier to encapsulate OLED and substrates. In this method, multiple alternate layers of $\text{SiO}_x\text{N}_y/\text{SiO}_x\text{C}_y$ are deposited at room temperature by PECVD. A single hybrid barrier layer can be grown by plasma enhanced chemical vapor deposition (PECVD) of an organic precursor with a reactive gas such as oxygen, e.g., HMDSO/ O_2 . The barrier coating process is described in Patent number US 7,968,146 B2. The barrier film is highly impermeable yet flexible. This material is a hybrid of inorganic SiO_2 and polymeric silicone that is deposited at room temperature. The barrier film has permeation and optical properties of glass, but with a partial polymer character that gives a thin barrier film a low permeability and flexibility.

[0006] A typical thin film encapsulated OLED panel on a rigid substrate such as glass or metal foil is shown in Figure 1. The panel 10 of Figure 1 consists of a first electrode (anode) 11, insulating grid 12, an organic stack 13 and a second electrode (cathode) 14 between a substrate 15 and a thin film barrier 16. The anode 12 is typically a transparent conductive oxide having a high work function such as indium tin-oxide (ITO) or indium zinc oxide (IZO). The sheet resistance is typically in the range of 10-100 Ohm/square for a thickness range of 50-200 nm. This is in contrast to metal with a sheet resistance <1 Ohm/square, which is often used for the reflective cathode. High sheet resistance of the anode can result in brightness non-uniformity, which becomes more evident when scaling to large-area light panels. In order to improve uniformity, highly-conductive metal bus lines may be deposited in electrical contact with the TCO electrode to provide improved current distribution across the panel 20 as shown in Figure 2. The panel 20 of Figure 2 consists of a first electrode (anode) 21, insulating grid 22, an organic stack 23 and a second electrode (cathode) 24 between a substrate 25 and a thin film barrier 26. The insulating grid 22 is usually disposed over a portion of the first electrode (anode) 21, as shown in Figure 1 to define the active area. Additionally, insulating grid layer 22 is required to cover the bus lines 27 to prevent electrical shorting occurring between the bus lines 27 and the second electrode (cathode) 24. Polymer materials such as polyimide and inorganic insulating materials such as SiO_2 or Si_3N_4 are conventionally used as grids in active and passive matrix organic light emitting diode devices. The conventional way to pattern metal bus lines is through photolithography. In some device architectures, organic materials evaporated through a conventional shadow mask have also been used as insulating grids. The organic stack is comprised of several layers including a hole injecting layer (HIL), hole transporting

layer (HTL), emissive layer (EML), blocking layer (BL), and electron injecting layer (EIL). The organic layers are usually deposited by conventional vacuum thermal evaporation (VTE) method. Typically the emissive layers are patterned using a shadow mask to obtain RGB sub-pixels, while the transport layers are "blanket" deposited. In other device architectures such as micro cavity OLEDs, one or more injection/transport layers may be patterned to obtain maximum efficiency. During blanket deposition, organic material gets deposited on top and the sidewalls (depending upon the shape of the grid) of the insulating grid. The cathode is subsequently deposited on the organic stack to complete the device. Barrier films are deposited on top to hermetically seal the OLED panel.

[0007] A typical thin film encapsulated OLED panel on a flexible polymer substrate such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN) is shown in Figures 3 and 4. The panel structure is similar to a rigid substrate except for the addition of thin film barrier either on the top side of the substrate (prior to anode) or the bottom side of the substrate. These thin film barriers are required on the substrate side of the panel to protect the device from moisture. In the architecture shown in Figure 3, the barrier 37 is disposed on the back side of the substrate 35. The panel 30 of Figure 3 consists of a first electrode (anode) 31, insulating grid 32, an organic stack 33 and a second electrode (cathode) 34 between a substrate 35 and a thin film barrier 36. The barrier 37 is disposed on the back side of the substrate 35. In Figure 4, the panel 40 consists of a first electrode (anode) 41, insulating grid 42, an organic stack 43 and a second electrode (cathode) 44 between a substrate 45 and a thin film barrier 46. The barrier 47 is disposed on top of the substrate 45 before the anode 41.

[0008] Although, the above (current technology) thin film encapsulated OLED device architectures shown in Figures 1-4 have been demonstrated, these panels are not robust against any "damages". "Damages" may include defects/particles, pin holes, delamination/cracks induced during flexing or cutting the panel etc. For example, if a defect or a particle embedded in the pixel or the polymer grid penetrates the thin film barrier deposited on top of the device, moisture from the atmosphere will spread across the panel as both organic and polymer materials are highly permeable to moisture. This would eventually lead to dark spots and a dead panel. In addition, insulating grids made from polymer materials such as polyimide can be a reservoir of moisture themselves and may damage the OLED devices when the moisture contained within the polymer is released. If the polymer material is replaced by a low permeability material, it would not release any moisture and would prevent transfer of moisture from one pixel to other. Inorganic materials such as SiO_2 and Si_3N_4 have been used for this application. Although inorganic grids are effective, it is difficult to process them at low temperatures especially on flexible polymeric substrates. In most cases, these layers are very brittle and crack when flexed. Within the OLED

device structure, it is well known that the adhesion strength at the organic and cathode interface is weak. This interface is susceptible to delamination especially when a highly compressive barrier film is deposited over the cathode. Further, since the organic stack is blanket deposited (continuous), any local delamination/crack occurring at a weak spot in a pixel can propagate across the entire panel, especially after flexing. Similarly, damages can be induced during the cutting/shaping process of a panel, including: a) electrical short; b) delamination of the cathode and the barrier from the organic (adhesion strength of cathode to organic is very weak); and c) delamination combined with crack propagation when the panel is flexed. Additionally, a cut panel leaves exposed edges on the side that was cut. Exposed edges of organic and/or the polymer grid have no protection from moisture leading to a catastrophic failure of the panel. For example if the panel shown in Figure 3 is cut along AA'; i.e.: cutting through top barrier, cathode, organic, anode, substrate, and bottom thin film barrier, the entire panel is physically damaged and does not light up. Delamination or cracks induced by the cutting process tends to propagate across the entire panel; since the weak organic-cathode interface is continuous across the panel leading to a catastrophic failure.

[0009] To realize a long lasting panel, reliable means of preventing damage propagation and water penetration is needed after cutting. In other words, isolated hermetically sealed pixels are needed. Isolated hermetically sealed pixels can be realized by using one or more of a:

1) Barrier grid: A flexible material with good barrier property for a grid, especially for flexible display and electronic applications. This should be processed at low temperature; and

2) Isolated organic stack: The organic stack needs to be patterned and not continuous across the pixels. This will prevent delamination/crack propagation as organic-cathode regions are eliminated.

BRIEF SUMMARY

[0010] According to embodiments of the disclosed subject matter, a system and method is provided to substantially address the problems associated with the prior art and provide for the fabrication of high efficiency OLED devices and more specifically, to the fabrication of OLED panels wherein each OLED pixel of the panel is individually hermetically sealed and isolated from its neighboring pixels.

[0011] Some embodiments of the disclosed subject matter disclose a novel thin film encapsulated OLED panel architecture and a method for making the panels with improved shelf life. The OLED panel consists of a plurality of OLED pixels; each OLED pixel is individually hermetically sealed and isolated from its neighboring pixels. More specifically, the organic stack of the OLED pixel is

contained within its own hermetically sealed structure. Hermetic sealing is achieved by making the structure on a barrier coated substrate and using a first barrier material as the grid and a second barrier for encapsulating the entire OLED pixel. The first barrier material provides the edge seal while the second barrier disposed over the pixel provides adequate protection from top down moisture diffusion. By isolating and hermetically sealing individual pixels, any damage such as moisture and oxygen ingress due to defects or particles, delamination, cracking etc. can be effectively contained within the pixel thereby protecting the other pixels in the panel. Thus, a long lasting OLED lighting panel can be manufactured.

[0012] Some embodiments of the disclosed subject matter also disclose a method for making the OLED device. The focus is on choosing the barrier materials and processes for especially making the barrier grid and isolating the organic stack. Finally, some embodiments of the disclosed subject matter when experimentally tested, demonstrate the concept of hermetic sealing and an OLED device after cutting.

[0013] Although many embodiments are described above as comprising different features and/or combination of features, a person of ordinary skill in the art after reading this disclosure may understand that in some instances, one or more of these components could be combined with any of the components or features described above. That is, one or more features from any embodiment can be combined with one or more features of any other embodiment without departing from the scope of the invention. As noted previously, all measurements, dimensions, and materials provided herein within the specification or within the figures are by way of example only.

BRIEF DESCRIPTION OF THE FIGURES:

[0014] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present invention and, together with the description, further serve to explain the principles of the invention and to enable a person skilled in the pertinent art to make and use the invention.

Figure 1 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate.

Figure 2 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate. Metal bus lines are included.

Figure 3 shows a cross section of a thin film encapsulated OLED panel on a flexible polymer substrate such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN). A thin film barrier is disposed on the back side of the substrate.

Figure 4 shows a cross section of a thin film encapsulated OLED panel on a flexible polymer substrate

such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN). The thin film barrier is disposed on top of the substrate before the anode.

Figure 5 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis.

Figure 6 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis.

Figure 7 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis. The cathode is addressed through separate bus lines.

Figure 8 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis. Metal bus lines are included.

Figure 9 shows a cross section of a thin film encapsulated OLED panel containing 4 pixels on a flexible polymer substrate such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN) according to an embodiment of the disclosed subject matter. A thin film barrier is disposed on the back side of the substrate. Metal bus lines are included.

Figure 10 shows a cross section of a thin film encapsulated OLED panel containing 4 pixels on a flexible polymer substrate such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN) according to an embodiment of the disclosed subject matter. The thin film barrier is disposed on top of the substrate before the anode. Metal bus lines are included.

Figure 11 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis. The top thin film barrier is patterned.

Figure 12 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis. The top thin film barrier is patterned.

Figure 13 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing

4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis. The top thin film barrier is patterned. Metal bus lines are included.

Figure 14 shows a cross section of a thin film encapsulated OLED panel containing 4 pixels on a flexible polymer substrate such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN) according to an embodiment of the disclosed subject matter. A thin film barrier is disposed on the back side of the substrate. Metal bus lines are included. The top thin film barrier is patterned.

Figure 15 shows a cross section of a thin film encapsulated OLED panel containing 4 pixels on a flexible polymer substrate such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN) according to an embodiment of the disclosed subject matter. The thin film barrier is disposed on top of the substrate before the anode. Metal bus lines are included.

Figure 16 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis. The cathode is blanket deposited.

Figure 17 shows a cross section of a thin film encapsulated OLED panel on a rigid substrate containing 4 pixels according to an embodiment of the disclosed subject matter. AA' and BB' are the cutting axis. Cathode 1 is patterned, while cathode 2 is blanket deposited.

Figure 18 shows an architecture in which portions of the patterned cathode are deposited on the sidewalls and top of the barrier grid according to an embodiment of the disclosed subject matter.

Figure 19 shows an architecture in which portions of the patterned organic and cathode are deposited on the sidewalls and top of the barrier grid according to an embodiment of the disclosed subject matter.

Figure 20 shows an architecture in which the barrier grid is not continuous; i.e.: adjacent pixels do not share the same barrier grid, according to an embodiment of the disclosed subject matter.

Figure 21 shows an architecture in which the barrier grid is not continuous; i.e.: adjacent pixels do not share the same barrier grid and organic and cathode are deposited on the sidewalls and top of the barrier grid, according to an embodiment of the disclosed subject matter.

Figure 22 shows an architecture in which the barrier grid profile is inverted according to an embodiment of the disclosed subject matter. The inverted barrier grid acts as a secondary integrated shadow mask for organic stack isolation during deposition.

Figure 23 shows a picture of a thin film encapsulated OLED panel on a glass substrate according to an embodiment of the disclosed subject matter.

Figure 24 shows a picture of two hermetically sealed OLED pixels according to an embodiment of the disclosed subject matter.

15 DETAILED DESCRIPTION OF THE INVENTION:

[0015] Generally, an OLED comprises at least one organic layer disposed between and electrically connected to an anode and a cathode. When a current is applied, the anode injects holes and the cathode injects electrons into the organic layer(s). The injected holes and electrons each migrate toward the oppositely charged electrode. When an electron and hole localize on the same molecule, an "exciton," which is a localized electron-hole pair having an excited energy state, is formed. Light is emitted when the exciton relaxes via a photoemissive mechanism. In some cases, the exciton may be localized on an excimer or an exciplex. Non-radiative mechanisms, such as thermal relaxation, may also occur, but are generally considered undesirable.

[0016] The initial OLEDs used emissive molecules that emitted light from their singlet states ("fluorescence") as disclosed, for example, in U.S. Patent No. 4,769,292, which is incorporated by reference in its entirety. Fluorescent emission generally occurs in a time frame of less than 10 nanoseconds.

[0017] More recently, OLEDs having emissive materials that emit light from triplet states ("phosphorescence") have been demonstrated. Examples include Baldo et al., "Highly Efficient Phosphorescent Emission from Organic Electroluminescent Devices," *Nature*, Vol. 395, 151-154, 1998; ("Baldo-I") and Baldo et al., "Very high-efficiency green organic light-emitting devices based on electro phosphorescence," *Appl. Phys. Lett.*, vol. 75, No. 3, 4-6 (1999) ("Baldo-II"), which are incorporated by reference in their entirety. Phosphorescence is described in more detail in U.S. Patent No. 7,279,704 at cols. 5-6, More details on OLEDs, and the definitions described above, can be found in U.S. Patent No. 7,279,704, the entire content of which is incorporated herein by reference.

[0018] As used herein, the term "organic" includes polymeric materials as well as small molecule organic materials that may be used to fabricate organic optoelectronic devices. "Small molecule" refers to any organic material that is not a polymer, and "small molecules" may actually be quite large. Small molecules may include repeat units in some circumstances. For example, using a long chain alkyl group as a substituent does not remove

a molecule from the "small molecule" class. Small molecules may also be incorporated into polymers, for example as a pendent group on a polymer backbone or as a part of the backbone. Small molecules may also serve as the core moiety of a dendrimer, which consists of a series of chemical shells built on the core moiety. The core moiety of a dendrimer may be a fluorescent or phosphorescent small molecule emitter. A dendrimer may be a "small molecule," and it is believed that all dendrimers currently used in the field of OLEDs are small molecules.

[0019] As used herein, "top" means furthest away from the substrate, while "bottom" means closest to the substrate. Where a first layer is described as "disposed over" a second layer, the first layer is disposed further away from substrate. There may be other layers between the first and second layer, unless it is specified that the first layer is "in contact with" the second layer. For example, a cathode may be described as "disposed over" an anode, even though there are various organic layers in between.

[0020] In embodiments of the current invention, a novel thin film encapsulated OLED panel architecture and a method for making the panels with improved shelf life is disclosed. The OLED panel consists of a plurality of OLED pixels; each OLED pixel is individually hermetically sealed and isolated from its neighboring pixels. More specifically, the organic stack of the OLED pixel is contained within its own hermetically sealed structure. Hermetic sealing is achieved by making the structure on a barrier coated substrate and using a first barrier material as the grid and a second barrier for encapsulating the entire OLED pixel. The first barrier material provides the edge seal while the second barrier disposed over the pixel provides adequate protection from top down moisture diffusion. By isolating and hermetically sealing individual pixels; any damage such as moisture and oxygen ingress due to defects or particles, delamination, cracking etc. can be effectively contained within the pixel thereby protecting the other pixels in the panel. The advantage of patterning the organic stack and cathode layout into pixels is to enable cutting tolerance, especially for flexible OLED panels. It is commonly known that when organic and cathode materials are exposed to ambient environment, the materials will degrade or delaminate. On the other hand, anode materials such as ITO or IZO, bus lines that use gold, and grids that use inorganic dielectric are stable in the air environment. Therefore, as long as organic and cathode materials are well protected from exposure to air, the device should retain its shelf lifetime. In order to maintain the lifetime of a thin film encapsulated panel during cutting, the organic and cathode layer of each pixel needs to be isolated from neighboring pixel cathode layers, so that the exposure to ambient environment (moisture, and oxygen) of one pixel will not propagate to the others. Therefore, if the panel is cut, only the pixels, or partial pixels of the cut edge, will degrade in air, but the rest of the panel will still be hermetically sealed.

[0021] Embodiment 1: (Patterned organic and cathode layer, and blanket barrier):

[0022] A cross section of one embodiment of the present invention is shown in Figure 5. The panel 50 of Figure 5 consists of a plurality of electrodes (anodes) 51, insulating grid 52, organic stacks 53 and second electrodes (cathodes) 54 between a substrate 55 and a thin film barrier 56. In this figure, a section of the OLED panel containing 3 pixels (Pixels 1, 2, 3) is shown. A lighting panel generally contains a plurality of these hermetically sealed pixels electrically connected to each other. The anode, organic stack and the cathode are patterned. Figure 6 shows another variation of the current embodiment in which the anode is continuous (not patterned). The panel 60 of Figure 6 consists of an electrode (anode) 61, insulating grid 62, organic stacks 63 and second electrodes (cathodes) 64 between a substrate 65 and a thin film barrier 66. The grid disposed over a portion of the anode is a barrier material. This barrier grid provides the required edge seal for the pixels. The organic stack is patterned in such a way that the organic material is not continuous over the entire panel. The top contact or cathode of the device will cover the organic layers and forms an electrical contact outside of the pixel footprint. This can be accomplished using vias that connect the cathode to a bus line as shown in Figure 7, or by using a cathode material that is also an excellent barrier, such as metals or certain TCO materials, such as IZO. The panel 70 of Figure 7 consists of a plurality of electrodes (anodes) 71, insulating grid 72, organic stacks 73 and second electrodes (cathodes) 74 between a substrate 75 and a thin film barrier 76. A plurality of bus lines 77 are provided between discontinuous grid portions. The entire panel is thin film encapsulated by one or more barrier materials. This barrier material will henceforth be addressed as "top barrier". The top barrier is continuous, i.e.: not patterned. In the illustrated example, the top barrier 76 is shown to be planarizing for simplicity. The top barrier may be planarizing or may be conformal. Thus, in each pixel, the top barrier material is in contact with the barrier grid material. The pixels are thus hermetically sealed and isolated.

[0023] Another variation of the current embodiment is shown in Figure 8. The panel 80 of Figure 8 consists of a plurality of electrodes (anodes) 81, insulating grid 82, organic stacks 83 and second electrodes (cathodes) 84 between a substrate 85 and a top barrier 86. A plurality of bus lines 87 are also provided. The device architecture is similar to Figure 5 except for the addition of metal bus lines 87 to improve current distribution across the panel 80. The barrier grid 82 here is disposed over the bus lines 87 to prevent electrical shorting with the cathode 84. Additionally, for flexible lighting panels fabricated on polymeric substrates such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN), thin film barriers are required on the substrate side of the panel to protect the device from moisture. Examples are shown in Figures 9 and 10. In the architecture shown in Figure

9, a thin film barrier is disposed on the back side of the substrate. The panel 90 of Figure 9 consists of a plurality of electrodes (anodes) 91, insulating grid 92, organic stacks 93 and second electrodes (cathodes) 94 between a substrate 95 and a top barrier 96. A plurality of bus lines 97 are also provided. A thin film barrier 98 is disposed on the back side of the substrate 95. In the architecture shown in Figure 10, the barrier is disposed on top of the substrate before the anode. The panel 100 of Figure 10 consists of a plurality of electrodes (anodes) 101, insulating grid 102, organic stacks 103 and second electrodes (cathodes) 104 between a substrate 105 and a top barrier 106. A plurality of bus lines 107 are also provided. A thin film barrier 108 is disposed on top of the substrate 105 before the anodes 101.

[0024] A novel aspect of the invention is hermetic sealing of individual pixels which is achieved by using a barrier grid in conjunction with an isolated organic stack. More specifically, the organic stack of the OLED pixel is contained within its own hermetically sealed structure.

[0025] Barrier grid materials according to some embodiments of the invention are patterned to isolate each organic stack of an OLED pixel and can be transparent or opaque depending on the design and application of the device. Inorganic materials such as metal oxides, metal nitrides, metal oxynitrides, metal carbides, metal oxyborides and combinations thereof can be used as a barrier grid material. Although inorganic grids are effective for rigid substrates, it is difficult to process them at low temperatures especially on flexible polymeric substrates. Further, in most cases, these layers are very brittle and crack when flexed. An alternative is to use a hybrid barrier material such as $\text{SiO}_x\text{C}_y\text{H}_z$. Some organic content may be preferred to ensure that a thick layer can be made without cracking or delamination due to defects or internal stress. This organic content may also improve the flexibility of the film. One such example is the hybrid barrier layer taught in US 7,968,146 B2. This material is a hybrid of inorganic SiO_2 and polymeric silicone. This barrier grid provides the required edge seal for the pixels. Patterning of barrier grid depends on the barrier material chosen. For example, if the hybrid material $\text{SiO}_x\text{C}_y\text{H}_z$ is chosen, patterning can be achieved by wet etching or dry etching. Dry etching methods include plasma etching, reactive ion etching (RIE), deep reactive ion etching (DRIE) etc.

[0026] Each organic stack of an OLED pixel is patterned and isolated by the barrier grid according to some embodiments of the invention, which takes into account the adhesion strength at the organic and cathode interface in an OLED is weak. This interface is susceptible to delamination especially when a highly compressive barrier film is deposited over the cathode. If the organic stack is blanket deposited (continuous), any local delamination occurring at a weak spot in a pixel can spread to other pixels. To avoid delamination/crack propagation, the organic stack is patterned in such a way that the organic material is not continuous across the entire panel. The

organic stack is thus "isolated" from its neighboring pixel. The top barrier layer deposited over this structure is in contact with the grid material forming an isolated pixel. Any local delamination/crack occurring at a weak spot in a pixel is confined to that pixel and does not spread. Thus, in each pixel the top barrier material is in contact with the barrier grid material. The pixels are thus hermetically sealed and isolated.

[0027] Referring to Figures 5 through 10, if this panel is cut along AA'; i.e.: cutting through top barrier, cathode, organic, anode, substrate, and thin film barrier (if present), can damage the pixel in few ways: a) by introducing an electrical short; b) delamination of the cathode and the barrier from the organic; and c) delamination/crack propagation when the panel is flexed. Although Pixel 1 is compromised after the cutting process, Pixels 0, 2 and 3 stay intact. The delamination/cracks do not spread to Pixels 0, 2 and 3 as the organic stack is isolated. Further since the grid made from a barrier material, Pixels 0, 2 and 3 remain hermetically sealed.

[0028] If the panel is cut along BB'; i.e.: cutting through top barrier, barrier grid, substrate, and thin film barrier (if present), none of the pixels are damaged as this region does not have the weak organic-cathode interface. Additionally, the adhesion strength between the barrier grid and top barrier is very good. Pixels 0, 1, 2 and 3 should function since the electrical contact is intact. Delamination/cracks do not spread to Pixels 0, 1, 2 or 3 as the organic stack is isolated and remains hermetically sealed. In all the cases, the lifetime of the panel will be determined by the edge sealing ability of the barrier grid.

Embodiment 2 (Patterned organic, cathode and barrier):

[0029] In another embodiment of the present invention, the top barrier is also patterned to further isolate the pixels. This embodiment is shown in Figure 11. The panel 110 of Figure 11 consists of a plurality of electrodes (anodes) 111, insulating grid 112, organic stacks 113 and second electrodes (cathodes) 114 between a substrate 115 and a patterned top barrier 116. Figure 12 shows another variation of the current embodiment in which the anode is continuous (not patterned). The panel 120 of Figure 12 consists of an electrode (anode) 121, insulating grid 122, organic stacks 123 and second electrodes (cathodes) 124 between a substrate 125 and a patterned top barrier 126. The organic stacks 123, cathodes 124 and top thin film barrier 126 are patterned. The grid 122 disposed over a portion of the anode 121 is a barrier material. This barrier grid provides the required edge seal for Pixels 1, 2 and 3. The organic stack is patterned in such a way that no organic material is deposited directly on top or sidewall of the barrier grid or in other words, the organic material is not continuous over the entire panel. This can be accomplished using vias that connect the cathode to a bus line, or by using a cathode material that is also an excellent barrier, such as metals or certain TCO materials, such as IZO. Thus, in each pixel the top

barrier material is in contact with the barrier grid material. The pixels are thus hermetically sealed and isolated.

[0030] Another variation of the current embodiment is shown in Figure 13. The panel 130 of Figure 13 consists of a plurality of electrodes (anodes) 131, insulating grid 132, organic stacks 133 and second electrodes (cathodes) 134 between a substrate 135 and a patterned top barrier 136. The device architecture is similar to Figure 11, except for the addition of metal bus lines 137 to improve current distribution across the panel. The barrier grid 132 here is disposed over the bus lines 137 to prevent electrical shorting with the cathodes 134.

[0031] Additionally for flexible lighting panels fabricated on polymeric substrates such as poly ethylene terephthalate (PET) and poly ethylene naphthalate (PEN), thin film barriers are required on the substrate side of the panel to protect the device from moisture. Examples are shown in Figures 14 and 15. In Figure 14, a thin film barrier is disposed on the back side of the substrate, while in Figure 15, the barrier is disposed on top of the substrate before the anode. The panel 140 of Figure 14 consists of a plurality of electrodes (anodes) 141, insulating grid 142, organic stacks 143 and second electrodes (cathodes) 144 between a substrate 145 and a patterned top barrier 146. A plurality of bus lines 147 are also provided. A thin film barrier 148 is disposed on the back side of the substrate 145. In the architecture shown in Figure 15, the barrier is disposed on top of the substrate before the anode. The panel 150 of Figure 15 consists of a plurality of electrodes (anodes) 151, insulating grid 152, organic stacks 153 and second electrodes (cathodes) 154 between a substrate 155 and a patterned top barrier 156. A plurality of bus lines 157 are also provided. A thin film barrier 158 is disposed on top of the substrate 155 before the anodes 151.

[0032] If this panel is cut along AA'; i.e.: cutting through top barrier, cathode, organic, anode, substrate, and bottom thin film barrier, Pixel 1 is physically destroyed and does not light up. Further, the cutting process can damage the pixel in other ways: a) by introducing an electrical short; b) delamination of the cathode and the barrier from the organic; and c) delamination/crack propagation when the panel is flexed. Although Pixel 1 is compromised after the cutting process, Pixels 0, 2 and 3 stay intact. The delamination/cracks do not spread to Pixels 0, 2 and 3 as the organic stack is isolated. Further since the grid is made from a barrier material, Pixels 0, 2 and 3 remain hermetically sealed.

[0033] If the panel is cut along BB'; i.e.: cutting through, barrier grid, substrate, and bottom thin film barrier (if present), none of the pixels are damaged as this region does not have the weak organic-cathode interface. Additionally, the adhesion strength between the barrier grid and top barrier is very good. Pixels 0, 2 and 3 are functional since the electrical contact is intact. Delamination/cracks do not spread to Pixels 0, 2 and 3 as the organic stack is isolated and remains hermetically sealed.

[0034] In all the cases, the lifetime of the panel will be determined by the edge sealing ability of the barrier grid.

[0035] Other variations of Embodiments 1 and 2 for a rigid substrate are shown in Figures 16-22. Various other combinations including metal bus lines, fuses, and bottom barrier layers are possible for all types of substrates. In all the architectures, the organic stack of the OLED pixel is contained within its own hermetically sealed structure.

[0036] Figure 16 shows an architecture in which the cathode is continuous (not patterned). The panel 160 of Figure 16 consists of a plurality of electrodes (anodes) 161, insulating grid 162, organic stacks 163 and a continuous second electrode (cathode) 164 between a substrate 165 and a top barrier 166. The cathode 164 mentioned here may be made of a single layer or multiple layers. Further if the cathode is comprised of multiple layers, the first cathode layer may be patterned while the second cathode layer may be continuous as shown in Figure 17. The panel 170 of Figure 17 consists of a plurality of electrodes (anodes) 171, insulating grid 172, organic stacks 173, a patterned second electrode layer (cathode) 174 and a continuous second electrode layer (cathode) 175 between a substrate 176 and a top barrier 177. For example: the bilayer cathode may be Ca/IZO or Mg:Ag/IZO. Ca or Mg can be deposited as the patterned electrode (cathode) 174 in the active region (within the grid boundaries) while the IZO can be deposited as the continuous electrode (cathode) 175. This is advantageous especially after the panel is cut since IZO is less reactive to moisture when compared to reactive low work function reflective/transparent cathodes.

[0037] Figure 18 shows an architecture in which portions of the patterned cathode are deposited on the sidewalls and top of the barrier grid. The panel 180 of Figure 18 consists of a plurality of electrodes (anodes) 181, insulating grid 182, organic stacks 183 and a second electrode (cathode) 184 between a substrate 185 and a top barrier 186. Portions of the patterned cathode 184 are deposited on the sidewalls and top of the barrier grid 182. Figure 19 shows an architecture in which portions of the patterned organic and cathode are deposited on the sidewalls and top of the barrier grid. The panel 190 of Figure 19 consists of a plurality of electrodes (anodes) 191, insulating grid 192, organic stacks 193 and a second electrode (cathode) 194 between a substrate 195 and a top barrier 196. Portions of both the patterned organic 193 and cathode 194 are deposited on the sidewalls and top of the barrier grid 192. Figure 20 shows an architecture in which the barrier grid is not continuous; i.e.: adjacent pixels do not share the same barrier grid. The panel 200 of Figure 20 consists of a plurality of electrodes (anodes) 201, insulating grid 202, organic stacks 203 and a second electrode (cathode) 204 between a substrate 205 and a top barrier 206. The barrier grid 202 is not continuous across Pixels 0, 1, 2 and 3. Figure 21 shows an architecture in which the barrier grid is not continuous; i.e.: adjacent pixels do not share the same barrier grid and

organic and cathode are deposited on the sidewalls and top of the barrier grid. The panel 210 of Figure 21 consists of a plurality of electrodes (anodes) 211, insulating grid 212, organic stacks 213 and a second electrode (cathode) 214 between a substrate 215 and a top barrier 216. The barrier grid 212 is not continuous across Pixels 0, 1, 2 and 3. Further, portions of both the patterned organic 213 and cathode 214 are deposited on the sidewalls and top of the barrier grid 212. Figure 22 shows an architecture in which the barrier grid profile is inverted. The panel 220 of Figure 21 consists of a plurality of electrodes (anodes) 221, insulating grid 222, organic stacks 223 and a second electrode (cathode) 224 between a substrate 225 and a top barrier 226. The inverted barrier grid 222 acts a secondary integrated shadow mask for organic stack 213 and/or cathode 224 isolation during deposition.

[0038] Another aspect of the current invention discloses a method for making hermetically sealed OLED pixels shown in the above architectures. The invention particularly teaches a method of making the barrier grid and isolated organic stacks according to some embodiments of the invention.

[0039] For rigid substrates, the patterned anode is directly disposed over the substrate. In polymeric substrates, thin film barriers may be disposed on the top and/or bottom sides of the substrate before anode deposition. The barrier grid is then disposed over a portion of the anode. The grid is subsequently patterned during deposition or post-deposition. The organic stack is then deposited and isolated either during deposition or post-deposition. The cathode is deposited to complete the pixel. The entire pixel is then encapsulated with thin film barriers to hermetically seal the OLED pixels.

[0040] According to some embodiments of the invention, barrier grids are made by a vacuum deposition. Vacuum deposition may include, but is not limited to sputtering, chemical vapor deposition, evaporation, sublimation, atomic layer deposition (ALD), plasma enhanced chemical vapor deposition (PECVD), plasma assisted atomic layer deposition and combinations thereof. Patterning of the barrier grid to obtain the desired grid profile can be achieved during deposition or post-deposition or a combination of both. During deposition, techniques include but are not limited to the use of a single or plurality of shadow masks to obtain the desired grid profile. Post-deposition patterning techniques include but are not limited to photolithography and wet chemical etching, dry etching or a combination of both. Dry etching processes include non-plasma based etching, plasma based etching and ion beam etching.

[0041] Barrier grids can be made from a single material or different materials. For example, if the materials are deposited by sputtering, sputtering targets of different compositions can be used to obtain this layer. Alternatively, two targets of same composition can be used with different reactive gases. Similarly, when the layer is deposited by PECVD, different types of precursors or reactive gasses may be used. Different types of deposition

sources could be used. For example, the barrier grid can be made from alternating layers of $\text{SiO}_2/\text{SiN}_x$. When barrier grid is made from multiple layers, alternate insulating and conductive barrier layers may be used. For example $\text{SiO}_x\text{C}_y\text{H}_z/\text{IZO}/\text{SiO}_x\text{C}_y\text{H}_z$ can form a barrier grid.

[0042] Barrier grids can be amorphous or polycrystalline. For example, thin films of indium zinc oxide deposited by reactive sputtering from an indium zinc oxide target with oxygen reactive gas are typically amorphous. Thin films of Aluminum oxide deposited by reactive sputtering from an aluminum target with oxygen reactive gas are typically polycrystalline. Nanolaminates consisting of alternate thin stacks of zinc oxide and aluminum oxide can also be used for barrier layers. For example, if the thin films are deposited by atomic layer deposition, alternate thin stacks of $\text{ZnO}/\text{Al}_2\text{O}_3$ may be used.

[0043] Barrier grid material can be transparent or opaque depending on the design and application of the device. Inorganic materials such as metal oxides, metal nitrides, metal oxynitrides, metal carbides, metal oxyborides and combinations thereof can be used as a barrier grid material. Metal oxides are preferably selected from silicon oxide, aluminum oxide, tin oxide, zinc oxide, indium tin oxide, indium zinc oxide, aluminum zinc oxide, tantalum oxide, zirconium oxide, niobium oxide, molybdenum oxide and combinations thereof. Metal nitrides are preferably selected from silicon nitride, aluminum nitride, boron nitride and combinations thereof. Metal oxynitrides are preferably selected from aluminum oxynitride, silicon oxynitride, boron oxynitride and combinations thereof. Metal carbides are preferably selected from tungsten carbide, boron carbide, silicon carbide and combinations thereof. Metal oxyborides are preferably zirconium oxyboride, titanium oxyboride and combinations thereof. An alternative is to use a hybrid barrier material such as $\text{SiO}_x\text{C}_y\text{H}_z$. Some organic content may be preferred to ensure that a thick layer can be made without cracking or delamination due to defects or internal stress. This organic content may also improve the flexibility of the film. One such example is the hybrid barrier layer taught in US 7,968,146 B2. This material is a hybrid of inorganic SiO_2 and polymeric silicone.

[0044] According to some embodiments of the invention, patterning/isolation of the organic stack can be achieved during deposition or post deposition or a combination of both. Patterning during deposition can be by vacuum thermal evaporation (VTE) or organic vapor phase deposition (OVPD) through a shadow mask or other deposition techniques including but not limited to ink jet printing, nozzle printing, organic vapor jet printing (OVJP), thermal jet printing (T-JET) and laser induced thermal imaging (LITI). Alternatively, organic stacks can be isolated post-deposition by plasma etching through shadow masks. Another isolation can be achieved by using inverted barrier grid structures as shown in Figure 22. In the structure the grids may act as a second mask. Alternatively, organics can be blanket deposited on this structure, and organics on top of the barrier grid can be

selectively etched off with plasma etching through shadow masks.

[0045] Some embodiments of the disclosed subject matter were experimentally verified by fabricating OLED panels and cutting them. In all the experiments, the barrier grid was a single hybrid barrier layer grown by plasma enhanced chemical vapor deposition (PECVD) of an organic precursor with a reactive gas such as oxygen; e.g.: HMDSO/O₂

[0046] During a hermetic sealing and cutting test (Encapsulation of OLED), OLED device architecture shown in Figure 7 was fabricated to test the invention. The devices were grown on glass substrates. Five pre-patterned ITO strips were used as the anode. A 0.5 μm thin SiO_x-C_yH_z hybrid barrier was blanket deposited on the anode strips. The hybrid barrier layer was grown by plasma enhanced chemical vapor deposition (PECVD) of an organic precursor (HMDSO) with oxygen as the reactive gas. The barrier grid was made by selectively dry etching the barrier using a shadow mask in a reactive ion etch (RIE) tool with CF₄ and oxygen plasma. Isolated organic was deposited by VTE using a shadow mask. The cathode was subsequently deposited by VTE using a shadow mask. The devices were then encapsulated with a 2 μm thick hybrid thin film barrier. The thin film barrier was blanket deposited. A picture of OLED devices is shown in Figure 23. The panel was cut along AA' (Pixel 1 and 4), i.e.: cutting through top barrier, cathode, organic, anode, and substrate. As expected, Pixels 1 and 4 were compromised during the cutting process. The barrier and cathode delaminated from the underlying organic stack. Although these two pixels delaminated, the delamination did not spread to other pixels. The panel was then cut along BB'; i.e.: cutting through barrier grid and substrate. Both Pixels 2 and 3 survived the process and no delamination was seen as this region does not have the weak organic-cathode interface. All the pixels that survived the cutting process (Pixels 2, 3, 5, 6) remained hermetically sealed. Figure 24 is a picture of Pixels 2 and 3 after the cutting process.

[0047] Devices fabricated in accordance with embodiments of the invention may be incorporated into a wide variety of consumer products, including flat panel displays, lighting devices, computer monitors, medical monitors, televisions, billboards, lights for interior or exterior illumination and/or signaling, heads up displays, fully transparent displays, flexible displays, laser printers, telephones, cell phones, personal digital assistants (PDAs), laptop computers, digital cameras, camcorders, viewfinders, micro-displays, 3-D displays, vehicles, a large area wall, theater or stadium screen, or a sign. Various control mechanisms may be used to control devices fabricated in accordance with the present invention, including passive matrix and active matrix. Many of the devices are intended for use in a temperature range comfortable to humans, such as 18°C to 30°C, and more preferably at room temperature (20°C to 25°C), but could be used outside this temperature range, for example, from -40°C

to +80°C.

[0048] The materials and structures described herein may have applications in devices other than OLEDs. For example, other optoelectronic devices such as organic solar cells and organic photodetectors may employ the materials and structures. More generally, organic devices, such as organic transistors, may employ the materials and structures.

[0049] It is to be appreciated that the Detailed Description section, and not the Summary and Abstract sections, is intended to be used to interpret the claims. The Summary and Abstract sections may set forth one or more but not all illustrative embodiments of the present invention as contemplated by the inventor(s), and thus, are not intended to limit the present invention and the appended claims in any way.

[0050] The foregoing description of the specific embodiments will so fully reveal the general nature of the invention that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present invention. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein. It is to be understood that the phraseology or terminology herein is for the purpose of description and not limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

Preferred embodiments 1 to 43:

1. An organic light emitting device (OLED), comprising:

a substrate;
a plurality of OLED pixels, each comprising an OLED pixel, disposed over the substrate;
a first barrier element, disposed over the substrate and forming an insulating grid surrounding the OLED pixel; and
a second barrier element, disposed over the OLED pixel and first barrier element,
wherein the first barrier element predominantly provides an edge seal for each respective OLED pixel, and the second barrier element encapsulates the OLED pixel to provide a top seal.

2. The device of embodiment 1, wherein the substrate comprises a first surface and a second surface, the device further comprising a third barrier element disposed over one of the second surface of the substrate, and the first surface of the substrate between the substrate and the OLED pixel, to provide a bottom seal.

3. The device of embodiment 1, wherein each re-

spective OLED pixel comprises a stack having a first cathode layer, an organic layer and an anode layer.

4. The device of embodiment 3, wherein each stack is patterned and surrounded by the first barrier element to isolate the organic layer of the respective OLED pixel from an organic layer of adjacent stacks.

5. The device of embodiment 3, wherein each stack is patterned and surrounded by the first barrier element to isolate the cathode layer of the respective OLED pixel from a cathode layer of adjacent stacks.

6. The device of embodiment 3, wherein each stack is patterned and surrounded by the first barrier element to isolate the anode layer of the respective OLED pixel from an anode layer of adjacent stacks.

7. The device of embodiment 3, wherein the first cathode layer of the respective OLED pixel is continuous with a first cathode layer of adjacent stacks, and the organic layer of the respective OLED pixel is discontinuous with an organic layer of adjacent stacks.

8. The device of embodiment 3, further comprising a second cathode layer, wherein the first cathode layer of the respective OLED pixel is continuous with a first cathode layer of adjacent stacks, and the second cathode layer and the organic layer of the respective OLED pixel are discontinuous with a second cathode layer and organic layer of adjacent stacks, respectively.

9. The device of embodiment 8, wherein the first cathode layer of the respective OLED pixel is comprised of a Transparent Conductive Oxide (TCO), and wherein the second cathode layer of the respective OLED pixel is comprised of a material including one or more of calcium (Ca), magnesium (Mg) or silver (Ag).

10. The device of embodiment 1, wherein the first barrier element is discontinuous between adjacent OLED pixels.

11. The device of embodiment 1, wherein the second barrier element is discontinuous between adjacent OLED pixels.

12. The device of embodiment 1, wherein the first barrier element is inverted to form a shadow mask for OLED pixel isolation from the first barrier element during disposition.

13. The device of embodiment 1, wherein the first barrier element is an amorphous or polycrystalline material, a metal oxide, metal nitride, metal oxy-

tride, metal carbide and metal oxyboride.

14. The device of embodiment 13, wherein the first barrier element is comprised of multiple alternate layers of $\text{SiO}_x\text{N}_y/\text{SiO}_x\text{C}_y$ deposited at room temperature by plasma enhanced chemical vapor deposition (PECVD).

15. The device of embodiment 13, wherein the first barrier element is comprised of a single hybrid barrier layer deposited by plasma enhanced chemical vapor deposition (PECVD) of an organic precursor with a reactive gas such as oxygen.

16. The device of embodiment 13, wherein the first barrier element is comprised of a hybrid of inorganic SiO_2 and polymeric silicone deposited at room temperature.

17. The device of embodiment 13, wherein the first barrier element is comprised of a hybrid barrier material such as $\text{SiO}_x\text{C}_y\text{H}_z$.

18. The device of embodiment 1, wherein the first barrier element material can be transparent or opaque.

19. The device of embodiment 1, wherein the substrate is comprised of a flexible polymer material including one or more of a poly carbonate material, a polyimide material, a poly ethylene terephthalate (PET) material and a poly ethylene naphthalate (PEN) material.

20. The device of embodiment 1, wherein the device is flexible.

21. The device of embodiment 2, wherein at least one of the substrate, first barrier element, second barrier element and third barrier element comprises an impact resistant transparent structure.

22. The device of embodiment 1, wherein the first barrier element and second barrier element are in direct contact with each other.

23. A method of fabricating an organic light emitting device (OLED) comprising:

forming a first barrier element over a substrate to provide an insulating grid for an OLED pixel disposed over the substrate;
forming a plurality of OLED pixels over the substrate, wherein each respective OLED pixel is formed over the substrate within a boundary of the first barrier element, such that the first barrier element surrounds the OLED pixel; and
forming a second barrier element over the OLED

pixel and first barrier element,
wherein the first barrier element provides an
edge seal for each respective OLED pixel, and
the second barrier element encapsulates the
OLED pixel to provide a top seal.

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24. The method of embodiment 23, wherein the first
barrier element is formed over the substrate by a
vacuum deposition, including one or more of a sput-
tering, chemical vapor deposition, evaporation, sub-
limation, atomic layer deposition (ALD), plasma en-
hanced chemical vapor deposition (PECVD) and
plasma assisted atomic layer deposition operation,
and combinations thereof.

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25. The method of embodiment 24, wherein pattern-
ing of the first barrier element is performed during
deposition using a single or plurality of shadow
masks to obtain a desired grid profile.

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26. The method of embodiment 24, wherein pattern-
ing of the first barrier element is performed during
post-deposition using photolithography.

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27. The method of embodiment 24, wherein pattern-
ing of the first barrier element is performed during
post-deposition using one or more of a wet chemical
etching and dry etching, wherein dry etching includes
non-plasma based etching, plasma based etching
and ion beam etching.

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28. The method of embodiment 24, wherein:

if the first barrier element is formed over the sub-
strate by a sputtering deposition, sputtering tar-
gets of different compositions can be used or
two targets of same composition can be used
with different reactive gases; and
if the first barrier element is formed over the sub-
strate by PECVD, different types of precursors
or reactive gasses can be used, different types
of deposition sources can be used, including al-
ternating layers of $\text{SiO}_2/\text{SiN}_x$, and alternating in-
sulating and conductive layers can be used.

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29. The method of embodiment 23, wherein the first
barrier element is an amorphous or polycrystalline
material, comprised of a flexible material including
one or more of a metal oxide, metal nitride, metal
oxynitride, metal carbide and metal oxyboride.

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30. The method of embodiment 23, wherein the first
barrier element is comprised of multiple alternate lay-
ers of $\text{SiO}_x\text{N}_y/\text{SiO}_x\text{C}_y$ deposited at room temperature
by plasma enhanced chemical vapor deposition
(PECVD).

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31. The method of embodiment 23, wherein the first

barrier element is comprised of a single hybrid barrier
layer deposited by plasma enhanced chemical vapor
deposition (PECVD) of an organic precursor with a
reactive gas such as oxygen.

32. The method of embodiment 23, wherein the first
barrier element is comprised of a hybrid of inorganic
 SiO_2 and polymeric silicone deposited at room tem-
perature.

33. The method of embodiment 23, wherein the first
barrier element is comprised of a hybrid barrier ma-
terial such as $\text{SiO}_x\text{C}_y\text{H}_z$.

34. The method of embodiment 23, wherein the first
barrier element material can be transparent or
opaque.

35. The method of embodiment 23, wherein each
respective OLED pixel comprises a stack having a
first cathode layer, an organic layer and an anode
layer, wherein each stack is patterned and formed
on the substrate, and wherein the first barrier ele-
ment is formed over a portion of the anode layer.

36. The method of embodiment 35, wherein each
stack is patterned and surrounded by the first barrier
element to isolate the organic layer of the respective
OLED pixel from an organic layer of adjacent stacks.

37. The method of embodiment 35, wherein each
stack is patterned and surrounded by the first barrier
element to isolate the cathode layer of the respective
OLED pixel from a cathode layer of adjacent stacks.

38. The method of embodiment 35, wherein each
stack is patterned and surrounded by the first barrier
element to isolate the anode layer of the respective
OLED pixel from an anode layer of adjacent stacks.

39. The method of embodiment 35, wherein the sub-
strate is comprised of a flexible polymer material in-
cluding one or more of a poly carbonate material, a
polymeric material, a poly ethylene terephthalate
(PET) material and a poly ethylene naphthalate
(PEN) material, and thin film barriers are formed over
at least one surface of the substrate before anode
formation.

40. The method of embodiment 35, wherein pattern-
ing of the stack is performed during one or more of
deposition using vacuum thermal evaporation
(VTE), organic vapor phase deposition (OVPD)
through a shadow mask, ink jet printing, nozzle print-
ing, organic vapor jet printing (OVJP), thermal jet
printing (T-JET) and laser induced thermal imaging
(LITI), and post-deposition using plasma etching
through shadow masks.

41. The method of embodiment 35, wherein patterning of the stack is performed using inverted first barrier elements as a mask.

42. The method of embodiment 23, wherein the device is flexible. 5

43. The method of embodiment 23, wherein at least one of the substrate, first barrier element and second barrier element comprise an impact resistant transparent structure. 10

Claims

1. An organic light emitting device (OLED), comprising:

a substrate;
a plurality of OLED pixels, each comprising an OLED pixel, disposed over the substrate;
a first barrier element, disposed over the substrate and forming an insulating grid surrounding the OLED pixel; and
a second barrier element, disposed over the OLED pixel and first barrier element, wherein the first barrier element predominantly provides an edge seal for each respective OLED pixel, and the second barrier element encapsulates the OLED pixel to provide a top seal. 20

2. The device of claim 1, wherein the substrate comprises a first surface and a second surface, the device further comprising a third barrier element disposed over one of the second surface of the substrate, and the first surface of the substrate between the substrate and the OLED pixel, to provide a bottom seal. 25

3. The device of claim 1 or 2, wherein each respective OLED pixel comprises a stack having a cathode layer, an organic layer and an anode layer, wherein each stack is patterned and surrounded by the first barrier element to isolate at least one of the organic layer of the respective OLED pixel from an organic layer of adjacent stacks, the cathode layer of the respective OLED pixel from a cathode layer of adjacent stacks, and the anode layer of the respective OLED pixel from an anode layer of adjacent stacks. 30

4. The device of claim 3, wherein the cathode layer is comprised of a first cathode layer and a second cathode layer, wherein the first cathode layer of the respective OLED pixel is continuous with a first cathode layer of adjacent stacks, and the organic layer of the respective OLED pixel is discontinuous with an organic layer of adjacent stacks, or 35

wherein the first cathode layer of the respective OLED pixel is continuous with a first cathode layer of adjacent stacks, and the second cathode layer and the organic layer of the respective OLED pixel are discontinuous with a second cathode layer and organic layer of adjacent stacks, respectively.

5. The device of any of the preceding claims, wherein at least one of the first barrier element and the second barrier element is discontinuous between adjacent OLED pixels. 40

6. The device of any of the preceding claims, wherein the first barrier element is inverted to form a shadow mask for OLED pixel isolation from the first barrier element during disposition. 45

7. The device of any of the preceding claims, wherein the first barrier element is an amorphous or polycrystalline material, a metal oxide, metal nitride, metal oxynitride, metal carbide and metal oxyboride, including multiple alternate layers of $\text{SiO}_x\text{N}_y/\text{SiO}_x\text{C}_y$ deposited at room temperature by plasma enhanced chemical vapor deposition (PECVD), a single hybrid barrier layer deposited by plasma enhanced chemical vapor deposition (PECVD) of an organic precursor with a reactive gas such as oxygen, a hybrid of inorganic SiO_2 and polymeric silicone deposited at room temperature, or a hybrid barrier material such as $\text{SiO}_x\text{C}_y\text{H}_z$; and wherein the substrate is comprised of a flexible polymer material including one or more of a polycarbonate material, a polyimide material, a polyethylene terephthalate (PET) material and a polyethylene naphthalate (PEN) material. 50

8. The device of any of the preceding claims, wherein the device is flexible.

9. The device of claim 2, wherein at least one of the substrate, first barrier element, second barrier element and third barrier element comprises an impact resistant transparent structure.

10. The device of any of the preceding claims, wherein the first barrier element and second barrier element are in direct contact with each other.

11. A method of fabricating an organic light emitting device (OLED) comprising: 55

forming a first barrier element over a substrate to provide an insulating grid for an OLED pixel disposed over the substrate;
forming a plurality of OLED pixels over the substrate, wherein each respective OLED pixel is formed over the substrate within a boundary of

- the first barrier element, such that the first barrier element surrounds the OLED pixel; and forming a second barrier element over the OLED pixel and first barrier element, wherein the first barrier element provides an edge seal for each respective OLED pixel, and the second barrier element encapsulates the OLED pixel to provide a top seal.
12. The method of claim 11, wherein the first barrier element is formed over the substrate by a vacuum deposition, including one or more of a sputtering, chemical vapor deposition, evaporation, sublimation, atomic layer deposition (ALD), plasma enhanced chemical vapor deposition (PECVD) and plasma assisted atomic layer deposition operation, and combinations thereof.
13. The method of claim 12, wherein patterning of the first barrier element is performed during a period selected from the group consisting of, during deposition, using a single or plurality of shadow masks to obtain a desired grid profile, during post-deposition, using photolithography, and during post-deposition, using one or more of a wet chemical etching and dry etching, wherein dry etching includes non-plasma based etching, plasma based etching and ion beam etching.
14. The method of claim 12, wherein:
- if the first barrier element is formed over the substrate by a sputtering deposition, sputtering targets of different compositions can be used or two targets of same composition can be used with different reactive gases; and
- if the first barrier element is formed over the substrate by PECVD, different types of precursors or reactive gasses can be used, different types of deposition sources can be used, including alternating layers of $\text{SiO}_2/\text{SiN}_x$, and alternating insulating and conductive layers can be used.
15. The method of claim 11, wherein the first barrier element is an amorphous or polycrystalline material, comprised of a flexible material including one or more of a metal oxide, metal nitride, metal oxynitride, metal carbide and metal oxyboride, including multiple alternate layers of $\text{SiO}_x\text{N}_y/\text{SiO}_x\text{C}_y$ deposited at room temperature by plasma enhanced chemical vapor deposition (PECVD), a single hybrid barrier layer deposited by plasma enhanced chemical vapor deposition (PECVD) of an organic precursor with a reactive gas such as oxygen, a hybrid of inorganic SiO_2 and polymeric silicone deposited at room temperature, or
- a hybrid barrier material such as $\text{SiO}_x\text{C}_y\text{H}_z$; and wherein the substrate is comprised of a flexible polymer material including one or more of a polycarbonate material, a polymeric material, a polyethylene terephthalate (PET) material and a polyethylene naphthalate (PEN) material, and thin film barriers are formed over at least one surface of the substrate before anode formation.
16. The method of any of the preceding claims, wherein each respective OLED pixel comprises a stack having a cathode layer, an organic layer and an anode layer, wherein each stack is patterned and surrounded by the first barrier element to isolate at least one of the organic layer of the respective OLED pixel from an organic layer of adjacent stacks, the cathode layer of the respective OLED pixel from a cathode layer of adjacent stacks, and the anode layer of the respective OLED pixel from an anode layer of adjacent stacks.
17. The method of claim 16, wherein patterning of the stack is performed during one or more of deposition using vacuum thermal evaporation (VTE), organic vapor phase deposition (OVPD) through a shadow mask, ink jet printing, nozzle printing, organic vapor jet printing (OVJP), thermal jet printing (T-JET) and laser induced thermal imaging (LITI), and post-deposition using plasma etching through shadow masks.
18. The method of claim 16, wherein patterning of the stack is performed using inverted first barrier elements as a mask.
19. The method of any of the preceding claims, wherein the device is flexible.
20. The method of any of the preceding claims, wherein at least one of the substrate, first barrier element and second barrier element comprise an impact resistant transparent structure.

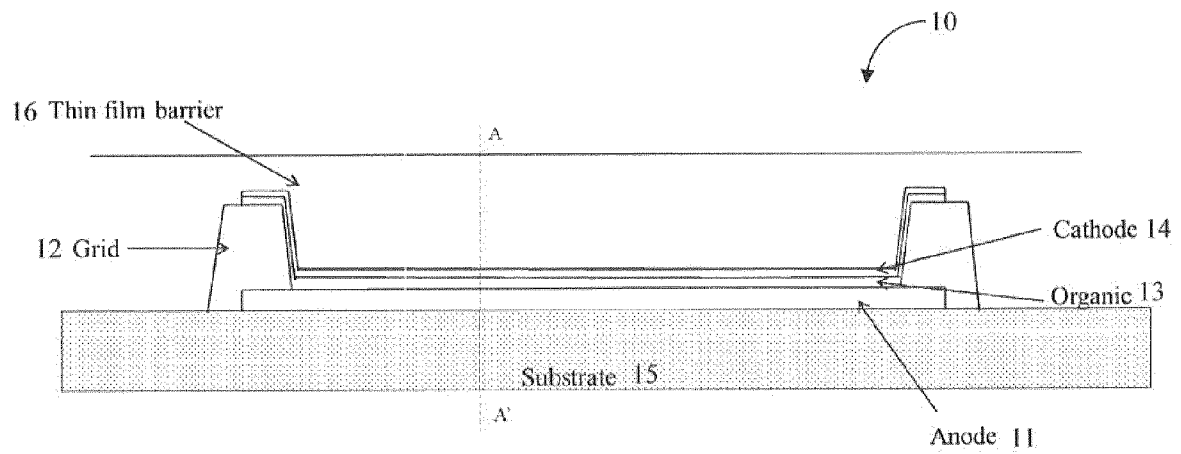


Figure 1

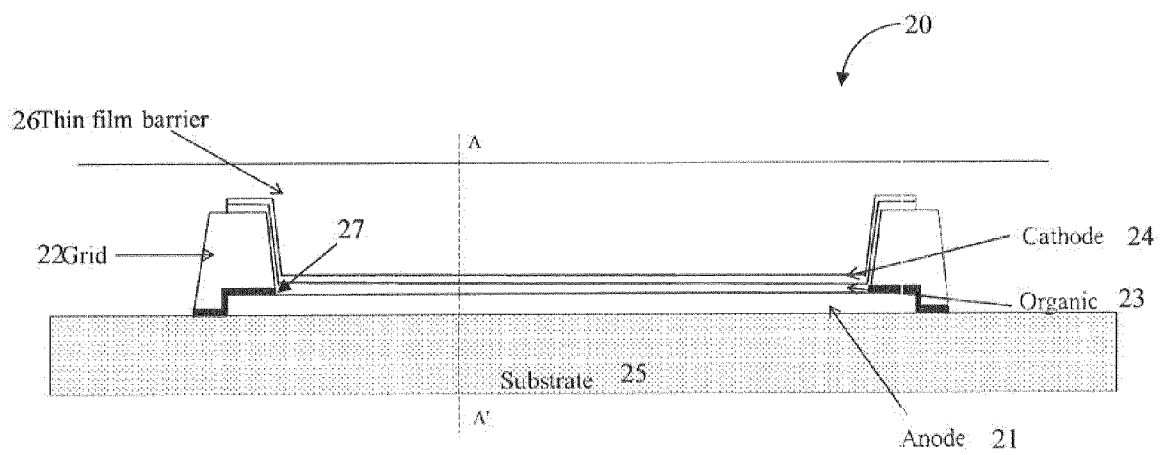


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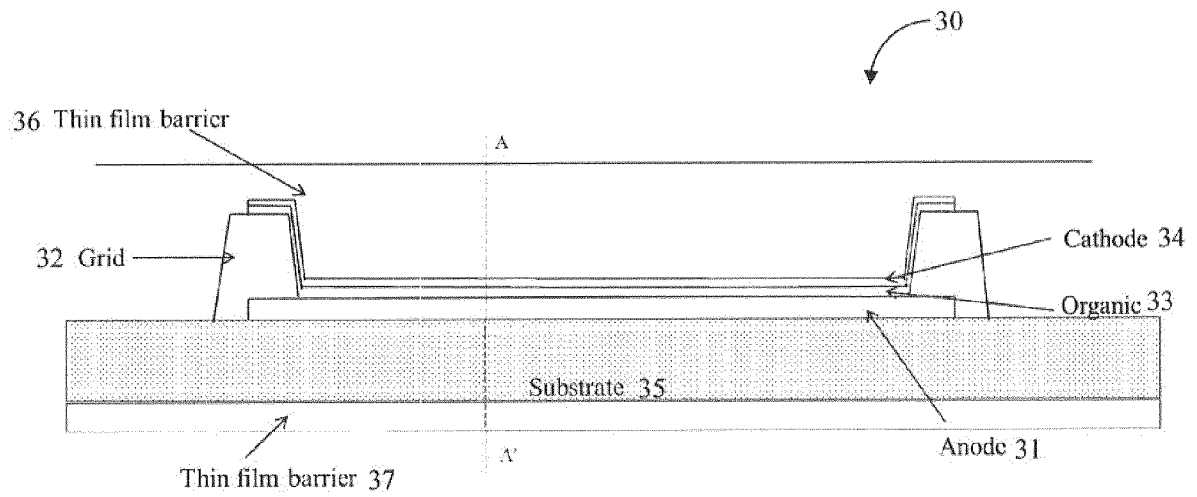


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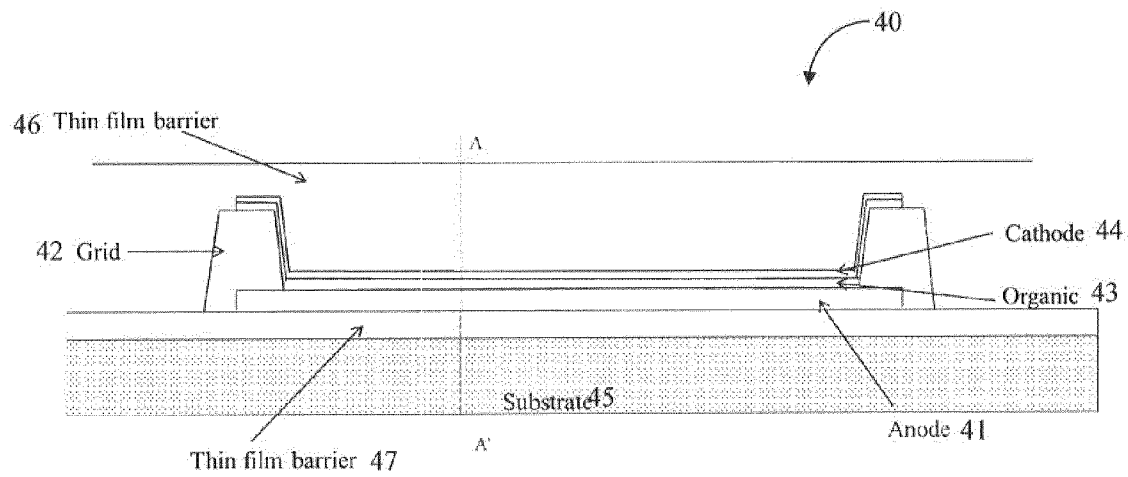


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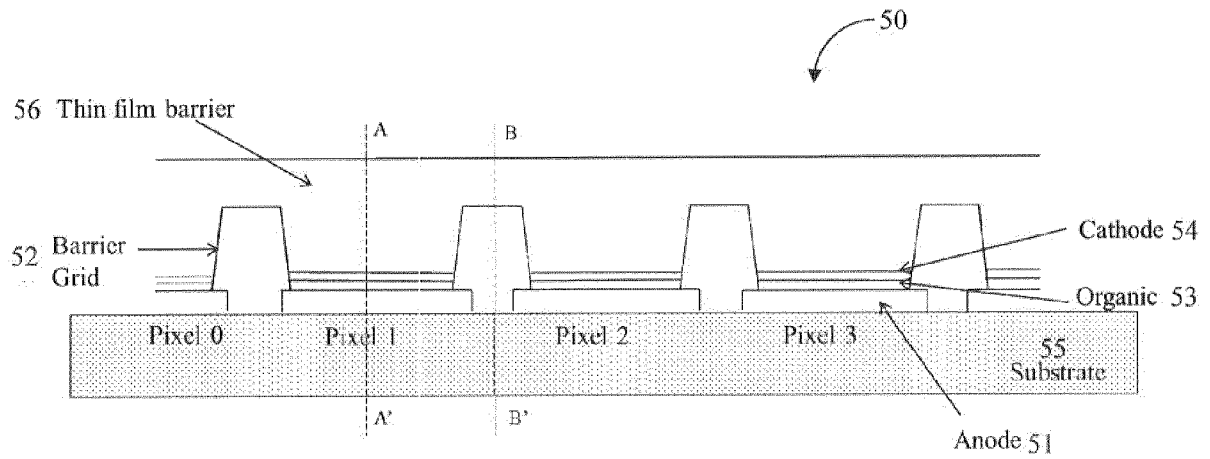


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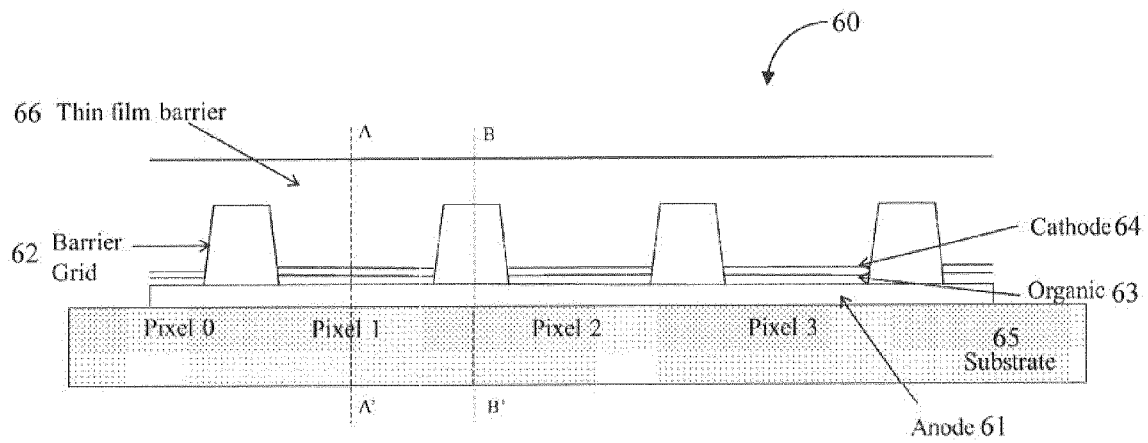


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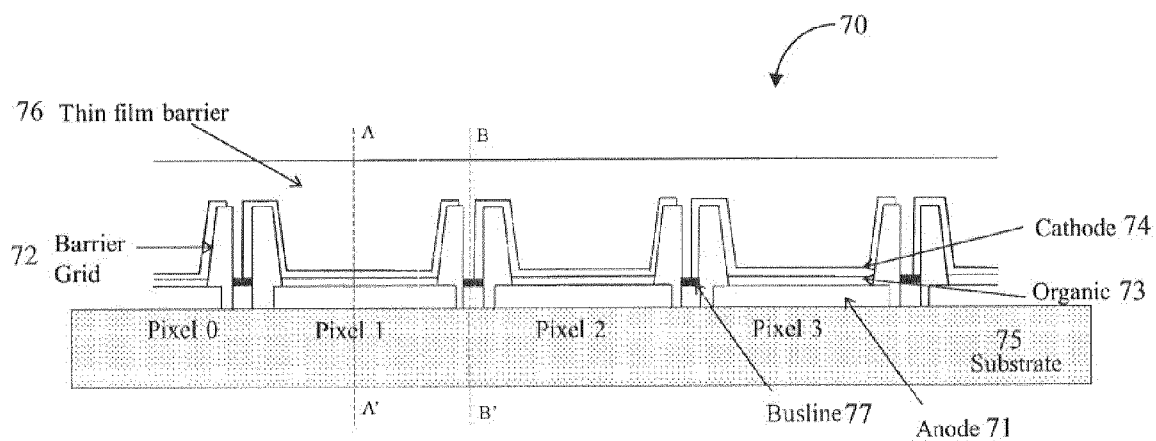


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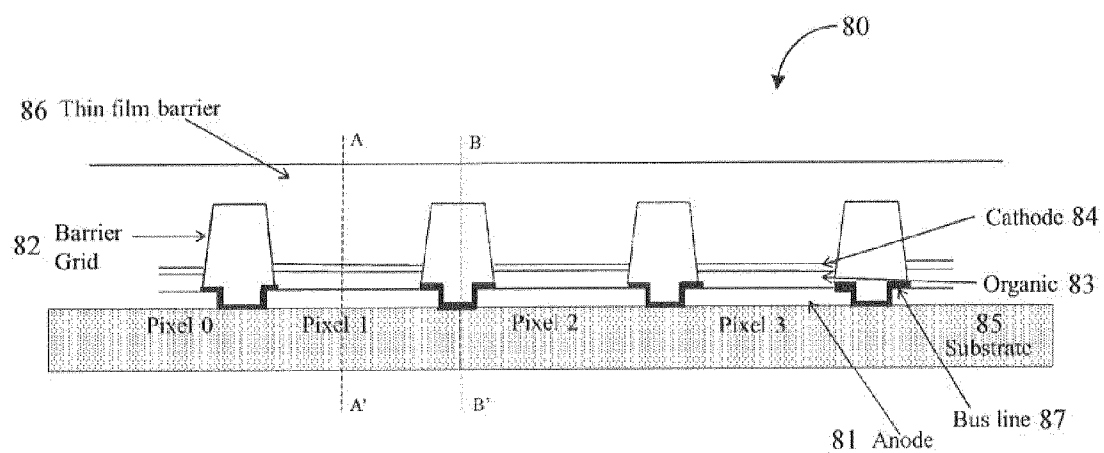


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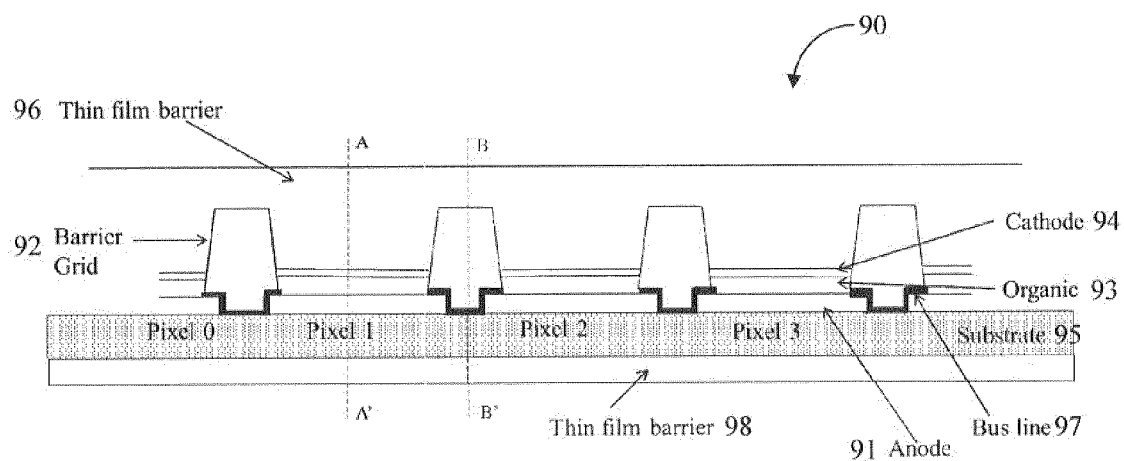


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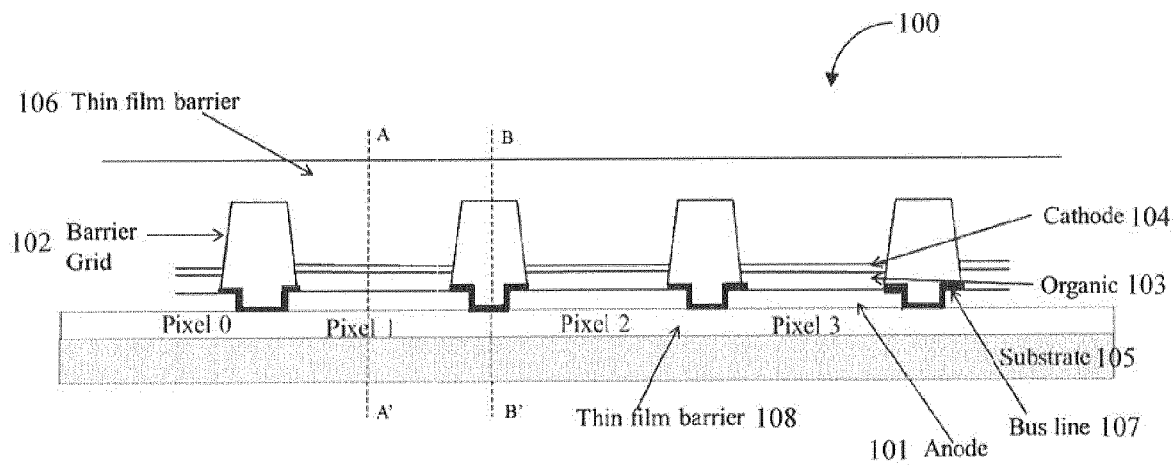


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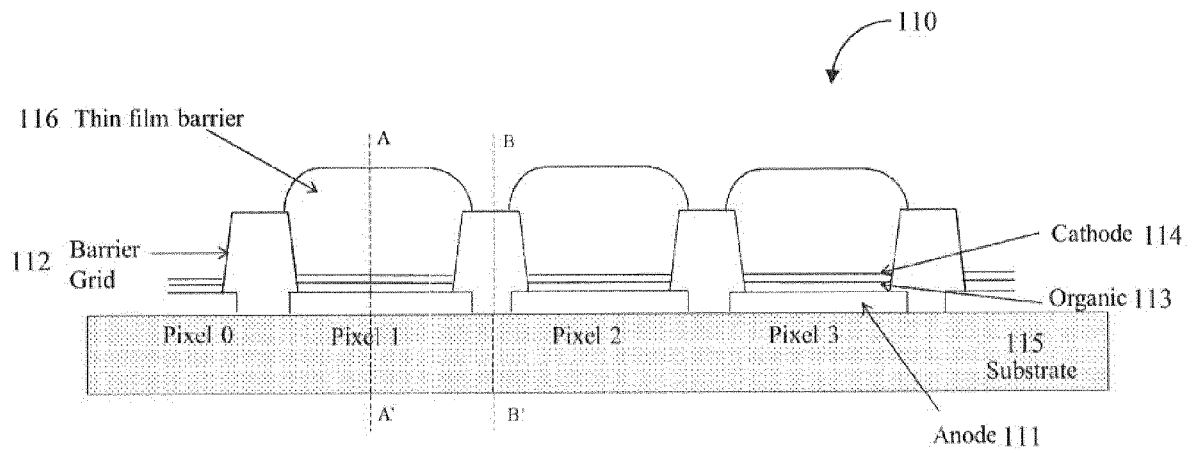


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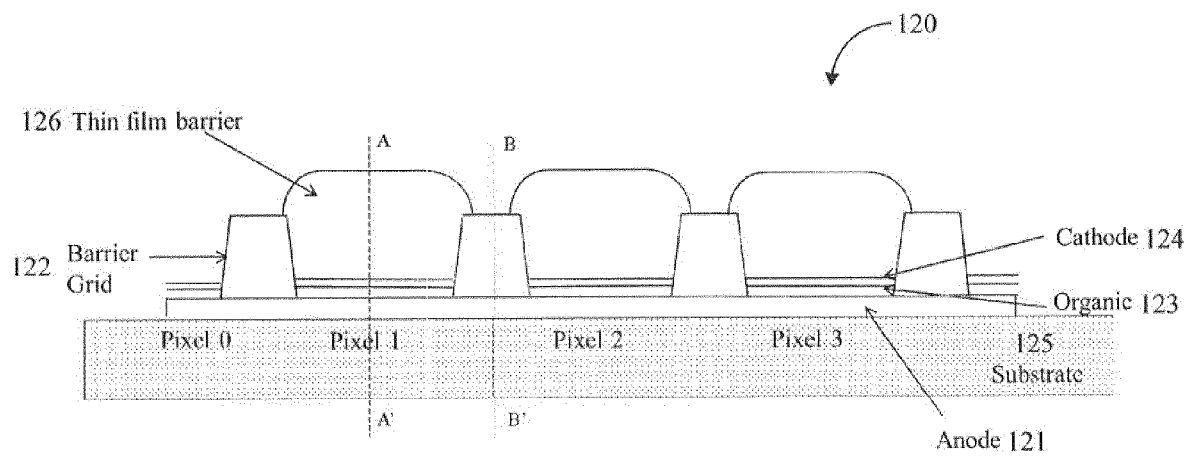


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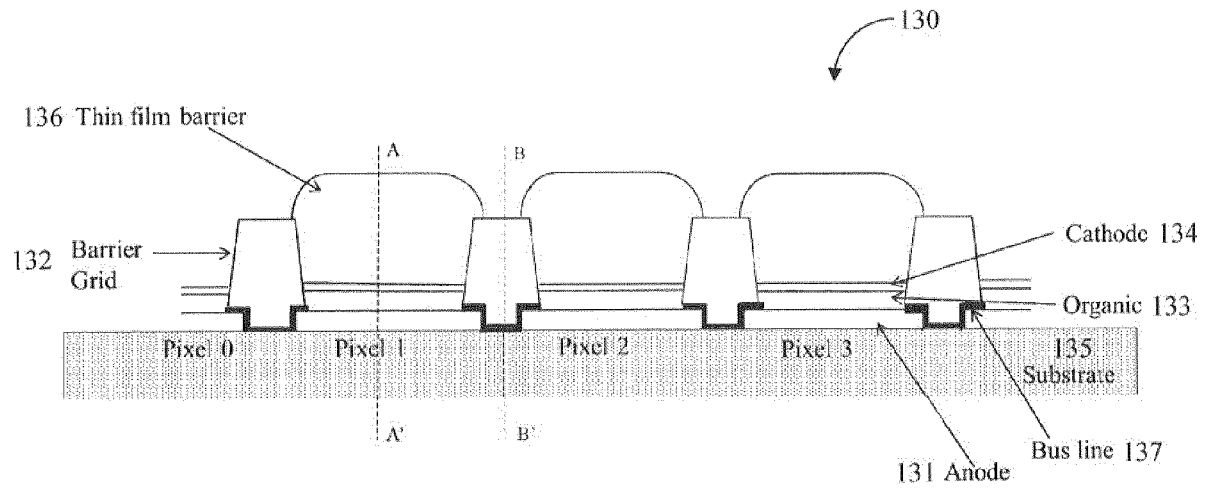


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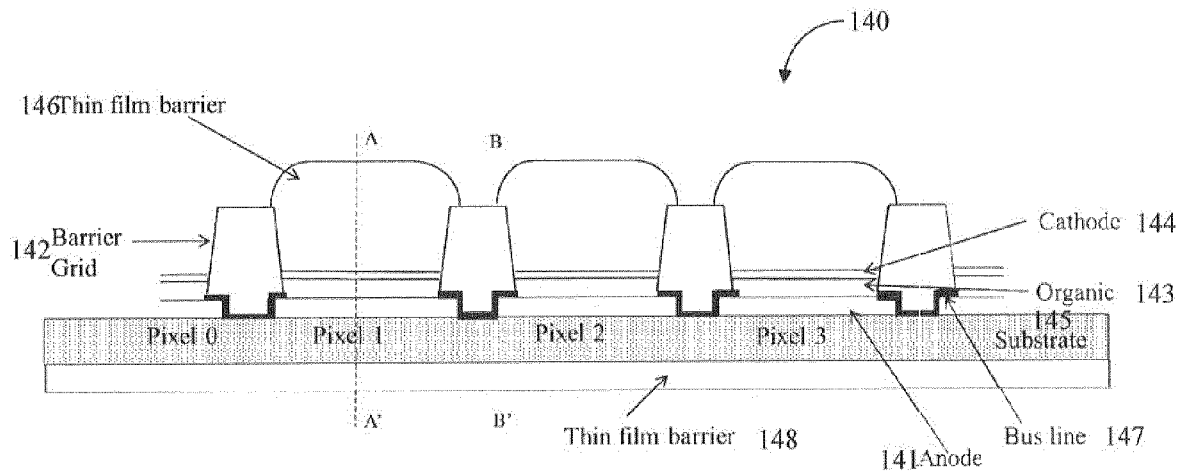


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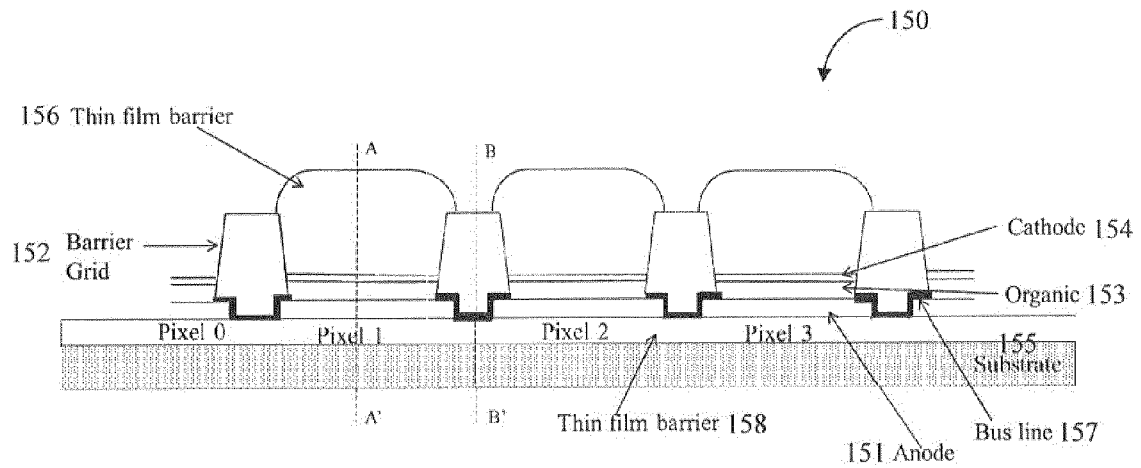


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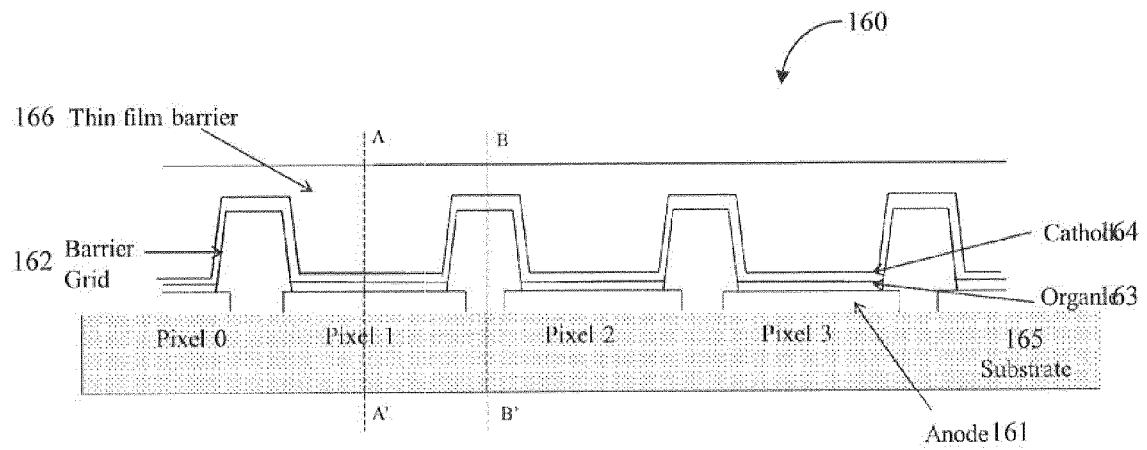


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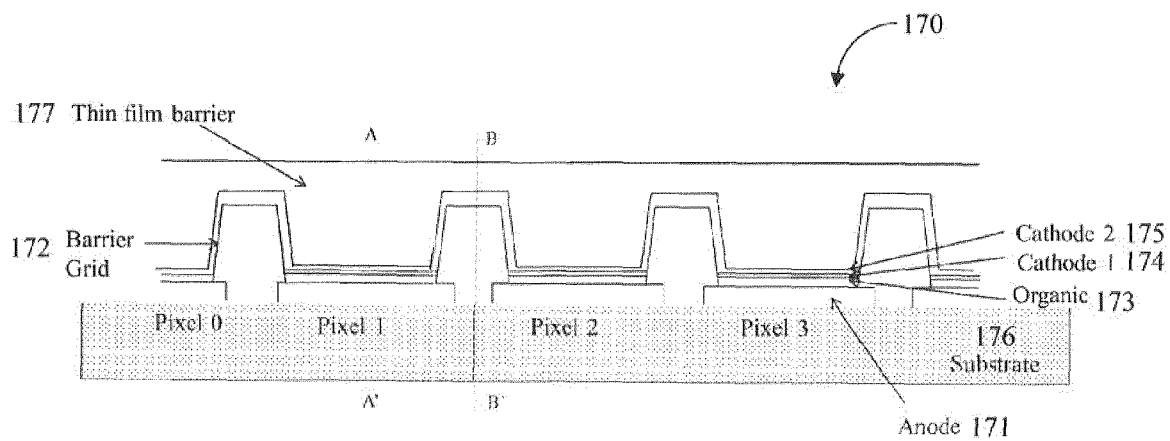


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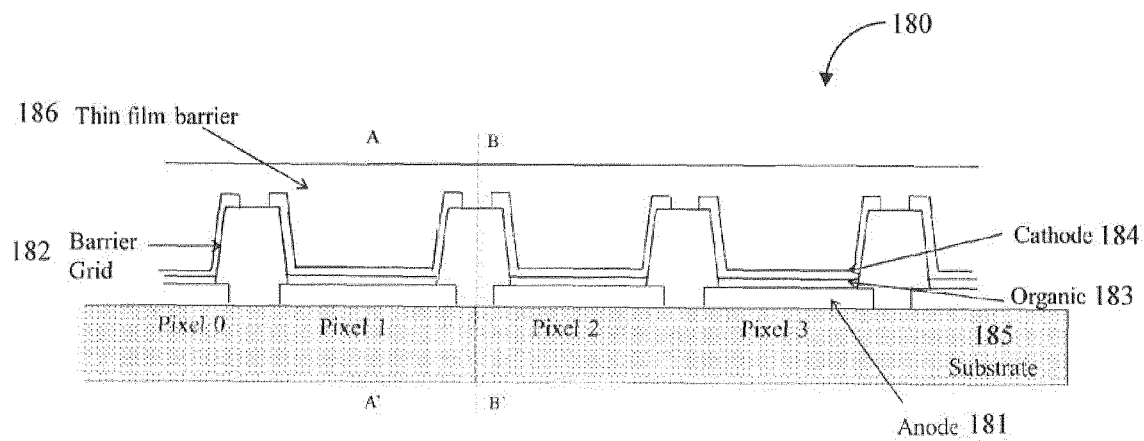


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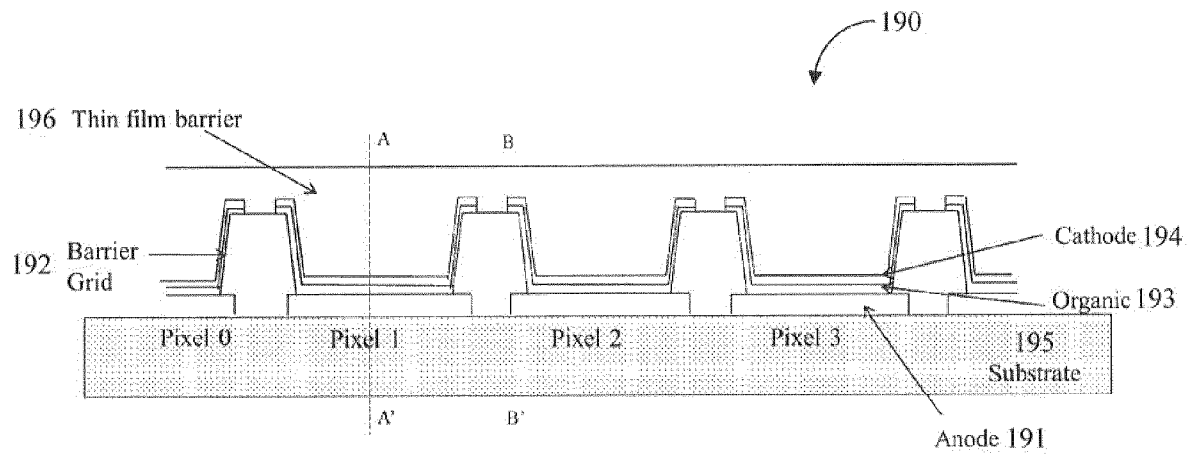


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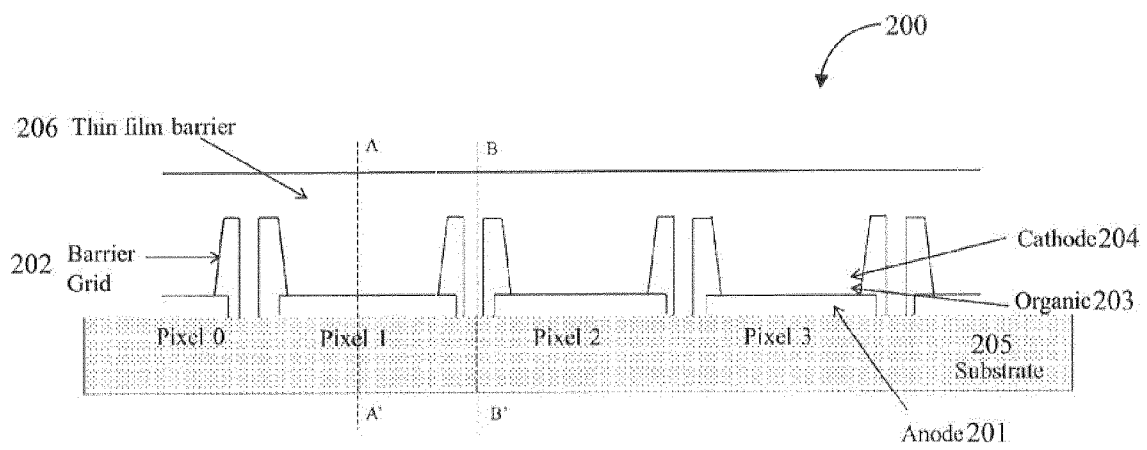


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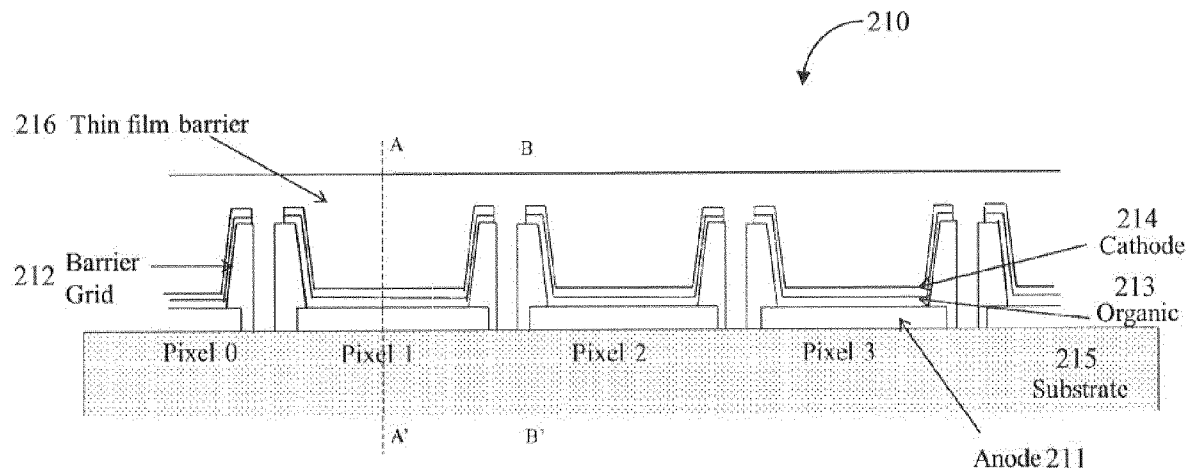


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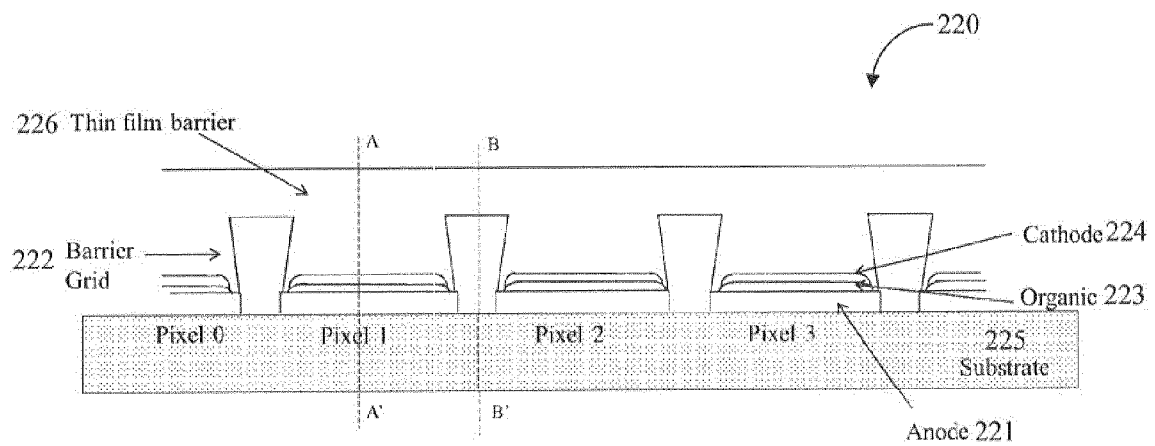


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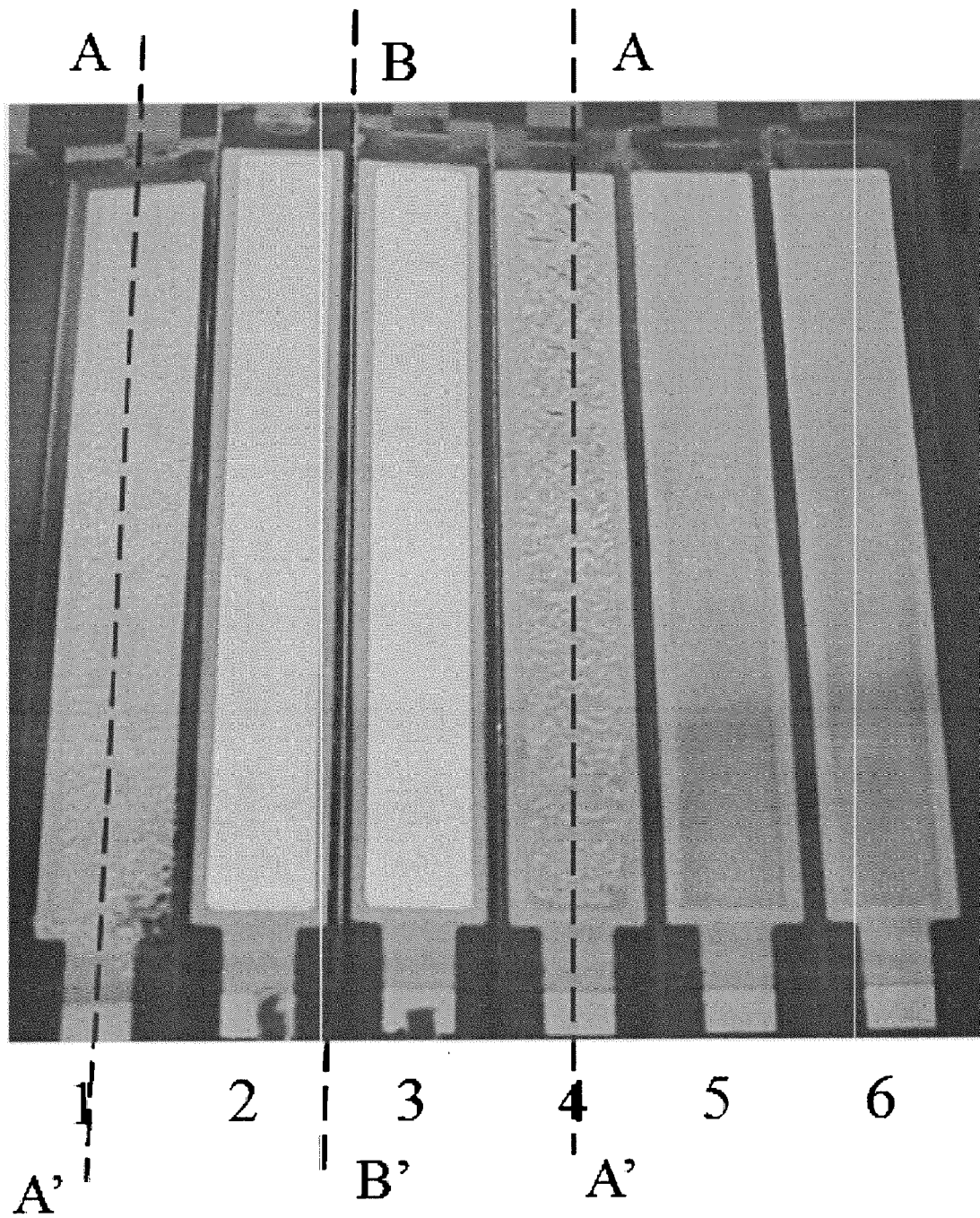


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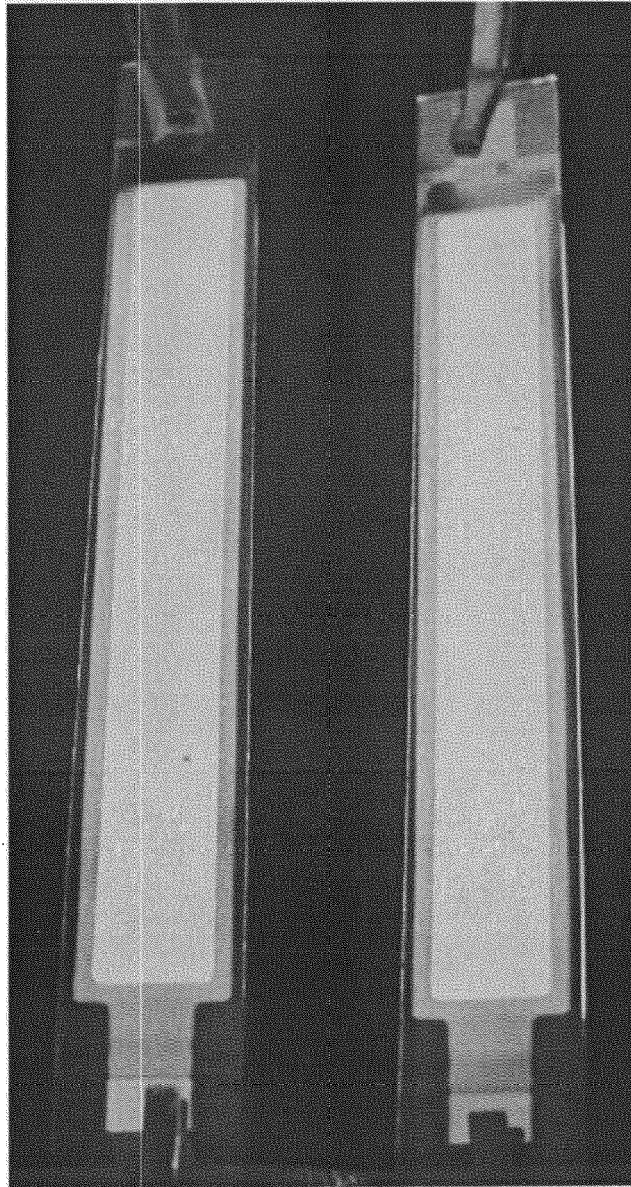


Figure 24

REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	密封隔离的OLED像素		
公开(公告)号	EP2927985A2	公开(公告)日	2015-10-07
申请号	EP2015161233	申请日	2015-03-27
[标]申请(专利权)人(译)	环球展览公司		
申请(专利权)人(译)	通用显示器公司		
当前申请(专利权)人(译)	通用显示器公司		
[标]发明人	HARIKRISHNA MOHAN SIDDHARTH QUINN WILLIAM E MA RUIQING KRALL EMORY WALSKI LUKE		
发明人	HARIKRISHNA MOHAN, SIDDHARTH QUINN, WILLIAM E. MA, RUIQING KRALL, EMORY WALSKI, LUKE		
IPC分类号	H01L51/52 H01L27/32		
CPC分类号	H01L27/3246 H01L51/5209 H01L51/5225 H01L51/5253 H01L27/3258 H01L27/326 H01L51/0097 H01L51/5012 H01L51/5206 H01L51/5221 H01L51/5246 H01L51/56 H01L2251/5338		
代理机构(译)	MAIWALD专利ADVOCATE GMBH		
优先权	61/970937 2014-03-27 US 14/661335 2015-03-18 US		
其他公开文献	EP2927985A3		
外部链接	Espacenet		

摘要(译)

公开了一种新颖的薄膜封装的OLED面板结构 (50) 和制造具有改善的保质期的面板的方法。 OLED面板 (50) 由多个OLED像素组成;每个 OLED像素单独密封并与其相邻像素隔离。 OLED像素的有机叠层 (53) 包含在其自身的气密封结构内, 通过在阻挡涂覆的基板 (55) 上制造结构并使用第一阻挡材料作为栅格 (52) 和第二阻挡层 (56) 来实现。) 用于封装整个OLED像素。第一阻挡材料 (52) 提供边缘密封, 而设置在像素上方的第二阻挡层 (56) 提供防止自上而下的水分扩散。通过隔离和密封单个像素;由于缺陷或颗粒, 分层, 破裂等引起的水分和氧气进入等任何损坏都可以有效地包含在像素内, 从而保护面板中的其他像素。

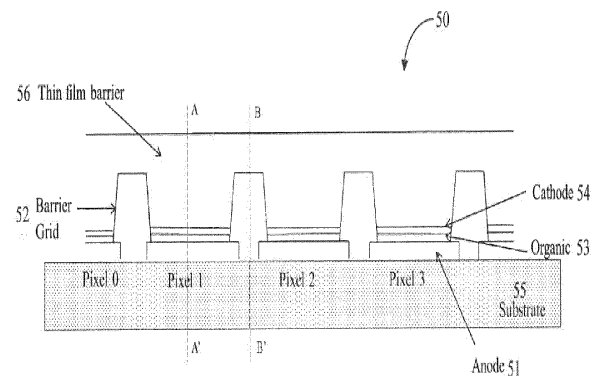


Figure 5