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(54) **Driving circuit for electroluminescent display device and its related method of operation**

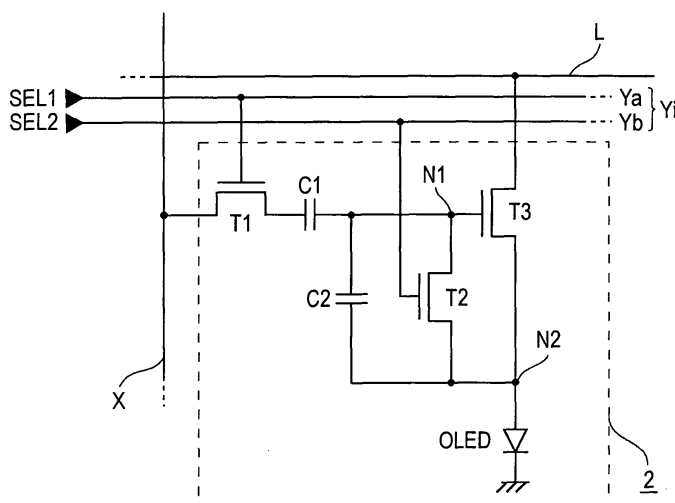
(57) A gate of a driving transistor is set to a offset level corresponding to the threshold of the driving transistor by an initializing current flowing between a source and a drain of the driving transistor or a compensating transistor for the driving transistor.

A conduction state of the driving transistor is set ac-

cording to a gate voltage of the gate of the driving transistor that corresponds to a data signal and the threshold of the driving transistor.

A current of which a level corresponds to the conduction state and of which the direction is opposite to the direction of the initializing current flows through driving transistor.

FIG. 2





EUROPEAN SEARCH REPORT

Application Number
EP 04 02 0280

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	SANFORD J L ET AL: "TFT AMOLED PIXEL CIRCUITS AND DRIVING METHODS" 2003 SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS. BALTIMORE, MD, MAY 20 - 22, 2003; [SID INTERNATIONAL SYMPOSIUM DIGEST OF TECHNICAL PAPERS], SAN JOSE, CA : SID, US, 20 May 2003 (2003-05-20), pages 10-13, XP001171706 * paragraphs [0004], [0005]; figures 5-7 *	1-6,19, 20,24, 26,40,41	INV. G09G3/32
X	----- US 2003/095087 A1 (LIBSCH FRANK R [US] ET AL) 22 May 2003 (2003-05-22) * figures 1-4 * * paragraphs [0023] - [0044] *	8-15, 39-41	
X	----- WO 98/48403 A (SARNOFF CORP [US]) 29 October 1998 (1998-10-29) * page 6, line 15 - page 8, line 2; figure 3 *	40,41	
X	----- US 2003/020705 A1 (KONDO SHIGEKI [JP] ET AL) 30 January 2003 (2003-01-30) * figure 9 * -----	16-18,25	TECHNICAL FIELDS SEARCHED (IPC) G09G
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 11 February 2009	Examiner Fulcheri, Alessandro
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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EPO FORM 1503 03.82 (P04C01)



Application Number

EP 04 02 0280

CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing claims for which payment was due.

☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due and for those claims for which claims fees have been paid, namely claim(s):

☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for those claims for which no payment was due.

LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.

☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.

☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:

☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:

☐ The present supplementary European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims (Rule 164 (1) EPC).



LACK OF UNITY OF INVENTION
SHEET B

Application Number

EP 04 02 0280

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. claims: 1-7, 19,20,24,26-29,36-38, 40,41

Method of driving a pixel circuit of an OLED display device.

The voltage level of the first terminal is set to a voltage level lower than the predetermined voltage level, the voltage of the counter electrode being fixed to the predetermined voltage level during at least a part of a period in which the third step is performed

2. claims: 8-15,21-23,30-35

Method of driving a pixel circuit of an OLED display device comprising a compensating transistor that has a third terminal, a fourth terminal, and a channel region disposed between the third terminal and the fourth terminal.

A potential difference between the third terminal and the fourth terminal is generated, such that the third terminal functions as a drain of the compensating transistor; and a voltage level of the fourth terminal during at least a part of a period in which the second step is performed being set to be different from a voltage level of the fourth terminal during at least a part of a period in which the first is performed.

3. claims: 16,17,18,25

Pixel circuit for OLED display device.

A first capacitor has a first electrode and a second electrode, a capacitance being formed between the first electrode and the second electrode, the first electrode being coupled to the gate of the driving transistor and the second electrode being coupled to the first terminal.

4. claim: 39

Method of driving a pixel circuit of an OLED display device.

A voltage of a node coupled to a gate of a driving transistor is set to an offset level according to the threshold value of the driving transistor by connecting electrically the gate and one of a source and a drain of the driving transistor to each other and applying a non-forward bias between the source and the drain.

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 04 02 0280

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

11-02-2009

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003095087 A1	22-05-2003	NONE	

WO 9848403 A	29-10-1998	EP 0978114 A1	09-02-2000
		JP 2002514320 T	14-05-2002
		KR 20050084509 A	26-08-2005

US 2003020705 A1	30-01-2003	WO 02075710 A1	26-09-2002

专利名称(译)	用于电致发光显示装置的驱动电路及其相关的操作方法		
公开(公告)号	EP1517290A3	公开(公告)日	2009-03-18
申请号	EP2004020280	申请日	2004-08-26
[标]申请(专利权)人(译)	精工爱普生株式会社		
申请(专利权)人(译)	SEIKO EPSON CORPORATION		
当前申请(专利权)人(译)	SEIKO EPSON CORPORATION		
[标]发明人	MIYAZAWA TAKASHI C O SEIKO EPSON CORPORATION		
发明人	MIYAZAWA, TAKASHI C/O SEIKO EPSON CORPORATION		
IPC分类号	G09G3/32 H01L51/50 G09G3/20 G09G3/30		
CPC分类号	G09G3/3233 G09G3/3291 G09G2300/0819 G09G2300/0852 G09G2300/0866 G09G2310/0251 G09G2310/0254 G09G2310/0256 G09G2310/0262 G09G2320/043		
优先权	2003306804 2003-08-29 JP 2004191357 2004-06-29 JP		
其他公开文献	EP1517290A2		
外部链接	Espacenet		

摘要(译)

通过在驱动晶体管的源极和漏极之间流动的初始化电流或用于驱动晶体管的补偿晶体管，将驱动晶体管的栅极设置为与驱动晶体管的阈值对应的偏移电平。根据驱动晶体管的栅极的栅极电压来设置驱动晶体管的导通状态，该栅极电压对应于数据信号和驱动晶体管的阈值。电平对应于导通状态并且其方向与初始化电流的方向相反的电流流过驱动晶体管。

FIG. 2

