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(54) **Active matrix electroluminescent display devices and their manufacture**

Elektrolumineszente Anzeigevorrichtungen mit aktiver Matrix und ihr Herstellungsverfahren

Dispositifs d'affichage électroluminescents à matrice active et leur fabrication

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Description

[0001] This invention relates to active-matrix electroluminescent display devices, particularly but not exclusively using light-emitting diodes of semiconducting conjugated polymer or other organic semiconductor materials. The invention also relates to methods of manufacturing such devices.

[0002] Such active-matrix electroluminescent display devices are known, comprising an array of pixels present on a circuit substrate, wherein each pixel comprises an electroluminescent element, typically of organic semiconductor material. The electroluminescent elements are connected to circuitry in the substrate, for example drive circuitry that includes supply lines and matrix addressing circuitry that includes addressing (row) and signal (column) lines. These lines are generally formed by thin-film conductor layers in the substrate. The circuit substrate also includes addressing and drive elements (typically thin-film transistors, hereafter termed "TFT"s) for each pixel.

[0003] In many such arrays, physical barriers of insulating material are present between neighbouring pixels in at least one direction of the array. Examples of such barriers are given in published United Kingdom patent application GB-A-2347017, published PCT patent application WO-A1-99/43031, published European patent applications EP-A-0 895 219, EP-A-1 096 568, and EP-A-1 102 317, the whole contents of which are hereby incorporated herein as reference material.

[0004] Such barriers are sometimes termed "walls", "partitions", "banks", "ribs", "separators", or "dams", for example. As can be seen from the cited references, they may serve several functions. They may be used in manufacture to define electroluminescent layers and/or electrode layers of the individual pixels and/or of columns of pixels. Thus, for example, the barriers prevent pixel overflow of conjugate polymer materials that may be ink-jet printed for red, green and blue pixels of a colour display or spin-coated for a monochrome display. The barriers in the manufactured device can provide a well-defined optical separation of pixels. They may also carry or comprise conductive material (such as upper electrode material of the electroluminescent element), as auxiliary wiring for reducing the resistance of (and hence the voltage drops across) the common upper electrode of the electroluminescent elements.

[0005] Very good image quality is achievable active-matrix electroluminescent displays with switched current mirror pixel circuits. Such a display device is disclosed in published United States patent application US-A-2001/0052606 (Philips ref: PHNL000281), the whole contents of which are hereby incorporated herein as reference material. This requires the columns of the display to be addressed with very small currents over the line time of the display. In the case of large displays the column capacitance becomes high, which means that the time constant for addressing the pixels to the correct current level becomes large. High resolutions for the display make the situation even more difficult by shortening the line time.

[0006] It is an aim of the present invention to exploit, develop, adapt and/or extend particular features of active-matrix electroluminescent display devices, so as to reduce such problems relating to the signal lines (column conductors), in a manner that is compatible with the basic device structure, its layout and its electronics.

[0007] According to one aspect of the present invention, there is provided an active-matrix electroluminescent display device having the features set out in Claim 1.

[0008] In accordance with the invention, the physical barriers between pixels are formed with electrically-conductive material (typically metal), that is used to provide at least part of the signal lines (column conductors) at a higher level than the circuit substrate. Thus, the column capacitance issues are transferred from within the circuit substrate (where they are severely constrained by circuitry layout) to the much freer environment of the pixel barriers on the substrate. This transfer readily permits a reduction in column capacitance and hence in the time constant for addressing pixels to the correct current level. The conductive barrier material is connected with the matrix addressing circuitry within the circuit substrate, while also being insulated at least at the sides of the barriers adjacent to the electroluminescent elements.

[0009] Much versatility is possible in accordance with the invention. Various structural features can be adopted for the pixel barriers. Thus, the barriers may be predominantly of conductive material or insulating material and may have insulating and/or conducting coatings. Preferably an inter-capacitance guard line is included at least between the signal lines of the barriers and the circuitry of the circuit substrate. A voltage buffer may be connected between the signal line and the guard line to keep the voltage therebetween near zero.

[0010] According to another aspect of the present invention, there are also provided advantageous methods of manufacturing such an active-matrix electroluminescent display device.

[0011] Various advantageous features and feature-combinations in accordance with the present invention are set out in the appended Claims. These and others are illustrated in embodiments of the invention that are now described, by way of example, with reference to the accompanying diagrammatic drawings, in which:

Figure 1 is a circuit diagram for four pixel areas of an active-matrix electroluminescent display device which can be provided with conductive barrier material for its signal lines in accordance with the invention;

Figure 2 is a schematic section illustrating parasitic capacitances in a pixel area of a prior art type of display device;

Figure 3 is a cross-sectional view of part of the pixel array and circuit substrate of one embodiment of an active-matrix electroluminescent display device, showing one example of a conductive barrier construction for its signal lines in accordance with the invention;

Figure 4 is a sectional view of a device part with another example of a conductive barrier construction using a metal coating for its signal lines in accordance with the invention;

Figure 5 is a plan view of the layout of a conductive layer pattern of the circuit substrate of the Figure 4 device, for including a guard line in a particular embodiment of a device in accordance with the invention,

Figure 6 is a schematic section similar to that of Figure 2, but illustrating parasitic capacitances in a pixel area of the display device of Figure 4 and 5 in accordance with the invention;

Figure 7 is a circuit diagram of a voltage buffer arrangement for a guard line in a device embodiment such as that of Figures 4 to 6;

Figure 8 is a cross-sectional view of a conductive barrier construction that is similar to that of Figure 3, but with the additionally inclusion of a metal coating for a modified embodiment in accordance with the invention;

Figure 9 is a plan view of an example of layout features for a particular embodiment of a device in accordance with the invention, with transverse conductive barriers;

Figures 10 to 12 are sectional views of a device part such as that of Figure 3 at stages in its manufacture with one particular embodiment in accordance with the invention; and

Figure 13 is a sectional view a device part at the Figure 12 stage, illustrating a modification in the insulation of the conductive barrier material that is also in accordance with the present invention.

[0012] It should be noted that all the Figures are diagrammatic. Relative dimensions and proportions of parts of these Figures have been shown exaggerated or reduced in size, for the sake of clarity and convenience in the drawings. The same reference signs are generally used to refer to corresponding or similar features in modified and different embodiments.

Embodiments of Figures 1 and 3

[0013] The active-matrix electroluminescent display device of the Figures 1 and 3 embodiments comprises an array of pixels 200 on a circuit substrate 100 with matrix addressing circuitry. Physical barriers 210 are present between at least some of the neighbouring pixels in at least one direction of the array. At least some of these barriers 210 are constructed with conductive barrier material 240 that is used as at least part of the signal lines (column conductors) 160 in accordance with the present invention. Apart from this special construction and use of the barriers 210 in accordance with the present invention, the display may be constructed using known device technologies and circuit technologies, for example as in the background references cited hereinbefore.

[0014] The matrix addressing circuitry comprises transverse sets of addressing (row) and signal (column) lines 150 and 160, respectively, as illustrated in Figure 1. An addressing element T2 (typically a thin-film transistor, hereafter termed "TFT") is incorporated at each interception of these lines 150 and 160. It should be understood that Figure 1 depicts, by way of example, one specific pixel circuit configuration. Other pixel circuit configurations are known for active matrix electroluminescent display devices. It should readily be understood that the present invention may be applied to the pixel barriers of such a device regardless of the specific pixel circuit configuration of the device.

[0015] As illustrated in Figure 1, each pixel 200 comprises a current-driven electroluminescent element 25 (21,22,23), typically a light-emitting diode (LED) of organic semiconductor material. The LED 25 is connected in series with a drive element T1 (typically a TFT) between two voltage supply lines 140 and 230 of the array. These two supply lines are typically a power supply line 140 (with voltage Vdd) and a ground line 230 (also termed "return line"). Light emission from the LED 25 is controlled by the current flow through the LED 25, as altered by its respective drive TFT T1.

[0016] Each row of pixels is addressed in turn in a frame period by means of a selection signal that is applied to the relevant row conductor 150 (and hence to the gate of the addressing TFTs T2 of the pixels of that row). This signal turns on the addressing TFT T2, so loading the pixels of that row with respective data signals from the column conductors 160. These data signals are applied to the gate of the individual drive TFT T1 of the respective pixel. In order to hold the resulting conductive state of the drive TFT T1, this data signal is maintained on its gate 5 by a holding capacitor Ch that is coupled between this gate 5 and the drive line 140,240. Thus, the drive current through the LED 25 of each pixel 200 is controlled by the driving TFT T1 based on a drive signal applied during the preceding address period and stored as a voltage on the associated capacitor Ch. In the specific example of Figure 1, T1 is shown as a P-channel TFT, whereas T2 is shown as an N-channel TFT.

[0017] This circuitry can be constructed with known thin-film technology. The substrate 100 may have an insulating glass base 10 on which an insulating surface-buffer layer 11, for example, of silicon dioxide is deposited. The thin-film circuitry is built up on the layer 11 in known manner

[0018] Figure 3 shows a particular example for the TFT T2 comprising: an active semiconductor layer 1 (typically of polysilicon); a gate dielectric layer 2 (typically of silicon dioxide); a gate electrode 5 (typically of polysilicon or aluminium); and metal electrodes 3 and 4 (typically of aluminium) which contact doped source and drain regions of the semiconductor layer 1 through windows (vias) in the over-lying insulating layer(s) 2 and 8.

[0019] Depending on the particular TFT (for example T1 or T2 or another TFT of the circuit substrate) and its circuit function, extensions of the electrodes 3, 4 and 5 may form, for example, interconnections between the elements T1, T2, Ch and LED 25, and/or at least part of the conductor lines 140, 150 and 160. Figure 3 shows a small-area local extension 160a of electrode 4 of T2 as a connection for the signal line 160. A line extension of gate electrode 5 of T2 forms the addressing (row) line 150. A line extension of electrode 4 of T1 (not shown in Figure 3) may form the power supply line 140.

[0020] The holding capacitor Ch may be formed similarly, in known manner, as a thin-film structure inside the circuit substrate 100.

[0021] The LED 25 typically comprises a light-emitting organic semiconductor material 22 between a lower electrode 21 and an upper electrode 23. In a preferred particular embodiment, semiconducting conjugated polymers may be used for the electroluminescent material 22. For a LED that emits its light 250 through the substrate 100, the lower electrode 21 may be an anode of indium tin oxide (ITO), and the upper electrode 23 may be a cathode comprising, for example, calcium and aluminium. Figure 3 illustrates a LED construction in which the lower electrode 21 is formed as a thin film in the circuit substrate 100. The subsequently-deposited organic semiconductor material 22 contacts this thin-film electrode layer 21 at a window 12a in a planar insulating layer 12 (for example of silicon nitride) that extends over the thin-film structure of the substrate 100.

[0022] As in known devices, the device of Figures 1 and 3 in accordance with the present invention include physical barriers 210, between at least some of the neighbouring pixels in at least one direction of the array. These barriers 210 may also be termed "walls", "partitions", "banks", "ribs", "separators", or "dams", for example. Depending on the particular device embodiment and its manufacture, they may be used in known manner, for example:

- to separate and prevent overflow of a polymer solution between the respective areas of the individual pixels 200 and/or columns of pixels 200, during the provision of semiconducting polymer layers 22;
- to provide a self-patterning ability on the substrate surface in the definition of the semiconducting polymer or other electroluminescent layers 22 for the individual pixels 200 and/or for columns of pixels 200 (and possibly even a self-separation of individual electrodes for the pixels, for example an individual bottom layer of the upper electrodes 23);
- to act as a spacer for a mask over the substrate surface during the deposition of at least an organic semiconductor material 22 and/or electrode material;
- to form opaque barriers 210 for a well-defined optical separation of the pixels 200 in the array, when light 250 is emitted through the top (instead of, or as well as, the bottom substrate 100).

[0023] Whatever their specific use in these known ways, the physical barriers 210 that extend parallel to the array columns in embodiments of the present invention are constructed and used in a special manner. Thus, the pixel barriers 210 of Figure 3 comprises metal 240 (or other electrically-conductive material 240) that provides at least part of the signal lines (column conductors) 160 at a higher level than the circuit substrate 100, thereby reducing the column capacitances.

[0024] This conductive barrier material 240 is insulated at its sides adjacent the LEDs 25 and is connected to the main electrode 4 of the addressing TFT at its extension 160a. As illustrated in Figure 3, these connections of the conductive barrier material 240 to the TFTs T2 occur at individual connection windows 12b in the intermediate insulating layer 12 at each pixel along the column. Thus, this conductive barrier material 240 is able to provide the signal lines 160 over most of their length adjacent to the pixels.

[0025] This special construction and use of the barriers 210 for the signal lines 160 in accordance with the invention permits the reduction of prior art column capacitances that are illustrated in Figure 2. Thus, Figure 2 illustrates the capacitances seen by the signal (column) line over each individual pixel in a typical prior art arrangement. In this known arrangement, the signal (column) lines 160X are formed entirely within the circuit substrate 100 as, for example, a line extension 160X of the TFT electrode 4. The barriers 210X are simply of insulating material (for example, an insulating polymer). There is a parasitic capacitance (C_D & C_{SN}) between the thin-film column line 160X and the LED upper electrode 23 (typically the cathode in a polymer LED 25), across the dielectrics 12 and 210X. High parasitic capacitances C_P and C_A occur between the thin-film column line 160X and the power supply line 140 and address (row) line 150, respectively, across the dielectric 8 (typically silicon nitride). As a result of this high column capacitance the time constant for addressing the individual pixels in this device arrangement to the correct current levels becomes unacceptably large for a large display.

[0026] The present invention avoids this problem by forming and using the pixel barriers 210 with metal 240 (or other electrically-conductive material 240), in the pixel areas, as the signal lines (column conductors) 160, i.e. at a higher level than the circuit substrate 100. Thus, as can be seen from Figure 3, the top planarising insulating layer 12 of the circuit substrate 100 is now interposed as an additional dielectric between the barrier-formed signal lines 160 and the thin-film lines 150 and 5,150 of the circuit substrate 100. Thus, the high parasitic capacitances C_P and C_A are reduced significantly.

[0027] Figure 3 illustrates one particular embodiment in which the pixel barriers 210 are predominantly of electrically-conductive material 240, 240x, preferably metal for very low resistivity (for example aluminium or copper or nickel or silver). Thus, these barriers 210 of Figure 3 comprise a bulk or core 240 of the conductive material that has an insulating coating 40 (for example of silicon dioxide or nitride) on its sides and on its top. Figure 3 shows, by way of example, the upper electrode 23 of the pixel LED 25 adjoining this insulating coating 40. Thus, the electrodes 23 may have a stripe-geometry in their layout across the pixel array. Alternatively, if sufficient thick insulator is used for the coating 40, the pixel array may have a common electrode 23 that extends also over the pixel barriers 210.

Alternative Column-line Barrier Embodiments of Figures 4 and 5

[0028] Figure 4 shows a modified embodiment wherein the barrier 210 is predominantly of insulating material 244. In this case, vias 244b are etched or milled through the insulating material 244 to the electrode area 160a, 4, in the circuit substrate 100. A metal coating 240 provides the conductive barrier material that extends on top of the insulating barrier 210 and in the vias 244b therethrough.

[0029] The metal coating 240 of this barrier 210 may be formed simultaneously with a main part 23a of the upper electrode 23 of the LED 25, in a self-aligned manner. Thus, a layer of metal may be deposited simultaneously for the metal coating 240 and electrode 23 which are separated by a shadow-masking effect of an overhang shape in the side of the barrier 210, as illustrated in Figure 4. This is one possible process embodiment for column-line barriers 210, 240 in accordance with the present invention. Figures 11 to 13 illustrate other process embodiments for column-line barriers 210, 240 that are predominantly of metal.

[0030] Figures 4 and 5 together illustrate a guard-line feature that can also be advantageously included in an embodiment of the present invention. In this embodiment, a thin-film conductor layer 9 (that can be formed simultaneously with TFT electrode areas 3, 4 and 160a) extends as an inter-capacitance guard line below the conductive barrier material 240 of the signal lines 160. Thus, this guard line 9 is present as a shield between the circuitry of the substrate 100 and the column lines 160 over most of their length. Figure 6 illustrates the capacitances now seen by the column line 160 over each individual pixel. Very low column capacitances can be achieved, particularly when the Figure 6 arrangement is used together with an advantageous buffer circuit feature such as that shown in Figure 7.

Particular Guard-line embodiments of Figures 6 and 7

[0031] In the Figure 6 arrangement, the respective capacitances C_P and C_A of the power line 140 and row line 150 are formed (across dielectric 8) with the guard line 9 (rather than with the column line 160 as in the prior art Figure 2). Furthermore, the respective capacitances C_{SN} and C_D of dielectrics 12 and 244 are formed between the guard line 9 and the column line 160 in the Figure 4 embodiment.

[0032] Very low column capacitance can now be achieved using the buffer circuit configuration of Figure 7. In this case, a voltage buffer 600 is connected between the column line 160 and the guard line 9. The basic circuit of Figure 7 can be of known type, apart from the inclusion of buffer 600 and guard line 9 and the barrier construction of the column line 160. Thus, 620 may represent a known type of current mirror pixel circuit, for example as disclosed in US-A-2001/0052606. Signals are supplied to the column line 160 by a column driver 610 of, for example, a know current sink type. The column driver 610 and the voltage buffer 600 can be implemented externally in an IC (integrated circuit) connected to the circuit substrate 100. Alternatively, they may be integrated internally on the circuit substrate 100, using polysilicon TFT technology.

[0033] The voltage buffer 600 takes as its input the signal voltage at the output of the column driver 610 and buffers it onto the guard line 9. As a result, the voltage between the column line 160 and guard line 9 is zero or nearly zero, so that no charge accumulates on this column-guard capacitance C_D, C_{SN} and all current is drawn from the pixel circuit 620. This allows rapid operation. The voltage buffer needs to charge the capacitances C_P and C_A between the guard line 9 and the respective power and address lines 140 and 150, but a low output impedance of the buffer 600 allows this to be achieved rapidly.

Multi-conductor barrier embodiments of Figures 8 and 9

[0034] The embodiment of Figure 8 is similar to that of Figure 3, in that the barrier 210 comprises a metal core 240x with an insulating coating 40a thereon. However, the Figure 8 embodiment additionally comprises a metal coating 240y that is present on the insulating coating 40a, over the top and sides of the core 240x.

[0035] This structure of Figure 8 is more versatile than that of Figure 3. It permits the metal core 240x and metal coating 240y to be used for different purposes. Thus, for example, the metal core 240x may provide the column (signal) line 160 as in Figure 3, and so be connected with the electrode 4 of TFT T2. The metal coating 240y may serve as a co-axial shield for the signal on the core line 240x. The metal coating 240y may be connected to part of a guard line 9b in the substrate 100 and/or to another circuit element, for example, of another TFT. Alternatively, the metal coating 240y may provide the column (signal) line 160, and the metal core 240x may form part of a guard line 9a.

[0036] Instead of shielding the column (signal) line 160, this multi-conductor structure 240x, 240y for the barrier 210 might be used elsewhere in the display for a different purpose, for example to overlap two lines such as 140 and 150, or to form an additional component. The metal coating 240y may be localised to specific locations along the barrier 210 where particular connections or components are required, for example at individual pixels or sub-pixels.

[0037] Of particular importance is an embodiment in which the multi-conductor structure 240x, 240y of Figure 8 is designed to form a capacitor with a capacitor dielectric 40a. Thus, separate and/or insulated lengths of the metal core 240x, insulating coating 40a and metal coating 240y may together form a capacitor connected between the substrate circuit elements 4, 5, etc. Such a capacitor may be, for example, the individual holding capacitor Ch for each respective pixel 200 which is connected between the supply line 140 (main electrode line 4 of TFT T1) and the gate line 5 of TFT T2 (and main electrode line 3 of TFT T1).

[0038] Figure 9 illustrates a suitable pixel layout for integrating such a multi-conductor barrier construction 240x, 240y as a holding capacitor Ch for each pixel area 200. In this case, the multi-conductor barrier construction 240x, 240y comprises insulated barrier lengths that extend transverse to the column-forming barriers 210 (240, 160).

[0039] Alternatively, the transverse barrier layout of Figure 9 may be adopted with barriers 210 and 210c each of which comprises a single metal conductor 240 (without the metal coating 240y) as in Figure 3 or as in Figure 4. In this case, the conductive barrier material 240 of the transverse barriers 210c may be connected to the gate line 5, 150 of TFT T2 to back-up and/or replace lengths of the addressing (row) lines 150. The line resistance of the row line can be significantly reduced in this way, due to the conductive barrier material 240 having a cross-sectional area that is at least twice (possibly even an order of magnitude) larger than that of the conductor layer that typically provides a gate line 5(150) of a TFT in the circuit substrate 100. Furthermore, the gate line 5(150) is typically of doped polysilicon, whereas the conductive barrier material 240 is typically metal having a much higher conductivity.

<u>Process Embodiment of Figures 10 to 12</u>

[0040] Apart from constructing and using its barriers 210 with conductive material 240 for the signal lines 160, the active-matrix electroluminescent display of a device in accordance with the present invention may be constructed using known device technologies and circuit technologies, for example as in the cited background references.

[0041] Figures 10 to 12 illustrate novel process steps in a particular manufacturing embodiment. The thin-film circuit substrate 100 with its upper planar insulating layer 12 (for example, of silicon nitride) is manufactured in known manner. Connection windows (such as vias 12a, 12b, 12x, etc.) are opened in the layer 12 in known manner, for example by photolithographic masking and etching. However, in order to manufacture a device in accordance with the present invention, the pattern of these vias include the vias 12b, 12x, 12y that expose elements 4, 5, etc. for bottom connection with the conductive barrier material 240, 240x, 240y etc. The resulting structure is illustrated in Figure 10. This stage is common regardless of whether the barriers 210 have a metal core as in Figures 3 and 8 or are predominantly of insulating material as in Figure 4.

[0042] The formation of barriers 210 predominantly of insulating material has been described above with reference to Figure 4. Suitable process steps for barriers 210 with a metal core will now be described with reference to Figures 11 and 12.

[0043] In this case, electrically-conductive material for the barriers 210 is deposited on the insulating layer 12 at least in its vias 12a, 12b etc. The desired lengths and layout pattern for the barriers 210 is obtained using known masking techniques. Figure 11 illustrates an embodiment in which at least the bulk 240 of the conductive barrier material (for example, copper or nickel or silver) is deposited by plating. In this case, a thin seed layer 240a of, for example, copper or nickel or silver is first deposited over the insulating layer 12 and its vias 12a, 12b, 12x etc, the barrier layout pattern is defined with a photolithographic mask, and then the bulk 240 of the conductive barrier material is plated to the desired thickness. The resulting structure is illustrated in Figure 11.

[0044] Then, using CVD (chemical vapour deposition), insulating material (for example silicon dioxide or silicon nitride) is deposited for the insulating coating 40. The deposited material is left on the sides and top of the conductive barrier material by patterning using known photolithographic masking and etching techniques, as illustrated in Figure 12.

[0045] Thereafter the manufacture is continued in known manner. Thus, for example, conjugate polymer materials 22 may be ink-jet printed or spin-coated for the pixels 200. The barriers 240,40 with their insulating coating 40 can be used in known manner to prevent polymer overflow from the pixel areas in between the physical barriers 240,40. The upper electrode material 23 is then deposited.

<u>Modified Process Embodiment of Figure 13</u>

[0046] This embodiment uses an anodisation treatment (instead of deposition) to provide the insulating coating 40 at least at the sides of the barriers 210 adjacent to the pixel areas. Typically, the conductive barrier material 240 may comprise aluminium. The desired lengths and layout pattern of the deposited aluminium can be defined using known photolithographic masking and etching techniques. Figure 13 shows the photolithically-defined etchant-mask 44 retained on the top of the aluminium barrier pattern 240.

[0047] Then, an anodic insulating coating of aluminium oxide is formed on at least the sides of the aluminium barrier material 240 using known anodisation techniques. Thus, no extra mask is needed to define the layout for this coating 40.

[0048] As illustrated in Figure 13, the mask 44 can be retained during this anodisation, in areas where it is desired to protect and form an un-insulated top connection area 240t. In these areas, the anodic coating is formed at only the sides of the aluminium barrier pattern 240. The mask 44 may be removed before this anodisation, from areas where the anodic coating is required at both the sides and top of the aluminium barrier pattern 240. Alternatively, the mask 44 of an insulating polymer or, for example, silicon dioxide or nitride may be retained in these areas where insulation is desired over the top of the barrier 210(240,40) in the manufactured device.

[0049] In the embodiments described so far, the conductive barrier material 240 is a thick opaque metal, for example, aluminium, copper, nickel or silver. However, other conductive materials 240 may be used, for example a metal silicide or (less advantageously) a degenerately-doped polysilicon both of which may be surface-oxidised to form the insulating coating 40. If transparent barriers 210 are required, then ITO may be used for the conductive barrier material 240.

Claims

1. An active-matrix electroluminescent display device comprising: a circuit substrate (100) on which an array of pixels is present with physical barriers (210) between at least some of the neighboring pixels (200) in at least one direction of the array, each pixel comprising an electroluminescent element (25), the circuit substrate comprising matrix addressing circuitry that provides pixel addressing via transverse addressing and signal lines, the physical barriers (210) comprising conductive barrier material (240), **characterized in that** the conductive barrier material (240) provides at least part of the signal lines (160) at a higher level than the circuit substrate (100), the conductive barrier material (240) is connected with the matrix addressing circuitry of the circuit substrate (100) via contact windows (12a) in an intermediate insulating layer (12) on the circuit substrate (100), and the conductive barrier material (240) is insulated at least at the sides of the physical barriers (210) adjacent to the electroluminescent elements (25).

2. A device according to Claim 1, wherein the conductive barrier material (240) provides the signal lines (160) over most of their length adjacent to the pixels (200) to reduce parasitic capacitance in the circuit substrate (100), and the conductive barrier material is connected to the matrix addressing circuitry of the circuit substrate via individual contact windows for each pixel of the line.

3. A device according to Claim 1 or 2, wherein a conductor layer in the circuit substrate extends below the conductive barrier material of the signal lines as an inter-capacitance guard line (9) between the signal lines (160) and the circuitry of the circuit substrate (100).

4. A device according to Claim 3, wherein a voltage buffer is connected between the signal line (160) and the guard line (9).

5. A device according to any one of the preceding Claims, wherein the physical barrier (210) comprises a metal coating that provides the conductive barrier material (240) of the signal lines (160) and that is connected to the pixels via respective circuit elements in the substrate (100).

6. A device according to Claim 5, wherein the physical barrier (210) is predominantly of insulating material through which vias extend for connection with the electrode connections for the matrix addressing circuitry at the contact windows (12a) of the intermediate insulating layer (12), and wherein the metal coating extends on top of the physical barrier (210) and in the vias through the physical barrier (210).

7. A device according to Claim 5, wherein there is an insulating coating on at least the sides of the metal coating as insulation adjacent to the electroluminescent elements.

8. A device according to any one of Claims 1 to 4, wherein the physical barrier (210) comprises a metal core that provides the conductive barrier material (240) of the signal lines (160), which metal core is connected to the pixels (200) via respective circuit elements in the substrate and has an insulating coating on at least its sides.

9. A device according to Claim 8, wherein a metal coating is present over the insulating coating over the top and sides of the metal core.

10. A device according to any one of the preceding Claims, wherein additional barriers extend parallel to the addressing lines and comprise additional conductive barrier material (240Y) that is insulated from the conductive barrier material (240X) of the signal lines (160), and the additional conductive barrier material (240Y) is connected via contact windows to parts of the addressing lines in the substrate (100) to reduce voltage drops along the addressing lines.

11. A device according to any one of the preceding Claims, wherein the electroluminescent element (200) is a light-emitting diode (25) of organic semiconductor material.

12. A method of manufacturing an active-matrix electroluminescent display device according to any one of the preceding Claims, including the steps of:

(a) opening contact windows (12a) in the intermediate insulating layer (12) on the circuit substrate (100) to expose electrode connections for the matrix addressing to circuitry in the circuit substrate (100);
(b) forming the physical barriers (210) on the circuit substrate with insulation at least at the sides of the physical barriers adjacent to the pixel areas (200); and
(c) providing the electroluminescent elements in the pixel areas (200) in between the physical barriers (210),

in which method electrically-conductive material (240) is deposited as a part of the physical barriers (210) to provide at least part of the signal lines (160) at a higher level than the circuit substrate (100), which electrically-conductive material (240) connects with the electrode connections for the matrix addressing circuitry via the contact windows (12a) of the intermediate insulating layer (12).

13. A method according to Claim 12, wherein the step (b) involves forming the physical barrier (210) predominantly of the electrically-conductive material (240), and an insulating coating (40) is deposited on at least the sides of this conductive barrier material.

14. A method according to Claim 13, wherein at least the bulk of the conductive barrier material (240) is deposited by plating.

15. A method according to Claim 13, wherein the conductive barrier material (240) comprises aluminum, and the insulating coating (40) is formed on at least the sides of the aluminum barrier material by anodization.

16. A method according to Claim 12, wherein the step (b) involves forming the physical barrier (210) predominantly of insulating material through which vias extend for connection with the electrode connections for the matrix addressing circuitry at the contact windows (12a) of the intermediate insulating layer (12), and wherein the electrically-conductive material (240) of the signal lines (160) is deposited as a conductive coating on top of the physical barrier (240) and in the vias through the physical barrier (210).

17. A method according to Claim 16, wherein the conductive coating for the signal lines (160) and an upper electrode of the electroluminescent element (200) are deposited simultaneously and are separated by a shadow-masking effect of an overhang shape in the side of the physical barrier (210).

Patentansprüche

1. Elektrolumineszenzanzeigeeinrichtung mit aktiver Matrix, welche aufweist: ein Schaltungssubstrat (100), auf dem sich ein Array aus Pixeln mit physikalischen Barrieren (210) zwischen zumindest einigen der benachbarten Pixel (200) in mindestens einer Richtung des Arrays befindet, wobei jedes Pixel ein Elektrolumineszenzelement (25) umfasst, wobei das Schaltungssubstrat eine Matrixadressierschaltung aufweist, die eine Pixeladressierung über transversale Adressier- und Signalleitungen vorsieht, wobei die physikalischen Barrieren (210) leitendes Barrierematerial (240) enthalten, **dadurch gekennzeichnet, dass** das leitende Barrierematerial (240) zumindest einen Teil der Signalleitungen (160) auf einer höheren Ebene als das Schaltungssubstrat (100) vorsieht, das leitende Barrierematerial (240) über Kontaktfenster (12a) in einer isolierenden Zwischenschicht (12) auf dem Schaltungssubstrat (100) mit der Matrixadressierschaltung des Schaltungssubstrats (100) verbunden ist, und das leitende Barrierematerial (240) zumindest auf den Seiten der physikalischen Barrieren (210) in Angrenzung an die Elektrolumineszenzelemente (25) isoliert ist.

2. Einrichtung nach Anspruch 1, wobei das leitende Barrierematerial (240) die Signalleitungen (160) über den größten Teil ihrer Länge in Angrenzung an die Pixel (200) vorsieht, um parasitäre Kapazität in dem Schaltungssubstrat (100) zu reduzieren, und das leitende Barrierematerial über einzelne Kontaktfenster für jedes Pixel der Zeile mit der Matrixadressierschaltung des Schaltungssubstrats verbunden ist.

3. Einrichtung nach Anspruch 1 oder 2, wobei eine Leiterschicht in dem Schaltungssubstrat sich unterhalb des leitenden Barrierematerials der Signalleitungen als Zwischenkapazitäts-Schutzleitung (9) zwischen den Signalleitungen (160) und dem Schaltkreis des Schaltungssubstrats (100) erstreckt.

4. Einrichtung nach Anspruch 3, wobei ein Spannungspuffer zwischen der Signalleitung (160) und der Schutzleitung (9) geschaltet ist.

5. Einrichtung nach einem der vorangegangenen Ansprüche, wobei die physikalische Barriere (210) eine Metallbeschichtung aufweist, welche das leitende Barrierematerial (240) der Signalleitungen (160) vorsieht und über jeweilige Schaltkreiselemente in dem Substrat (100) mit den Pixeln verbunden ist.

6. Einrichtung nach Anspruch 5, wobei die physikalische Barriere (210) vorwiegend aus Isoliermaterial besteht, durch welches sich Durchkontakte zur Verbindung mit den Elektrodenanschlüssen für die Matrixadressierschaltung an den Kontaktfenstern (12a) der isolierenden Zwischenschicht (12) erstrecken, und wobei sich die Metallbeschichtung auf der Oberseite der physikalischen Barriere (210) und in den Durchkontakten durch die physikalische Barriere (210) erstreckt.

7. Einrichtung nach Anspruch 5, wobei eine Isolationsbeschichtung auf zumindest den Seiten der Metallbeschichtung als Isolation in Angrenzung an die Elektrolumineszenzelemente vorgesehen ist.

8. Einrichtung nach einem der Ansprüche 1 bis 4, wobei die physikalische Barriere (210) einen Metallkern aufweist , welcher das leitende Barrierematerial (240) der Signalleitungen (160) vorsieht, wobei der Metallkern über jeweilige Schaltkreiselemente in dem Substrat mit den Pixeln (200) verbunden ist und zumindest auf seinen Seiten eine Isolationsbeschichtung aufweist.

9. Einrichtung nach Anspruch 8, wobei über der Isolationsbeschichtung über der Oberseite und den Seiten des Metallkerns eine Metallbeschichtung vorgesehen ist.

10. Einrichtung nach einem der vorangegangenen Ansprüche, wobei sich zusätzliche Barrieren parallel zu den Adressierleitungen erstrecken und zusätzliches, leitendes Barrierematerial (240Y) enthalten, welches von dem leitenden Barrierematerial (240X) der Signalleitungen (160) isoliert ist, und das zusätzliche, leitende Barrierematerial (240Y) über Kontaktfenster mit Teilen der Adressierleitungen in dem Substrat (100) verbunden ist, um Spannungsabfälle entlang den Adressierleitungen zu reduzieren.

11. Einrichtung nach einem der vorangegangenen Ansprüche, wobei das Elektrolumineszenzelement (200) eine Licht emittierende Diode (25) aus organischem Halbleitermaterial ist.

12. Verfahren zur Herstellung einer Aktivmatrix-Elektrolumineszenzanzeigeeinrichtung nach einem der vorangegangenen Ansprüche, wonach:

(a) Kontaktfenster (12a) in der isolierenden Zwischenschicht (12) auf dem Schaltungssubstrat (100) geöffnet werden, um Elektrodenanschlüsse für die Matrixadressierschaltung in dem Schaltungssubstrat (100) freizulegen,
(b) die physikalischen Barrieren (210) auf dem Schaltungssubstrat mit Isolation zumindest auf den Seiten der physikalischen Barrieren in Angrenzung an die Pixelflächen (200) gebildet werden, und
(c) die Elektrolumineszenzelemente auf den Pixelflächen (200) zwischen den physikalischen Barrieren (210) vorgesehen werden,

wobei das elektrisch leitende Material (240) als Teil der physikalischen Barrieren (210) aufgebracht wird, um zumindest einen Teil der Signalleitungen (160) auf einer höheren Ebene als das Schaltungssubstrat (100) vorzusehen, wobei das elektrisch leitende Material (240) über die Kontaktfenster (12a) der isolierenden Zwischenschicht (12) mit den Elektrodenanschlüssen für die Matrixadressierschaltung verbindet.

13. Verfahren nach Anspruch 12, wobei gemäß Schritt (b) die physikalische Barriere (210) überwiegend aus dem elektrisch leitenden Material (240) gebildet wird und eine Isolationsbeschichtung (40) auf zumindest den Seiten dieses leitenden Barrierematerials aufgebracht wird.

14. Verfahren nach Anspruch 13, wobei zumindest der Großteil des leitenden Barrierematerials (240) durch Plattierung aufgebracht wird.

15. Verfahren nach Anspruch 13, wobei das leitende Barrierematerial (240) Aluminium enthält und die Isolationsbeschichtung (40) auf zumindest den Seiten des Aluminiumbarrierematerials durch Anodisierung gebildet wird.

16. Verfahren nach Anspruch 12, wobei gemäß Schritt (b) die physikalische Barriere (210) überwiegend aus Isolationsmaterial gebildet wird, durch welches sich Durchkontakte zur Verbindung mit den Elektrodenanschlüssen für die Matrixadressierschaltung an den Kontaktfenstern (12a) der isolierenden Zwischenschicht (12) erstrecken, und wobei das elektrisch leitende Material (240) der Signalleitungen (160) als leitende Beschichtung (240) auf der Oberseite der physikalischen Barriere und in den Durchkontakten durch die physikalische Barriere (210) aufgebracht wird.

17. Verfahren nach Anspruch 16, wobei die leitende Beschichtung für die Signalleitungen (160) und eine obere Elektrode des Elektrolumineszenzelements (200) gleichzeitig aufgebracht und durch einen Schattenmaskierungseffekt überhängender Form auf der Seite der physikalischen Barriere (210) getrennt werden.

Revendications

1. Dispositif d'affichage électroluminescent à matrice active comprenant : un substrat de circuits (100) sur lequel se trouve un groupement de pixels avec des barrières physiques (210) entre une partie au moins des pixels voisins (200) dans un sens au moins du groupement, chaque pixel comprenant un élément électroluminescent (25), le substrat de circuits comprenant des circuits d'adressage matriciel qui permettent l'adressage des pixels par le biais de lignes d'adressage et de signal transversales, les barrières physiques (210) comprenant un matériau de barrière conducteur (240), **caractérisé en ce que** le matériau de barrière conducteur (240) fournit une partie au moins des lignes de signal (160) à un niveau supérieur à celui du substrat de circuits (100), le matériau de barrière conducteur (240) est connecté aux circuits d'adressage matriciel du substrat de circuits (100) par le biais d'ouvertures de contact (12a) dans une couche isolante intermédiaire (12) sur le substrat de circuits (100), et le matériau de barrière conducteur (240) est isolé sur les côtés au moins des barrières physiques (210) jouxtant les éléments électroluminescents (25).

2. Dispositif suivant la revendication 1, dans lequel le matériau de barrière conducteur (240) fournit les lignes de signal (160) par-dessus la majeure partie de leur longueur jouxtant les pixels (200) pour réduire la capacité parasite dans le substrat de circuits (100), et le matériau de barrière conducteur est connecté aux circuits d'adressage matriciel du substrat de circuits par le biais d'ouvertures de contact individuelles pour chaque pixel de la ligne.

3. Dispositif suivant la revendication 1 ou 2, dans lequel une couche de conducteurs dans le substrat de circuits s'étend en dessous du matériau de barrière conducteur des lignes de signal comme ligne de garde inter-capacité (9) entre les lignes de signal (160) et les circuits du substrat de circuits (100).

4. Dispositif suivant la revendication 3, dans lequel un tampon de tension est connecté entre la ligne de signal (160) et la ligne de garde (9).

5. Dispositif suivant l'une quelconque des revendications précédentes, dans lequel la barrière physique (210) comprend un revêtement métallique qui fournit le matériau de barrière conducteur (240) des lignes de signal (160) et qui est connecté aux pixels par le biais d'éléments de circuit respectifs dans le substrat (100).

6. Dispositif suivant la revendication 5, dans lequel la barrière physique (210) est en grande partie faite d'un matériau isolant à travers lequel s'étendent des traversées pour sa connexion avec les connexions d'électrode pour les circuits d'adressage matriciel au niveau des ouvertures de contact (12a) de la couche isolante intermédiaire (12), et dans lequel le revêtement métallique s'étend au-dessus de la barrière physique (210) et dans les traversées à travers la barrière physique (210).

7. Dispositif suivant la revendication 5, dans lequel un revêtement isolant se trouve sur les côtés au moins du revêtement métallique comme isolant jouxtant les éléments électroluminescents.

8. Dispositif suivant l'une quelconque des revendications 1 à 4, dans lequel la barrière physique (210) comprend un noyau métallique qui fournit le matériau de barrière conducteur (240) des lignes de signal (160), lequel noyau métallique est connecté aux pixels (200) par le biais d'éléments de circuit respectifs dans le substrat et comporte un revêtement isolant sur ses côtés au moins.

9. Dispositif suivant la revendication 8, dans lequel un revêtement métallique est présent par-dessus le revêtement isolant sur le sommet et les côtés du noyau métallique.

10. Dispositif suivant l'une quelconque des revendications précédentes, dans lequel des barrières supplémentaires s'étendent parallèlement aux lignes d'adressage et comprennent un matériau de barrière conducteur (240Y) supplémentaire qui est isolé du matériau de barrière conducteur (240X) des lignes de signal (160), et le matériau de barrière conducteur (240Y) supplémentaire est connecté par le biais d'ouvertures de contact à des parties des lignes d'adressage dans le substrat (100) pour réduire les baisses de tension le long des lignes d'adressage.

11. Dispositif suivant l'une quelconque des revendications précédentes, dans lequel l'élément électroluminescent (200) est une diode lumineuse (25) d'un matériau semiconducteur organique.

12. Procédé de fabrication d'un dispositif d'affichage électroluminescent à matrice active suivant l'une quelconque des revendications précédentes, incluant les étapes suivantes :

(a) l'ouverture d'ouvertures de contact (12a) dans la couche isolante intermédiaire (12) sur le substrat de circuits (100) pour exposer des connexions d'électrode pour les circuits d'adressage matriciel dans le substrat de circuits (100) ;
(b) la formation des barrières physiques (210) sur le substrat de circuits avec une isolation sur les côtés au moins des barrières physiques jouxtant les zones de pixel (200), et
(c) la fourniture des éléments électroluminescents dans les zones de pixel (200) entre les barrières physiques (210) ;

procédé dans lequel un matériau conducteur de l'électricité (240) est déposé comme partie des barrières physiques (210) pour fournir une partie au moins des lignes de signal (160) à un niveau supérieur à celui du substrat de circuits (100), lequel matériau conducteur de l'électricité (240) est connecté aux connexions d'électrode pour les circuits d'adressage matriciel par le biais des ouvertures de contact (12a) de la couche isolante intermédiaire (12).

13. Procédé suivant la revendication 12, dans lequel l'étape (b) implique la formation de la barrière physique (210) faite en grande partie du matériau conducteur de l'électricité (240), et un revêtement isolant (40) est déposé sur les côtés au moins de ce matériau de barrière conducteur.

14. Procédé suivant la revendication 13, dans lequel la masse au moins du matériau de barrière conducteur (240) est déposée par placage.

15. Procédé suivant la revendication 13, dans lequel le matériau de barrière conducteur (240) comprend de l'aluminium, et le revêtement isolant (40) est formé par anodisation sur les côtés au moins du matériau de barrière en aluminium.

16. Procédé suivant la revendication 12, dans lequel l'étape (b) implique la formation de la barrière physique (210) faite en grande partie d'un matériau isolant à travers lequel s'étendent des traversées pour sa connexion avec les connexions d'électrode pour les circuits d'adressage matriciel au niveau des ouvertures de contact (12a) de la couche isolante intermédiaire (12), et dans lequel le matériau conducteur de l'électricité (240) des lignes de signal (160) est déposé comme revêtement conducteur audessus de la barrière physique (240) et dans les traversées à travers la barrière physique (210).

17. Procédé suivant la revendication 16, dans lequel le revêtement conducteur pour les lignes de signal (160) et une électrode supérieure de l'élément électroluminescent (200) sont déposés simultanément et sont séparés par un effet de masque perforé en surplomb dans le côté de la barrière physique (210).

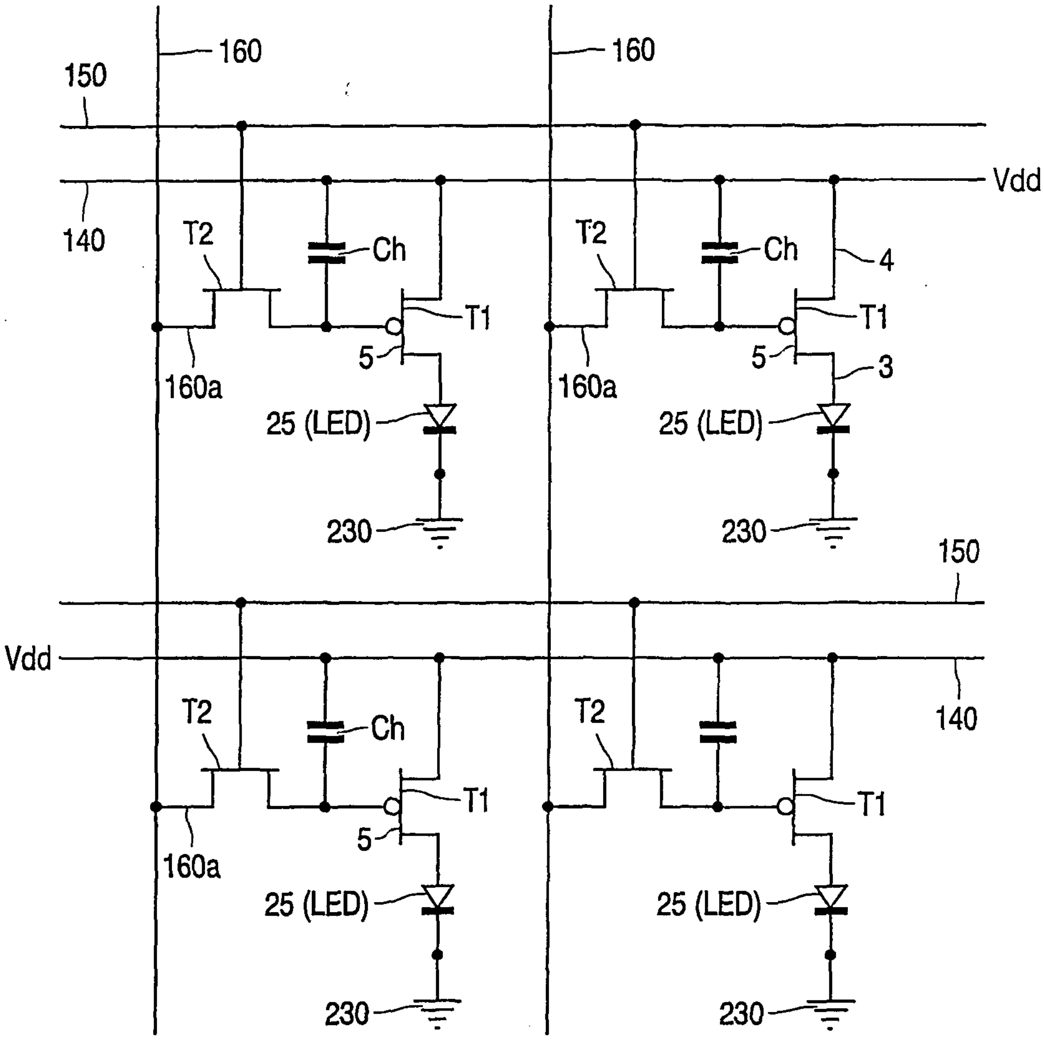
160
160
150
Vdd
140
T2
Ch
4
T1
5
3
160a
25 (LED)
230
150
Vdd
140
T2
Ch
T1
5
160a
25 (LED)
230

FIG. 1

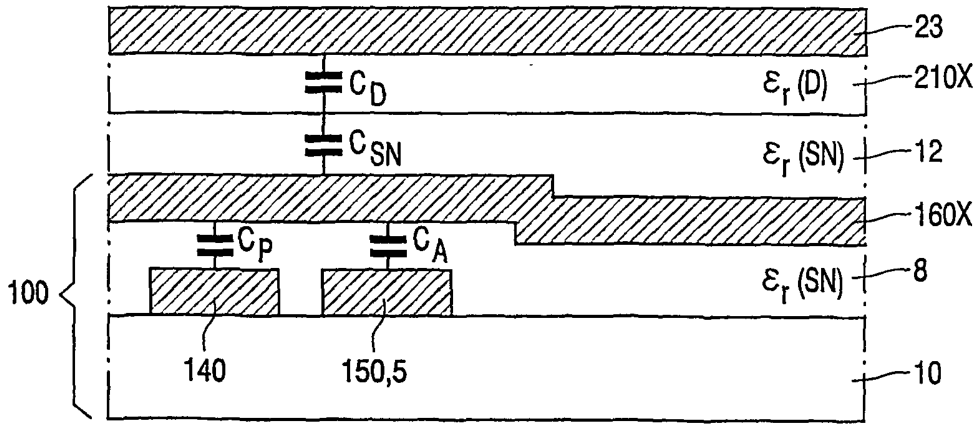
23
C_D
ε_r (D)
210X
C_{SN}
ε_r (SN)
12
160X
C_P
C_A
ε_r (SN)
8
100
140
150,5
10

FIG. 2

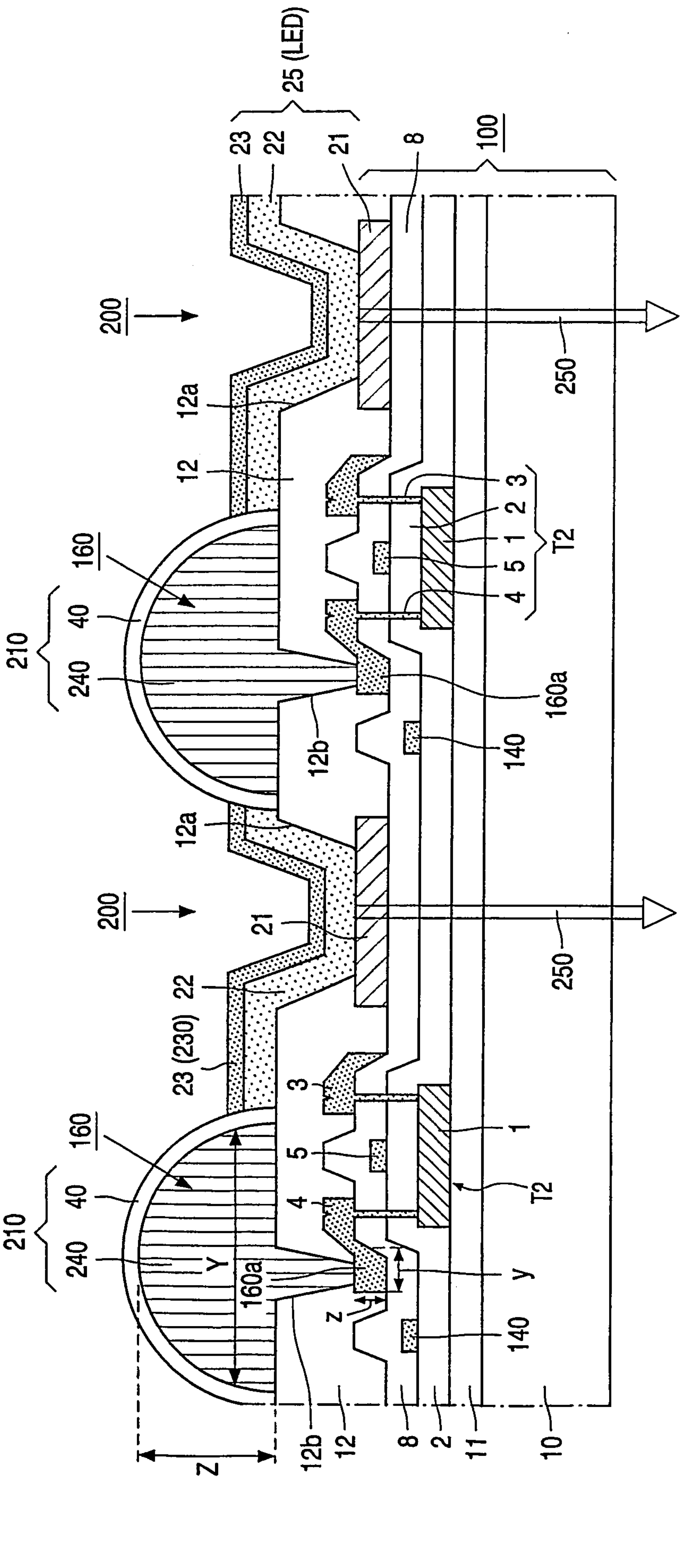
25 (LED)
23
22
21
8
100
200
12a
12
3
2
1
5
4
T2
160
40
210
240
160a
12b
140
250
23 (230)
Y
y
z
Z
11
10

FIG. 3

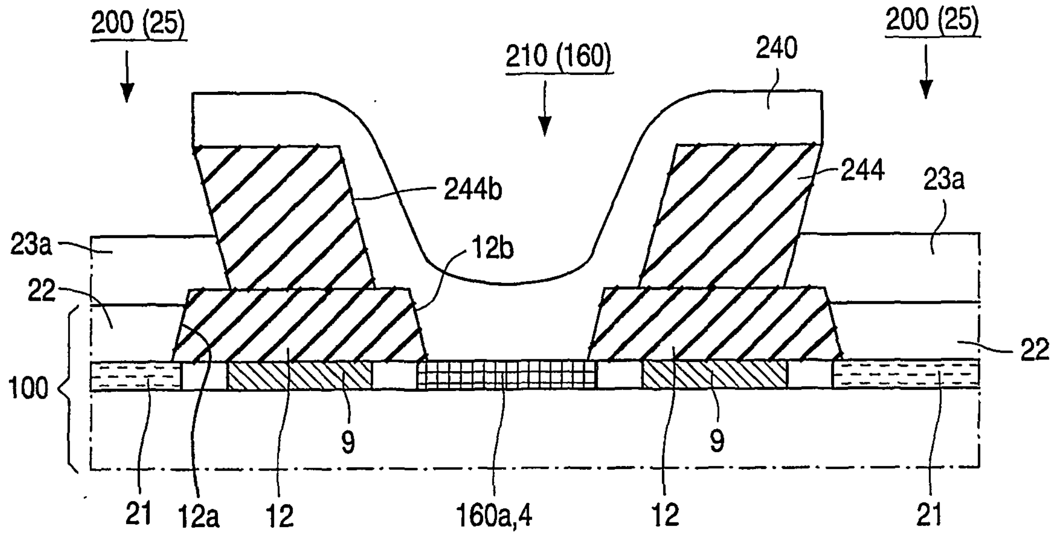

FIG. 4

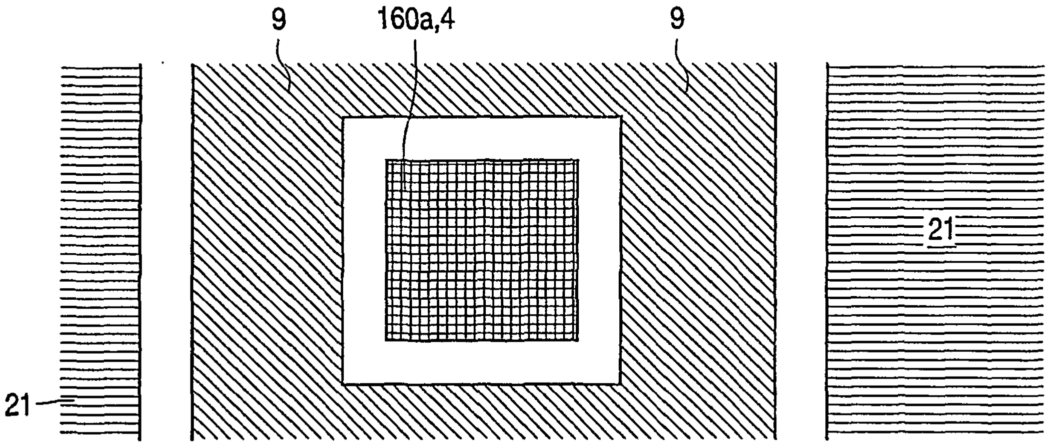

FIG. 5

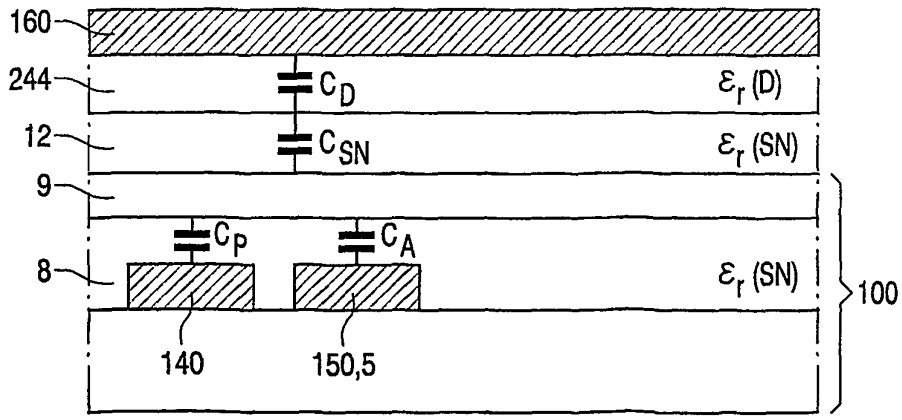

FIG. 6

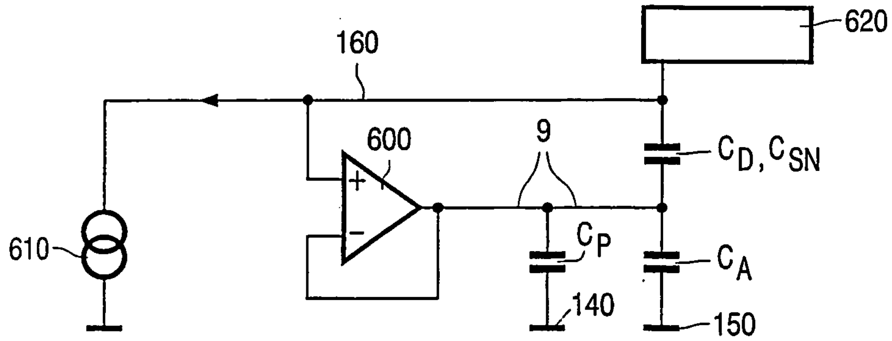

FIG. 7

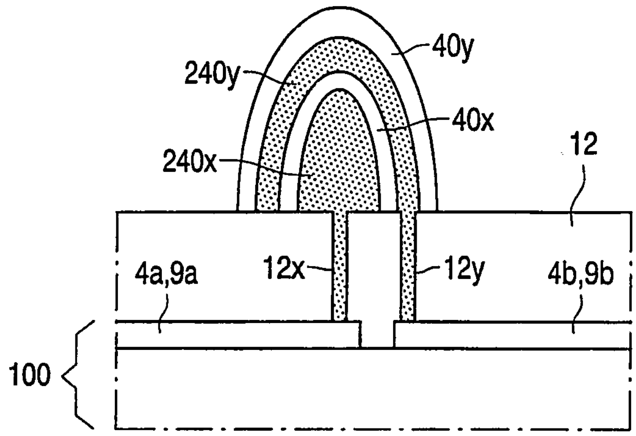

FIG. 8

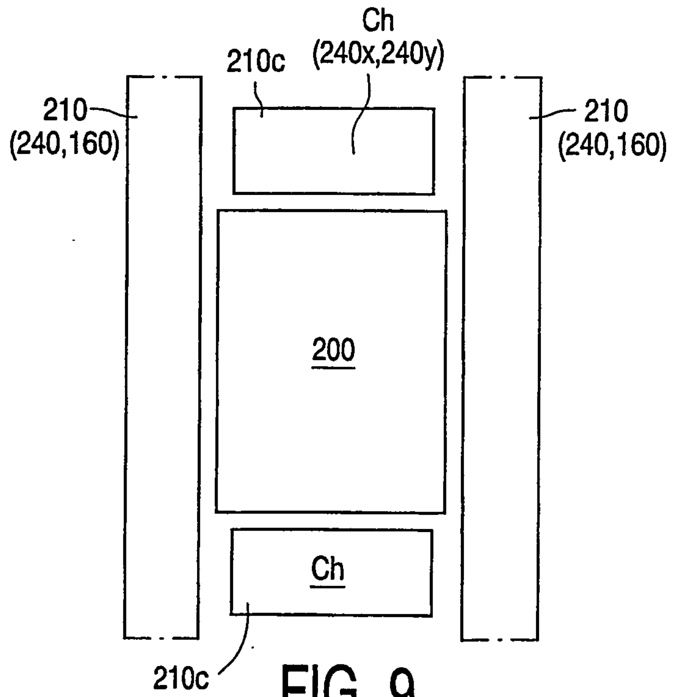

FIG. 9

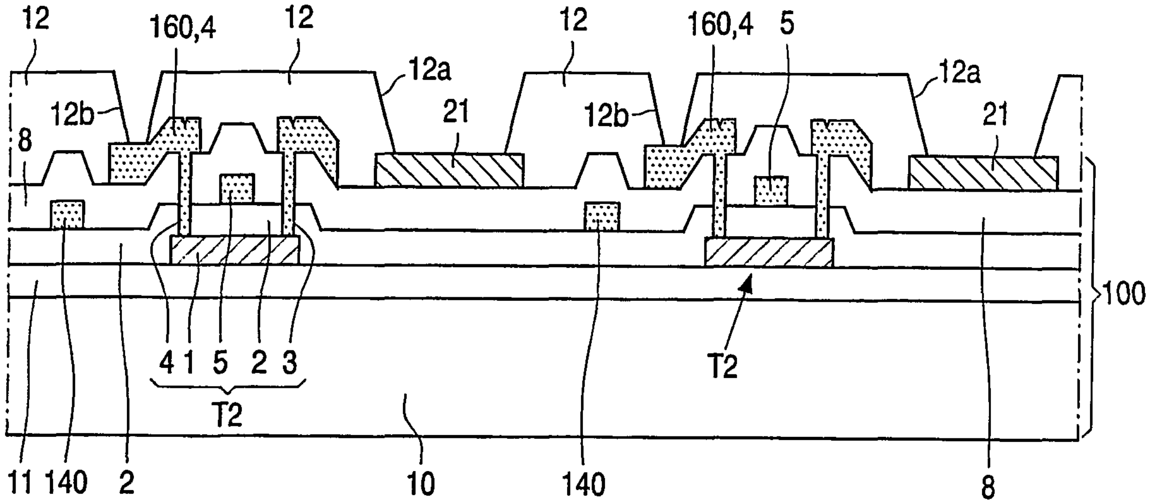
12
160,4
12
12
160,4
5
12a
12a
12b
21
12b
21
8
8
4 1 5 2 3
T2
T2
100
11 140 2
10
140
8

FIG. 10

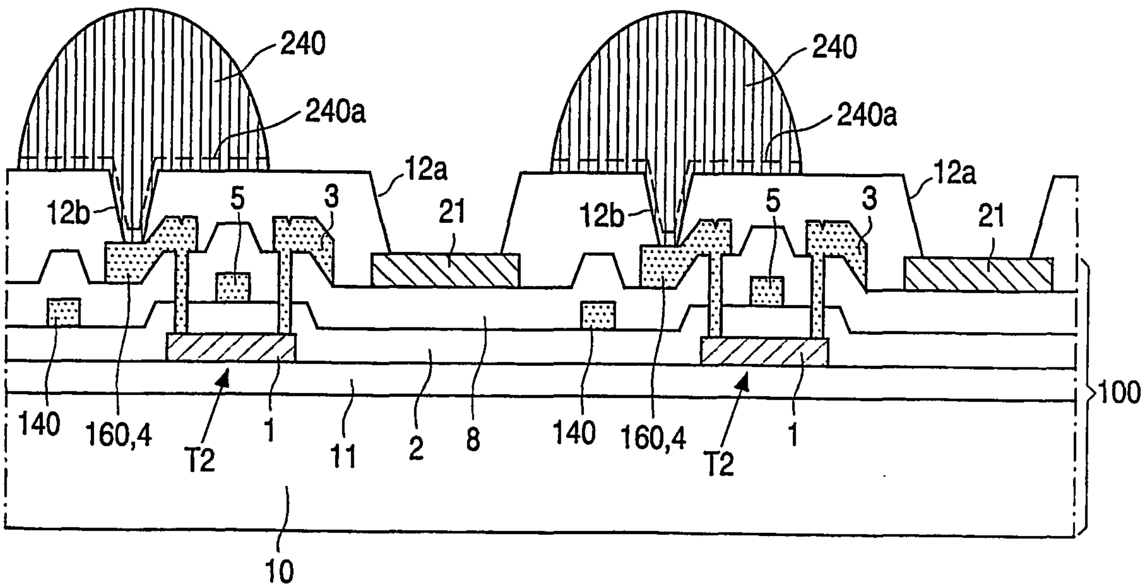
240
240
240a
240a
12a
12a
12b
5
3
21
12b
5
3
21
100
140
160,4
T2
1
11
2
8
140
160,4
T2
1
10

FIG. 11

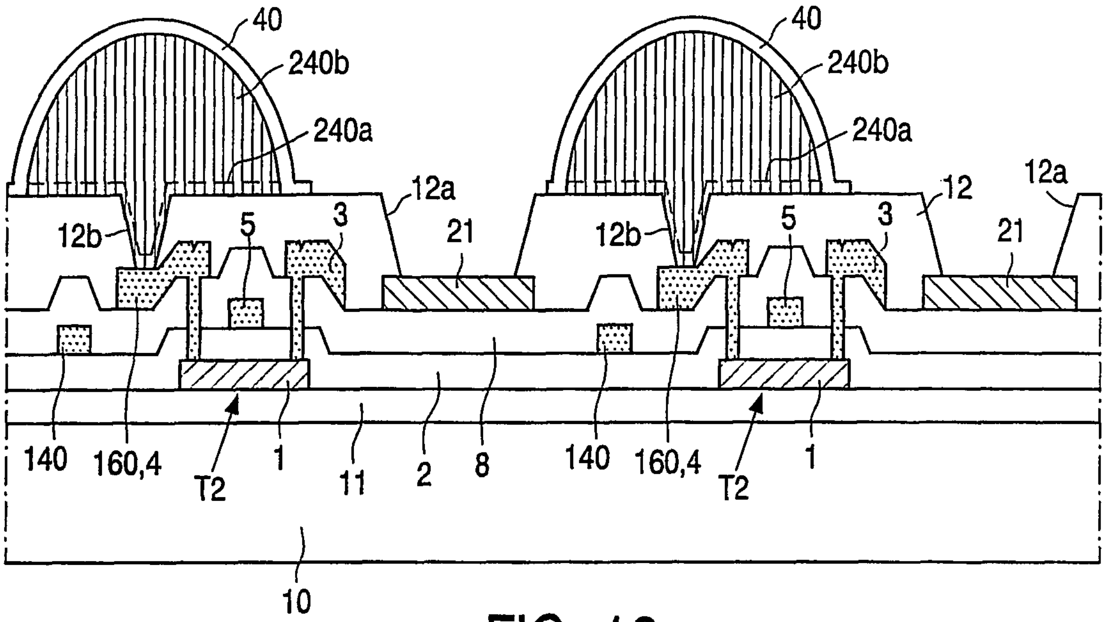
40
240b
240a
12a
12b
5
3
21
40
240b
240a
12
12a
12b
5
3
21
140
160,4
T2
1
11
2
8
140
160,4
T2
1
10

FIG. 12

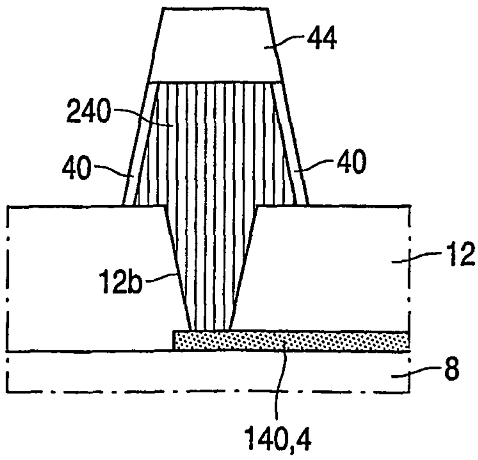
44
240
40
40
12
12b
8
140,4

FIG. 13

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- GB 2347017 A **[0003]**
- WO 9943031 A1 **[0003]**
- EP 0895219 A **[0003]**
- EP 1096568 A **[0003]**
- EP 1102317 A **[0003]**
- US 20010052606 A **[0005] [0032]**

专利名称(译)	有源矩阵电致发光显示装置及其制造		
公开(公告)号	[EP1490909B1](EP1490909B1)	公开(公告)日	2007-08-22
申请号	EP2003744455	申请日	2003-02-21
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司		
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当前申请(专利权)人(译)	皇家飞利浦电子N.V.		
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IPC分类号	H01L27/00 H05B33/22 G09F9/30 G09G3/30 H01L21/3205 H01L23/52 H01L27/32 H01L29/786 H01L51/50 H05B33/10 H05B33/12 H05B33/14		
CPC分类号	H01L27/124 H01L27/3246 H01L27/3276 H01L27/3279		
代理机构(译)	DAMEN，DANIEL马亭		
优先权	2002009559 2002-04-26 GB 2002006551 2002-03-20 GB 2002016058 2002-07-11 GB		
其他公开文献	EP1490909A1		
外部链接	Espacenet		

摘要(译)

物理屏障（210）存在于有源矩阵电致发光显示装置的电路基板（100）上的相邻像素（200）之间，特别是有机半导体材料的LED（25）。为了减少电路基板中的寄生电容，本发明利用金属或其他导电材料（240）形成这些屏障（210），所述金属或其他导电材料（240）提供比电路基板更高水平的至少部分信号线（160）。（100）。该导电阻挡材料（240）连接到基板（100）内的矩阵电路，但至少在与LED（25）相邻的侧面处绝缘（40）。优选地，电容器保护线（9）包括在信号线（160）和基板（100）中的电路之间的电路基板（100）中。

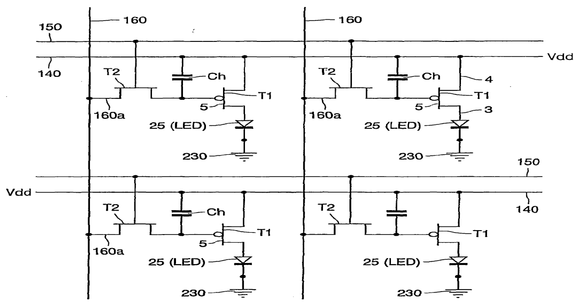

FIG. 1

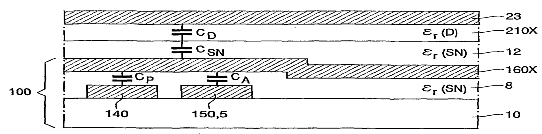

FIG. 2