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(71) Applicant: **Sanyo Electric Co., Ltd.**
Moriguchi-shi, Osaka-fu 570-8677 (JP)

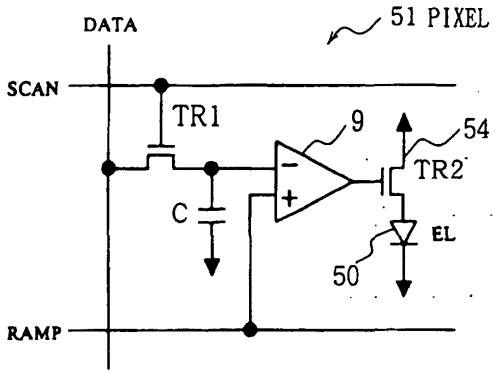
(72) Inventors:
- **YAMASHITA, Atsuhiro,**
  SANYO ELECTRIC CO., LTD.
  Moriguchi-shi, Osaka 570-8677 (JP)
- **MURATA, Haruhiko,**
  SANYO ELECTRIC CO., LTD.
  Moriguchi-shi, Osaka 570-8677 (JP)
- **MORI, Yukio, SANYO ELECTRIC CO., LTD.**
  Moriguchi-shi, Osaka 570-8677 (JP)
- **INOUE, Masutaka, SANYO ELECTRIC CO., LTD.**
  Moriguchi-shi, Osaka 570-8677 (JP)
- **KINOSHITA, Shigeo,**
  SANYO ELECTRIC CO., LTD.
  Moriguchi-shi, Osaka 570-8677 (JP)
- **TANASE, Susumu, SANYO ELECTRIC CO., LTD.**
  Moriguchi-shi, Osaka 570-8677 (JP)

(74) Representative: **Glawe. Delfs. Moll**
Patentanwälte
Postfach 26 01 62
80058 München (DE)

(54) **DIGITALLY DRIVEN TYPE DISPLAY DEVICE**

(57) The invention provides an organic LED display device of the digital drive type which has a display panel comprising a plurality of pixels 51. Each of the pixels 51 comprises an organic EL element 50, a drive transistor TR2 for effecting or interrupting the passage of current through the EL element 50 in response to the input of an on/off control signal, a write transistor TR1 to be brought into conduction upon receiving scanning voltage applied thereto from a scanning driver, a capacitance element C to be supplied with data voltage from a data driver by the write transistor TR1 conducting, and a comparator 9 for comparing a predetermined ramp voltage with the output voltage of the capacitance element C and supplying the result of comparison to the drive transistor TR2 as the on/off control signal.

FIG.3



EP 1 455 335 A1

Description

TECHNICAL FIELD

[0001] The present invention relates to display devices, such as organic LED display devices, which have a display panel comprising a plurality of pixels arranged in the form of a matrix.

BACKGROUND ART

[0002] Progress has been made in developing organic electroluminescence displays (hereinafter referred to as "organic LED displays") in recent years. Use of organic LED displays, for example, in portable telephones is under study.

[0003] FIGS. 33 and 34 show an organic LED display 1, which is fabricated by forming an organic hole transport layer 15 and an organic electron transport layer 16 on opposite sides of an organic luminescent layer 14 to provide an organic layer 13 on a glass substrate 11, and forming anodes 12 and cathodes 17 on opposite sides of the organic layer 13. The organic luminescent layer 14 is caused to luminesce by applying a predetermined voltage across the anode 12 and the cathode 17.

[0004] The anodes 12 are made from transparent ITO (indium tin oxide), and the cathodes 17, for example, from an Al-Li alloy. The electrodes of each type are prepared in the form of stripes to intersect those of the other type in the form of a matrix. The anodes 12 are used as data electrodes, and the cathodes 17 as scanning electrodes. With one of horizontally extending scanning electrodes selected, voltage in accordance with input data is applied to data electrodes extending perpendicular to the scanning electrode, whereby the organic layer 13 is caused to luminesce at the intersections of the scanning electrode and the data electrodes to give a display of one line. The scanning electrodes are changed over one after anther in the perpendicular direction to scan the matrix in the perpendicular direction to give a display of one frame.

[0005] The methods of driving such organic LED displays include the passive matrix driving method wherein the scanning electrodes and the data electrodes are used for time division driving, and the active matrix driving method wherein each pixel is held luminescent for one vertical scanning period. The organic LED display of the active matrix drive type will be described with reference to FIG. 4. Each pixel 52 is provided with an organic EL element 50 comprising a portion of organic layer, a drive transistor TR2 for controlling the passage of current through the EL element 50, a write transistor TR1 which is brought into conduction in response to the application of scanning voltage SCAN by a scanning electrode and a capacitance element C in which charge is stored by the application of data voltage DATA from a data electrode when the write transistor TR1 is in conduction. The capacitance element C applies an output voltage to the gate of the drive transistor TR2.

[0006] First, voltage is applied to the scanning electrodes one after another, and a plurality of first transistors TR1 connected to the same scanning electrode are brought into conduction. Data voltage (input signal) is applied to each data electrode as timed with this scanning. Since the first transistor TR1 is in conduction, the data voltage is stored in the capacitance element C.

[0007] The operating state of the second transistor TR2 depends on the amount of charge of data voltage stored in the capacitance element C. For example when the second transistor TR2 conducts, current of a magnitude corresponding to the data voltage is supplied to the EL element 50 via the transistor TR2. Consequently, the EL element 50 luminesces with a brightness in accordance with the data voltage. This luminescent state is maintained over one vertical scanning period.

[0008] With the organic LED display of the analog drive type, current of a magnitude corresponding to the data voltage is supplied to the EL element 50 to turn on the EL element 50 with a brightness corresponding to the data voltage as described above. On the other hand, organic LED displays of the digital drive type have been proposed in which a multi-level gradation is produced by supplying to an organic EL element 50 a pulse current having a duty ratio in accordance with the data voltage (e.g., JP-A No.312173/1998).

[0009] With organic LED displays of the digital drive type, one field (or one frame) which is the display cycle of one frame is divided into a plurality of (N) subfields (or subframes) SF, and each subfield SF comprises a scanning period and a luminescence period. The scanning periods included in one field all have the same length, but the luminescence periods have varying lengths each equal to nth power of 2 (n=0, 1, 2, ... N-1). In the illustrated case (N=4), the four luminescence periods have respective lengths of 8, 4, 2, 1, and on-off control of luminescence period realizes expression of a 16-level gradation.

[0010] In subfield driving described, scanning voltage is applied to a write transistor TR1 providing each pixel 53 as shown in FIG. 5, within the scanning period in each subfield SF to write binary data to a capacitance element C, and a drive transistor TR2 supplies current corresponding to the binary data to an organic EL element 50 during the subsequent luminescence period. In subfield driving, the line for supplying current to the drive transistor TR2 constituting each pixel 53 is provided with an on/off switch SW as shown in FIG. 5, whereby the EL elements 50 of the pixels can be made simultaneous with respect to the same luminescence starting time and luminescence termination time in the subfield.

[0011] With the organic LED display using the subfield driving method described, all horizontal scanning lines of each of the subfields within one field must be scanned, hence the problem of necessitating high-speed scanning for a multi-level gradation or the problem of producing quasi-contours.

[0012] Accordingly, an object of the present invention is to provide a display device of the digital drive type which does not require high-speed scanning for producing a multi-level gradation and which will not permit generation of quasi-contours.

DISCLOSURE OF THE INVENTION

[0013] The present invention provides a display device of the digital drive type which comprises a display panel comprising a plurality of pixels arranged in the form of a matrix, and a scanning driver and a data driver which are connected to the display panel. Each of the pixels of the display panel comprises:

a display element operable to luminesce when supplied with current or voltage,
a write element to be brought into conduction with scanning voltage applied thereto by the scanning driver,
voltage holding means for holding therein data voltage applied thereto by the data driver by the write element conducting, and
drive means for supplying current or voltage to the display element only for a period of time corresponding to the magnitude of the voltage held in the voltage holding means.

[0014] Stated more specifically, the drive means compares ramp voltage having a predetermined variation curve with the output voltage of the voltage holding means and supplies current or voltage to the display element in accordance with the result of comparison. For example, the drive means can be provided by:

a drive element for effecting or interrupting passage of current through the display element in response to the input of an on/off control signal, and
a comparison element for comparing ramp voltage having a predetermined variation curve with the output voltage of the voltage holding means and supplying an output signal representing the result of comparison to the drive element as the on/off control signal.

[0015] With the display device of the digital drive type of the invention, the scanning driver applies scanning voltage to the write element constituting each pixel during a scanning period within the display cycle of one frame to bring the write element into conduction, whereby data voltage is applied by the data driver to the voltage holding means for this means to hold the voltage.

[0016] During a luminescence period within the display cycle of one frame, on the other hand, ramp voltage having a predetermined variation curve is applied to the comparison element, which compares the ramp voltage with the output voltage (data voltage) of the voltage holding means. The ramp voltage varies with the predetermined variation curve, so that the magnitude relationship between the ramp voltage and the data voltage becomes reversed at a time point corresponding to the magnitude of the data voltage. Consequently, the output signal of the comparison element is given one of a high value and a low value only for a period corresponding to the data voltage. Thus, the data voltage is subjected to pulse width modulation to prepare an on/off control signal for the drive element. The drive element is on/off-controlled with this control signal to effect or interrupt the passage of current through the display element.

[0017] Stated specifically, the display element is an organic EL element, and one scanning period and one luminescence period are provided within one display cycle of one frame. The scanning voltage is applied to the write element of each pixel by the scanning driver during the scanning period for the voltage holding means of the pixel to hold the data voltage, and the ramp voltage is compared with the output voltage of the voltage holding means by the comparison element during the luminescence period to on/off-control the display element of the pixel.

[0018] Stated specifically, the ramp voltage is variable between a first value permitting the output signal of the comparison element to turn on the drive element at all times despite the data voltage and a second value permitting the output signal of the comparison element to turn off the drive element at all times despite the data voltage, and within the display cycle of one frame, retains the second value during the scanning period and varies between the first value and the second value during the luminescence period other than the scanning period. Accordingly, the drive element is off during the scanning period, holding the organic EL element unenergized at all times. Within the luminescence period other than the scanning period, the drive element is on only for a period corresponding to the data voltage, energizing the EL element.

[0019] For example, the ramp voltage has a variation curve gradually increasing or decreasing between the first value and the second value. In the case where the curve is straight, the organic EL element can be caused to luminesce only for a period of time in proportion to the magnitude of the data voltage. When the variation curve is a desired curve, the luminescence time of the organic EL element is adjustable as desired relative to the magnitude of the data voltage. For example, if a variation curve is used which involves consideration to gamma correction, required gamma correction can be made without additionally providing a gamma correction circuit.

[0020] Further if the ramp voltage has a variation curve varying from one of the first value and the second value to the other value and then returning to said one value, the organic EL element can be caused to luminesce at the midportion of the luminescence period other than the scanning period and within the display cycle of one frame.

[0021] Further it is possible to use an arrangement wherein the ramp voltage for the pixels arranged on odd-numbered lines included in horizontal or vertical lines constituting one frame has a variation curve varying from one of the first value and the second value to the other value, and the ramp voltage for the pixels arranged on even-numbered lines included in the horizontal or vertical lines has a variation curve varying from said other value to said one value. With this arrangement, the period for which the organic EL elements of the pixels on the odd-numbered lines luminesce and the period for which the organic EL elements of the pixels on the even-numbered lines luminesce can be shifted from each other to thereby disperse, with respect to time, the total quantity of current to be passed through the organic EL elements constituting one frame.

[0022] It is further possible to use an arrangement wherein the ramp voltage for the pixels arranged on lines of one of three primary colors included in horizontal or vertical lines constituting one frame has a variation curve varying from one of the first value and the second value to the other value, and the ramp voltage for the pixels arranged on lines provided for the other two colors and included in the horizontal or vertical lines has a variation curve varying from said other value to said one value. With this arrangement, the period during which the organic EL elements of the pixels on the lines of one color luminesce and the period during which the organic EL elements of the pixels on the lines for the other two colors luminesce can be shifted from each other to thereby disperse, with respect to time, the total quantity of current to be passed through the organic EL elements constituting one frame.

[0023] It is further possible to use an arrangement wherein the pixels arranged on odd-numbered lines included in horizontal or vertical lines constituting one frame and the pixels arranged on even-numbered lines included in the horizontal or vertical lines are alternately reversed in the order of the scanning period and the luminescence period within the display cycle of one frame. With this arrangement, the period during which the organic EL elements of the pixels on the odd-numbered lines luminesce and the period during which the organic EL elements of the pixels on the even-numbered lines luminesce are shifted toward the first half and the second half of the display cycle of one frame. This serves to disperse, with respect to time, the total quantity of current to be passed through the organic EL elements constituting one frame.

[0024] It is further possible to use an arrangement wherein the ramp voltage for the pixels arranged on lines of three primary colors included in horizontal or vertical lines constituting one frame differs from color to color in the variation rate (slope). With this arrangement, the proportion of the luminescence period for the pixels on the lines of three primary colors can be altered from color to color relative to the data voltage. White balance is then adjustable.

[0025] With the display device of the digital drive type according to the present invention described, a multi-level gradation can be realized by scanning all the horizontal scan lines within the display cycle of one frame only once. This obviates the necessity of resorting to high speed scanning, further eliminating the likelihood of producing quasi-contours.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026]

FIG. 1 is a block diagram showing the construction of an organic LED display device embodying the invention.

FIG. 2 is a block diagram showing the construction of another organic LED display device embodying the invention.

FIG. 3 is a circuit diagram of each pixel constituting the display panel of organic LED display device of the invention.

FIG. 4 is a circuit diagram of each pixel constituting a conventional organic LED display of the active matrix drive type.

FIG. 5 is a circuit diagram of each pixel constituting an organic LED display for which a subfield driving method is used.

FIG. 6 is a diagram showing the timing of scanning period and luminescence period in the prior art and according to the invention, and various examples of waveforms of ramp voltages according to the invention.

FIG. 7 is a diagram showing the timing of scanning period and luminescence period according to the invention, and other examples of waveforms of ramp voltages according to the invention.

FIG. 8 is a diagram showing the timing of scanning period and luminescence period according to the invention, and other examples of waveforms of ramp voltages according to the invention.

FIG. 9 is a diagram showing the timing of scanning period and luminescence period according to the invention, and other examples of waveforms of ramp voltages according to the invention.

FIG. 10 is a circuit diagram showing the specific construction of a comparator.

FIG. 11 is a waveform diagram showing the operation of the comparator.

FIG. 12 is a circuit diagram showing the specific construction of another comparator.

FIG. 13 is a circuit diagram showing the specific construction of another comparator.

FIG. 14 is a circuit diagram showing the specific construction of another comparator.

FIG. 15 is a circuit diagram showing the specific construction of another comparator.

FIG. 16 is a circuit diagram showing the specific construction of another comparator.

FIG. 17 is a circuit diagram showing the specific construction of another comparator.
FIG. 18 is a circuit diagram showing the specific construction of another comparator.
FIG. 19 is a waveform diagram showing the operation of the comparator.
FIG. 20 is a circuit diagram showing the specific construction of another comparator.
FIG. 21 is a waveform diagram showing the operation of the comparator.
FIG. 22 is a diagram showing the specific construction of a ramp voltage generating circuit incorporated into the pixel.
FIG. 23 is a waveform diagram showing the operation of the ramp voltage generating circuit.
FIG. 24 is a diagram showing the specific construction of another ramp voltage generating circuit incorporated into the pixel.
FIG. 25 is a waveform diagram showing the operation of the ramp voltage generating circuit.
FIG. 26 is a diagram showing the specific construction of another ramp voltage generating circuit incorporated into the pixel.
FIG. 27 is a waveform diagram showing the operation of the ramp voltage generating circuit.
FIG. 28 is a circuit diagram of a pixel wherein the level of ramp voltage is altered according to data voltage.
FIG. 29 is a waveform diagram showing the operation of the circuit.
FIG. 30 is a block diagram showing the construction of an organic LED display device wherein the phase of ramp voltage is shifted every horizontal line.
FIG. 31 is a waveform diagram showing the operation of the LED display device.
FIG. 32 is a diagram showing the timing of scanning period and luminescence period according to the invention, and other examples of waveforms of ramp voltages according to the invention.
FIG. 33 is a diagram showing the layered structure of an organic LED display of the passive matrix drive type.
FIG. 34 is a perspective view partly broken away and showing the LED display of the passive matrix drive type.

BEST MODE OF CARRYING OUT THE INVENTION

[0027] The present invention as embodied into organic LED display devices will be described below in detail with reference to the drawings. FIG. 1 shows an organic LED display device of the invention, which comprises a display panel 5 provided by a plurality of pixels arranged in the form of a matrix, and a scanning driver 3 and a data driver 4 which are connected to the display panel 5. A video signal from a video source such as a TV receiver is fed to a video signal processing circuit 6 for processing the signal as required for video display, and video signals of RGB three primary colors obtained are fed to the data driver 4 of the organic LED display 2.

[0028] A horizontal synchronizing signal Hsync and a vertical synchronizing signal Vsync obtained from the video signal processing circuit 6 are fed to a timing signal generating circuit 7, whereby a timing signal is obtained, which is fed to the scanning driver 3 and the data driver 4. The timing signal obtained from the circuit 7 is fed also to a ramp voltage generating circuit 8, whereby a ramp voltage is produced for use in driving the display 2 as will be described later. The ramp voltage is supplied to pixels of the display panel 5. A power source circuit (not shown) is connected to the circuits, drivers and display shown in FIG. 1.

[0029] The display panel 5 comprises pixels 51 each having the circuit construction shown in FIG. 3 and arranged in,the form of a matrix. Each pixel 51 comprises an organic EL element 50 provided by an organic layer, a drive transistor TR2 for effecting or interrupting the passage of current through the EL element 50 in response to the input of an on/off control signal to the gate, a write transistor TR1 which is brought into conduction by the application of a scanning voltage from the scanning driver to the gate, a capacitance element C to be supplied with a data voltage from the data driver by the write transistor TR1 conducting, and a comparator 9 having a pair of positive and negative input terminals to be supplied with the ramp voltage from the ramp voltage generating circuit and the output voltage of the capacitance element C for comparing the two voltages. The output voltage of the comparator 9 is fed to the gate of the drive transistor TR2.

[0030] The drive transistor TR2 has a source connected to a current supply line 54 and a drain connected to the EL element 50. The data driver is connected to one electrode (e.g., source) of the write transistor TR1, the other electrode (e.g., drain) of which has connected thereto one end of the capacitance element C and an inversion input terminal of the comparator 9. The output terminal of the ramp voltage generating circuit 8 is connected to a non-inversion input terminal of the comparator 9.

[0031] With the organic LED display 2, one field period is divided into a first half scanning period and a second half luminescence period as shown in FIG. 6(b). During the scanning period, the scanning driver applies a scanning voltage to the write transistor TR1 constituting each pixel 51 on each horizontal line, bringing the transistor TR1 into conduction, whereby data voltage is applied to the capacitance element C by the data driver to store the voltage as a charge. As a result, data corresponding to one field is set in all the pixels constituting the LED display 2.

[0032] As shown in FIG. 6(c), the ramp voltage generating circuit 8 maintains a high voltage value during the first half scanning period of every field period and generates during the second half luminescence period thereof a ramp voltage linearly varying from a low volt-

age value to a high voltage value. During the first half scanning period, the high voltage from the ramp voltage generating circuit 8 is applied to the non-inversion input terminal of the comparator 9. This causes the comparator 9 to always deliver a high output as shown in FIG. 6 (d) despite the input voltage to the inversion input terminal thereof.

[0033] When the circuit 8 applies the ramp voltage to the non-inversion input terminal of the comparator 9 in the second half luminescence period, the output voltage (data voltage) of the capacitance element C is simultaneously applied to the inversion input terminal of the comparator 9. This gives one of two values of high and low as shown in FIG. 6(d) to the output of the comparator 9 in accordance with the result of comparison of the two voltages. Stated more specifically, the output of the comparator is low while the ramp voltage is lower than the data voltage, whereas the output of the comparator is high while the ramp voltage is higher than the data voltage. The length of the period during which the comparator output is low is in proportion to the magnitude of the data voltage.

[0034] Thus, the output of the comparator 9 is low during a period proportional to the magnitude of the data voltage, whereby the drive transistor TR2 is held on only during this period, holding the EL element 50 on. Consequently, the organic EL element 50 constituting each pixel 51 providing the display panel 5 luminesces only for a period proportional to the magnitude of the data voltage for the pixels 51, within the period of one field, whereby multi-level gradation can be realized.

[0035] The organic LED display device is adapted to produce a multi-level gradation only by scanning once within one field period as described above. This eliminates the need for high speed scanning, further obviating the likelihood of producing quasi-contours. Furthermore, the organic LED display device of the invention for which the digital drive method is used is less prone to the influence of variations in the characteristics of drive transistors TR2 while realizing low power consumption due to a reduction in the power source voltage.

[0036] According to the embodiment described, the curve of variations in the ramp voltage:is a straight line representing an increase but can be a desired curve so as to adjust as desired the luminescence time of the organic EL element 50 relative to the magnitude of the data voltage. For example as shown in FIG. 6(e), (1), required gamma correction can be made by using a variation curve involving consideration to gamma correction without using an additional gamma correction circuit.

[0037] FIG. 6(e), (2) shows a ramp voltage variation curve which is reversely sloped. This makes it possible to provide a luminescence period in the second half of the ramp period. Further if the two inputs to the comparator 9 are reversed in positive-negative relationship, the ramp voltage may be reversed also in positive-negative relationship as represented by FIG. 6(e), (3) or (4). When the ramp voltage variation curve to be used is in the form of a triangular wave extending from low to high and to low again as represented by FIG. 6(e), (5), the organic EL element 50 can be made to luminesce in the midportion of the ramp period.

[0038] With reference to FIG. 7(a), (b), the ramp voltage for the pixels arranged on odd-numbered lines included in the horizontal or vertical lines in one field period and the ramp voltage for the pixels arranged on even-numbered lines included in the above lines are altered along variation lines having respective variation rates which are opposite in positive-negative relationship, whereby the luminescence period of organic EL elements of the pixels on the odd-numbered lines and the luminescence period of organic EL elements of the pixels on the even-numbered lines can be shifted from each other. This makes it possible to disperse, with respect to time, the total quantity of current to be passed through the EL elements forming one providing one frame.

[0039] Further as shown in FIG. 7(c), the ramp voltage for the pixels arranged on the lines of one color (e.g., G) among the three primary colors of RGB and the ramp voltage for the pixels on the lines of the other two colors (e.g., R and B) are altered along variation lines having respective variation rates which are opposite in positive-negative relationship. This makes it possible to disperse, with respect to time, the total quantity of current to be passed through the EL elements providing one frame as in the above case.

[0040] Further as shown in FIG. 8(a), (b), one field period for the pixels arranged on the odd-numbered lines included in the horizontal or vertical lines constituting one frame and one field period for the pixels arranged on the even-numbered lines included in the above lines are shifted from each other by 1/2 of the cycle, whereby the luminescence period for the pixels arranged on the odd-numbered lines and the luminescence period for the pixels arranged on the even-numbered lines can be shifted from each other by 1/2 the cycle. This makes it possible to disperse, with respect to time, the total quantity of current to be passed through the EL elements providing one frame. The scanning speed also can then be decreased.

[0041] Further as seen in FIG. 32(a), (b), the scanning period, as well as the luminescence period, can be made to differ from RGB color to color. This makes it possible to disperse the quantity of current and to alter the ramp voltage from RGB color to color.

[0042] Further as shown in FIG. 9(a), (b), the variation rate (slope) of the ramp voltage for the pixels arranged on the lines of the three primary colors RGB can be altered from color to color to thereby alter the proportion of the luminescence period from color to color relative to the data voltage. White balance is then adjustable. In this case, an R ramp voltage generating circuit 81, a G ramp voltage generating circuit 82 and a B ramp voltage generating circuit 83 are provided for the respective lines of three primary colors as shown in FIG. 2.

[0043] FIG. 10 shows the construction of the comparator 9 in detail. As illustrated, the comparator 9 comprises a plurality of transistors TR3 to TR7. A constant voltage is applied to the gate of the transistor TR3 via a constant voltage supply line CONST for this transistor to serve as a constant current source. A capacitor C applies an output voltage (data voltage) to the gate of the transistor TR4. Ramp voltage is applied to the gate of the transistor TR5. The transistors TR6 and TR7 each serve the function of a resistor. When the data voltage is higher than the ramp voltage, current flows through the transistor TR4 for the comparator to deliver a high output, whereas if the ramp voltage is higher than the data voltage, current flows through the transistor TR5, causing the comparator to deliver a low output.

[0044] With the comparator 9 described, the data voltage alters within the scanning period as shown in FIG. 11, and the ramp voltage thereafter gradually increases within the luminescence period to exceed the data voltage. This changes the comparator output from high to low to bring the drive transistor TR2 into conduction and pass current through the organic EL element 50.

[0045] FIG. 12 shows a comparator 9, which has the construction shown in FIG. 10 from which one of the resistance components, i.e., transistor TR6, is omitted. Similarly with this comparator 9, the comparator output changes from high to low when the ramp voltage is in excess of the data voltage, causing the drive transistor TR2 to conduct and passing current through the organic EL element 50.

[0046] FIG. 13 shows another comparator 9, wherein the pair of transistors TR6, TR7 shown in FIG. 10 and serving as resistance components are connected in a different manner as illustrated. This comparator 9 also performs the same function.

[0047] FIG. 14 shows another comparator 9, wherein the arrangement shown in FIG. 10 of the transistor TR3 serving as a constant voltage source and the pair of transistors TR6, TR7 serving as resistance components is reversed with respect to the positive-negative relationship. A transistor TR3' serving as a constant current source is provided at the positive side, and transistors TR6', TR7' serving as resistors are arranged at the negative side. In corresponding relationship with this modification, a pair of transistors TR4', TR5' for comparing voltages are of the p-channel type, and the transistors TR6', TR7' serving as resistors are of the n-channel type.

[0048] FIG. 15 shows a comparator 9, which corresponds to the arrangement shown in FIG. 14 from which the drive transistor TR2 is removed and in which the organic EL element 50 is connected to the drain of the transistor TR5' in the pair of transistors TR4', TR5' so as to on/off-control the flow of current through the EL element 50 by the transistor TR5'.

[0049] FIG. 16 shows a comparator 9, in which the transistor TR3 shown in FIG. 10 and serving as a constant current source is provided at the positive side. With this modification, a transistor TR3' of the p-channel type is used. FIG. 17 shows another comparator 9, wherein transistors of the depletion type are used as the pair of transistors TR6, TR7 serving as resistance components.

[0050] FIG. 18 shows a comparator 9, which has transistors TR8, TR9 for effecting or interrupting luminescence, and a transistor TR10 of the depletion type serving as a resistance component. Data voltage is applied to the gate of the transistor TR8 for effecting luminescence, and ramp voltage to the source thereof. A voltage source Vcc is connected via the transistor TR10 to the drain thereof. A constant d.c. voltage DC is applied to the gate of the transistor TR9 for interrupting luminescence, ramp voltage to the source thereof, and data voltage to the drain thereof.

[0051] With reference to FIG. 19, the data voltage (voltage at point A) alters during the scanning period, the ramp voltage thereafter drops during the luminescence period, and the difference between these voltages increases. When the difference exceeds a threshold level Vth between the gate of the luminescence effecting transistor TR8 and the source thereof, the transistor TR8 conducts, and the gate voltage (voltage at point B) of the drive transistor TR2 decreases, whereby the transistor TR2 is brought into conduction, passing current through the organic EL element 50 to start luminescence.

[0052] The ramp voltage thereafter further decreases to produce an increased difference between the ramp voltage and d.c. voltage DC. When the difference exceeds a threshold level Vth between the gate of the luminescence interrupting transistor TR9 and the source thereof, this transistor TR9 conducts to reduce the gate-source potential difference of the luminescence effecting transistor TR8. This brings the transistor TR8 out of conduction, raising the gate voltage (voltage at point B) of the drive transistor TR2. Consequently, the drive transistor TR2 is turned off to deenergize the organic EL element 50 to complete luminescence.

[0053] The luminescence effecting transistor TR8 and the luminescence interrupting transistor TR9 are used in the comparator 9 described, so that even if the gate-source threshold level Vth of these transistors varies from pixel to pixel, the luminescence effecting timing and the luminescence interrupting timing similarly shift as shown in FIG. 19 if the two transistors within the pixel have the same threshold level Vth, hence no variations in the luminescence period.

[0054] FIG. 20 shows another comparator 9, which corresponds to the comparator shown in FIG. 18 wherein a pair of transistors TR11, TR12 for on/off-controlling the gate voltage are provided between point B and the drive transistor TR2. The d.c. voltage DC and ramp voltage are in reversed positive-negative relationship to FIG. 18, and in accordance with this modification, transistors TR8', TR9', TR10' used are of the p-channel type. When the potential at point B exceeds a threshold

value, the transistor TR11 for turning on the gate voltage conducts to reduce the potential at point C to zero, while when the potential at point B drops below the threshold value, the transistor TR12 for turning off the gate voltage conducts to change the potential at point C to a high value.

[0055] With reference to FIG. 21, the data voltage (voltage at point A) alters during the scanning period, the ramp voltage thereafter rises during the luminescence period, and the difference between these voltages increases. When the difference exceeds a threshold level Vth between the gate of the luminescence effecting transistor TR8' and the source thereof, the transistor TR8' conducts. This raises the voltage at point B, bringing the transistor TR11 for turning on the gate voltage into conduction to decrease the potential at point C to a low value. Consequently, the drive transistor TR2 is brought into conduction, passing current through the organic EL element 50 to start luminescence.

[0056] The ramp voltage thereafter further increases to produce an increased difference between the ramp voltage and d.c. voltage DC. When the difference exceeds a threshold level Vth between the gate of the luminescence interrupting transistor TR9' and the source thereof, this transistor TR9' conducts to reduce the gate-source potential difference of the luminescence effecting transistor TR8'. This brings the transistor TR8' out of conduction, reducing the voltage at point B. The transistor TR12 for turning off the gate voltage conducts to give a high potential at point C. Consequently, the drive transistor TR2 is turned off to deenergize the organic EL element 50 to complete luminescence.

[0057] The luminescence effecting transistor TR8' and the luminescence interrupting transistor TR9' are used in the comparator 9 described, so that even if the gate-source threshold level Vth of these transistors varies from pixel to pixel, no variations occur in the luminescence period as shown in FIG. 21 provided that the two transistors within the pixel have the same threshold level Vth. Since the gate voltage (voltage at point C) of the drive transistor TR2 is held at a definite value during the luminescence period, the drive transistor TR2 is operable with high reliability.

[0058] According to the foregoing embodiments, the ramp voltage is supplied from the ramp voltage generating circuit 8 which is provided externally of the organic LED display 2, whereas the ramp voltage can be generated inside each of the pixels constituting the display 2. For example, FIG. 22 shows a ramp voltage generating circuit 80, which comprises a transistor TR13 to be turned on/off with switching pulses SW, a capacitor C1 chargeable by the conduction of the transistor TR13, and a transistor TR14 of the depletion type performing the function of a discharging resistor. The voltage discharged from the capacitor C1 is applied to the positive terminal of the comparator as the ramp voltage.

[0059] With reference to FIG. 23, switching pulses SW change from high to low within the luminescence period. The transistor TR13 conducts while SW is high to charge the capacitor C1, and the transistor TR13 is brought out of conduction while SW is low to discharge the capacitor C1. The voltage of the capacitor C1 gradually drops with discharging, and the voltage to be applied to the positive terminal of the comparator 9 serves as the ramp voltage as shown in FIG. 23.

[0060] FIG. 24 shows a ramp voltage generating circuit 80 wherein the transistor TR13 shown in FIG. 22 is transferred from the positive power source side to the negative power source side. The voltage discharged from a capacitor C1 is applied to the positive terminal of a comparator as the ramp voltage. Switching pulses SW change from high to low during the luminescence period as shown in FIG. 25. While the pulses SW are high, the transistor TR13 conducts to charge the capacitor C1. While SW is low, the transistor TR13 is turned off to discharge the capacitor C1. The voltage of the capacitor C1 gradually drops with discharging, and the voltage to be applied to the positive terminal of the comparator 9 serves as the ramp voltage as shown in FIG. 25.

[0061] FIG. 26 shows a ramp voltage generating circuit 80, which corresponds to the circuit 80 of FIG. 22 wherein a transistor TR15 is connected in series with the transistor TR14 of the depletion type. Second switching pulses SW2 are supplied to the gate of the transistor TR15. First switching pulses SW1 change from low to high during the scanning period as seen in FIG. 27. While SW1 is high, the transistor TR13 conducts to charge the capacitor C1, and while SW1 is low, the transistor TR13 is turned off to discharge the capacitor C1.

[0062] Second switching pulses SW2 change from low to high during the luminescence period. While SW2 is low, the transistor TR15 is turned off, preventing current from flowing through the transistor TR14 serving as a resistance element. While SW2 is high, the transistor TR15 conducts, permitting current to flow through the transistor TR14 serving as the resistance element. Thus, no current flows through the transistor TR14 during the scanning period. This results in reduced power consumption.

[0063] According to the foregoing embodiments, the ramp voltage is applied to the positive terminal of the comparator 9. However, the luminescence period is controllable by applying a constant voltage to the positive terminal while applying a ramp voltage, altered in level in accordance with the data voltage, to the negative terminal of the comparator 9.

[0064] For example, FIG. 28 shows an arrangement which can be used and in which the output terminal of a capacitor C has connected thereto a transistor TR17 of the depletion type serving as a resistance element, via a transistor TR16 to be on/off-controlled with switching pulses SW. With this arrangement, switching pulses SW are low during the scanning period or high during the luminescence period. While SW is low, the transistor TR16 is out of conduction, permitting charging of the ca-

pacitor C. While SW is high, the transistor TR16 conducts, causing the transistor TR17 serving as a resistance element to discharge the capacitor C.

[0065] As shown in FIG. 29, therefore, the voltage applied to the negative terminal of the comparator 9 during the scanning period has its level altered in accordance with the data voltage. The data voltage gradually decreases during the discharging process of the capacity C following a change of SW from low to high.

[0066] The output of the comparator 9 is low, when the voltage of the negative terminal is in excess of the voltage of the positive terminal, bringing the drive transistor TR2 into conduction to pass current through the organic EL element 50. Subsequently when the voltage of the negative terminal drops below the voltage of the positive terminal, the output of the comparator 9 becomes high to turn off the drive transistor TR2 and block the current to be passed through the EL element 50. As a result, the luminescence period of the EL element 50 varies in corresponding relationship with the magnitude of the data voltage.

[0067] In the embodiments of FIGS. 6 and 7, data is written within the first half scanning period, and luminescence is thereafter controlled in the second half luminescence period according to the data, for all the pixels constituting the organic LED display 2. Scanning must therefore be done at a somewhat high speed. Further with the embodiment shown in FIG. 8, the odd-numbered lines and the even-numbered lines are alternately reversed in the order of the scanning period and the luminescence period, so that the scanning speed then decreases, and the embodiment has the drawback that the luminescence period becomes shorter when there is a limitation on the scanning speed.

[0068] Accordingly, FIGS. 30 and 31 show an embodiment wherein the ramp voltage is shifted in phase from horizontal line to line so as to effect luminescence of each line immediately after data has been written to the line. The ramp voltage to be delivered from the ramp voltage generating circuit 8 as a digital signal is fed to the pixels of each horizontal line via a delay circuit 84 and DA converter 85, whereby the ramp voltage to be supplied to each horizontal line has its phase shifted by a predetermined time lag for each line, from the first line to the final line as shown in FIG. 31. The data supplied by the data driver 4 is written immediately before the ramp voltage for each horizontal line rises.

[0069] Accordingly, the ramp voltage for each horizontal line has a gentle slope, varying from low to high (or from high to low) over one frame period as shown in FIG. 31, and almost the entire frame period can be made to serve as luminescence periods.

[0070] Since all the horizontal lines can be scanned using nearly the entire frame period, the scanning speed may be low. Further because the luminescence of pixels is dispersed with respect to time, the influence of voltage drop of the power source line within the display panel can be mitigated.

[0071] The device of the present invention is not limited.only to the foregoing embodiments in construction but can be modified variously within the technical scope defined in the appended claims. For example, although organic EL elements are used as display elements according to the above embodiments, such elements are not limitative but various other display elements are usable to provide display devices of the invention insofar as these elements luminesce when supplied with current.

[0072] In the case where the comparator 9 has satisfactory current drive ability, the drive transistor TR2 can be dispensed with to connect the output terminal of the comparator 9 directly to the organic EL element 50. When the ramp voltage shown in FIG. 6(3) is used, or when the ramp voltage shown in FIG. 6(c) is used in this case, the non-inversion input terminal and the inversion input terminal of the comparator 9 need to be reversed for connection. A voltage drive type element is then usable as the display element.

[0073] In the comparator shown in FIG. 10, the voltage of the constant voltage supply line CONST can be set at the source potential of the transistor TR3 so as not to pass any current through the comparator 9 during the scanning period. This results in a reduction of power consumption.

Claims

1. A display device of the digital drive type comprising a display panel comprising a plurality of pixels arranged in the form of a matrix, and a scanning driver and a data driver which are connected to the display panel, each of the pixels of the display panel comprising:

   a display element operable to luminesce when supplied with current or voltage,
   a write element to be brought into conduction with scanning voltage applied thereto by the scanning driver,
   voltage holding means for holding therein data voltage applied thereto by the data driver by the write element conducting, and
   drive means for supplying current or voltage to the display element only for a period of time corresponding to the magnitude of the voltage held in the voltage holding means.

2. A display device of the digital drive type according to claim 1 wherein the drive means compares ramp voltage having a predetermined variation curve with the output voltage of the voltage holding means and supplies current or voltage to the display element in accordance with the result of comparison.

3. A display device of the digital drive type according

to claim 1 or 2 wherein the drive means comprises:

a drive element for effecting or interrupting passage of current through the display element in response to the input of an on/off control signal, and

a comparison element for comparing ramp voltage having a predetermined variation curve with the output voltage of the voltage holding means and supplying an output signal representing the result of comparison to the drive element as the on/off control signal.

4. A display device of the digital drive type according to claim 3 wherein one scanning period and one luminescence period are provided within one display cycle of one frame, the scanning voltage is applied to the write element of each pixel by the scanning driver during the scanning period for the voltage holding means of the pixel to hold the data voltage, and the ramp voltage is compared with the output voltage of the voltage holding means during the luminescence period to on/off-control the display element of the pixel.

5. A display device of the digital drive type according to claim 4 wherein the ramp voltage is variable between a first value permitting the output signal of the comparison element to turn on the drive element at all times despite the data voltage and a second value permitting the output signal of the comparison element to turn off the drive element at all times despite the data voltage, and within the display cycle of one frame, retains the second value during the scanning period and varies between the first value and the second value during the luminescence period other than the scanning period.

6. A display device of the digital drive type according to claim 5 wherein the ramp voltage has a variation curve gradually increasing or decreasing between the first value and the second value.

7. A display device of the digital drive type according to claim 5 wherein the ramp voltage has a variation curve involving consideration to gamma correction between the first value and the second value.

8. A display device of the digital drive type according to claim 5 wherein the ramp voltage has a variation curve varying from one of the first value and the second value to the other value and then returning to said one value.

9. A display device of the digital drive type according to claim 5 wherein the ramp voltage for the pixels arranged on odd-numbered lines included in horizontal or vertical lines constituting one frame has a variation curve varying from one of the first value and the second value to the other value, and the ramp voltage for the pixels arranged on even-numbered lines included in the horizontal or vertical lines has a variation curve varying from said other value to said one value.

10. A display device of the digital drive type according to claim 5 wherein the ramp voltage for the pixels arranged on lines of one of three primary colors included in horizontal or vertical lines constituting one frame has a variation curve varying from one of the first value and the second value to the other value, and the ramp voltage for the pixels arranged on lines provided for the other two colors and included in the horizontal or vertical lines has a variation curve varying from said other value to said one value.

11. A display device of the digital drive type according to claim 5 wherein the pixels arranged on odd-numbered lines included in horizontal or vertical lines constituting one frame and the pixels arranged on even-numbered lines included in the horizontal or vertical lines are alternately reversed in the order of the scanning period and the luminescence within the display cycle of one frame.

12. A display device of the digital drive type according to claim 5 wherein the ramp voltage for the pixels arranged on lines of three primary colors included in horizontal or vertical lines constituting one frame differs from color to color in the rate of variation between the first value and the second value.

13. A display device of the digital drive type according to any one of claims 3 to 12 wherein the drive element comprises a drive transistor for effecting or interrupting passage of current through the display element in responses to the on/off control signal received at a gate thereof, the write element comprising a write transistor to be brought into conduction by the scanning voltage applied to a gate thereof, the voltage holding means comprising a capacitance element for storing therein the data voltage as a charge, the comparison element comprising a comparator for receiving lamp voltage to be supplied from a lamp voltage generating circuit and the output voltage of the capacitance element at a pair of positive and negative input terminals thereof and delivering a high/low signal representing the result of comparison from an output terminal thereof to the gate of the drive transistor.

14. A display device of the digital drive type according to claim 13 wherein the comparator comprises a pair of voltage comparing transistors having respective gates for receiving the ramp voltage to be

supplied from the ramp voltage generating circuit and the output voltage of the capacitance element, a current source for supplying current to the voltage comparing transistors, and a resistance element serving as resistance to the current to be passed through the voltage comparing transistors, and has a point where a voltage variation is produced by the passage of current through one of the voltage comparing transistors and which serves as an output terminal.

15. A display device of the digital drive type according to claim 14 wherein one of the voltage comparing transistors serves as the drive transistor for effecting or interrupting passage of current through the display element.

16. A display device of the digital drive type according to claim 13 wherein the comparator comprises a pair of luminescence effecting/interrupting transistors, the luminescence effecting transistor conducts when the difference between the ramp voltage and the output voltage of the capacitance element exceeds a predetermined threshold value to bring the drive transistor into conduction, and the luminescence interrupting transistor conducts when the difference between the ramp voltage and a predetermined d.c. voltage exceeds a predetermined threshold value to bring the drive transistor out of conduction.

17. A display device of the digital drive type according to any one of claims 13 to 16 wherein the ramp voltage generating circuit is provided externally of the display panel.

18. A display device of the digital drive type according to any one of claims 13 to 16 wherein the ramp voltage generating circuit is provided in each pixel of the display panel and supplied with switching pulses from outside the display panel to generate the ramp voltage by charging or discharging of a capacitor during a high or low period of the pulses.

19. A display device of the digital drive type according to claim 18 wherein the ramp voltage generating circuit is provided comprises a transistor for blocking current to be passed with the charging of the capacitor during the scanning period.

20. A display device of the digital drive type according to claim 1 wherein the drive means comprises:

a drive element for effecting or interrupting passage of current through the display element in response to the input of an on/off control signal, resistance means for causing the voltage holding means to discharge, and comparison element for comparing output voltage delivered from the voltage holding means by discharging with a specified voltage and supplying an output signal representing the result of comparison to the drive element as the on/off control signal.

21. A display device of the digital drive type according to any one of claims 1 to 3 wherein ramp voltage for a plurality of horizontal lines providing one frame has a ramp period same as or substantially the same as the display cycle of one frame and is shifted in phase from horizontal line to line, and immediately after data voltage is applied to the voltage holding means of all the pixels on each horizontal line, the ramp voltage for the horizontal line is generated to effect luminescence of the display elements on the horizontal line.

22. A display device of the digital drive type according to any one of claims 1 to 21 wherein the display element is an organic electroluminescence element.

FIG.1

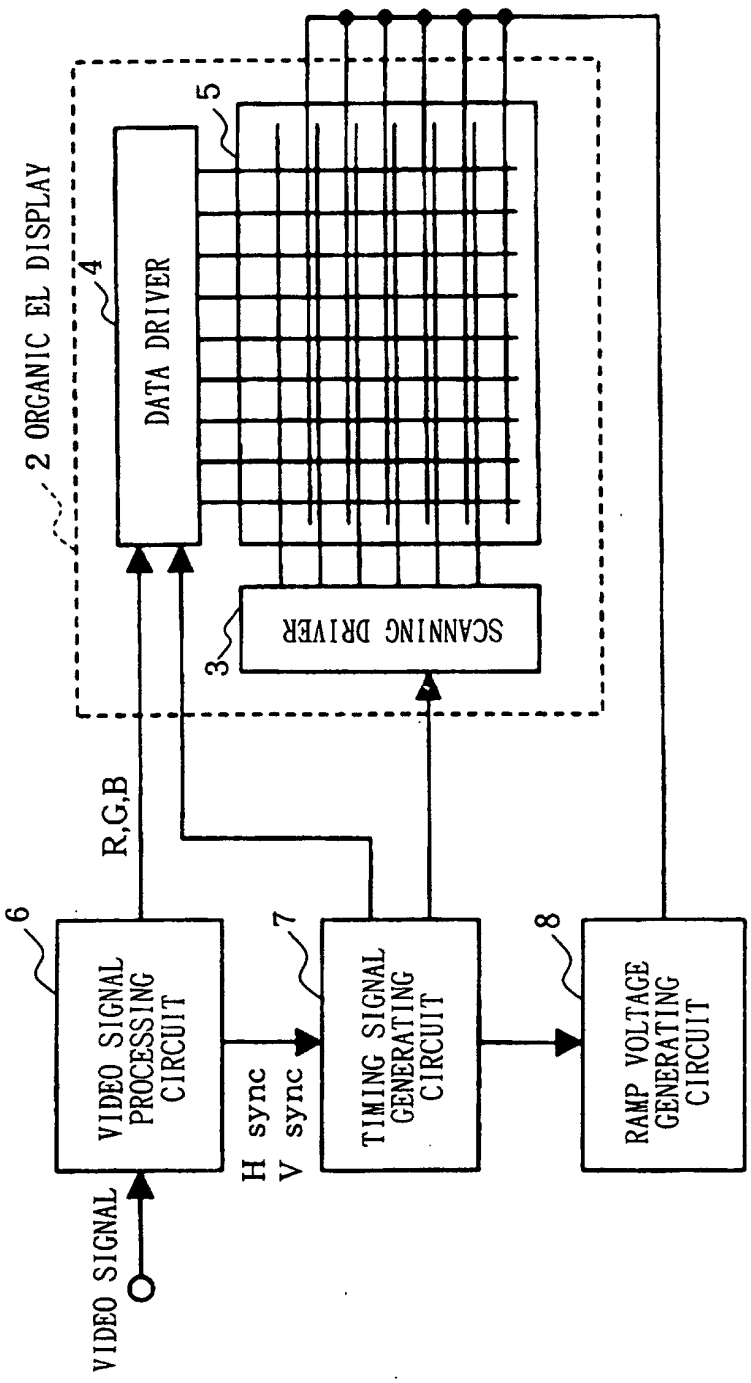

2 ORGANIC EL DISPLAY
DATA DRIVER
4
5
SCANNING DRIVER
3
R,G,B
6
VIDEO SIGNAL PROCESSING CIRCUIT
7
TIMING SIGNAL GENERATING CIRCUIT
8
RAMP VOLTAGE GENERATING CIRCUIT
H sync
V sync
VIDEO SIGNAL

FIG.2

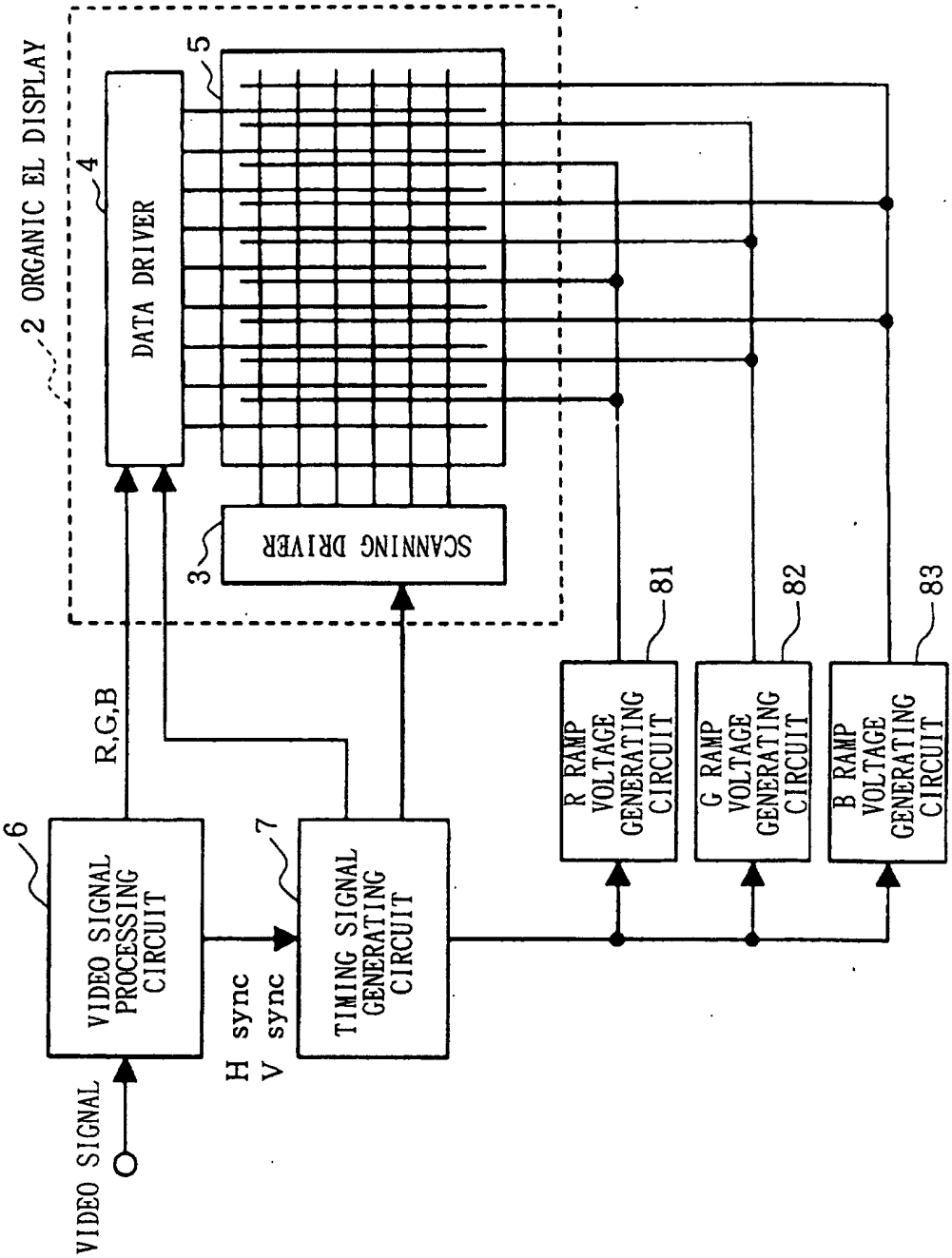

2 ORGANIC EL DISPLAY
DATA DRIVER
4
5
SCANNING DRIVER
3
R,G,B
6
VIDEO SIGNAL PROCESSING CIRCUIT
7
TIMING SIGNAL GENERATING CIRCUIT
H sync
V sync
VIDEO SIGNAL
81
R RAMP VOLTAGE GENERATING CIRCUIT
82
G RAMP VOLTAGE GENERATING CIRCUIT
83
B RAMP VOLTAGE GENERATING CIRCUIT

FIG.3

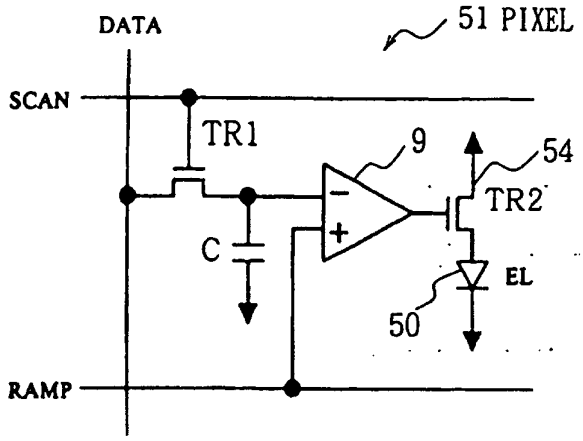


FIG.4

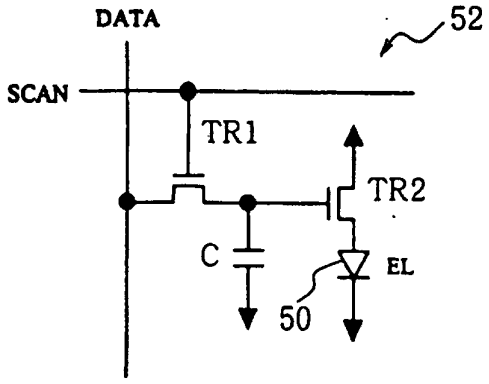


FIG.5

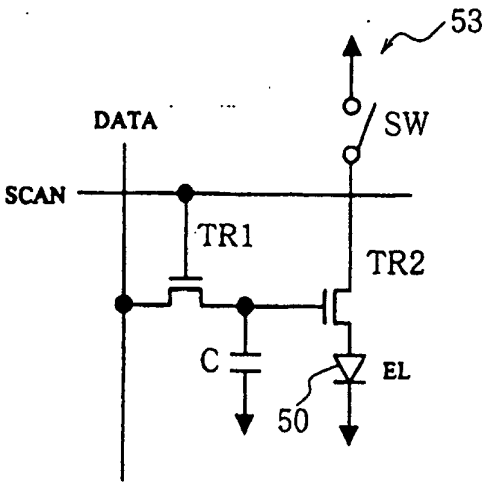


FIG.6

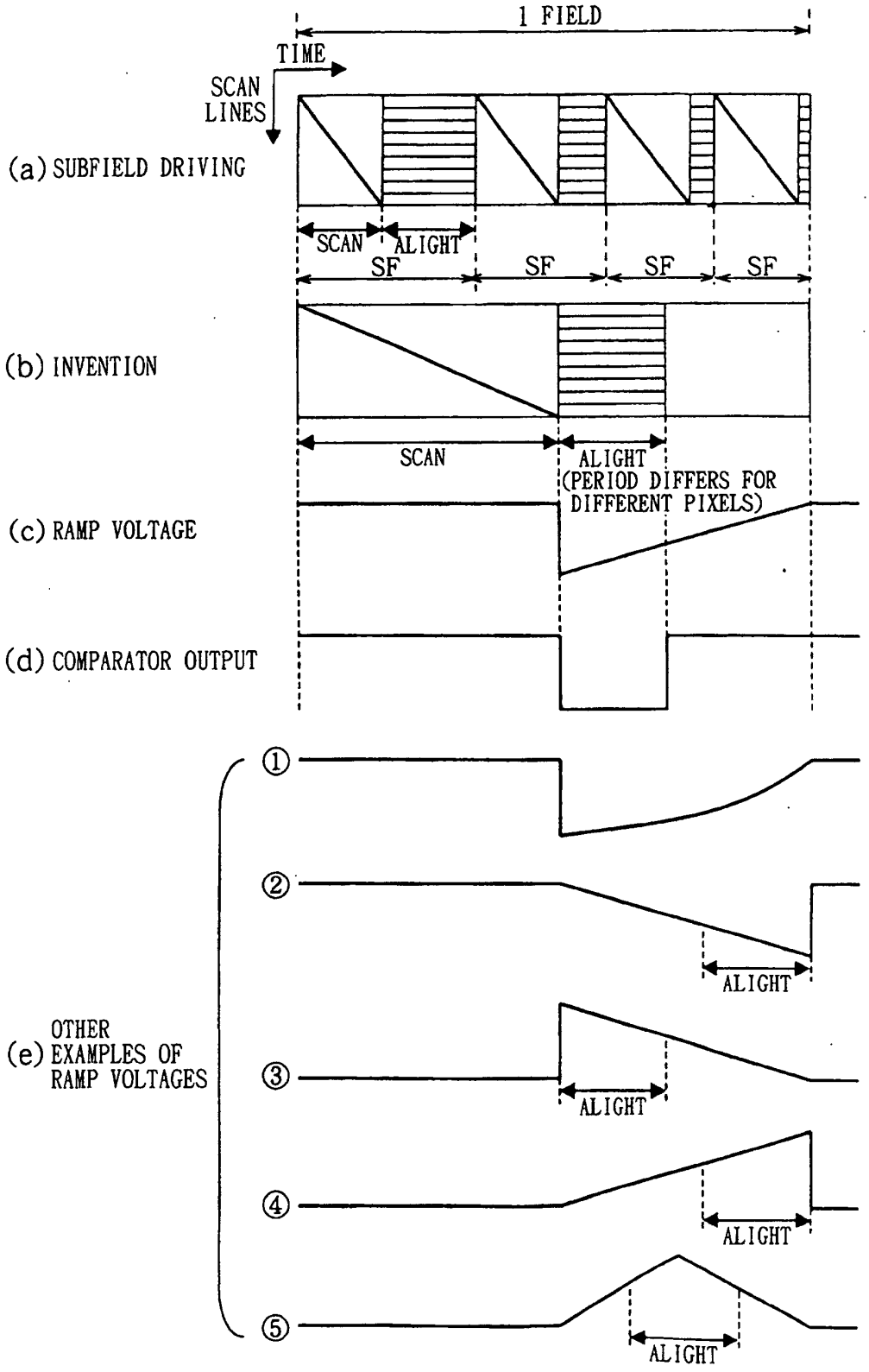

1 FIELD
TIME
SCAN LINES
(a) SUBFIELD DRIVING
SCAN
ALIGHT
SF
SF
SF
SF
(b) INVENTION
SCAN
ALIGHT
(PERIOD DIFFERS FOR DIFFERENT PIXELS)
(c) RAMP VOLTAGE
(d) COMPARATOR OUTPUT
(e) OTHER EXAMPLES OF RAMP VOLTAGES
①
②
ALIGHT
③
ALIGHT
④
ALIGHT
⑤
ALIGHT

FIG.7

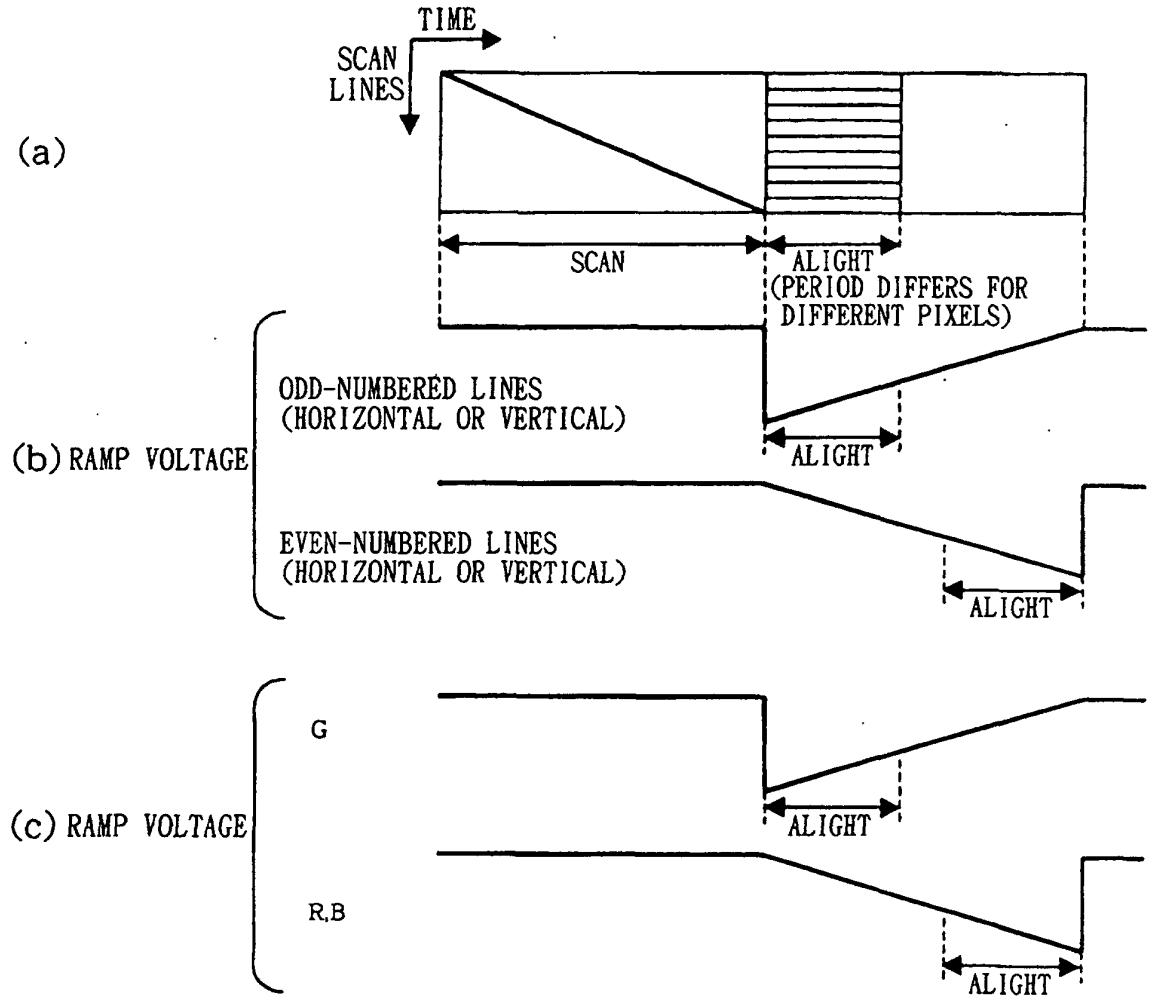

(a)
TIME
SCAN LINES
SCAN
ALIGHT
(PERIOD DIFFERS FOR DIFFERENT PIXELS)
(b) RAMP VOLTAGE
ODD-NUMBERED LINES
(HORIZONTAL OR VERTICAL)
ALIGHT
EVEN-NUMBERED LINES
(HORIZONTAL OR VERTICAL)
ALIGHT
(c) RAMP VOLTAGE
G
ALIGHT
R,B
ALIGHT

FIG.8

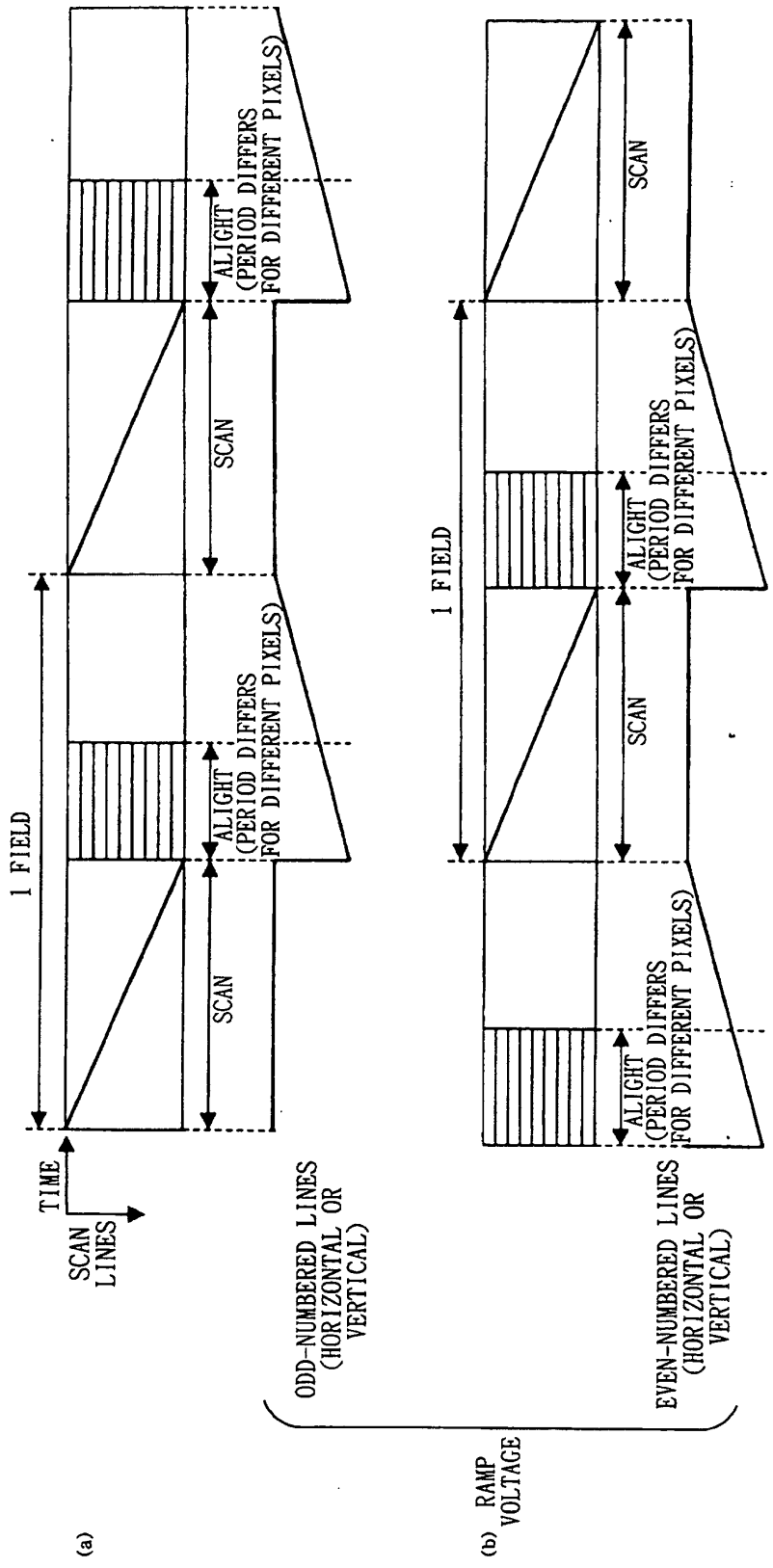

(a)
TIME
SCAN LINES
1 FIELD
ALIGHT (PERIOD DIFFERS FOR DIFFERENT PIXELS)
SCAN
ALIGHT (PERIOD DIFFERS FOR DIFFERENT PIXELS)
SCAN
ODD-NUMBERED LINES (HORIZONTAL OR VERTICAL)
(b) RAMP VOLTAGE
1 FIELD
SCAN
ALIGHT (PERIOD DIFFERS FOR DIFFERENT PIXELS)
SCAN
ALIGHT (PERIOD DIFFERS FOR DIFFERENT PIXELS)
EVEN-NUMBERED LINES (HORIZONTAL OR VERTICAL)

FIG.9

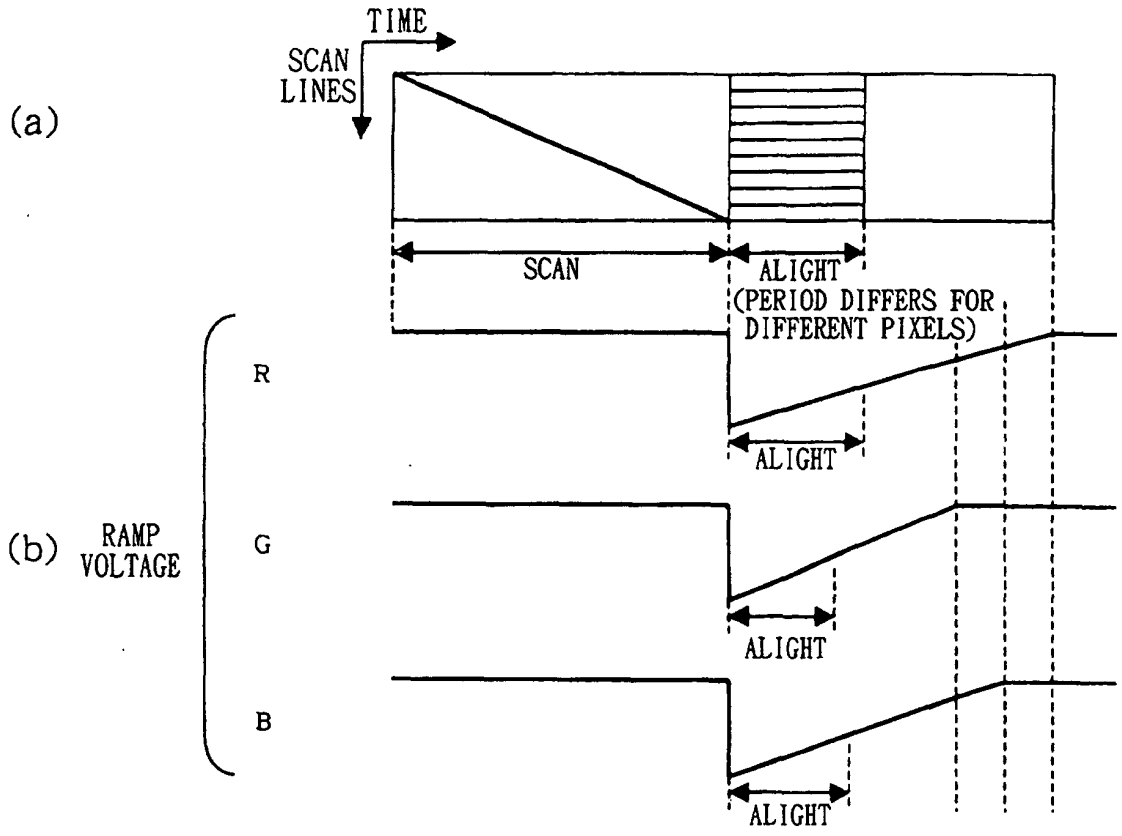

(a)
TIME
SCAN LINES
SCAN
ALIGHT
(PERIOD DIFFERS FOR DIFFERENT PIXELS)
(b)
RAMP VOLTAGE
R
G
B
ALIGHT
ALIGHT
ALIGHT

FIG.10

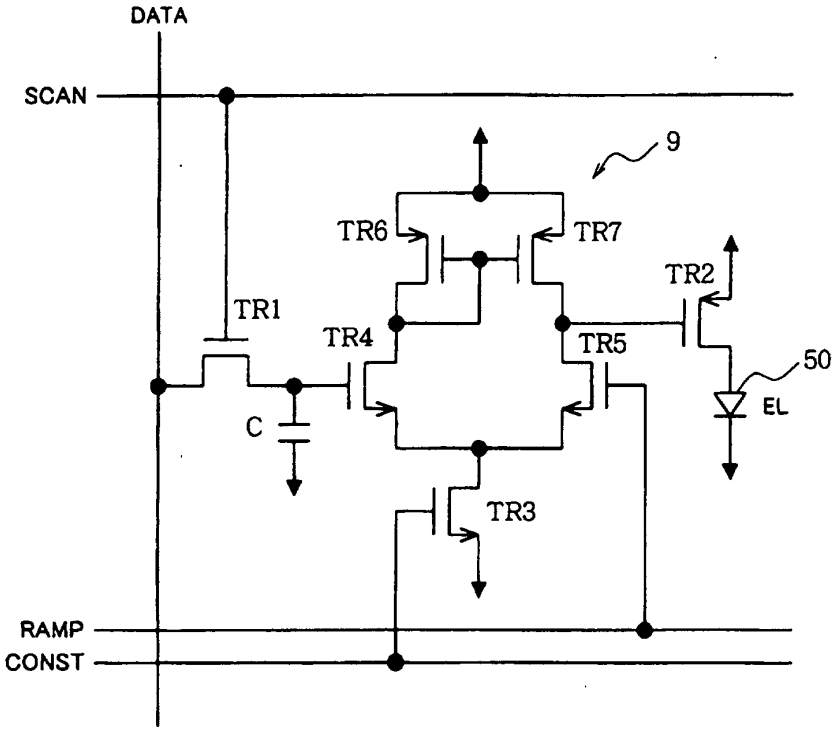

DATA
SCAN
9
TR6
TR7
TR2
TR1
TR4
TR5
50
EL
C
TR3
RAMP
CONST

FIG.11

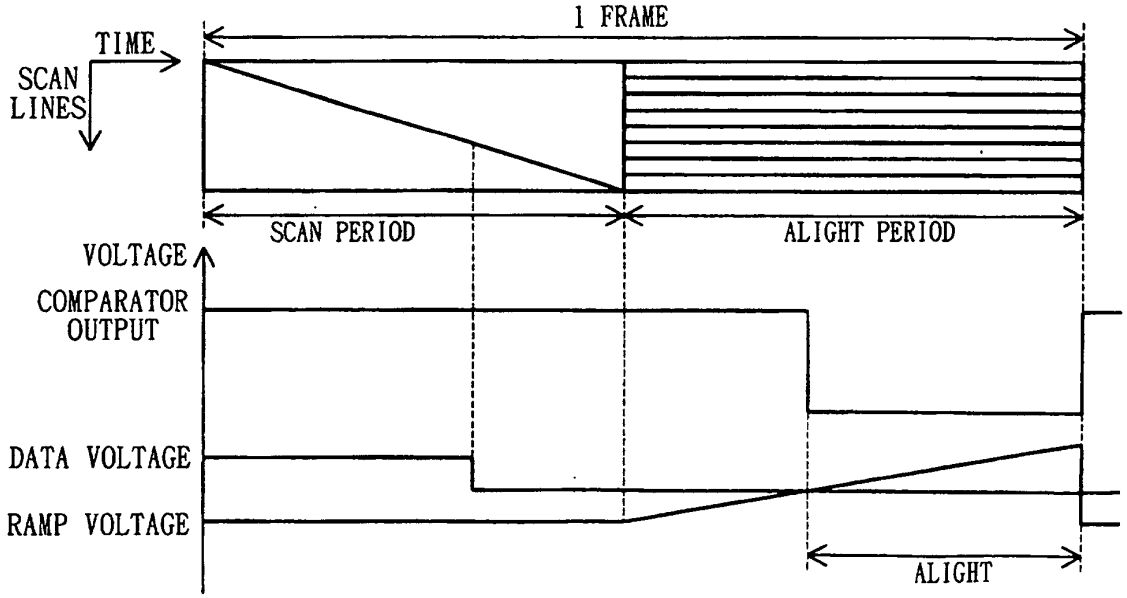

1 FRAME
TIME
SCAN LINES
SCAN PERIOD
ALIGHT PERIOD
VOLTAGE
COMPARATOR OUTPUT
DATA VOLTAGE
RAMP VOLTAGE
ALIGHT

FIG.12

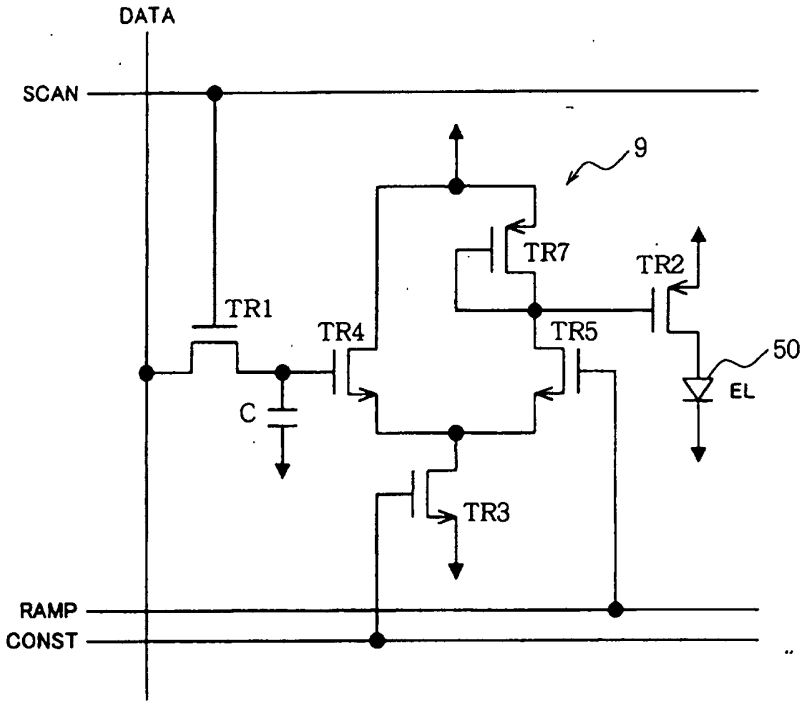

DATA
SCAN
9
TR7
TR2
TR1
TR4
TR5
50
EL
C
TR3
RAMP
CONST

FIG.13

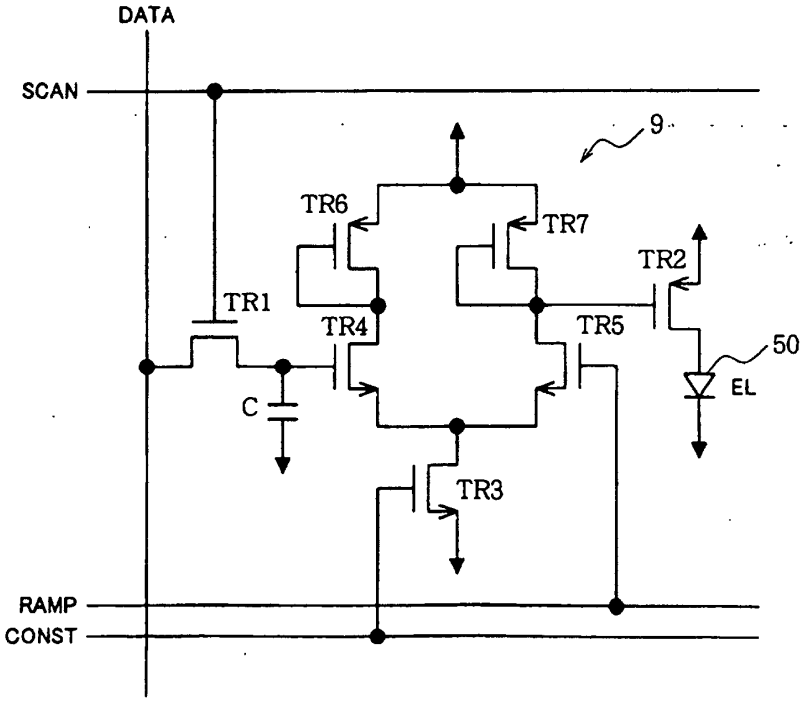

DATA
SCAN
9
TR6
TR7
TR2
TR1
TR4
TR5
50
EL
C
TR3
RAMP
CONST

FIG.14

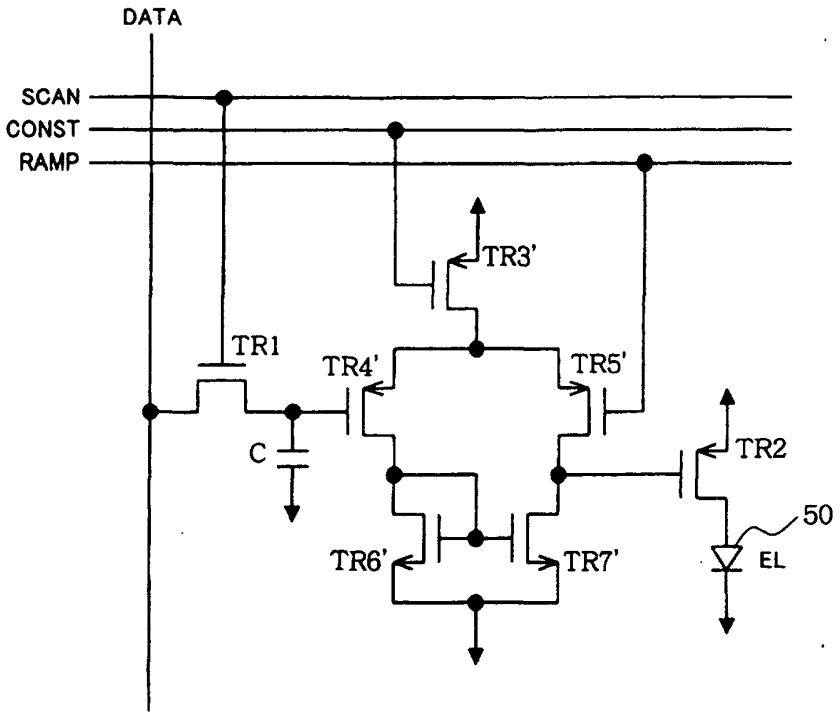

DATA
SCAN
CONST
RAMP
TR3'
TR1
TR4'
TR5'
C
TR2
50
TR6'
TR7'
EL

FIG.15

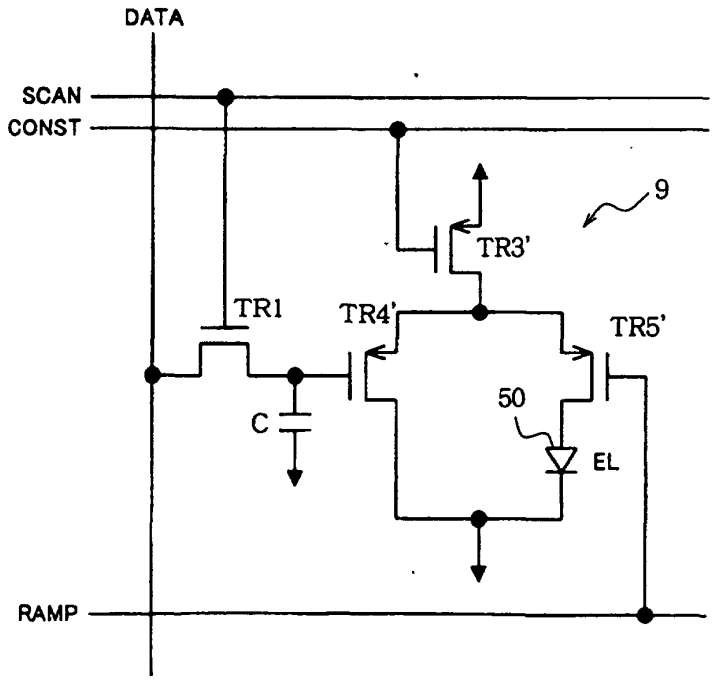

DATA
SCAN
CONST
9
TR3'
TR1
TR4'
TR5'
50
C
EL
RAMP

FIG.16

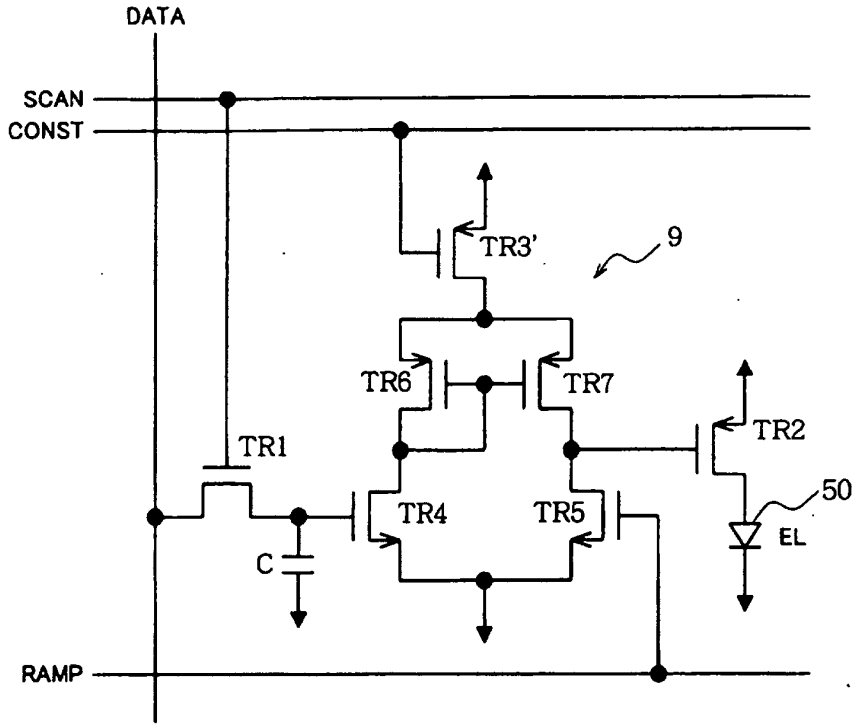

DATA
SCAN
CONST
TR3'
9
TR6
TR7
TR2
TR1
50
TR4
TR5
EL
C
RAMP

FIG.17

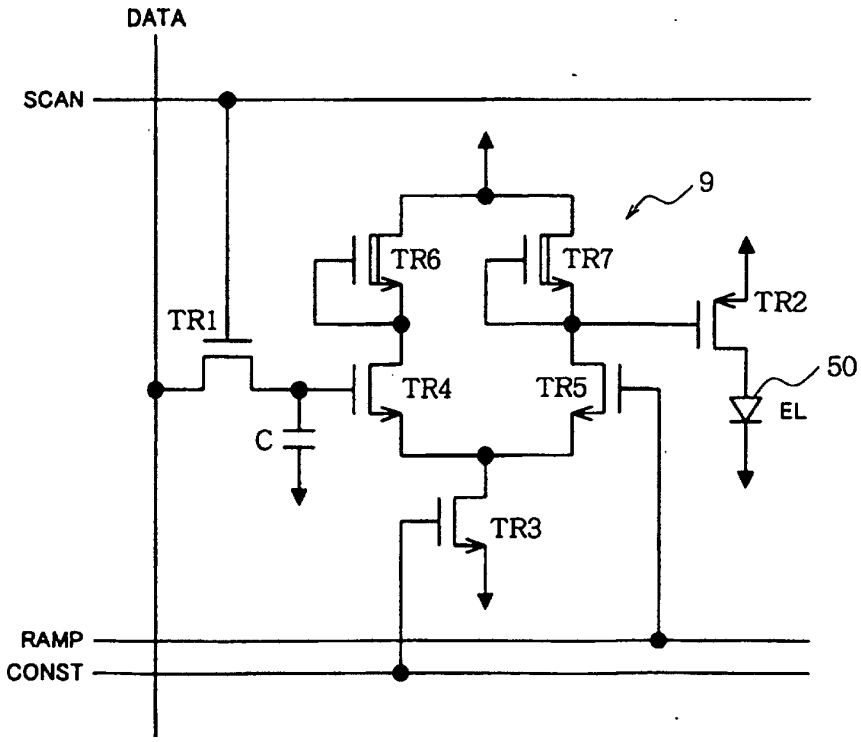

DATA
SCAN
9
TR6
TR7
TR2
TR1
50
TR4
TR5
EL
C
TR3
RAMP
CONST

FIG.18

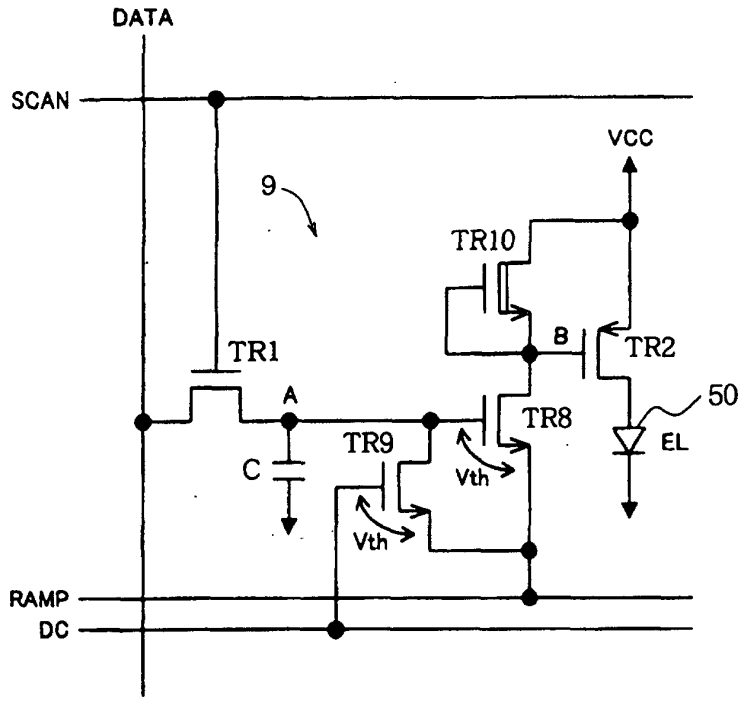

DATA
SCAN
VCC
9
TR10
TR1
B
TR2
A
50
TR8
TR9
EL
C
Vth
Vth
RAMP
DC

FIG.19

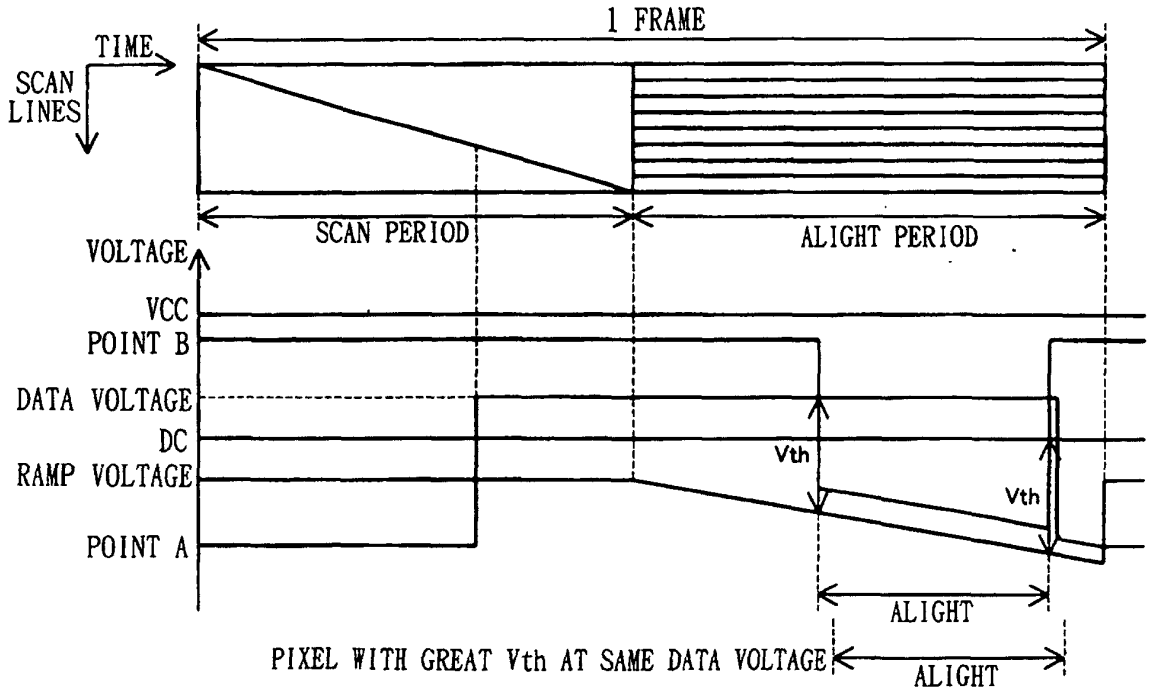

1 FRAME
TIME
SCAN LINES
SCAN PERIOD
ALIGHT PERIOD
VOLTAGE
VCC
POINT B
DATA VOLTAGE
DC
RAMP VOLTAGE
POINT A
Vth
Vth
ALIGHT
PIXEL WITH GREAT Vth AT SAME DATA VOLTAGE
ALIGHT

FIG.20

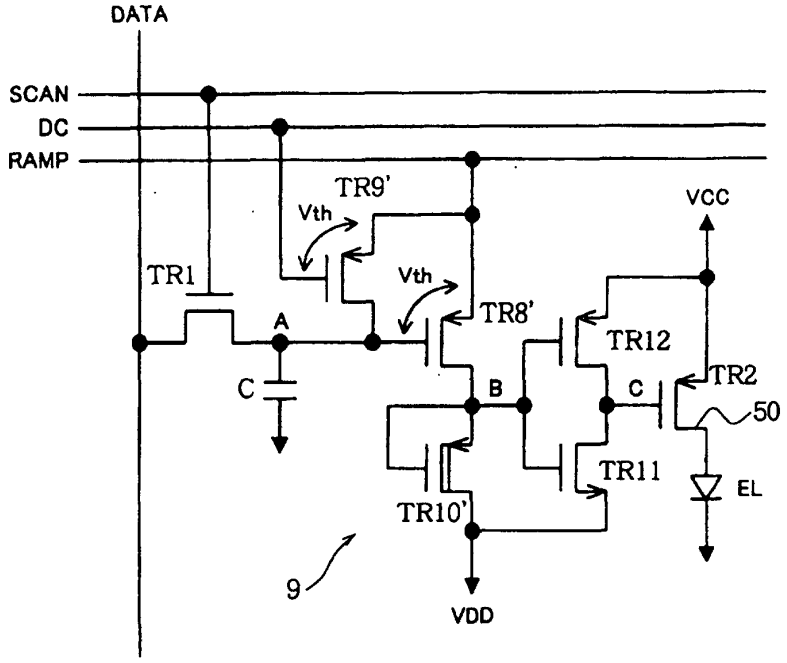

DATA
SCAN
DC
RAMP
TR9'
Vth
VCC
TR1
Vth
TR8'
TR12
A
C
B
C
TR2
50
TR11
EL
TR10'
9
VDD

FIG.21

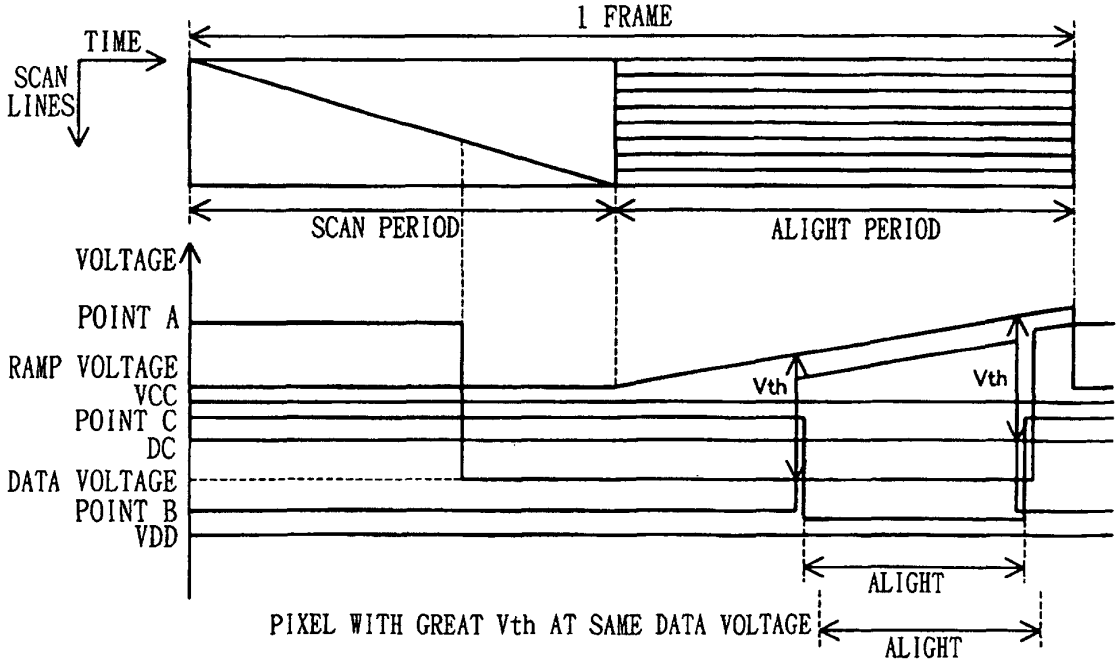

1 FRAME
TIME
SCAN LINES
SCAN PERIOD
ALIGHT PERIOD
VOLTAGE
POINT A
RAMP VOLTAGE
VCC
POINT C
DC
DATA VOLTAGE
POINT B
VDD
Vth
Vth
ALIGHT
PIXEL WITH GREAT Vth AT SAME DATA VOLTAGE
ALIGHT

FIG.22

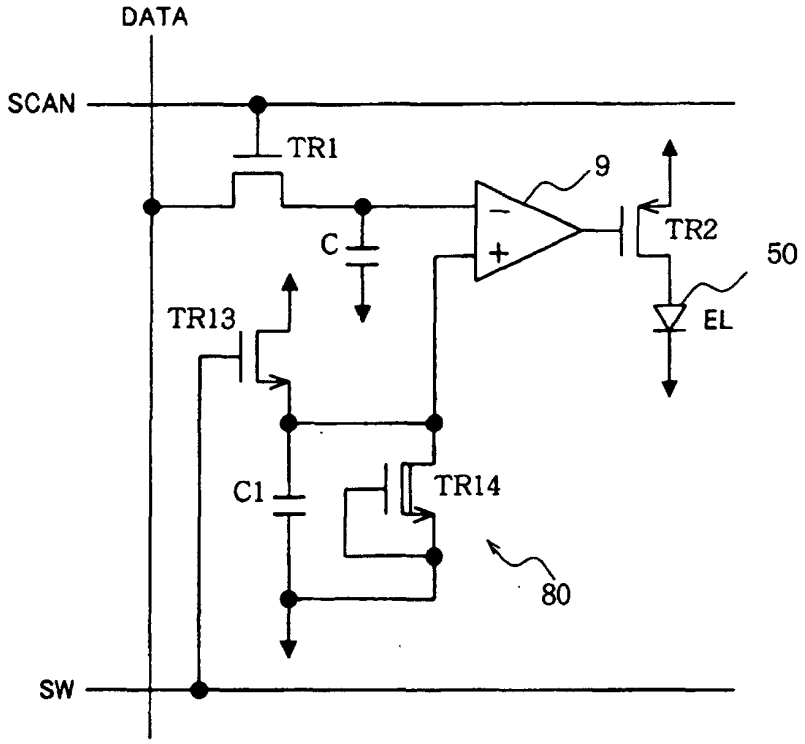


FIG.23

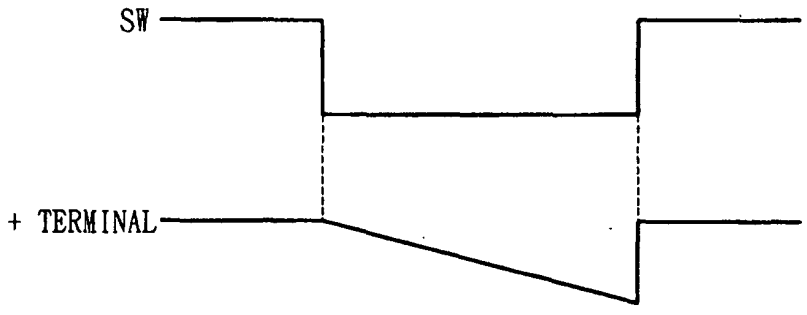


FIG.24

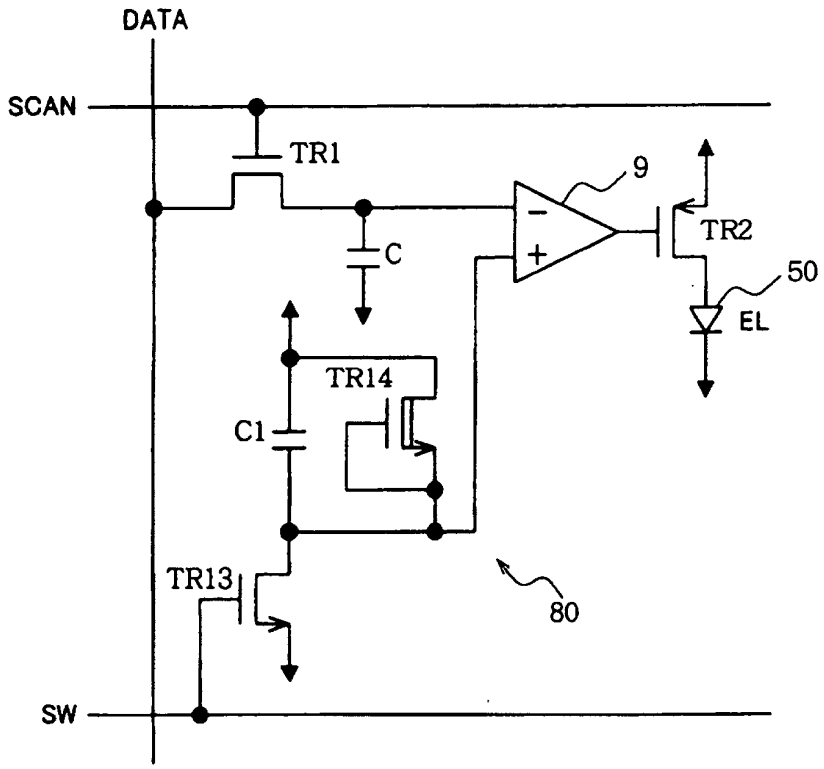


FIG.25

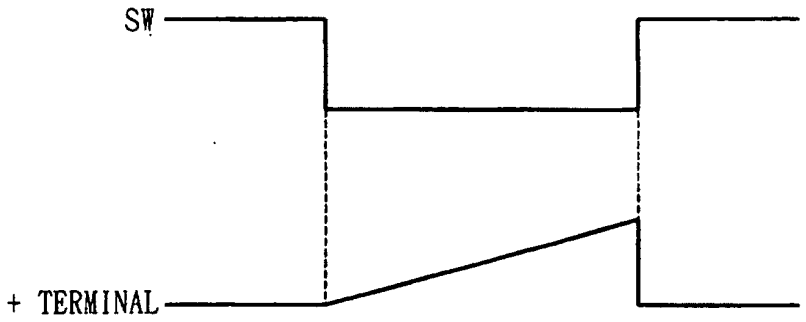


FIG.26

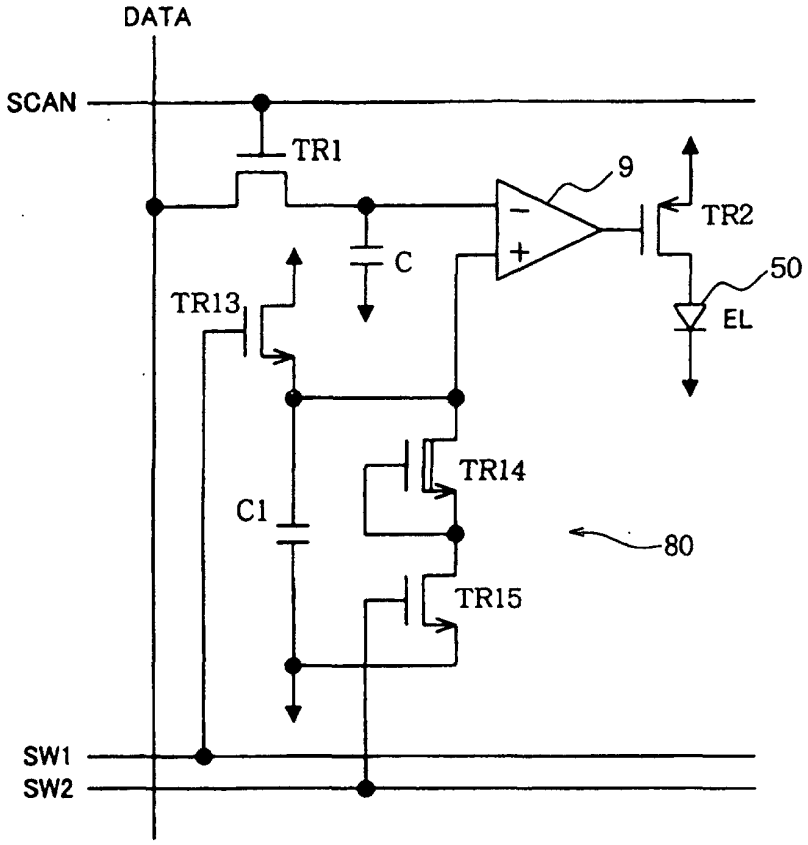

DATA
SCAN
TR1
9
TR2
C
50
TR13
EL
TR14
C1
80
TR15
SW1
SW2

FIG.27

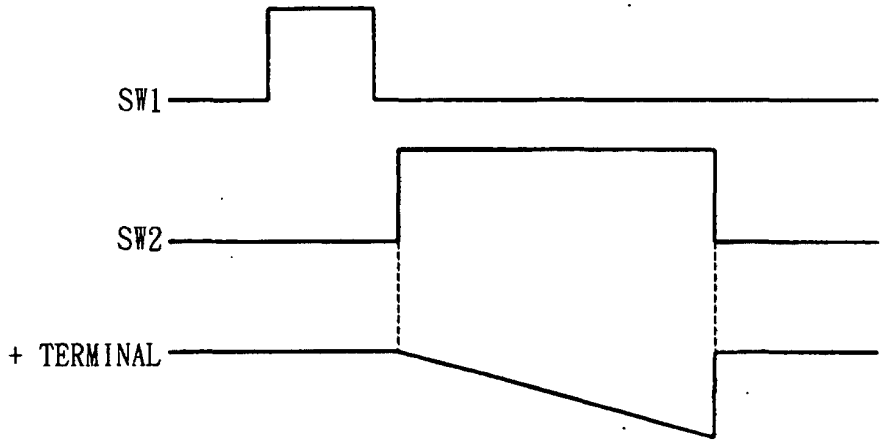

SW1
SW2
+ TERMINAL

FIG.28

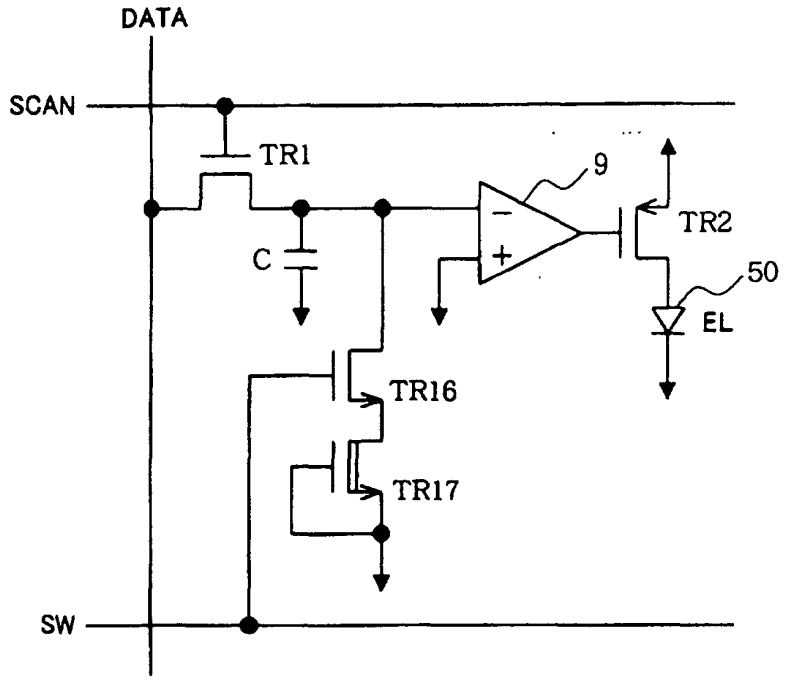

DATA
SCAN
TR1
9
TR2
C
50
EL
TR16
TR17
SW

FIG.29

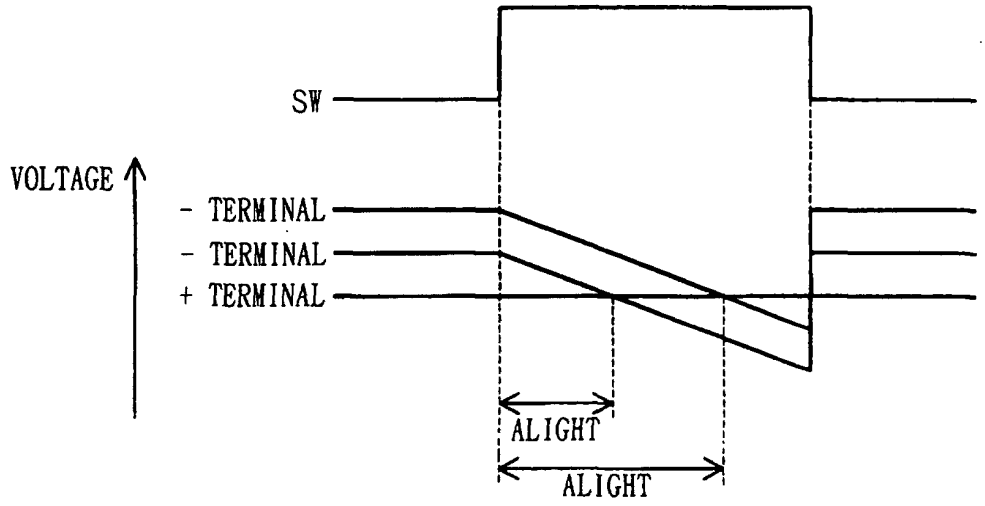

SW
VOLTAGE
- TERMINAL
- TERMINAL
+ TERMINAL
ALIGHT
ALIGHT

FIG.30

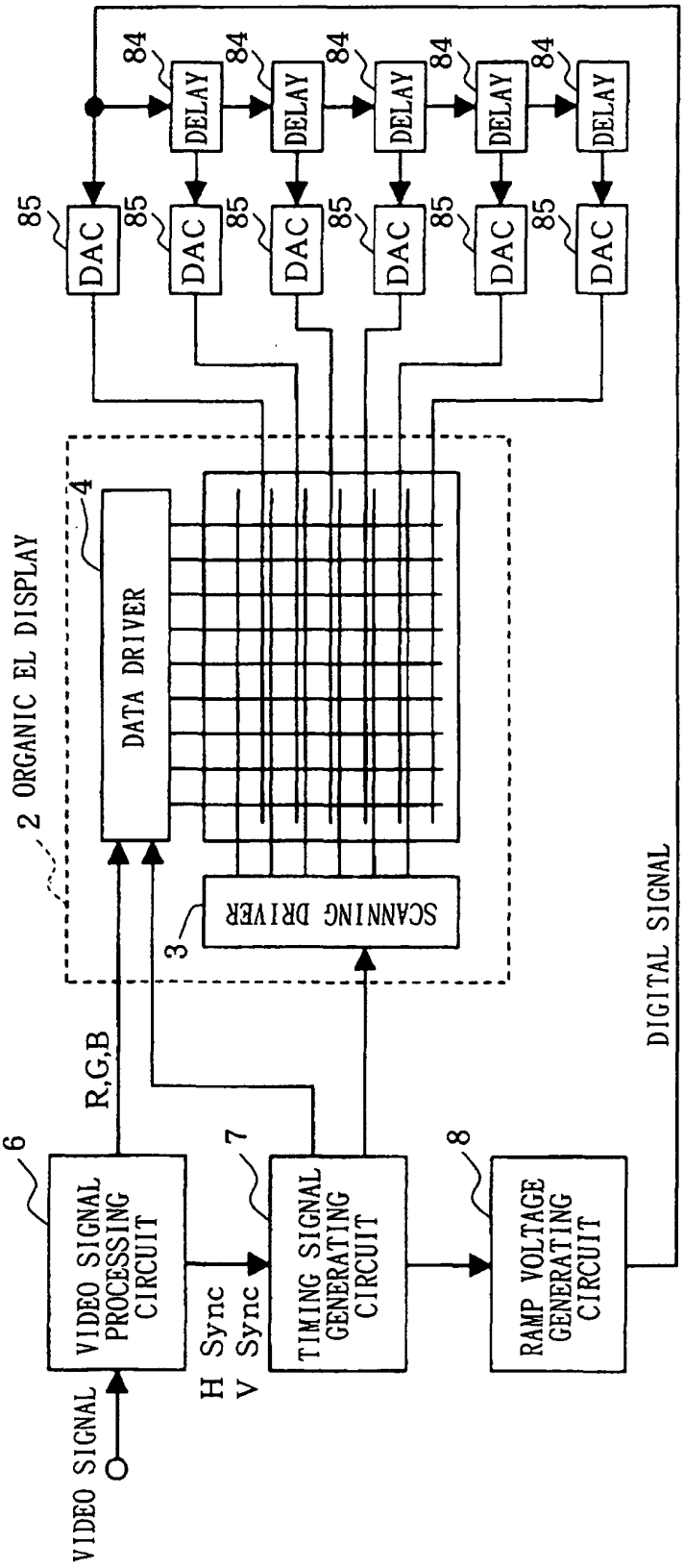

VIDEO SIGNAL
VIDEO SIGNAL PROCESSING CIRCUIT
6
R,G,B
H Sync
V Sync
TIMING SIGNAL GENERATING CIRCUIT
7
RAMP VOLTAGE GENERATING CIRCUIT
8
DIGITAL SIGNAL
2 ORGANIC EL DISPLAY
DATA DRIVER
4
SCANNING DRIVER
3
DAC
85
DELAY
84

FIG.31

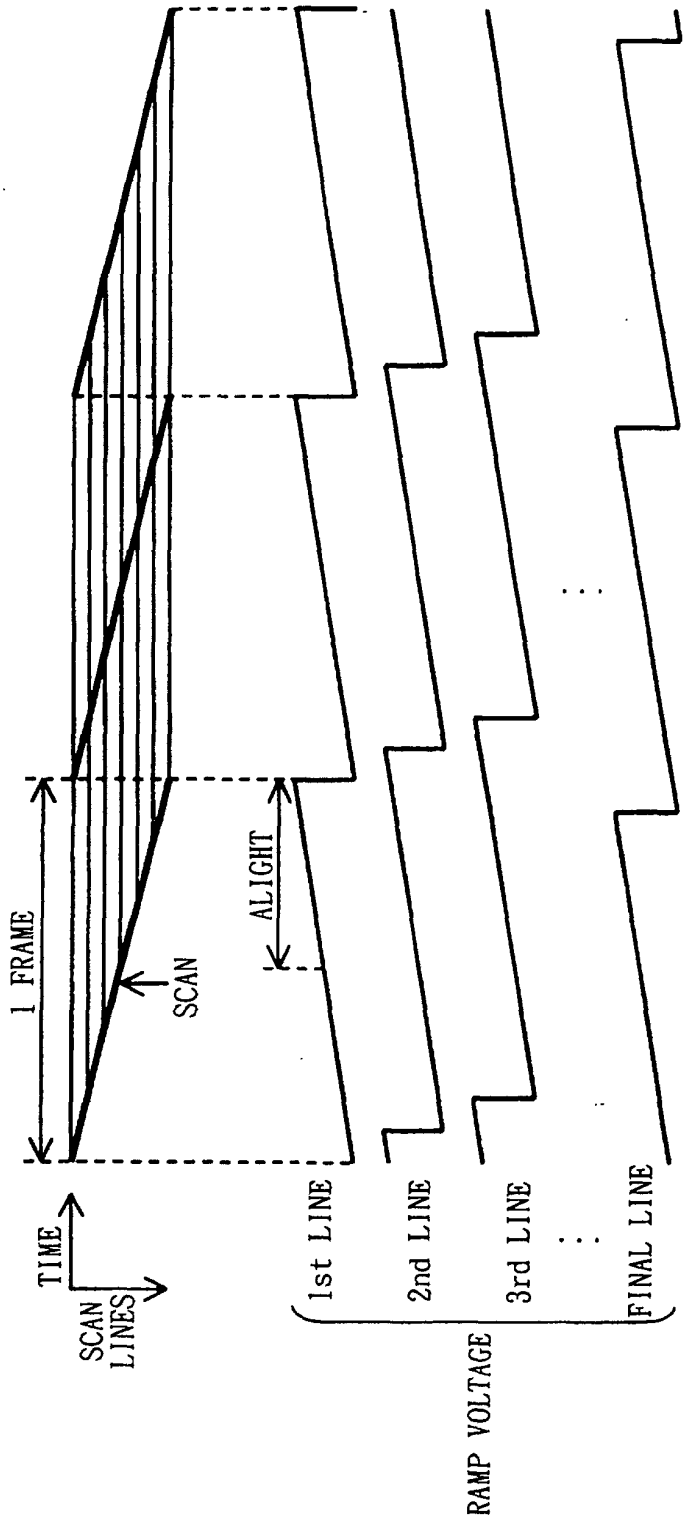

1 FRAME
SCAN
ALIGHT
TIME
SCAN LINES
1st LINE
2nd LINE
3rd LINE
FINAL LINE
RAMP VOLTAGE

FIG.32

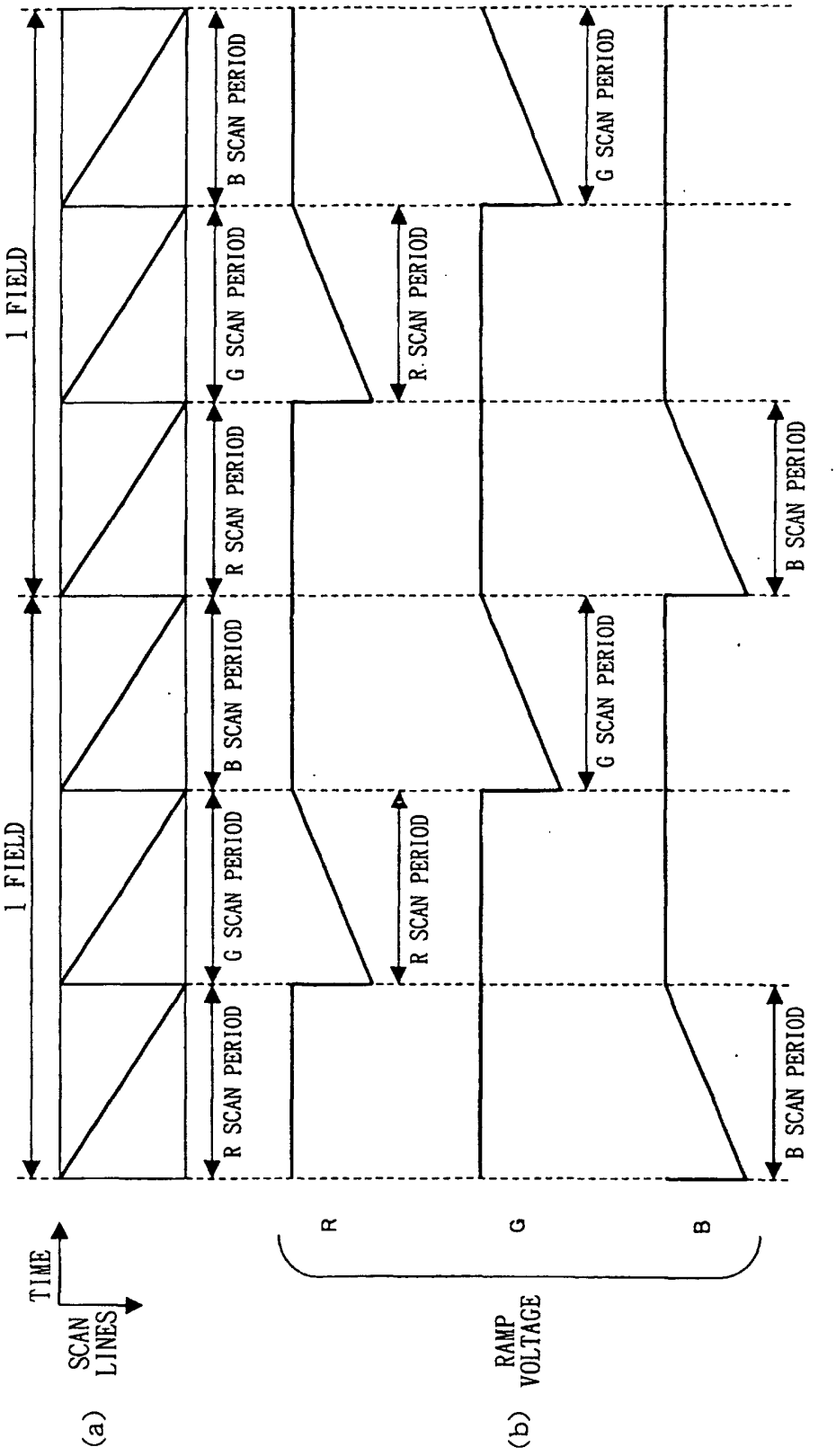

1 FIELD
1 FIELD
R SCAN PERIOD
G SCAN PERIOD
B SCAN PERIOD
R SCAN PERIOD
G SCAN PERIOD
B SCAN PERIOD
R SCAN PERIOD
G SCAN PERIOD
B SCAN PERIOD
R SCAN PERIOD
G SCAN PERIOD
B SCAN PERIOD
TIME
SCAN LINES
(a)
R
G
B
RAMP VOLTAGE
(b)

FIG.33

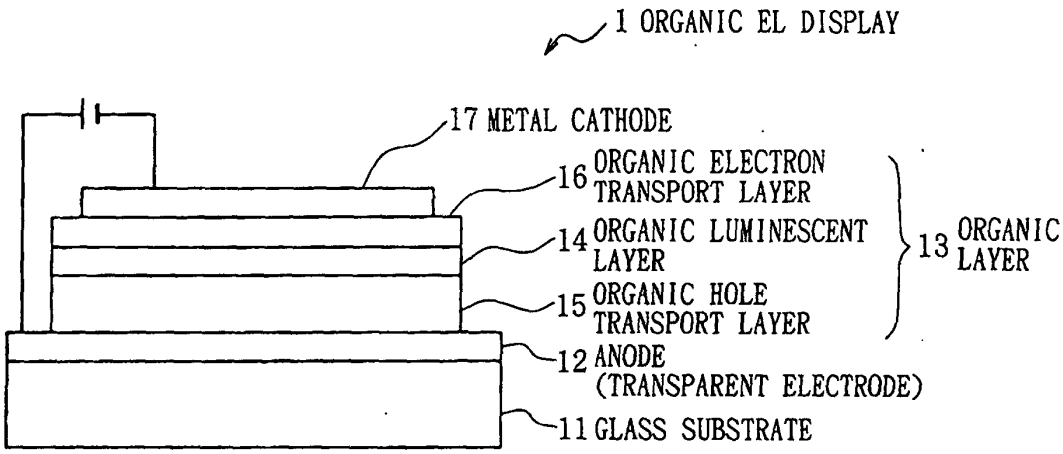
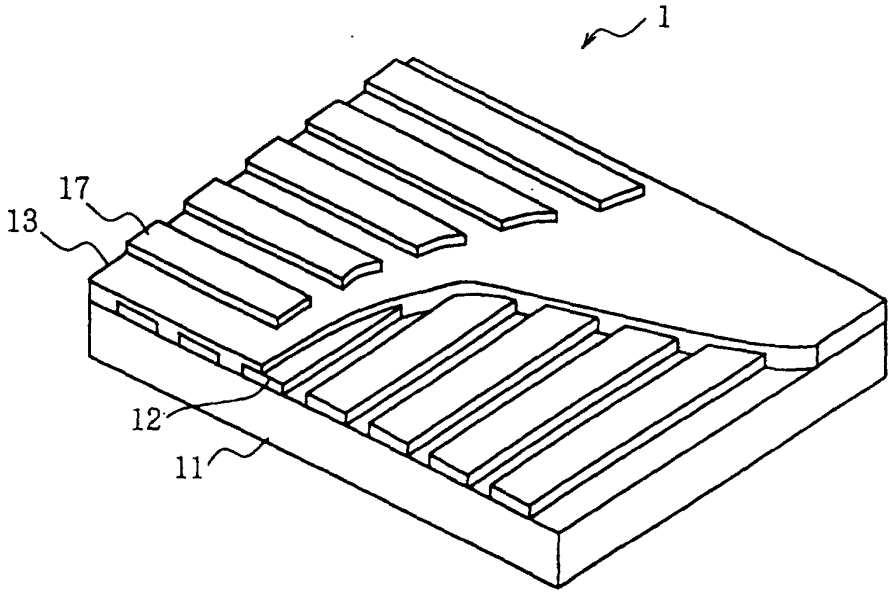

1 ORGANIC EL DISPLAY
17 METAL CATHODE
16 ORGANIC ELECTRON TRANSPORT LAYER
14 ORGANIC LUMINESCENT LAYER
15 ORGANIC HOLE TRANSPORT LAYER
13 ORGANIC LAYER
12 ANODE (TRANSPARENT ELECTRODE)
11 GLASS SUBSTRATE

FIG.34


1
17
13
12
11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP02/12876

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] G09G3/30, 3/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] G09G3/20-3/38

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1926-1996	Jitsuyo Shinan Toroku Koho	1996-2003
Kokai Jitsuyo Shinan Koho	1971-2003	Toroku Jitsuyo Shinan Koho	1994-2003

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y A	JP 2000-235370 A (NEC Corp.), 29 August, 2000 (29.08.00), Par. Nos. [0022] to [0042]; Figs. 1 to 3 (Family: none)	1,22 2-9,12-14, 17,20-21 10-11,15-16, 18-19
X Y A	JP 2001-22315 A (Seiko Epson Corp.), 26 January, 2001 (26.01.01), Par. Nos. [0049] to [0055] [0084]; Figs. 2, 4 (Family: none)	1,20 2-9,12-14, 17,21-22 10-11,15-16, 18-19
Y A	JP 9-243994 A (Toshiba Corp.), 19 September, 1997 (19.09.97), Par. Nos. [0022] to [0036]; Figs. 1 to 4 (Family: none)	1-9,12-14, 17,21-22 10-11,15-16, 18-20

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 January, 2003 (14.01.03)	28 January, 2003 (28.01.03)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP02/12876

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	JP 11-338402 A (Hewlett-Packard Co.), 10 December, 1999 (10.12.99), Full text; all drawings & EP 0953959 A2 & US 6329974 B1 & US 2002/0021267 A1	1-9,12-13, 17,21-22 10-11,14-16, 18-20
A	JP 60-73581 A (Toshiba Denzai Kabushiki Kaisha), 25 April, 1985 (25.04.85), Full text; all drawings (Family: none)	1-22
Y	JP 5-328269 A (Citizen Watch Co., Ltd.), 10 December, 1993 (10.12.10), Figs. 5 to 7 & WO 93/25045 A1	6-7
Y	JP 2-55280 U (Casio Computer Co., Ltd.), 20 April, 1990 (20.04.90), Full text; all drawings (Family: none)	8-9
Y	JP 1-124827 A (Citizen Watch Co., Ltd.), 17 May, 1989 (17.05.89), Full text; all drawings & GB 2212361 A & US 4942458 A	12
A	JP 5-503175 A (THOMSON S.A.), 27 May, 1993 (27.05.93), Full text; all drawings & WO 92/07351 A1	1-22
P,X	JP 2002-297097 A (Hitachi, Ltd.), 09 October, 2002 (09.10.02), Full text; all drawings (Family: none)	1-6,13-14, 17,20-22
P,X	WO 02/27700 A2 (Seiko Epson Corp.), 04 April, 2002 (04.04.02), Full text; all drawings & GB 2367413 A	1-6,8-9, 13-14,17, 21-22

Form PCT/ISA/210 (continuation of second sheet) (July 1998)

专利名称(译)	数字驱动型显示装置		
公开(公告)号	EP1455335A1	公开(公告)日	2004-09-08
申请号	EP2002790707	申请日	2002-12-09
[标]申请(专利权)人(译)	三洋电机株式会社		
申请(专利权)人(译)	SANYO ELECTRIC CO.，LTD.		
当前申请(专利权)人(译)	SANYO ELECTRIC CO.，LTD.		
[标]发明人	YAMASHITA ATSUHIRO SANYO ELECTRIC CO LTD MURATA HARUHIKO SANYO ELECTRIC CO LTD MORI YUKIO SANYO ELECTRIC CO LTD INOUE MASUTAKA SANYO ELECTRIC CO LTD KINOSHITA SHIGEO SANYO ELECTRIC CO LTD TANASE SUSUMU SANYO ELECTRIC CO LTD		
发明人	YAMASHITA, ATSUHIRO, SANYO ELECTRIC CO., LTD. MURATA, HARUHIKO, SANYO ELECTRIC CO., LTD. MORI, YUKIO, SANYO ELECTRIC CO., LTD. INOUE, MASUTAKA, SANYO ELECTRIC CO., LTD. KINOSHITA, SHIGEO, SANYO ELECTRIC CO., LTD. TANASE, SUSUMU, SANYO ELECTRIC CO., LTD.		
IPC分类号	H01L51/50 G09G3/20 G09G3/30 G09G3/32 H04N5/70		
CPC分类号	G09G3/2022 G09G3/2014 G09G3/3258 G09G2300/0809 G09G2300/0833 G09G2300/0842 G09G2300/0852 G09G2300/0861 G09G2310/0259 G09G2310/066 G09G2320/0242		
优先权	2002095425 2002-03-29 JP 2001381240 2001-12-14 JP		
其他公开文献	EP1455335A4 EP1455335B1		
外部链接	Espacenet		

摘要(译)

本发明提供一种数字驱动型有机LED显示装置，其具有包括多个像素51的显示面板。每个像素51包括有机EL元件50，用于实现或中断电流通过的驱动晶体管TR2。 EL元件50响应于开/关控制信号的输入，写入晶体管TR1在接收从扫描驱动器施加到其上的扫描电压时导通，电容元件C从数据提供数据电压写入晶体管TR1导通的驱动器和比较器9，用于将预定的斜坡电压与电容元件C的输出电压进行比较，并将比较结果作为导通/截止控制信号提供给驱动晶体管TR2。

FIG.3