



- (51) **International Patent Classification:**
H01L 27/12 (2006.01) **H01L 27/32** (2006.01)
H01L 21/77 (2006.01)
- (21) **International Application Number:**
PCT/CN2016/078554
- (22) **International Filing Date:**
6 April 2016 (06.04.2016)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**
201510446925.3 27 July 2015 (27.07.2015) CN
- (71) **Applicant:** BOE TECHNOLOGY GROUP CO., LTD.
[CN/CN]; No.10 Jiuxianqiao Rd., Chaoyang District,
Beijing 100015 (CN).
- (72) **Inventors:** FANG, Jingang; No.9 Dize Rd., BDA, Beijing
100176 (CN). LIU, Xiaodi; No.9 Dize Rd., BDA, Beijing
100176 (CN). WANG, Dongfang; No.9 Dize Rd., BDA,
Beijing 100176 (CN). HSIN, Lungpao; No.9 Dize Rd.,
BDA, Beijing 100176 (CN).
- (74) **Agent:** TEE&HOWE INTELLECTUAL PROPERTY
ATTORNEYS; CHEN, Yuan, 10th Floor, Tower D, Min-
sheng Financial Center, 28 Jianguomennei Avenue,
Dongcheng District, Beijing 100005 (CN).

- (81) **Designated States** (unless otherwise indicated, for every
kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY,
BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR,
KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG,
MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM,
PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC,
SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) **Designated States** (unless otherwise indicated, for every
kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ,
TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU,
TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE,
DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,
LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK,
SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,
GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

- (54) **Title:** LIGHT EMITTING DIODE, DISPLAY SUBSTRATE AND DISPLAY DEVICE HAVING THE SAME, AND FABRICATING METHOD THEREOF

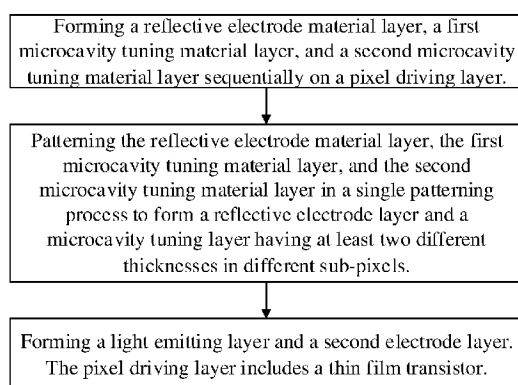


FIG. 1

- (57) **Abstract:** A light emitting diode comprising a plurality of sub-pixels comprises a first electrode layer, wherein the first electrode layer is a reflective electrode layer, a second electrode layer, a light emitting layer between the first electrode layer and the second electrode layer, a first microcavity tuning layer sandwiched by the first electrode layer and the light emitting layer within the plurality of sub-pixels and a second microcavity tuning layer sandwiched by the first microcavity tuning layer and the light emitting layer within at least one of the plurality of sub-pixels. The first microcavity tuning layer is sandwiched by the first electrode layer and the second microcavity tuning layer within the at least one of the plurality of sub-pixels. The first microcavity tuning layer is made of a material including a transparent conductive material in a first state and the second microcavity tuning layer is made of a material including a transparent conductive material in a second state. The first state and the second state are different states selected from a crystalline state and an amorphous state.



LIGHT EMITTING DIODE, DISPLAY SUBSTRATE AND DISPLAY DEVICE HAVING THE SAME, AND FABRICATING METHOD THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to Chinese Patent Application No. 201510446925.3, filed July 27, 2015, the contents of which are incorporated by reference in the entirety.

TECHNICAL FIELD

[0002] The present invention relates to display technology, more particularly, to a light emitting diode, a display substrate and a display device having the same, and a fabricating method thereof.

BACKGROUND

[0003] As compared to other display devices such as liquid crystal display (LCD) devices, the organic light emitting diode (OLED) display devices are self-emitting apparatuses that do not require a backlight. Having the advantages of fast response, a wider viewing angle, high brightness, more vivid color rendering, thinner and lighter, they have found a wide range of applications in display field.

[0004] Typically, a convention OLED includes an anode, a light emitting layer and a cathode. The light emitting layer often includes an emitting layer (EML), and optionally one or more of a hole injection layer (HIL), a hole transport layer (HTL), an electron transport layer (ETL), and an electrode injection layer (EIL). When a voltage is applied between the cathode and the anode, charge carriers (electrons and holes) are injected from the cathode and the anode into the emitting layer. The electrons and holes are recombined in the emitting layer, which emits light. Some OLED devices also include one or more microcavities.

SUMMARY

[0005] In one aspect, the present invention provides a light emitting diode comprising a plurality of sub-pixels comprising a first electrode layer, wherein the first electrode layer is a reflective electrode layer; a second electrode layer; a light emitting layer between the first electrode layer and the second electrode layer; a first microcavity tuning layer sandwiched by the first electrode layer and the light emitting layer within the plurality of sub-pixels; and a second microcavity tuning layer sandwiched by the first microcavity tuning layer and the

light emitting layer within at least one of the plurality of sub-pixels, and the first microcavity tuning layer is sandwiched by the first electrode layer and the second microcavity tuning layer within the at least one of the plurality of sub-pixels. The first microcavity tuning layer is made of a material comprising a transparent conductive material in a first state and the second microcavity tuning layer is made of a material comprising a transparent conductive material in a second state, the first state and the second state are different states selected from a crystalline state and an amorphous state.

[0006] Optionally, the first microcavity layer is made of material comprising a crystalline transparent conductive oxide and the second microcavity tuning layer is made of a material comprising an amorphous transparent conductive oxide.

[0007] Optionally, the crystalline transparent conductive oxide is a crystalline transparent conductive indium tin oxide.

[0008] Optionally, the amorphous transparent conductive oxide is selected from one or a combination of an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide.

[0009] Optionally, the first electrode layer has a thickness in the range of about 50 nm to about 300 nm.

[0010] Optionally, the first microcavity tuning layer has a thickness in the range of about 5 nm to about 15 nm.

[0011] Optionally, the second microcavity tuning layer has a thickness in the range of about 50 nm to about 70 nm.

[0012] Optionally, the first electrode layer is made of a material comprising an alloy having a reflectivity higher than 90%.

[0013] Optionally, a first sub-pixel has the first microcavity, and a second sub-pixel and a third sub-pixel have the second microcavity.

[0014] Optionally, the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel.

[0015] In another aspect, the present invention provides a method of fabricating a display substrate comprising an array of pixels, each pixel comprising at least three sub-pixels, the method comprising forming a first electrode layer, wherein the first electrode layer is a

reflective electrode layer; forming a microcavity tuning layer comprising a first microcavity tuning layer and a second microcavity tuning layer on the first electrode layer; forming a light emitting layer on a side of the microcavity tuning layer distal to the first electrode layer; and forming a second electrode layer on a side of the light emitting layer distal to the microcavity tuning layer. The first microcavity tuning layer is sandwiched by the first electrode layer and the light emitting layer within three sub-pixels. The second microcavity tuning layer is sandwiched by the first microcavity tuning layer and the light emitting layer within at least one of three sub-pixels, and the first microcavity tuning layer is sandwiched by the first electrode layer and the second microcavity tuning layer within the at least one of three sub-pixels. The first microcavity tuning layer is made of a material comprising a transparent conductive material in a first state and the second microcavity tuning layer is made of a material comprising a transparent conductive material in a second state, the first state and the second state are different states selected from a crystalline state and an amorphous state.

[0016] Optionally, the first microcavity layer is made of a material comprising a crystalline transparent conductive oxide and the second microcavity tuning layer is made of a material comprising an amorphous transparent conductive oxide.

[0017] Optionally, the crystalline transparent conductive oxide is a crystalline transparent conductive indium tin oxide.

[0018] Optionally, the amorphous transparent conductive oxide is selected from one or a combination of an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide.

[0019] Optionally, the first electrode layer, the first microcavity tuning layer and the second microcavity tuning layer are patterned using a single mask.

[0020] Optionally, the single mask is a gray-tone mask plate or a half-tone mask plate, and the step of forming a microcavity tuning layer comprises using a gray-tone mask plate or a half-tone mask plate to obtain a pattern, wherein the pattern comprises a first section corresponding to the first microcavity, the second section corresponding to the second microcavity, and a third section corresponding to the remaining portion of the photoresist layer.

[0021] Optionally, the step of forming a microcavity tuning layer comprising forming a reflective electrode material layer; forming a first microcavity tuning material layer on the reflective electrode material layer; forming a second microcavity tuning material layer on a

side of the first microcavity tuning layer distal to the reflective electrode material layer; forming a photoresist layer on a side of the second microcavity tuning material layer distal to the first microcavity tuning material layer; exposing the photoresist layer with a gray-tone mask plate or a half-tone mask plate; developing the exposed photoresist layer to obtain a pattern, wherein the pattern comprises a first section corresponding to the first microcavity, the second section corresponding to the second microcavity, and a third section corresponding to the remaining portion of the photoresist layer; removing the photoresist layer in the third section and partially removing the photoresist layer in the first section; etching the second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section thereby forming the first electrode layer; removing the photoresist layer in the first section thereby exposing the second microcavity tuning material layer in the first section; etching the second microcavity tuning material layer in the first section thereby exposing the first microcavity tuning material layer in the first section; and removing the photoresist layer in the second section.

[0022] Optionally, the step of etching the second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section comprises sequentially etching the third section with a second microcavity tuning material etchant, a first microcavity tuning material etchant, and a reflective electrode material etchant.

[0023] Optionally, the step of etching the second microcavity tuning material layer in the first section comprises etching the first section with a second microcavity tuning material etchant.

[0024] Optionally, a first sub-pixel has the first microcavity, and a second sub-pixel and a third sub-pixel have the second microcavity.

[0025] Optionally, the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel.

[0026] Optionally, the first electrode layer is made of a material comprising an alloy having a reflectivity higher than 90%.

[0027] Optionally, the first electrode layer has a thickness in the range of about 50 nm to about 300 nm.

[0028] Optionally, the first microcavity tuning layer has a thickness in the range of about 5 nm to about 15 nm.

[0029] Optionally, the second microcavity tuning layer has a thickness in the range of about 50 nm to about 70 nm.

[0030] In another aspect, the present invention provides a display substrate comprising the light emitting diode described herein or manufactured by a method described herein.

[0031] In another aspect, the present invention provides a display device comprising the array substrate described herein.

BRIEF DESCRIPTION OF THE FIGURES

[0032] The following drawings are merely examples for illustrative purposes according to various disclosed embodiments and are not intended to limit the scope of the present invention.

[0033] FIG. 1 is a flow chart illustrating a method of fabricating a display substrate in some embodiments.

[0034] FIG. 2 is a flow chart illustrating a method of fabricating a display substrate in some embodiments.

[0035] FIG. 3 is a diagram illustrating the structure of various layers of a display substrate in some embodiments.

[0036] FIG. 4 is a diagram illustrating the structure of various layers of a display substrate in some embodiments.

[0037] FIG. 5 is a diagram illustrating the structure of various layers of a display substrate in some embodiments.

[0038] FIG. 6 is a diagram illustrating the structure of various layers of a display substrate in some embodiments.

[0039] FIG. 7 is a diagram illustrating the structure of various layers of a display substrate in some embodiments.

[0040] FIG. 8 is a diagram illustrating the structure of a display substrate having a reflective electrode layer, a first microcavity tuning layer and a second microcavity tuning layer in some embodiments.

DETAILED DESCRIPTION

[0041] The disclosure will now describe more specifically with reference to the following embodiments. It is to be noted that the following descriptions of some embodiments are

presented herein for purpose of illustration and description only. It is not intended to be exhaustive or to be limited to the precise form disclosed.

[0042] In making a conventional microcavity OLED device, multiple patterning processes involving multiple mask plates are required to form a reflective electrode layer and multiple microcavity tuning layers in a display substrate. The microcavity tuning layer typically has a small thickness. When multiple etching processes are involved, it is difficult to control the etching processes to obtain a desired tuning layer thickness precisely, leading to a lower color purity and a lower light emitting efficiency. These shortcomings of the conventional OLED result in a complex manufacturing process and very high manufacturing costs.

[0043] The present disclosure provides a superior light emitting diode, a display substrate and a display device having the same, and a superior fabricating method for making the light emitting diode. In one aspect, the present disclosure provides a light emitting diode having multiple microcavity tuning layers, at least two of which differ from each other by the crystalline states of microcavity tuning materials used therein. For example, the light emitting diode may have one microcavity tuning layer made of a material including a substantially crystalline material, and another made of a material including a substantially amorphous material. As used herein, the term “crystalline material” refers to both a material in a polycrystalline state and a material in a single-crystalline state. Optionally, a crystalline material may include one or more molecules of another material. As used herein, the term “amorphous material” refers to both a material in a completely disordered non-crystalline state, and a fine crystal grain such as micro-crystal, nano-crystal, and a material having short range ordered structure and the like. Different crystalline states result in detectably different electrical characteristics, such as reactivity to various etchants and/or electrical conductivity. For example, an amorphous material may react to a wider range of etchants or weaker etchants, whereas a crystalline material may react to a smaller range of etchants or stronger etchants. Optionally, the amorphous material is an amorphous indium tin oxide and the crystalline material is a polycrystalline indium tin oxide. Optionally, the amorphous indium tin oxide may be etched by oxalic acid, hydrochloric acid, and nitric acid, and the polycrystalline indium tin oxide may be etched by nitric acid but not oxalic acid or hydrochloric acid. Optionally, the polycrystalline indium tin oxide may be etched by aqua regia, but not nitric acid, oxalic acid, or hydrochloric acid. Optionally, when a same material is used, a crystalline material has a higher electrical conductivity than an amorphous material. As used herein, the term “substantially” means and includes mostly, essentially, fully, or entirely. By way of example, the phrase “a substantially crystalline material” may refer to a

material with a portion in a crystalline state, the portion in the range of from about 90% (e.g., about 95%, about 99%) by volume up to and including about 100% by volume of the material, and a remaining portion (i.e., in the range of from about 10% (e.g., about 5%, about 1%) to about 0% by volume, respectively) in an amorphous state.

[0044] In some embodiments, the light emitting diode may have one microcavity tuning layer made of a material including a crystalline transparent conductive material, and another made of a material including an amorphous transparent conductive material. For example, the light emitting diode may include a plurality of sub-pixels in each pixel unit; a first microcavity tuning layer and a second microcavity tuning layer in each pixel unit. The first microcavity tuning layer is sandwiched by the first electrode layer (e.g., a reflective electrode layer) and the light emitting layer within the plurality of sub-pixels, and the second microcavity tuning layer sandwiched by the first microcavity tuning layer and the light emitting layer within at least one (e.g., one, two, or three) of the plurality of sub-pixels. Optionally, the first microcavity layer is made of material comprising a crystalline transparent conductive oxide and the second microcavity tuning layer is made of a material comprising an amorphous transparent conductive oxide. Optionally, the second microcavity layer is made of material comprising a crystalline transparent conductive oxide and the first microcavity tuning layer is made of a material comprising an amorphous transparent conductive oxide.

[0045] In some embodiments, the light emitting diode includes a first electrode layer, wherein the first electrode layer is a reflective electrode layer; a second electrode layer; a light emitting layer between the first electrode layer and the second electrode layer; a first microcavity tuning layer sandwiched by the first electrode layer and the light emitting layer within the plurality of sub-pixels; and a second microcavity tuning layer sandwiched by the first microcavity tuning layer and the light emitting layer within at least one of the plurality of sub-pixels, and the first microcavity tuning layer is sandwiched by the first electrode layer and the second microcavity tuning layer within the at least another of the three sub-pixels. The first microcavity tuning layer is made of a material including a transparent conductive material in a first state and the second microcavity tuning layer is made of a material including a transparent conductive material in a second state, the first state and the second state are different states selected from a crystalline state and an amorphous state. For example, the first microcavity layer may be made of material having a crystalline transparent conductive oxide and the second microcavity tuning layer may be made of a material having an amorphous transparent conductive oxide. Optionally, the second microcavity layer is

made of material comprising a crystalline transparent conductive oxide and the first microcavity tuning layer is made of a material comprising an amorphous transparent conductive oxide.

[0046] In another aspect, the present disclosure provides a method of fabricating a display substrate having an array of pixels, each pixel having three sub-pixels. In some embodiments, the fabricating method according to the present disclosure includes forming a first electrode layer (e.g., a reflective electrode layer); forming a microcavity tuning layer including a first microcavity tuning layer and a second microcavity tuning layer on the reflective electrode layer; forming a light emitting layer on a side of the microcavity tuning layer distal to the reflective electrode layer; and forming a second electrode layer on a side of the light emitting layer distal to the microcavity tuning layer. The first microcavity tuning layer is sandwiched by the reflective electrode layer and the light emitting layer within at least one of the three sub-pixels (e.g., all three sub-pixels). The second microcavity tuning layer is sandwiched by the first microcavity tuning layer and the light emitting layer within at least one of the three sub-pixels (e.g., a second sub-pixel and/or a third sub-pixel), and the first microcavity tuning layer is sandwiched by the reflective electrode layer and the second microcavity tuning layer within the at least one of the three sub-pixels. The first microcavity tuning layer is made of a material including a transparent conductive material in a first state and the second microcavity tuning layer is made of a material including a transparent conductive material in a second state, the first state and the second state are different states selected from a crystalline state and an amorphous state. For example, the first microcavity layer may be made of material having a crystalline transparent conductive oxide and the second microcavity tuning layer may be made of a material having an amorphous transparent conductive oxide. Accordingly, a first microcavity is formed between the reflective electrode layer and the second electrode layer within the at least one of the three sub-pixels (e.g., all three sub-pixels); and a second microcavity is formed between the reflective electrode layer and the second electrode layer within the at least one of the three sub-pixels (e.g., a second sub-pixel and/or a third sub-pixel); the second microcavity has a microcavity length larger than that of the first microcavity. The reflective electrode layer, the first microcavity tuning layer and the second microcavity tuning layer are formed in a single process (e.g., patterned using a single mask). Optionally, the reflective electrode layer comprises three sub-electrodes corresponding to three sub-pixels, respectively.

[0047] Various appropriate methods may be used for making an amorphous transparent conductive layer or a crystalline transparent conductive layer. The crystalline state of the

layer may be affected by various factors such as the temperature of the base substrate, the deposition rate of the material, the thickness of the layer, and the humidity level during the deposition process. Optionally, the amorphous transparent conductive layer and the crystalline transparent conductive layer may be made by adjusting the humidity level during the deposition process such as a sputtering process. When the humidity level is low, the crystalline transparent conductive layer may be formed. When the humidity level is increased during the sputtering process, the water molecule (e.g., the oxygen atom in the water molecule) occupies the crystal lattice of the transparent conductive material (e.g., indium tin oxide), introducing stress into the crystal lattice. Thus, by adjusting the humidity level during the sputtering process, the amorphous transparent conductive layer can be obtained. The crystalline state of the transparent conductive layer may result in different reactivity to different etchant, accordingly a particular transparent conductive layer may be selectively etched using an appropriate etchant. For example, when oxalic acid is used as the etchant, an amorphous transparent conductive material layer may be etched and removed, whereas a crystalline transparent conductive layer remains intact and is not etched.

[0048] In some embodiments, the reflective electrode layer and multiple microcavity tuning layers are formed in a single process (e.g., patterned using a single mask), greatly simplifies the fabricating process and lowers the manufacturing costs. In another aspect, the present disclosure provides a light emitting diode with multiple microcavity tuning layers of higher precision.

[0049] Optionally, the first microcavity layer and the second microcavity tuning layer are made of a same material. Optionally, the first microcavity layer and the second microcavity tuning layer are made of different materials. Optionally, the first microcavity layer and the second microcavity tuning layer are made of different forms of a same material, e.g., a crystalline form and an amorphous form of a same material such as a metal oxide. Optionally, the first microcavity layer and the second microcavity tuning layer are made of different forms of different materials, e.g., a crystalline form of one material (e.g., a first metal oxide) and an amorphous form of another material (e.g., a second metal oxide).

[0050] Optionally, the first microcavity tuning layer may have a single-layer structure or a stacked-layer structure including two or more sub-layers. Optionally, the second microcavity tuning layer may have a single-layer structure or a stacked-layer structure including two or more sub-layers.

[0051] FIG. 1 is a flow chart illustrating a method of fabricating a display substrate in some embodiments. Referring to FIG. 1, the method in the embodiment includes forming a reflective electrode material layer, a first microcavity tuning material layer, and a second microcavity tuning material layer sequentially on a pixel driving layer; patterning the reflective electrode material layer, the first microcavity tuning material layer, and the second microcavity tuning material layer in a single patterning process to form a reflective electrode layer and a microcavity tuning layer having at least two different thicknesses in different sub-pixels; and forming a light emitting layer and a second electrode layer. The microcavity tuning layer includes a first microcavity tuning layer. Optionally, the microcavity tuning layer includes a first microcavity tuning layer and a second microcavity tuning layer.

[0052] The present method enables a single patterning process for forming a reflective electrode layer and a microcavity tuning layer having at least two different thicknesses in different sub-pixel regions. The present method thus significantly simplifies the fabricating process and lowers the manufacturing costs, providing a light emitting diode with multiple microcavity tuning layers of higher precision.

[0053] In some embodiments, the method includes using a gray-tone mask plate or a half-tone mask plate to obtain a pattern, wherein the pattern includes a first section corresponding to the first microcavity, the second section corresponding to the second microcavity, and a third section corresponding to the remaining portion of the photoresist layer.

[0054] Optionally, the method includes one or a combination of the following steps: forming a reflective electrode material layer; forming a first microcavity tuning material layer on the reflective electrode layer; forming a second microcavity tuning material layer on a side of the first microcavity tuning layer distal to the reflective electrode material layer; forming a photoresist layer on a side of the second microcavity tuning material layer distal to the first microcavity tuning material layer; exposing the photoresist layer with a mask plate (e.g., a single mask plate); and developing the exposed photoresist layer to obtain a pattern. The pattern includes a first section corresponding to the first microcavity, the second section corresponding to the second microcavity, and a third section corresponding to the remaining portion of the photoresist layer.

[0055] Optionally, the step of exposing the photoresist layer with a mask plate includes exposing the photoresist layer with a gray-tone mask plate or a half-tone mask plate.

[0056] Optionally, the method further includes one or a combination of the following steps: removing the photoresist layer in the third section and partially removing the photoresist

layer in the first section; etching the second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section thereby forming the reflective electrode layer; removing the photoresist layer in the first section (e.g., by ashing the photoresist layer) thereby exposing the second microcavity tuning material layer in the first section; etching the second microcavity tuning material layer in the first section thereby exposing the first microcavity tuning material layer in the first section; and removing the photoresist layer in the second section.

[0057] Optionally, the step of etching the second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section includes sequentially etching the third section with a second microcavity tuning material etchant, a first microcavity tuning material etchant, and a reflective electrode material etchant.

[0058] Optionally, the step of etching the second microcavity tuning material layer in the first section includes etching the first section with a second microcavity tuning material etchant.

[0059] Optionally, a first sub-pixel contains the first microcavity, and a second sub-pixel and a third sub-pixel contain the second microcavity. Optionally, the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel.

[0060] Optionally, the reflective electrode layer is made of a material comprising an alloy having a reflectivity higher than 90%, e.g., higher than 92%, higher than 94%, higher than 96%, higher than 98%, or higher than 99%.

[0061] Optionally, the first microcavity layer is made of material including a crystalline transparent conductive oxide and the second microcavity tuning layer is made of a material including an amorphous transparent conductive oxide. Optionally, the crystalline transparent conductive oxide is a crystalline transparent conductive indium tin oxide. Optionally, the amorphous transparent conductive oxide is selected from one or a combination of an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide.

[0062] Optionally, the reflective electrode has a thickness in the range of about 50 nm to about 300 nm, e.g., about 50 nm to about 100 nm, about 100 nm to about 200 nm, or about 200 nm to about 300 nm.

[0063] Optionally, the first microcavity tuning layer has a thickness in the range of about 5 nm to about 15 nm, e.g., about 5 nm to about 10 nm, about 10 nm to about 15 nm, or about 7.5 nm to about 12.5 nm.

[0064] Optionally, the second microcavity tuning layer has a thickness in the range of about 50 nm to about 70 nm, e.g., about 50 nm to about 60 nm, about 60 nm to about 70 nm, about 55 nm to about 65 nm.

[0065] FIG. 2 is a flow chart illustrating a method of fabricating a display substrate in some embodiments. Referring to FIG. 2, the method in the embodiment includes forming a reflective electrode material layer, a first microcavity tuning material layer, and a second microcavity tuning material layer sequentially on a pixel driving layer; forming a photoresist layer on a side of the second microcavity tuning material layer distal to the first microcavity tuning material layer; exposing the photoresist layer with a single mask plate; developing the exposed photoresist layer to obtain a pattern comprising a first section corresponding to the first microcavity, the second section corresponding to the second microcavity, and a third section corresponding to the remaining portion of the photoresist layer; removing the photoresist layer in the third section and partially removing the photoresist layer in the first section; etching the second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section thereby forming the reflective electrode layer; ashing the photoresist layer to remove the photoresist in the first section thereby exposing the second microcavity tuning material layer in the first section; etching the second microcavity tuning material layer in the first section thereby exposing the first microcavity tuning material layer in the first section; removing the photoresist layer in the second section thereby forming a reflective electrode layer, a first microcavity tuning layer and a second microcavity tuning layer; and forming a light emitting layer and a second electrode layer sequentially on a side of the first microcavity tuning layer and the second microcavity tuning layer distal to the reflective electrode layer.

[0066] In some embodiments, the step of forming a reflective electrode material layer, a first microcavity tuning material layer, and a second microcavity tuning material layer sequentially on a pixel driving layer includes forming a reflective electrode material layer on a pixel driving layer. For example, the reflective electrode material may be deposited on the pixel driving layer by sputtering, vapor deposition, or coating. Optionally, the reflective electrode material layer has a thickness in the range of about 50 nm to about 300 nm, e.g., about 50 nm to about 100 nm, about 100 nm to about 200 nm, or about 200 nm to about 300 nm.

[0067] The pixel driving layer is formed on a base substrate (e.g., a glass substrate or a quartz substrate).

[0068] The reflective electrode layer is an oxidation-resistant layer having a high reflectivity and high work function. Optionally, the reflective electrode material layer is made of a material comprising an alloy having a reflectivity higher than 90%, e.g., higher than 92%, higher than 94%, higher than 96%, higher than 98%, or higher than 99%. Examples of appropriate alloys for making the reflective electrode layer include, but are not limited to, aluminum alloys, silver alloys, and molybdenum alloys. Optionally, the reflective electrode material layer is made of a material which can be specifically etched by a reflective electrode layer etchant (e.g., an aluminum etching solution), but not by other etchants such as those for etching microcavity tuning layers.

[0069] The OLED may be a conventional OLED or an inverted OLED. Optionally, the OLED is a conventional OLED, and the reflective electrode is an anode. Optionally, the OLED is an inverted OLED, and the reflective electrode is a cathode.

[0070] In some embodiments, the step of forming a reflective electrode material layer, a first microcavity tuning material layer, and a second microcavity tuning material layer sequentially on a pixel driving layer further includes forming a first microcavity tuning material layer on a side of the reflective electrode material layer distal to the pixel driving layer. For example, the first microcavity tuning material may be deposited on the reflective electrode material layer by sputtering, vapor deposition, or coating. Optionally, the first microcavity tuning material layer has a thickness in the range of about 5 nm to about 15 nm, e.g., about 5 nm to about 10 nm, about 10 nm to about 15 nm, or about 7.5 nm to about 12.5 nm.

[0071] Optionally, the first microcavity tuning material layer is a crystalline transparent conductive oxide layer, e.g., a crystalline transparent conductive indium tin oxide layer.

[0072] Optionally, the first microcavity tuning material layer is made of a material which can be specifically etched by a first microcavity tuning material layer etchant (e.g., a crystalline indium tin oxide etching solution such as a nitric acid-containing solution), but not by other etchants such as those for etching the reflective electrode material or the second microcavity tuning material.

[0073] In some embodiments, the step of forming a reflective electrode material layer, a first microcavity tuning material layer, and a second microcavity tuning material layer sequentially on a pixel driving layer further includes forming a second microcavity tuning

material layer on a side of the first microcavity tuning material layer distal to the reflective electrode material layer. For example, the second microcavity tuning material may be deposited on the first microcavity tuning material layer by sputtering, vapor deposition, or coating. Optionally, the second microcavity tuning material layer has a thickness in the range of about 50 nm to about 70 nm, e.g., about 50 nm to about 60 nm, about 60 nm to about 70 nm, about 55 nm to about 65 nm.

[0074] Optionally, the second microcavity tuning material layer is an amorphous transparent conductive oxide layer. Examples of suitable amorphous transparent conductive oxides include, but are not limited to, an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide. Optionally, the second microcavity tuning material layer has a light transmission rate higher than 85%, e.g., higher than 90%, higher than 95%, or higher than 98%.

[0075] Optionally, the second microcavity tuning material layer is made of a material which can be specifically etched by a second microcavity tuning material layer etchant (e.g., an amorphous indium tin oxide etching solution such as a solution containing oxalic acid and/or hydrochloric acid), but not by other etchants such as those for etching the reflective electrode material or the first microcavity tuning material.

[0076] To prevent oxidation of the reflective electrode material layer, the first microcavity tuning material layer, and the second microcavity tuning material layer, these layers may be formed and patterned in certain temperature ranges and atmosphere.

[0077] FIG. 3 is a diagram illustrating the structure of a display substrate in some embodiments having the reflective electrode material layer, the first microcavity tuning material layer, and the second microcavity tuning material layer.

[0078] FIG. 4 is a diagram illustrating the structure of a display substrate in some embodiments having the photoresist layer, the reflective electrode material layer, the first microcavity tuning material layer, and the second microcavity tuning material layer. The photoresist layer may be formed by various methods, such as by coating. An appropriate thickness of the photoresist layer suitable for subsequent patterning steps may be selected.

[0079] In some embodiments, the step of exposing the photoresist layer with a single mask plate includes exposing the photoresist layer with a gray-tone mask plate or a half-tone mask plate. Optionally, the gray-tone mask plate (or the half-tone mask plate) includes a transmissive section, a semi-light-shielding section, and a light-shielding section. When a

positive photoresist is used, the light-shielding section corresponds to the second section corresponding to the second microcavity (e.g., sub-pixel(s) in which the second microcavity tuning layer is sandwiched by the first microcavity tuning layer and the light emitting layer), the semi-light-shielding section corresponds to the first section corresponding to the first microcavity (e.g., sub-pixel(s) in which the first microcavity tuning layer is sandwiched by the reflective electrode layer and the light emitting layer), and the transmissive section corresponds to the third section corresponding to the remaining portion of the photoresist layer. When a negative photoresist is used, the transmissive section corresponds to the second section corresponding to the second microcavity (e.g., sub-pixel(s) in which the second microcavity tuning layer is sandwiched by the first microcavity tuning layer and the light emitting layer), the semi-light-shielding section corresponds to the first section corresponding to the first microcavity (e.g., sub-pixel(s) in which the first microcavity tuning layer is sandwiched by the reflective electrode layer and the light emitting layer), and the light-shielding section corresponds to the third section corresponding to the remaining portion of the photoresist layer.

[0080] The exposed photoresist layer is then developed. The photoresist layer in the third section is completely removed. The photoresist layer in the first section is partially removed (e.g., resulting in a reduced thickness of the photoresist layer). The photoresist layer in the second section is substantially not removed. The structure of the display substrate after this step is shown in FIG. 5.

[0081] As discussed above, subsequently the photoresist layer is sequentially etched by a second microcavity tuning material etchant, a first microcavity tuning material etchant, and a reflective electrode material etchant. The photoresist is completely removed in the third section. The second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section are not protected by the photoresist layer, and are dissolved by the etchants in the third section. The reflective electrode material layer is patterned to form a reflective electrode layer. The structure of the display substrate after this step is shown in FIG. 6.

[0082] In some embodiments, the display substrate is then subject to ashing. The photoresist layer in the first section is partially removed and has a reduced thickness, whereas the photoresist layer in the second section is substantially not removed. During the ashing, the photoresist layer in the first section is removed, exposing the second microcavity tuning material layer in the first section. The photoresist layer in the second section, having a larger thickness, is only partially removed during etched. Thus, the photoresist layer in the second

section is still protected by the photoresist layer after the ashing step. The structure of the display substrate after this step is shown in FIG. 7.

[0083] The display substrate is then subject to a second etching process using an etchant specific for etching the second microcavity tuning material. The exposed second microcavity tuning material layer in the first section is removed by the second etching process. Because the etchant in the step is specific for etching the second microcavity tuning material but not the first microcavity tuning material or the reflective electrode layer, the first microcavity tuning material layer underneath the second microcavity tuning material layer in the first section remains substantially intact. The reflective electrode material layer in the third section and the first microcavity tuning material layer in the second section remain substantially intact.

[0084] After the second etching process, the photoresist layer in the second section is removed. As shown in FIG. 8, the display substrate contains a reflective electrode layer, a first microcavity tuning layer and a second microcavity tuning layer. In the second section, the display substrate has a microcavity tuning layer including a first microcavity tuning layer and a second microcavity tuning layer. In the first section, the display substrate has a microcavity tuning layer including a first microcavity tuning layer but not a second microcavity tuning layer. The first section corresponds to the first microcavity. The second section corresponds to the second microcavity. The second microcavity has a microcavity length larger than that of the first microcavity. The display substrate in the embodiment includes a microcavity tuning layer having different microcavity lengths in different sub-pixels, and different microcavity tuning layer thicknesses in different sub-pixels.

[0085] The light emitting layer and the second electrode layer may be formed by various methods such as vapor deposition.

[0086] In some embodiments, the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel. Optionally, the first sub-pixel has a first microcavity, and the second sub-pixel and the third sub-pixel have a second microcavity.

[0087] The present method enables a single patterning process for forming a reflective electrode layer and a microcavity tuning layer having at least two different thicknesses in different sub-pixel regions. The present method thus significantly simplifies the fabricating process and lowers the manufacturing costs, providing a light emitting diode with multiple microcavity tuning layers of higher precision.

[0088] In some embodiments, the fabricating method further includes forming a gate electrode layer on the base substrate. In some embodiments, the step of forming the gate electrode layer includes cleansing the base substrate; depositing a gate electrode material layer on the base substrate (e.g., by sputtering or vapor deposition); and patterning the gate electrode material layer thereby forming a gate electrode layer (e.g., by lithography such as a wet etching process). Examples of gate electrode materials include, but are not limited to, aluminum, chromium, tungsten, titanium, tantalum, molybdenum, copper, and alloys containing the same. Optionally, the gate electrode layer may have a single-layer structure or a stacked-layer structure including two or more sub-layers. Optionally, the gate electrode layer has a thickness in the range of about 200 nm to about 1000 nm.

[0089] In some embodiments, the fabricating method further includes forming a gate insulating layer on the base substrate (e.g., on a side of the gate electrode layer distal to the base substrate). For example, a gate insulating material may be deposited on the base substrate by a plasma-enhanced chemical vapor deposition (PECVD) process. Examples of gate insulating materials include, but are not limited to, silicon oxide, silicon nitride (e.g., Si_3N_4), silicon oxynitride (SiO_xN_y). Optionally, the gate insulating layer may have a single-layer structure or a stacked-layer structure including two or more sub-layers. Optionally, the gate insulating layer has a thickness in the range of about 5 nm to about 300 nm.

[0090] In some embodiments, the fabricating method further includes forming an active layer on the base substrate (e.g., on a side of the gate insulating layer distal to the gate electrode layer). For example, an oxide active layer material may be deposited on the base substrate by, e.g., vapor deposition. Optionally, the step of forming the active layer includes depositing an active layer material layer on the base substrate (e.g., by vapor deposition); and patterning the active layer material layer thereby forming an active layer (e.g., by lithography such as a wet etching process). Examples of active layer materials include, but are not limited to, metal oxide semi-conductive materials such as indium gallium zinc oxide, zinc oxide, zinc oxynitride, and indium tin zinc oxide. Optionally, the gate insulating layer has a thickness in the range of about 5 nm to about 250 nm.

[0091] In some embodiments, the fabricating method further includes forming an etching stop layer on the base substrate (e.g., on a side of the active layer distal to the gate insulating layer). Optionally, the step of forming the etching stop layer includes depositing an etching stop layer material layer on the base substrate (e.g., by vapor deposition); and patterning the etching stop layer material layer thereby forming an etching stop layer (e.g., by lithography

such as a dry etching process). For example, the etching stop layer material may be deposited on the base substrate by a PECVD process.

[0092] In some embodiments, the fabricating method further includes forming a source electrode and a drain electrode on the base substrate (e.g., on a side of the etching stop layer distal to the active layer). Optionally, the step of forming the source/drain electrode includes depositing a source/drain electrode material on the base substrate (e.g., by sputtering); and patterning the source/drain electrode material layer thereby forming the source/drain electrode (e.g., by an etching process).

[0093] In some embodiments, the fabricating method further includes forming a passivation layer on the base substrate (e.g., on a side of the source/drain electrode distal to the base substrate). Optionally, the step of forming the passivation layer includes depositing a passivation material layer on the base substrate (e.g., by PECVD); and patterning the passivation material layer thereby forming a passivation layer (e.g., by etching).

[0094] In some embodiments, the fabricating method further includes forming a pixel driving layer on the base substrate (e.g., on a side of the reflective electrode layer proximal to the base substrate). Optionally, the step of forming the pixel driving layer includes patterning a pixel driving material layer thereby forming a pixel driving layer.

[0095] Various alternative embodiments may be practiced. Optionally, the thin film transistor is a bottom-gate type thin film transistor. Optionally, the thin film transistor is a top-gate type thin film transistor. Optionally, the active layer is made of a metal oxide material. Optionally, the active layer is made of a polycrystalline silicon or an amorphous silicon material. Optionally, the method includes forming an etching stop layer. Optionally, the method does not involve forming an etching stop layer. Optionally, the pixel driving layer includes an array of thin film transistors, and/or a passivation layer. Optionally, the pixel driving layer further includes a planarization layer and a water/oxygen barrier layer, etc.

[0096] In some embodiments, the fabricating method further includes forming an anode on the base substrate (e.g., on a side of the pixel driving layer distal to the base substrate). For example, an anode material layer may be sputtered on the base substrate, and the anode material layer may be patterned to form the anode.

[0097] In some embodiments, the fabricating method further includes forming a pixel definition layer on the base substrate (e.g., on a side of the anode distal to the base substrate). For example, a pixel definition material layer having a thickness in the range of about 1 μm

to about 4 μm is deposited on the base substrate, followed by patterning the pixel definition material layer to form the pixel definition layer.

[0098] In some embodiments, the fabricating method further includes forming a light emitting layer on the base substrate (e.g., on a side of the pixel definition layer distal to the base substrate). Optionally, the step of forming the light emitting layer includes depositing organic light emitting materials on the base substrate (e.g., by vapor deposition in vacuum and heat). Optionally, the step includes sequentially depositing an electron transport layer (e.g., at 190 °C), an emissive layer, and a hole transport layer (e.g., at 170 °C) in vacuum (e.g., 1×10^{-5} Pa). Optionally, the hole transport layer is a N,N'-Bis-(1-naphthalenyl)-N,N'-bis-phenyl-(1,1'-biphenyl)-4,4'-diamine (NPB) layer having a thickness of about 50 nm. Optionally, the electron transport layer is a 4,7-diphenyl-1,10-phenanthroline (Bphen) layer having a thickness of about 25 nm. Optionally, the light emitting layer includes a host material doped with a phosphor. Optionally, the light emitting layer in the green sub-pixel includes a CBP:(ppy)₂Ir(acac) layer of about 25 nm thickness. Optionally, the light emitting layer in the blue sub-pixel includes a CBP:FIrpic layer of about 25 nm thickness. Optionally, the light emitting layer in the red sub-pixel includes a CBP:Btp₂Ir(acac) layer of about 25 nm thickness. CBP stands for 4,4'-Bis(N-carbazolyl)-1,1'-biphenyl or derivatives thereof; (ppy)₂Ir(acac) stands for Bis[2-(2-pyridinyl-N)phenyl-C](2,4-pentanedionato-O²,O⁴)iridium(III) or derivatives thereof; FIrpic stands for Bis[2-(4,6-difluorophenyl)pyridinato-C²,N](picolinato)iridium(III) or derivatives thereof; and Btp₂Ir(acac) stands for bis(2-(2'-benzo[4,5-a]thienyl)pyridinato-N,C^{3'}) iridium (acetylacetonate) or derivatives thereof. Optionally, the step of forming the light emitting layer further includes one or more of the forming steps: forming a hole injection layer, forming a hole transport layer, forming an electron transport layer, and forming an electron injection layer.

[0099] In some embodiments, the fabricating method further includes forming a cathode layer. Examples of cathode materials include, but are not limited to, indium zinc oxide and aluminum zinc oxide. Optionally, the cathode layer is a transparent electrode layer. Optionally, the cathode layer is a transfective electrode layer. Optionally, the cathode layer has a thickness in the range of about 50 nm to about 200 nm.

[0100] In some embodiments, the display substrate further includes a color filter. Optionally, the display substrate includes a package substrate having a color filter. In some embodiments, the display substrate does not include a color filter.

[0101] In another aspect, the present disclosure provides a method of fabricating a package substrate having a color filter. Optionally, the method includes forming a black matrix layer on a package substrate; forming a color filter layer on the package substrate; and forming a post spacer layer on the substrate. Optionally, an organic black material having a thickness of about 1 μm is coated on the package substrate, the organic black material layer is then patterned to form the black matrix layer. Optionally, a red color filter film, a green color filter film, and a blue color filter film (each having a thickness in the range of about 1 μm to about 3 μm) are coated on the package substrate, and are patterned to form the color filter layer. The post spacer layer prevents damages caused by particles during assembly of the display substrate and the package substrate. Optionally, a post spacer material layer having a thickness in the range of about 3 μm to about 5 μm is coated on the package substrate, and is patterned to form the post spacer layer. The post spacer layer is formed in regions of the package substrate corresponding to the black matrix layer.

[0102] The display substrate and the package substrate are assembled together to form a display panel. Optionally, a transparent cover plate is attached to the assembled display panel. Optionally, the transparent cover plate is made of a material containing a glass (e.g., a glass made by Corning Inc. or Asahi Glass Co.), or other suitable quartz glass. Optionally, the transparent cover plate has a thickness in the range of about 50 μm to about 1000 μm .

[0103] In another aspect, the present disclosure provides a superior light emitting diode. In some embodiments, the light emitting diode includes a reflective electrode layer; a light emitting layer; a first microcavity tuning layer sandwiched by the first electrode layer and the light emitting layer within at least one of the three sub-pixels (e.g., all three sub-pixels); and a second microcavity tuning layer sandwiched by the first microcavity tuning layer and the light emitting layer within at least one of the three sub-pixels, and the first microcavity tuning layer is sandwiched by the first electrode layer and the second microcavity tuning layer within the at least one of the three sub-pixels. The first microcavity tuning layer is made of a material including a transparent conductive material in a first state and the second microcavity tuning layer is made of a material including a transparent conductive material in a second state, the first state and the second state are different states selected from a crystalline state and an amorphous state. For example, the first microcavity layer may be made of material having a crystalline transparent conductive oxide and the second microcavity tuning layer may be made of a material having an amorphous transparent conductive oxide. A first microcavity is formed between the first electrode layer and the second electrode layer within the at least one of the three sub-pixels (e.g., all three sub-pixels).

A second microcavity is formed between the first electrode layer and the second electrode layer within the at least one of the three sub-pixels; the second microcavity has a microcavity length larger than that of the first microcavity.

[0104] Optionally, a first sub-pixel has the first microcavity, and a second sub-pixel and a third sub-pixel have the second microcavity. For example, the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel.

[0105] Optionally, the reflective electrode material layer is made of a material comprising an alloy having a reflectivity higher than 90%, e.g., higher than 92%, higher than 94%, higher than 96%, higher than 98%, or higher than 99%. Examples of appropriate alloys for making the reflective electrode layer include, but are not limited to, aluminum alloys, silver alloys, and molybdenum alloys. Optionally, the reflective electrode material layer is made of a material which can be specifically etched by a reflective electrode layer etchant (e.g., an aluminum etching solution), but not by other etchants such as those for etching microcavity tuning layers.

[0106] Optionally, the reflective electrode has a thickness in the range of about 50 nm to about 300 nm, e.g., about 50 nm to about 100 nm, about 100 nm to about 200 nm, or about 200 nm to about 300 nm. Optionally, the first microcavity tuning layer has a thickness in the range of about 5 nm to about 15 nm, e.g., about 5 nm to about 10 nm, about 10 nm to about 15 nm, or about 7.5 nm to about 12.5 nm. Optionally, the second microcavity tuning layer has a thickness in the range of about 50 nm to about 70 nm, e.g., about 50 nm to about 60 nm, about 60 nm to about 70 nm, about 55 nm to about 65 nm. Optionally, the second microcavity tuning layer has a light transmission rate higher than 85%, e.g., higher than 90%, higher than 95%, or higher than 98%.

[0107] Optionally, the first microcavity tuning layer is a crystalline transparent conductive oxide layer, e.g., a crystalline transparent conductive indium tin oxide layer. Optionally, the second microcavity tuning material layer is an amorphous transparent conductive oxide layer. Examples of suitable amorphous transparent conductive oxides include, but are not limited to, an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide.

[0108] In another aspect, the present disclosure provides a display substrate having a light emitting diode described herein or manufactured by a method described herein. In another aspect, the present disclosure provides a display device having a display substrate described

herein. Examples of appropriate display devices include, but are not limited to, a smartphone, a tablet computer, a smart TV, etc.

[0109] FIG. 8 is a diagram illustrating the structure of a display substrate having a reflective electrode layer, a first microcavity tuning layer and a second microcavity tuning layer in some embodiments. Referring to FIG. 8, the display substrate in the embodiment includes a base substrate, a pixel driving layer on the base substrate, a reflective electrode layer on a side of the pixel driving layer distal to the base substrate, and a microcavity tuning layer on a side of the reflective electrode layer distal to the base substrate. The microcavity tuning layer in the embodiment has different thicknesses in different sub-pixels of the display substrate, e.g., it includes a first microcavity tuning layer and a second microcavity tuning layer. In some sub-pixel(s), the microcavity tuning layer only contains a first microcavity tuning layer. In other sub-pixel(s), the microcavity tuning layer contains both a first microcavity tuning layer and a second microcavity tuning layer. The display substrate in the embodiment further includes a light emitting layer and a second electrode.

[0110] The base substrate may be a glass substrate or a quartz substrate. The reflective electrode layer is an oxidation-resistant layer having a high reflectivity and high work function. Optionally, the reflective electrode material layer is made of a material comprising an alloy having a reflectivity higher than 90%, e.g., higher than 92%, higher than 94%, higher than 96%, higher than 98%, or higher than 99%. Examples of appropriate alloys for making the reflective electrode layer include, but are not limited to, aluminum alloys, silver alloys, and molybdenum alloys. Optionally, the first microcavity tuning layer is a crystalline transparent conductive oxide layer, e.g., a crystalline transparent conductive indium tin oxide layer. Optionally, the second microcavity tuning material layer is an amorphous transparent conductive oxide layer. Examples of suitable amorphous transparent conductive oxides include, but are not limited to, an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide. Optionally, the first microcavity tuning layer has a thickness in the range of about 5 nm to about 15 nm. Optionally, the second microcavity tuning layer has a thickness in the range of about 50 nm to about 70 nm.

[0111] A first microcavity is formed between the first electrode layer and the second electrode layer within the at least one of the three sub-pixels (e.g., all three sub-pixels). A second microcavity is formed between the first electrode layer and the second electrode layer within the at least one of the three sub-pixels (e.g., sub-pixels having both a first microcavity

tuning layer and a second microcavity tuning layer). The second microcavity has a microcavity length larger than that of the first microcavity.

[0112] Optionally, a first sub-pixel has the first microcavity, and a second sub-pixel and a third sub-pixel have the second microcavity. For example, the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel.

[0113] The present display substrate includes a microcavity tuning layer having different thicknesses in different sub-pixels of the display substrate, e.g., a first microcavity tuning layer and a second microcavity tuning layer, resulting in different microcavities having different microcavity lengths. Different microcavities correspond to different sub-pixels, tailored for generating resonant light of different colors. The present display substrate provides superior light emission efficiency and color purity.

[0114] The foregoing description of the embodiments of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments are chosen and described in order to best explain the principles of the invention and its best mode practical application, thereby to enable persons skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents in which all terms are meant in their broadest reasonable sense unless otherwise indicated. Therefore, the term “the invention”, “the present invention” or the like does not necessarily limit the claim scope to a specific embodiment, and the reference to exemplary embodiments of the invention does not imply a limitation on the invention, and no such limitation is to be inferred. The invention is limited only by the spirit and scope of the appended claims. Moreover, these claims may refer to use “first”, “second”, etc. following with noun or element. Such terms should be understood as a nomenclature and should not be construed as giving the limitation on the number of the elements modified by such nomenclature unless specific number has been given. Any advantages and benefits described may not apply to all embodiments of the invention. It should be appreciated that variations may be made in the embodiments described by persons skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element and component in the

present disclosure is intended to be dedicated to the public regardless of whether the element or component is explicitly recited in the following claims.

WHAT IS CLAIMED IS:

1. A light emitting diode comprising a plurality of sub-pixels, comprising:
a first electrode layer, wherein the first electrode layer is a reflective electrode layer;
a second electrode layer;
a light emitting layer between the first electrode layer and the second electrode layer;
a first microcavity tuning layer sandwiched by the first electrode layer and the light emitting layer within the plurality of sub-pixels; and
a second microcavity tuning layer sandwiched by the first microcavity tuning layer and the light emitting layer within at least one of the plurality of sub-pixels, and the first microcavity tuning layer is sandwiched by the first electrode layer and the second microcavity tuning layer within the at least one of the plurality of sub-pixels;
wherein the first microcavity tuning layer is made of a material comprising a transparent conductive material in a first state and the second microcavity tuning layer is made of a material comprising a transparent conductive material in a second state, the first state and the second state are different states selected from a crystalline state and an amorphous state.
2. The light emitting diode of claim 1, wherein the first microcavity layer is made of a material comprising a crystalline transparent conductive oxide and the second microcavity tuning layer is made of a material comprising an amorphous transparent conductive oxide.
3. The light emitting diode of claim 1, wherein the crystalline transparent conductive oxide is a crystalline transparent conductive indium tin oxide.
4. The light emitting diode of claim 1, wherein the amorphous transparent conductive oxide is selected from one or a combination of an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide.
5. The light emitting diode of claim 1, wherein the first electrode layer has a thickness in the range of about 50 nm to about 300 nm.

6. The light emitting diode of claim 1, wherein the first microcavity tuning layer has a thickness in the range of about 5 nm to about 15 nm.
7. The light emitting diode of claim 1, wherein the second microcavity tuning layer has a thickness in the range of about 50 nm to about 70 nm.
8. The light emitting diode of claim 1, wherein the first electrode layer is made of a material comprising an alloy having a reflectivity higher than 90%.
9. The light emitting diode of claim 1, wherein a first sub-pixel has the first microcavity, and a second sub-pixel and a third sub-pixel have the second microcavity.
10. The light emitting diode of claim 9, wherein the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel.
11. A display substrate comprising the light emitting diode of any one of claims 1-10.
12. A display device comprising the array substrate of claim 11.
13. A method of fabricating a display substrate comprising an array of pixels, each pixel comprising at least three sub-pixels, the method comprising:
 - forming a first electrode layer, wherein the first electrode layer is a reflective electrode layer;
 - forming a microcavity tuning layer comprising a first microcavity tuning layer and a second microcavity tuning layer on the first electrode layer;
 - forming a light emitting layer on a side of the microcavity tuning layer distal to the first electrode layer; and
 - forming a second electrode layer on a side of the light emitting layer distal to the microcavity tuning layer;wherein the first microcavity tuning layer is sandwiched by the first electrode layer and the light emitting layer within three sub-pixels;
 - the second microcavity tuning layer is sandwiched by the first microcavity tuning layer and the light emitting layer within at least one of three sub-pixels, and the first microcavity tuning layer is sandwiched by the first electrode layer and the second microcavity tuning layer within the at least one of three sub-pixels; and

the first microcavity tuning layer is made of a material comprising a transparent conductive material in a first state and the second microcavity tuning layer is made of a material comprising a transparent conductive material in a second state, the first state and the second state are different states selected from a crystalline state and an amorphous state.

14. The method of claim 13, wherein the first microcavity layer is made of a material comprising a crystalline transparent conductive oxide and the second microcavity tuning layer is made of a material comprising an amorphous transparent conductive oxide.

15. The method of claim 13, wherein the crystalline transparent conductive oxide is a crystalline transparent conductive indium tin oxide.

16. The method of claim 13, wherein the amorphous transparent conductive oxide is selected from one or a combination of an amorphous transparent conductive indium tin oxide, an amorphous transparent conductive indium tin zinc oxide, an amorphous transparent conductive indium zinc oxide, and an amorphous transparent conductive aluminum zinc oxide.

17. The method of claim 13, wherein the first electrode layer, the first microcavity tuning layer and the second microcavity tuning layer are patterned using a single mask.

18. The method of claim 13, wherein the single mask is a gray-tone mask plate or a half-tone mask plate, and the step of forming a microcavity tuning layer comprises using a gray-tone mask plate or a half-tone mask plate to obtain a pattern, wherein the pattern comprises a first section corresponding to the first microcavity, the second section corresponding to the second microcavity, and a third section corresponding to the remaining portion of the photoresist layer.

19. The method of claim 13, wherein the step of forming a microcavity tuning layer comprising:

forming a reflective electrode material layer;

forming a first microcavity tuning material layer on the reflective electrode material layer;

forming a second microcavity tuning material layer on a side of the first microcavity tuning layer distal to the reflective electrode material layer;

forming a photoresist layer on a side of the second microcavity tuning material layer distal to the first microcavity tuning material layer;

exposing the photoresist layer with a gray-tone mask plate or a half-tone mask plate;

developing the exposed photoresist layer to obtain a pattern, wherein the pattern comprises a first section corresponding to the first microcavity, the second section corresponding to the second microcavity, and a third section corresponding to the remaining portion of the photoresist layer;

removing the photoresist layer in the third section and partially removing the photoresist layer in the first section;

etching the second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section thereby forming the first electrode layer;

removing the photoresist layer in the first section thereby exposing the second microcavity tuning material layer in the first section;

etching the second microcavity tuning material layer in the first section thereby exposing the first microcavity tuning material layer in the first section; and

removing the photoresist layer in the second section.

20. The method of claim 19, wherein the step of etching the second microcavity tuning material layer, the first microcavity tuning material layer, and the reflective electrode material layer in the third section comprises sequentially etching the third section with a second microcavity tuning material etchant, a first microcavity tuning material etchant, and a reflective electrode material etchant.

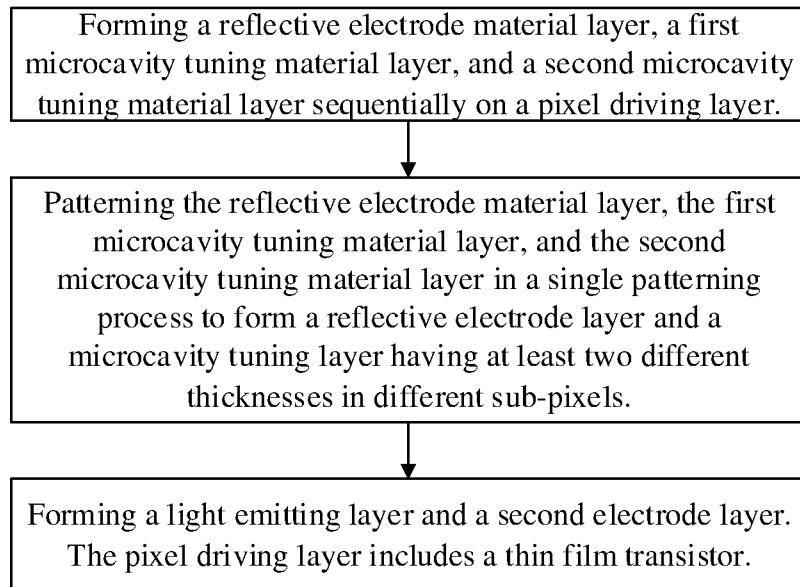
21. The method of claim 19, wherein the step of etching the second microcavity tuning material layer in the first section comprises etching the first section with a second microcavity tuning material etchant.

22. The method of claim 13, wherein a first sub-pixel has the first microcavity, and a second sub-pixel and a third sub-pixel have the second microcavity.

23. The method of claim 22, wherein the first sub-pixel is a green sub-pixel, the second sub-pixel is a red sub-pixel, and the third sub-pixel is a blue sub-pixel.

24. The method of claim 13, wherein the first electrode layer is made of a material comprising an alloy having a reflectivity higher than 90%.

25. The method of claim 13, wherein the first electrode layer has a thickness in the range of about 50 nm to about 300 nm.
26. The method of claim 13, wherein the first microcavity tuning layer has a thickness in the range of about 5 nm to about 15 nm.
27. The method of claim 13, wherein the second microcavity tuning layer has a thickness in the range of about 50 nm to about 70 nm.

**FIG. 1**

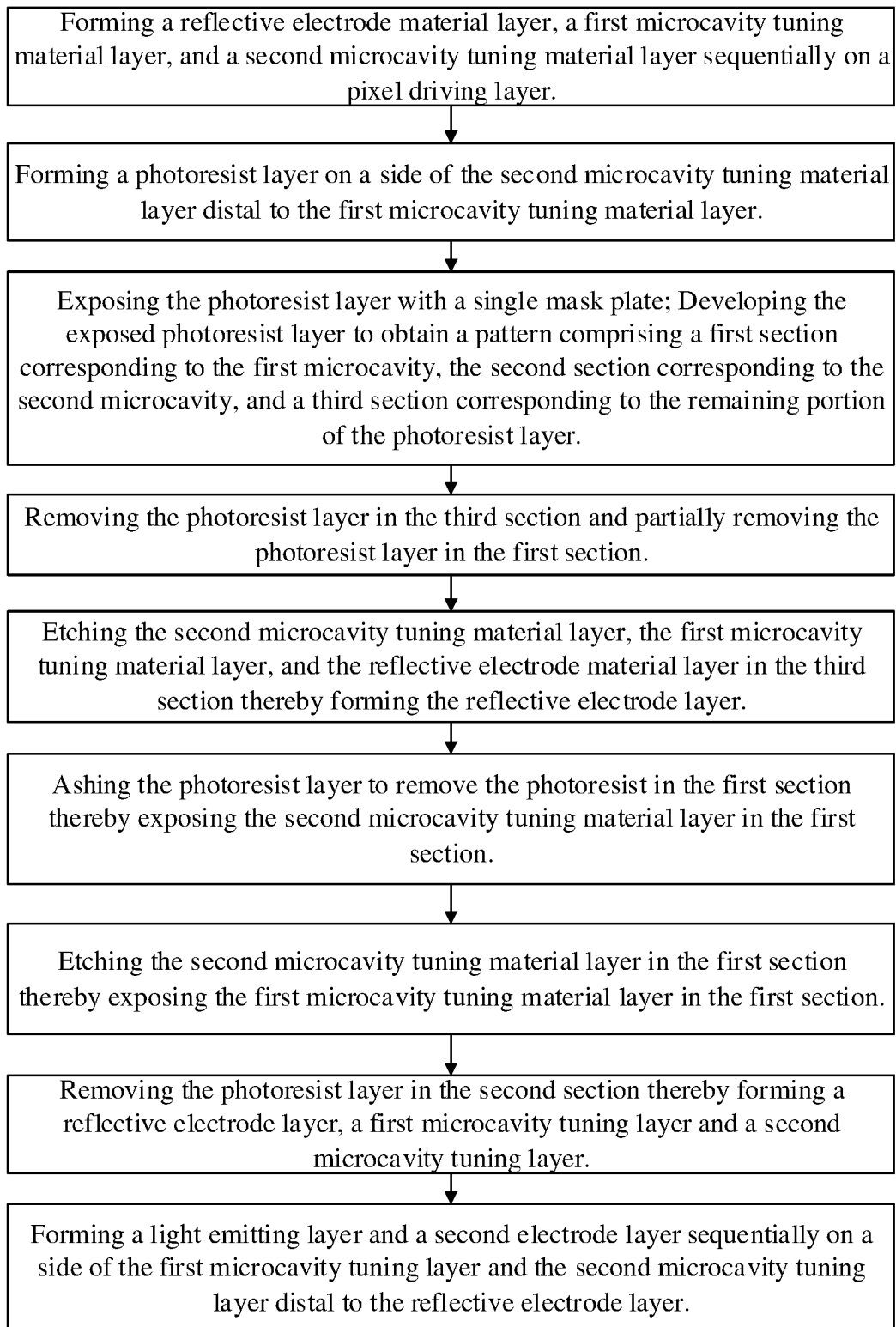


FIG. 2

Second microcavity tuning material layer
First microcavity tuning material layer
Reflective electrode material layer
Pixel driving layer

FIG. 3

Photoresist layer
Second microcavity tuning material layer
First microcavity tuning material layer
Reflective electrode material layer
Pixel driving layer

FIG. 4

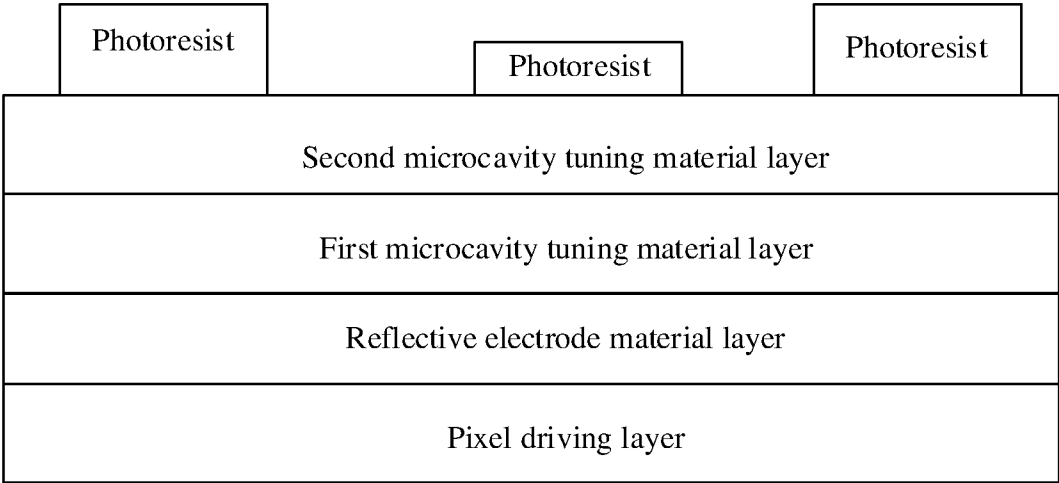


FIG. 5

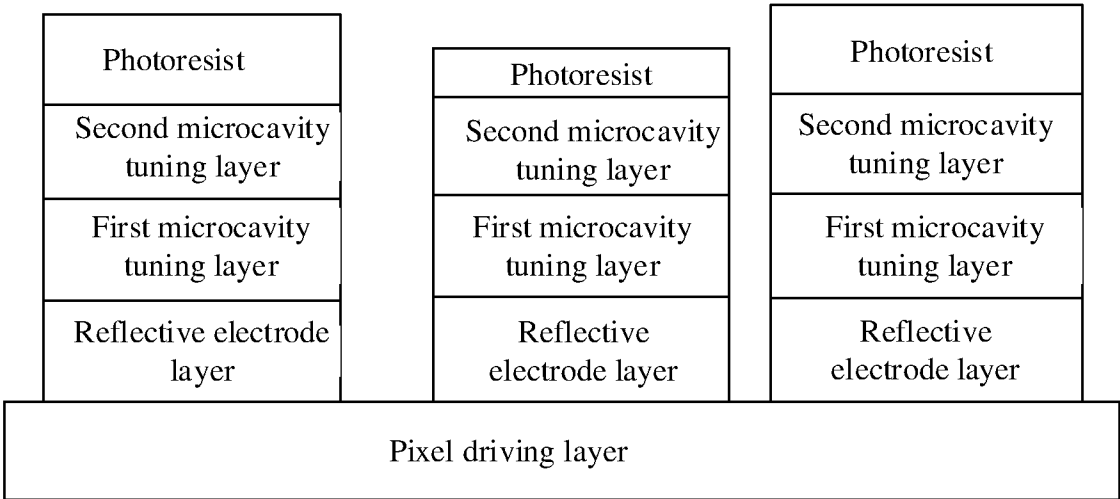


FIG. 6

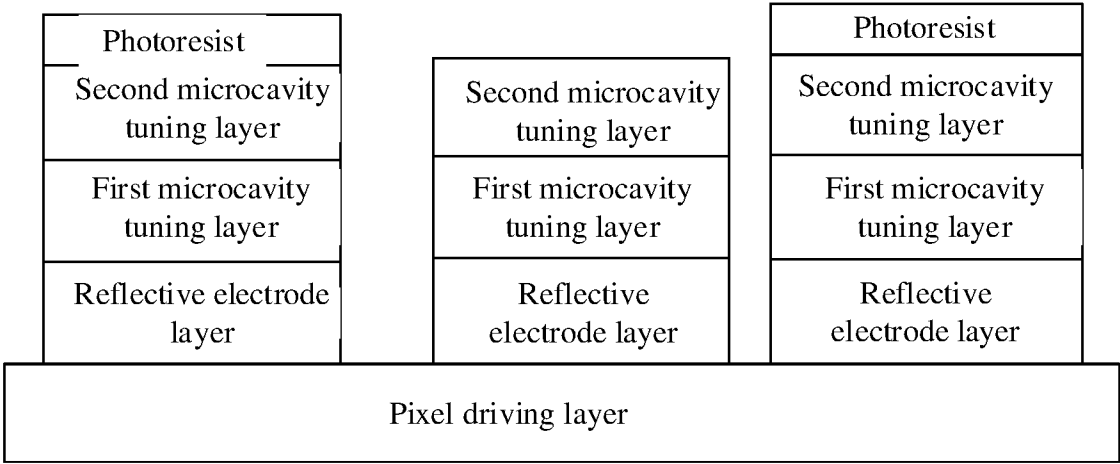


FIG. 7

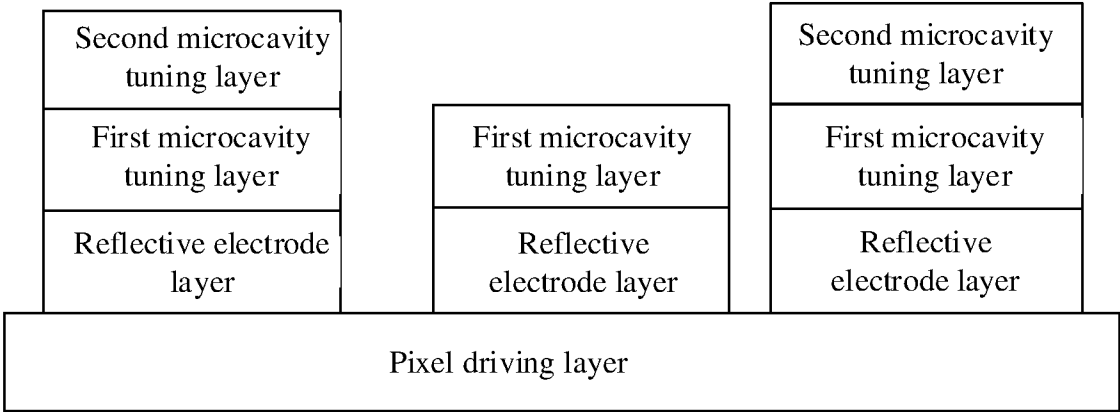


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2016/078554

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/12(2006.01)i; H01L 21/77(2006.01)i; H01L 27/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H0L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, CNKI, DWPI, SIPOABS: OLED, EL, LED, light, emit+, organic, display, resonate, resonator, ITO, polycrystalline, amorphous, cavity, tuning

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104966723 A (BOE TECHNOLOGY GROUP CO LTD) 07 October 2015 (2015-10-07) claims 1-23, description, paragraphs [0066]-[0183] and figures 1-8	1-27
X	CN 1638547 A (SANYO ELECTRIC CO LTD) 13 July 2005 (2005-07-13) description, page 2, line 20-page 21, line 3 and figures 1-8	1-27
A	US 5554911 A (HITACHI LTD) 10 September 1996 (1996-09-10) the whole document	1-27

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

09 May 2016

Date of mailing of the international search report

30 May 2016

Name and mailing address of the ISA/CN

STATE INTELLECTUAL PROPERTY OFFICE OF THE
P.R.CHINA
6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing
100088, China

Facsimile No. (86-10)62019451

Authorized officer

LI, Ying

Telephone No. (86-10)62089296

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2016/078554

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	104966723	A	07 October 2015	None			
CN	1638547	A	13 July 2005	CN	100454570	C	21 January 2009
				US	2005142976	A1	30 June 2005
				TW	200522792	A	01 July 2005
				KR	20050067055	A	30 June 2005
				JP	4439260	B2	24 March 2010
				JP	2005197010	A	21 July 2005
				US	7510455	B2	31 March 2009
US	5554911	A	10 September 1996	EP	0616488	A3	30 November 1994
				EP	0616488	A2	21 September 1994
				DE	69410513	T2	04 March 1999
				JP	H06275381	A	30 September 1994
				EP	0616488	B1	27 May 1998
				DE	69410513	D1	02 July 1998
				JP	2797883	B2	17 September 1998

专利名称(译)	发光二极管，显示基板和具有该发光二极管的显示装置及其制造方法		
公开(公告)号	EP3329513A4	公开(公告)日	2019-03-13
申请号	EP2016775446	申请日	2016-04-06
[标]申请(专利权)人(译)	京东方科技集团股份有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司.		
当前申请(专利权)人(译)	京东方科技集团有限公司		
[标]发明人	FANG JINGANG LIU XIAODI WANG DONGFANG HSIN LUNGPAO		
发明人	FANG, JINGANG LIU, XIAODI WANG, DONGFANG HSIN, LUNGPAO		
IPC分类号	H01L27/12 H01L21/77 H01L27/32		
CPC分类号	H01L51/5265 H01L27/3211 H01L27/3244 H01L51/5215 H01L51/5218 H01L51/56 H01L2227/323 H01L2251/305 H01L2251/308 H01L2251/558		
代理机构(译)	COHAUSZ & FLORACK		
优先权	201510446925.3 2015-07-27 CN		
其他公开文献	EP3329513A1		
外部链接	Espacenet		

摘要(译)

本申请公开了一种发光二极管，包括多个子像素，所述子像素包括第一电极层，其中所述第一电极层是反射电极层;第二电极层;第一电极层和第二电极层之间的发光层;第一微腔调谐层，夹在多个子像素内的第一电极层和发光层之间;第一微腔调谐层和发光层夹在多个子像素中的至少一个子像素内的第二微腔调谐层，第一微腔调谐层被第一电极层和第二微腔调谐层夹在内多个子像素中的至少一个。第一微腔调谐层由包括处于第一状态的透明导电材料材料制成，第二微腔调谐层由包括处于第二状态的透明导电材料材料制成，第一状态和第二状态是不同的状态。选自结晶态和非晶态。