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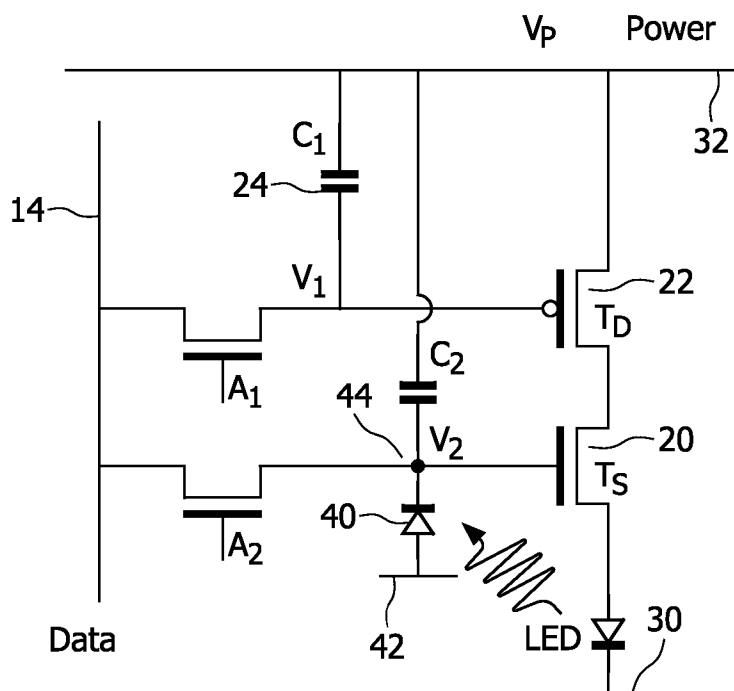
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(54) Title: EMISSIVE DISPLAY DEVICES



(57) Abstract: An active matrix display device comprises an array of display pixels, each pixel comprising a current-driven light emitting display element, a drive transistor for driving a current through the display element, a switching transistor in series with the drive transistor and an optical feedback arrangement for controlling the gate voltage of the switching transistor, thereby to enable control of the timing of switching off the switching transistor to isolate the display element from the drive transistor in dependence on the light output of the display element. This arrangement uses an optical feedback arrangement for the control of an additional switching transistor instead of controlling the drive transistor. The control of the drive transistor is therefore simplified, and the additional light-dependent control is for the additional switching transistor in series with the drive transistor.

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DESCRIPTION

EMISSIVE DISPLAY DEVICES

This invention relates to emissive display devices, particularly active
5 matrix display devices having an array of pixels comprising light-emitting
display elements and thin film transistors. More particularly, but not
exclusively, the invention is concerned with an active matrix
electroluminescent display device whose pixels include light sensing elements
which are responsive to light emitted by the display elements and used in the
10 control of energisation of the display elements.

Matrix display devices employing light-emitting display elements are
well known. The display elements commonly comprise organic thin film
electroluminescent elements, (OLEDs), including polymer materials (PLEDs),
15 or else light emitting diodes (LEDs). These materials typically comprise one or
more layers of a semiconducting conjugated polymer sandwiched between a
pair of electrodes, one of which is transparent and the other of which is of a
material suitable for injecting holes or electrons into the polymer layer.

The display elements in such display devices are current driven and a
20 conventional, analogue, drive scheme involves supplying a controllable current
to the display element. Typically a current source transistor is provided as
part of the pixel configuration, with the gate voltage supplied to the current
source transistor determining the current through the electroluminescent (EL)
display element. A storage capacitor holds the gate voltage after the
25 addressing phase.

Each pixel thus comprises the EL display element and associated driver
circuitry. The driver circuitry has an address transistor which is turned on by a
row address pulse on a row conductor. When the address transistor is turned
on, a data voltage on a column conductor can pass to the remainder of the
30 pixel. In particular, the address transistor supplies the column conductor
voltage to the current source circuit, which comprises the drive transistor and
the storage capacitor connected to the gate of the drive transistor. The

column, data, voltage is provided to the gate of the drive transistor and the gate is held at this voltage by the storage capacitor even after the row address pulse has ended. The storage capacitor holds the gate-source voltage fixed. This results in a fixed source-drain current through the transistor, which
5 therefore provides the desired current source operation of the pixel. The brightness of the EL display element is approximately proportional to the current flowing through it.

In the above basic pixel circuit, differential ageing, or degradation, of the LED material, leading to a reduction in the brightness level of a pixel for a
10 given drive current, can give rise to variations in image quality across a display. A display element that has been used extensively will be much dimmer than a display element that has been used rarely. Also, display non-uniformity problems can arise due to the variability in the characteristics of the drive transistors, particularly the threshold voltage level.

Improved voltage-addressed pixel circuits which can compensate for the ageing of the LED material and variation in transistor characteristics have been proposed. These include a light sensing element which is responsive to the light output of the display element and acts to leak stored charge on the storage capacitor in response to the light output so as to control the integrated
15 light output of the display element during the drive period which follows the initial addressing of the pixel. Examples of this type of pixel configuration are described in detail in WO 01/20591 and EP 1 096 466.

In an example embodiment, a photodiode in the pixel discharges the gate voltage stored on the storage capacitor and the EL display element
25 ceases to emit when the gate voltage on the drive transistor reaches the threshold voltage, at which time the storage capacitor stops discharging. The rate at which charge is leaked from the photodiode is a function of the display element output, so that the photodiode serves as a light-sensitive feedback device.

30 With this arrangement, the light output from a display element is independent of the EL display element efficiency and ageing compensation is thereby provided. Such a technique has been shown to be effective in

achieving a high quality display which suffers less from non-uniformities over a period of time. However, this method requires a high instantaneous peak brightness level to achieve adequate average brightness from a pixel in a frame time and this is not beneficial to the operation of the display as the LED
5 material is likely to age more rapidly as a result.

In an alternative approach developed by the applicant, the optical feedback system is used to change the duty cycle with which the display element is operated. The display element is driven to a fixed brightness, and the optical feedback is used to trigger a transistor switch which turns off the
10 drive transistor rapidly. This avoids the need for high instantaneous brightness levels, but introduces additional complexity to the pixel.

According to the invention, there is provided an active matrix display device comprising an array of display pixels, each pixel comprising:
15 a current-driven light emitting display element;
a drive transistor for driving a current through the display element;
a switching transistor in series with the drive transistor; and
an optical feedback arrangement for controlling the gate voltage of the switching transistor, thereby to enable control of the timing of switching off the
20 switching transistor to isolate the display element from the drive transistor in dependence on the light output of the display element.

This arrangement uses an optical feedback arrangement for the control of an additional switching transistor instead of controlling the drive transistor. The control of the drive transistor is therefore simplified, and the additional
25 light-dependent control is for the additional switching transistor in series with the drive transistor. This implements a duty cycle type control in a simple manner.

Each pixel may further comprise a first storage capacitor for storing a pixel drive voltage to be used for addressing the drive transistor, and which
30 can be connected between the gate and source of the drive transistor. The drive transistor, the switching transistor and the display element are preferably connected in series between power supply lines.

A second storage capacitor can be provided for storing a gate voltage for the control of the switching transistor. The optical feedback arrangement can then comprise a light-dependent device for detecting the brightness of the display element, and for altering the voltage stored on the second storage capacitor.

To enable two different address voltages to be stored in the pixel, a first address transistor is provided between a data line and the gate of the drive transistor, and a second address transistor is provided between a data line and one terminal of the second storage capacitor. A single data line may be used, with sequential operation, or two data lines may be used.

A feedback transistor can be connected between the gate of the switching transistor and a power supply line for increasing the switching speed of the switching transistor.

In another arrangement for increasing the switching speed of the switching transistor, one terminal of the second storage capacitor and one terminal of the light dependent device are connected together at a circuit node, and an inverter is provided between the circuit node and the gate of the switching transistor. The inverter can be controlled by its own power lines to increase further the switching speed.

The invention also provides a method of driving an active matrix display device comprising an array of display pixels each comprising a drive transistor and a current-driven light emitting display element, the method comprising, for each pixel:

storing a first, pixel drive voltage for controlling the gate voltage applied to the drive transistor;

storing a second, pixel control voltage for controlling the voltage applied to a switching transistor, the second pixel control voltage being sufficient to switch on the switching transistor;

driving the display element the pixel with a current derived from the first, pixel drive voltage; and

detecting the optical output of the display element, and varying the control of the switching transistor dependent on the optical output until the switching transistor turns off.

The invention is of particular benefit for electroluminescent display devices.

Advantageous features in accordance with the present invention are illustrated specifically in embodiments of various aspects of the present invention now to be described, by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a simplified schematic diagram of an embodiment of active matrix EL display device;

Figure 2 illustrates a known form of pixel circuit;

Figure 3 shows a first pixel circuit of the invention;

Figure 4 shows a light output of the pixel circuit of Figure 3

Figure 5 shows a second pixel circuit of the invention;

Figure 6 shows a third pixel circuit of the invention;

Figure 7 shows a fourth pixel circuit of the invention;

Figure 8 is a timing diagram for a first method of operating the pixel circuit;

Figure 9 is a timing diagram for a second method of operating the pixel circuit;

Figure 10 is a timing diagram for a third method of operating the pixel circuit;

Figure 11 is a timing diagram for a fourth method of operating the pixel circuit; and

Figure 12 is a timing diagram for a fifth method of operating the pixel circuit.

The same reference numbers are used throughout the Figures to denote the same or similar parts.

Referring to Figure 1, the active matrix EL display device comprises a panel having a row and column matrix array of regularly – spaced pixels, denoted by the blocks 10, each comprising an EL display element 20 and an associated driving circuit controlling the current through the display element.

5 The pixels are located at the intersections between crossing sets of row (selection) and column (data) address conductors, or lines, 12 and 14. Only a few pixels are shown here for simplicity. The pixels 10 are addressed via the sets of address conductors by a peripheral drive circuit comprising a row, scanning, driver circuit 16 and a column, data, driver circuit 18 connected to
10 the ends of the respective conductor sets.

Each row of pixels is addressed in turn in a frame period by means of a selection pulse signal applied by the circuit 16 to the relevant row conductor 12 so as to program the pixels of the row with respective data signals which determine their individual display outputs in a frame period that follows the
15 address period, the data signals being supplied in parallel by the circuit 18 to the column conductors 14. As each row is addressed, the data signals are supplied by the circuit 18 in appropriate synchronisation.

The EL display element 20 of each pixel comprises an organic light emitting diode, represented here as a diode element (LED), and comprising a
20 pair of electrodes between which one or more active layers of organic electroluminescent light-emitting material are sandwiched. In this particular embodiment the material comprises a polymer LED material, although other organic electroluminescent materials, such as low molecular weight materials, could be used. The display elements of the array are carried, together with
25 their associated active matrix circuitry, on the surface of an insulating substrate. The substrate is of transparent material, for example glass, and either the cathodes or anodes of the display elements 20 are formed of a transparent conductive material, such as ITO, so that light generated by the electroluminescent layer is transmitted through these electrodes.

30 The driving circuit of each pixel 10 includes a drive transistor, comprising a low temperature polysilicon TFT (thin film transistor), which is responsible for controlling the current through the display element 20 on the

basis of a data signal voltage applied to the pixel via a column conductor 14 which is shared by a respective column of pixels. The column conductor 14 is coupled to the gate of the current-controlling drive TFT through an address TFT in the pixel driving circuit and the gates for the address TFTs of a row pixels are all connected to a respective, common, row address conductor 12.

Although not shown in Figure 1, each row of pixels 10 also shares, in conventional manner, a respective power supply line held at a predetermined voltage, and a reference potential line, usually provided as a continuous electrode common to all pixels. The display element 20 and the drive TFT are connected in series between the power supply line and the common reference potential line. The reference potential line, for example, may be at ground potential and the power supply line at a positive potential around, for example, 12V with respect thereto.

The features of the display device described thus far are generally similar to those of known devices.

Figure 2 illustrates a known form of pixel circuit, as described in WO 01/20591 for example. Here the drive TFT and the address TFT, both comprising p-channel devices, are referenced at 22 and 26 respectively, and the power supply line and reference potential line are referenced at 32 and 30 respectively. When the address TFT 26 is turned on in a respective row address period by a selection pulse signal applied to the row conductor 12, a voltage (data signal) on the column conductor 14 can pass to the remainder of the pixel. In particular, the TFT 26 supplies the column conductor voltage to a current source circuit 25 comprising the drive TFT 22 and a storage capacitor 24 connected between the gate of the TFT 22 and the power supply line 32. Thus, the column voltage is provided to the gate of the TFT 22 which is held at this voltage, constituting a stored control value, by the storage capacitor 24 even after the address TFT 26 is turned off at the end of the row address period. The drive TFT 22 is here implemented as a P-channel TFT and the capacitor 24 holds the gate – source voltage. This results in a fixed source – drain current through the TFT 22, which therefore provides the desired current source operation of the pixel. Electrical current through the display element 20

is regulated by the drive TFT 22 and is a function of the gate voltage on the TFT 22, which is dependent upon the stored control value determined by the column voltage, data, signal. At the end of the row address period, the voltage retained by the storage capacitor 24 maintains the operation of the display element during the subsequent drive period before the pixel is addressed again in the next frame period. The voltage between the gate of the TFT 22 and the power line 32 thus determines the current passing through the display element 20, and in turn controls the instantaneous light output level of the pixel.

The known pixel circuit of Figure 2 further includes a discharge photodiode 34, which is reverse biased and responsive to light emitted by the display element 20 and acts to decay the charge stored on the storage capacitor 24 in dependence on light emitted by the element 20, via the photocurrent generated in the photodiode. The photodiode discharges the gate voltage stored on the capacitor 24 and when the gate voltage on the TFT 22 reaches the TFT's threshold voltage the display element 20 will no longer emit light and the storage capacitor stops discharging. The rate at which charge is leaked from the photodiode 34 is a function of the display element light output level so that the photodiode 34 functions as a light sensitive feedback device.

The photodiode feedback arrangement is used to compensate for the degradational effects of display element ageing, whereby the efficiency of its operation in terms of the light output level produced for a given drive current diminishes. Through such degradation, display elements that have been driven longer and harder will exhibit reduced brightness, causing display non-uniformities. The photodiode arrangement counteracts these effects by appropriately controlling the integrated, total, light output from a display element in the drive period, corresponding to a frame period at maximum. The length of time for which a display element is energized to generate light during the drive period which follows the address period is regulated according to the existing drive current light emission level characteristic of the display element, as well as the level of the applied data signal, such that the effects of

degradation are reduced. Degraded, dimmer, display elements will result in the pixel driving circuit energizing the display element for a period longer than that for an un-degraded, brighter, display element so that the average brightness can remain the same over an extended period of time of device operation.

The circuit of Figure 2 has the disadvantage that the current drive to the display element gradually diminishes to zero under the control of the feedback system, so that the maximum light output of the pixel is reduced. Modifications have been proposed to provide a duty cycle type control which maintains a constant output light intensity followed by a rapid switch off of the display element at a time dependent on the optical feedback system, and this invention relates to this type of control methodology.

The invention provides an optical feedback scheme, in which, instead of switching off the driving transistor using an optical feedback arrangement, the current to the display element is interrupted by means of an optically controlled switch between the driving transistor and the display element. The optical feedback action is applied to the gate of the switch.

Figure 3 illustrates a first embodiment of pixel circuit 10 in a display device according to the present invention.

The pixel circuit comprises a current-driven light emitting display element 20 (LED), a drive transistor 22 (T_D) for driving a current through the display element and a switching transistor T_S , with the drive transistor, switching transistor and display element in series between power supply lines.

An optical feedback arrangement controls the gate voltage of the switching transistor T_S , thereby to enable control of the timing of switching off the switching transistor to isolate the display element 20 from the drive transistor 22 in dependence on the light output of the display element.

A first storage capacitor 24 (C_1) is for storing the pixel drive voltage supplied to the pixel, and for use in addressing the drive transistor. The first storage capacitor is provided between the source and gate of the drive transistor. In the example shown, the drive transistor is p-type and the source is connected to the high power rail.

A second storage capacitor C_2 is provided for storing a gate voltage for the control of the switching transistor T_S . This second storage capacitor is provided between the high power rail 32 and the gate of the switching transistor T_S , although it may be between any fixed voltage and the gate of the switching transistor T_S .

The optical feedback arrangement comprises a light-dependent device in the form of a PIN photodiode 40 for detecting the brightness of the display element. The anode of the photodiode 40 is connected to a common line 42, and the cathode is connected to gate of the switching transistor T_S . A node 44 is thus defined at the gate of the switching transistor, which couples one terminal of the second capacitor C_2 , one terminal of the photodiode 40 and the gate of the switching transistor.

As a result of the low gate current of the switching transistor, the photodiode current acts to charge or discharge the second storage capacitor, so that the gate voltage is dependent on the display element output.

Two data voltages are written to the pixel. One is written on the gate of the drive transistor T_D and the other is written on the gate of the switching transistor T_S . This can be achieved sequentially using a shared data line 14 as shown in Figure 3, or by means of two data column lines (not shown).

For this purpose, a first address transistor A_1 is provided between the data line 14 and the gate of the drive transistor T_D , and a second address transistor A_2 is provided between the data line 14 and one terminal of the second storage capacitor C_2 , which in the example of Figure 3 is connected directly to the gate of the switching transistor.

The first data voltage sets the current output to drive the display element. The drive transistor T_D works in saturation so that the current is given by a squared function of the gate voltage V_1 .

The first data voltage can be a constant voltage independent of the pixel data, and which acts to set the display element output to a constant light output.

The second data voltage set the switching transistor T_S on. For this purpose, the second data voltage may be higher than the power line voltage

V_P , but it is pixel data dependent, so that the time taken to discharge the second capacitor C_2 by the photodiode current (to a voltage at which the switching transistor turns off) is dependent on the desired pixel output.

The change in charge stored on the second capacitor C_2 is equal to the
 5 integral of the photo-induced current flowing through the photo sensor. The original charge on the capacitor C_2 is removed by the action of the photodiode thereby bringing the node voltage V_2 down towards the common voltage on line 42, and therefore switching off the switching transistor T_S .

The amount of charge flow can be calculated as follows (Equation 1):

10

$$\begin{aligned} Q_2 &= \int I_{PIN} dt = \int \gamma L dt \\ &= \int \gamma \epsilon I_{LED} dt = \gamma \epsilon \beta (V_1 - V_P - V_{TD})^2 dt \\ &= \gamma \epsilon \beta (V_1 - V_P - V_{TD})^2 t_{ON} \end{aligned}$$

This equation works out the change in charge, as the integrated photodiode current. L is the light input to the photodiode, γ is the photodiode
 15 efficiency, ϵ is the display device efficiency, I_{LED} is the current driven through the display element, β is the beta factor of the transistor, V_{TD} is the threshold voltage of the drive transistor, and t_{ON} is the time during which the display element is on.

This assumes a constant light input to the photodiode of L followed by
 20 zero light output, and hence a sharp cutoff. This implements a duty cycle type control, and the average light output can be calculated as follows (Equation 2):

$$\begin{aligned} L_{av} &= \frac{t_{ON}}{T} L_{peak} = \frac{t_{ON}}{T} \epsilon \beta (V_1 - V_P - V_{TD})^2 \\ &= \frac{(Q_2 / \gamma \epsilon \beta (V_1 - V_P - V_{TD})^2)}{T \epsilon \beta (V_1 - V_P - V_{TD})^2} \\ &= Q_2 \frac{1}{\gamma} \frac{1}{T} \end{aligned}$$

This equation works out the average light output assuming a period t_{ON} of output brightness L_{peak} followed by the remainder of the frame period T off. C_2 and V_2 are the capacitance and original voltage across the capacitor C_2 . The relationship between t_{ON} and the change in charge Q_2 from Equation 1 is substituted into the equation.

This equation shows that the average light output is dependent on the amount of charge flow from the capacitor before the switching transistor turns off, and on the frame period T and the photodiode efficiency. There is no dependency on the display element efficiency.

The switching transistor will switch off when the voltage at the gate is equal to the threshold voltage. The change in charge will thus comprise the capacitance multiplied by the required voltage change for the gate to reach to the threshold voltage. This voltage change will depend on the initial voltage V_2 and on the threshold voltage of the switching transistor, but is independent of the LED characteristics.

For example, assuming the common line 42 and the cathode line 30 are at 0V, the switching transistor will turn off approximately when the voltage V_2 at the node 44 has changed from V_2 to 0V (as the threshold voltage can be ignored compared to the large change in voltage from V_2 to 0V, recalling that V_2 can be greater than the power line voltage V_P).

Thus, equation 2 can be approximated as (Equation 3):

$$L_{av} = \frac{V_2}{C_2} \frac{1}{\gamma} \frac{1}{T}$$

The light output characteristic is shown in Figure 4.

The equations above show that the average light is not dependent on the display element efficiency, and hence the pixel circuit compensates for the display element degradation.

In the circuit of Figure 3, the switching transistor T_S has to go from on to off very quickly otherwise the compensation is not correct.

Various modifications to the pixel are possible to improve the switching time.

Figure 5 shows a first modification to the pixel circuit of Figure 3. The circuit is the same as that of Figure 3, other than the modifications described below. Instead of supplying the second capacitor voltage directly to the gate of the switching transistor, it is supplied through an inverter, which is provided
5 between the node 44 and the gate of the switching transistor T_S .

The inverter comprises first 50 and second 52 opposite type transistors in series between power lines. In the example of Figure 5, these power lines are the high power rail 32 and the common line 42 for the photodiode anodes. The gates are controlled by the voltage at the circuit node 44. As this provides
10 inversion, the switching transistor T_S is p-type in the circuit of Figure 5, otherwise the remaining circuit elements are as in Figure 3.

In this circuit, the photodiode controls the input of the inverter. At the beginning of the light output, the inverter has a low level at the output, namely the gate of the switching transistor T_S and this corresponds to a high level V_2 ,
15 as previously described. The p-type switching transistor is thus on. The input of the inverter is brought low towards the common voltage by the photodiode, and the output of the inverter then goes high and switches off the switching transistor T_S . The abrupt characteristics of the inverter improve the switching performance of the switching transistor.

As explained above, the approximations used to explain the behaviour of the pixel circuit ignore the threshold voltage of the switching transistor. In fact, the light output will have a dependence on the threshold voltage and will therefore be sensitive to threshold voltage changes of the switching transistor. This effect may in some cases be negligible. However, the inverter used in
20 Figure 5 dramatically reduces the dependency of the light output on this switching transistor threshold voltage.

In Figure 6, a dedicated high power line 60 is used for the inverter, and this improves the operation of the inverter. The circuit is otherwise the same as Figure 5.

Another way to improve the switching speed is shown in Figure 7, in which positive feedback is implemented into the pixel circuit by means of a feedback transistor 70 connected between the gate of the switching transistor
30

T_S and the common voltage. The drain of the drive transistor T_D is connected to the gate of the feedback transistor 70. As the switching transistor begins to turn off, and its impedance increases, the voltage V_D begins to rise, which has the effect of accelerating the switching off of the feedback transistor.

5 The invention may be implemented using circuits with polycrystalline or amorphous silicon TFTs, or microcrystalline silicon TFTs. The optical feedback device is typically a photodiode in the form of a pin device.

 The invention is applicable to many different emissive display technologies (e.g. organic light emitting diode (OLED), Inorganic light emitting diode (iLED), field emission display (FED), electroluminescent display (EL)) on
10 any active matrix substrate (amorphous, polycrystalline and crystalline silicon substrate, organic TFT substrate) where the emissive elements suffer of degradation in the light output. The use of the invention prevents burn-in and keeps the colour point stable in time.

15 Because of the increased numbers of transistors, capacitor and lines, these pixel circuits are more suited to AMOLED displays with top emission where the entire pixel area can be used.

 In the example above, the cathode line 30 can be at a constant voltage, for example 0V. As soon as a pixel is addressed, it will start emitting light, and
20 this will happen as soon as the switching transistor is turned on while the voltage V_2 is being loaded into the second capacitor C_2 . As an alternative, the cathode line 30 can be switched, so that the display can be driven in two phases - an addressing phase followed by a driving phase.

 There are thus a number of different addressing methods, and some of
25 these are explained below with reference to Figures 8 to 12, and based on the most basic circuit of Figure 3.

(i) The rows can be addressed in turn, with each row being addressed by switching address lines A1 and A2 in sequence. The cathode is constant at 0V. In this method, the display element emits light during the
30 addressing phase and thereafter, until the switching transistor turns off. If the required time (t_{ON}) exceeds the frame time, the feedback system has failed, otherwise the light output is dependent only on the second voltage V_2 applied

to the pixel. This method is shown in Figure 8, which shows the address pulses for address lines A1 and A2 for the first row (plots 80) and the last row (plots 82).

(ii) The cathode is switched to turn off the display elements during an addressing phase. The addressing phase applies the sequential pulses for the address lines A1 and A2 for each row in sequence. This is phase 90 shown in Figure 9, and which is shown as a dark output. Again, plots for the first and last rows are shown as 92 and 94. The light output is during the phase 96. The light output is controlled again only by V2.

(iii) The method of (ii) is modified so that all address pulses for the address lines A1 are applied before the address pulses for the address lines A2. This is shown in Figure 10, which otherwise corresponds to Figure 9. The light output is controlled only by V2.

(iv) The cathode can be driven to a constant voltage, and two data voltages can be applied per frame. This is shown in Figure 11. The rows are again addressed in sequence, and the figure again shows the first and last rows. Initially, address pulses are provided for the lines A1 and A2 for a first bright sub-field 110, and then a second address pulse is provided for the address line A2 for a second sub-field 112. There are thus two data voltages, V2a and V2b for loading to the pixel from the data line through the second address transistor. In this method, the voltages V1 and V2 both influence the light output.

During the first phase, the voltage V2a is selected so that the switching transistor stays on, and the light output is dependent on the voltage V1. During the second phase, the voltage V2b is selected to provide the switch off of the switching transistor.

This approach ensures that the display element is always on for the first phase, and this avoids short pulses of light for low brightness levels. The two voltages V1 and V2b are data-dependent.

(v) The scheme of (iv) can be modified also to include cathode switching, as shown in Figure 12. The two phases 110 and 112 now include a

dark addressing portion and a bright output portion, controlled by the cathode line voltage.

Thus, in some examples, the drive transistor is driven to provide a fixed output (corresponding to L_{peak}), and all of the brightness control is achieved using the feedback system based on the voltage V_2 . In other examples, a voltage which is dependent on the pixel data may be applied to the drive transistor (the voltage V_1). In this way, the switching transistor can implement only fine tuning of the on-time, and this can be in a second phase. This will require more complicated determination of V_1 and V_2 , but with the advantage that low brightness levels will not be provided as a short flash. This combination of control approaches enables the duty cycle always to be in a high range (for example always above 50%), but the drive scheme still does not limit the maximum brightness, because the display element can still be driven to full brightness for the full frame time.

Thus, the feedback scheme can implement a combination of analogue drive and duty cycle control, or else it can implement a duty cycle control with fixed brightness. Thus, the level L_{peak} in Figure 4 can be constant or it can be dependent on the pixel data.

Various other modifications will be apparent to those skilled in the art.

CLAIMS

1. An active matrix display device comprising an array of display pixels, each pixel comprising:
 - 5 a current-driven light emitting display element (LED);
 - a drive transistor (22) for driving a current through the display element;
 - a switching transistor (20) in series with the drive transistor; and
 - an optical feedback arrangement (40) for controlling the gate voltage of the switching transistor, thereby to enable control of the timing of switching off
 - 10 the switching transistor to isolate the display element from the drive transistor (22) in dependence on the light output of the display element.
2. A device as claimed in claim 1, wherein each pixel further comprises:
 - a first storage capacitor (24) for storing a pixel drive voltage to be used
 - 15 for addressing the drive transistor.
3. A device as claimed in claim 2, wherein the first storage capacitor (24) is connected between the gate and source of the drive transistor (22).
- 20 4. A device as claimed in any preceding claim, wherein the drive transistor (22), the switching transistor (20) and the display element are connected in series between power supply lines (32,30).
5. A device as claimed in any preceding claim, wherein the current-driven
- 25 light emitting display element (LED) comprises an electroluminescent display element.
6. A device as claimed in any preceding claim, wherein each pixel further comprises:
 - 30 a second storage capacitor (C_2) for storing a gate voltage for the control of the switching transistor (20).

7. A device as claimed in claim 6, wherein the optical feedback arrangement comprises:

a light-dependent device (40) for detecting the brightness of the display element, and for altering the voltage stored on the second storage capacitor (C₂).

8. A device as claimed in claim 6 or 7, wherein the second storage capacitor is connected between one terminal of the light-dependent device (40) and a power line (42).

9. A device as claimed in any one of claims 6 to 8, wherein a first address transistor (A1) is provided between a data line (14) and the gate of the drive transistor (22), and a second address transistor (A2) is provided between a data line (14) and one terminal of the second storage capacitor (C₂).

10. A device as claimed in any one of claims 6 to 9, wherein one terminal of the second storage capacitor (C₂), one terminal of the light dependent device (40) and the gate of the switching transistor (20) are connected together (44).

11. A device as claimed in claim 10 further comprising a feedback transistor (70) connected between the gate of the switching transistor (20) and a power supply line for increasing the switching speed of the switching transistor.

12. A device as claimed in any one of claims 6 to 9, wherein one terminal of the second storage capacitor (C₂) and one terminal of the light dependent device (40) are connected together at a circuit node (44), and an inverter is provided between the node (44) and the gate of the switching transistor (20).

13. A device as claimed in claim 12, wherein the inverter comprises first and second opposite type transistors (50,52) in series between power lines, with the gates controlled by the voltage at the circuit node (44).

14. A device as claimed in claim 13, wherein the drive transistor (22), the switching transistor (20) and the display element (LED) are connected in series between first and second power supply lines (32,30), and the first and second opposite type transistors are in series between the first power supply line (32) and a third power supply line (42) to which the optical feedback arrangement (40) is connected.

15. A device as claimed in claim 13, wherein the drive transistor (22), the switching transistor (20) and the display element (LED) are connected in series between first and second power supply lines (32,30) and the first and second opposite type transistors (50,52) are in series between different third and fourth power supply lines (60,42).

16. A method of driving an active matrix display device comprising an array of display pixels each comprising a drive transistor (22) and a current-driven light emitting display element (LED), the method comprising, for each pixel:

storing a first, pixel drive voltage (V1) for controlling the gate voltage applied to the drive transistor (22);

storing a second, pixel control voltage (V2) for controlling the voltage applied to a switching transistor, the second pixel control voltage being sufficient to switch on the switching transistor (20);

driving the display element of the pixel with a current derived from the first, pixel drive voltage (V1);

detecting the optical output of the display element, and varying the control of the switching transistor (20) dependent on the optical output until the switching transistor turns off.

17. A method as claimed in claim 16, wherein the drive transistor (22), the switching transistor (20) and the display element (LED) are connected in series between power supply lines (32,30).

18. A method as claimed in claim 16 or 17, wherein detecting the optical output of the display element and varying the control of the switching transistor comprises using the optical output to vary the charge stored on a capacitor (C_2) which controls the gate voltage of the switching transistor (20).

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19. A method as claimed in any one of claims 16 to 18, wherein storing a first, pixel drive voltage (V_1) comprises charging a storage capacitor (24) which controls the gate voltage of the drive transistor (22).

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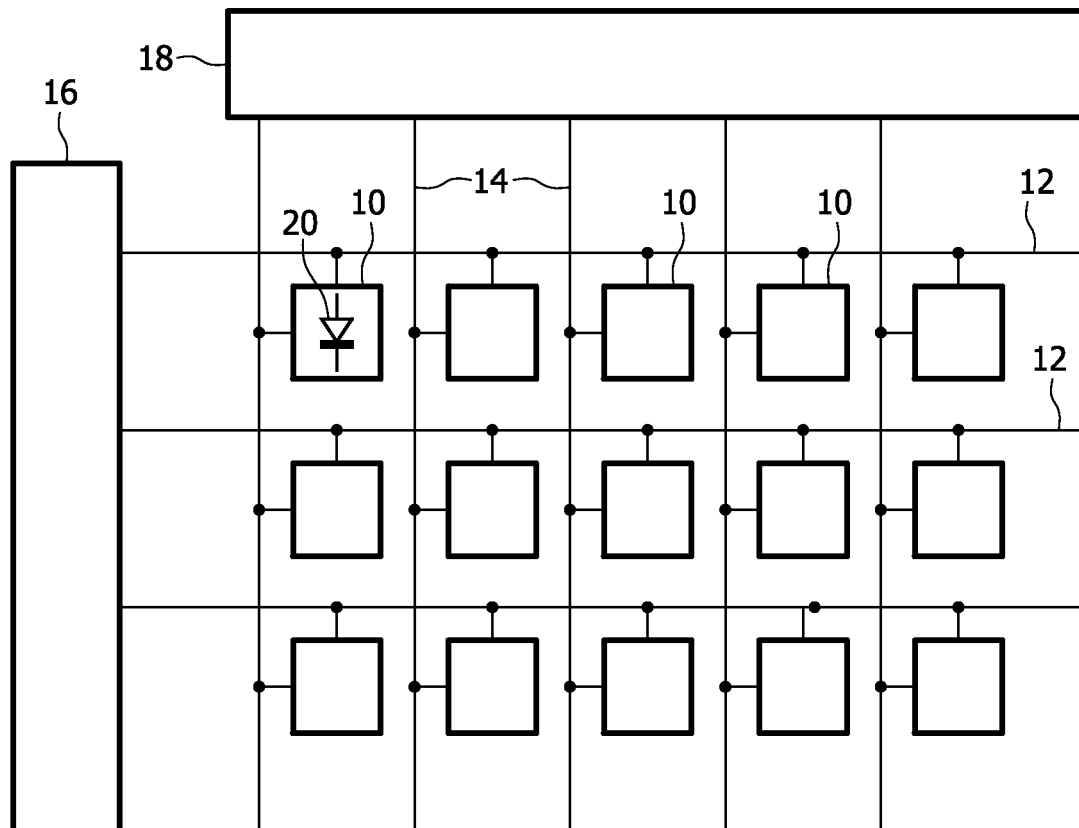


FIG. 1 PRIOR ART

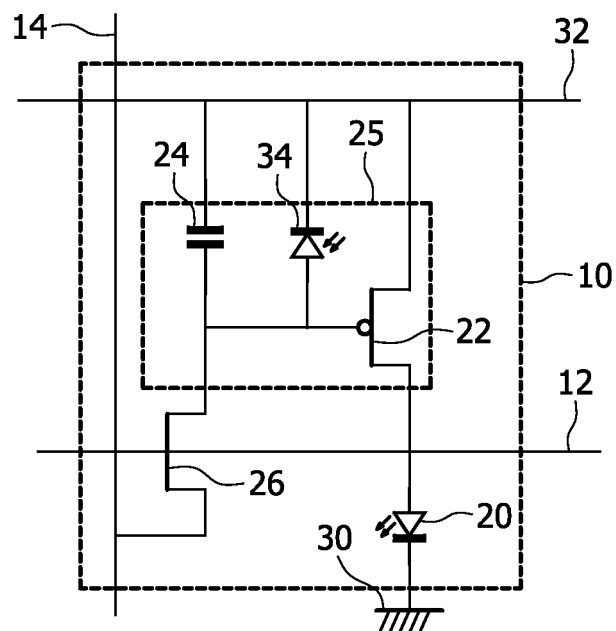


FIG. 2 PRIOR ART

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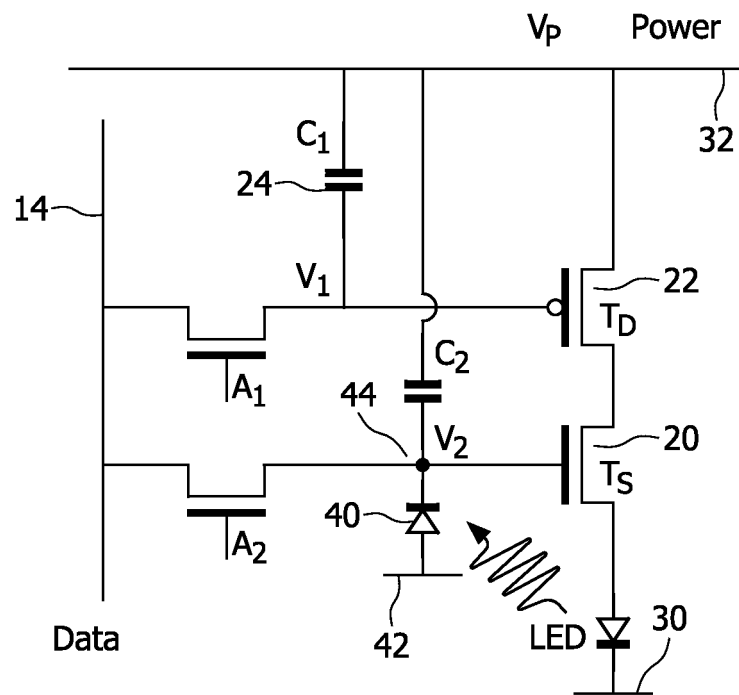


FIG. 3

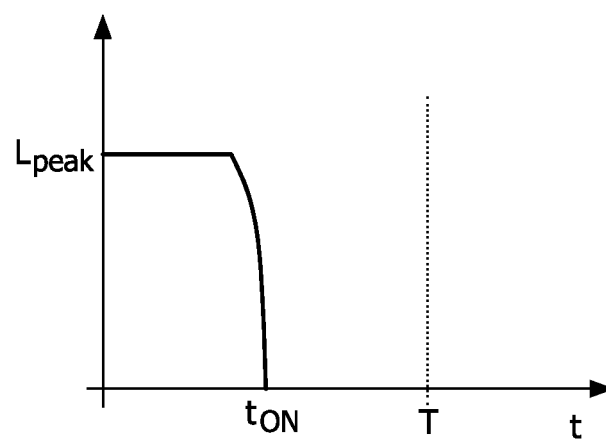


FIG. 4

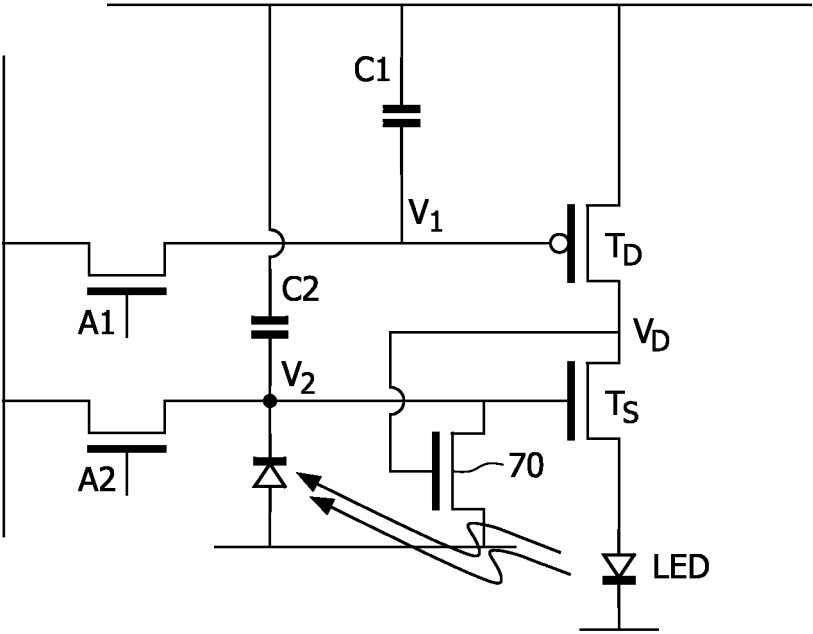


FIG. 7

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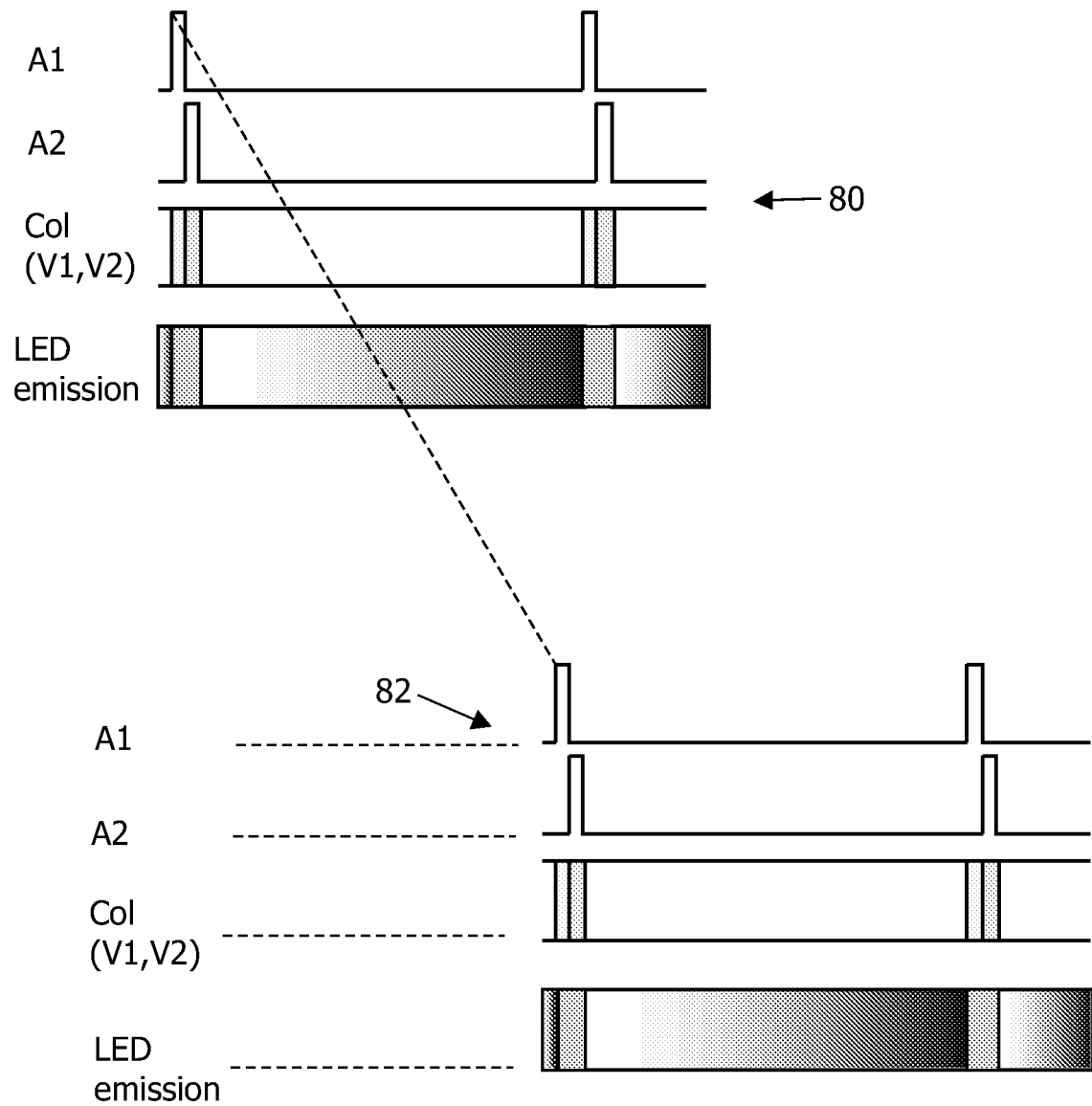


FIG. 8

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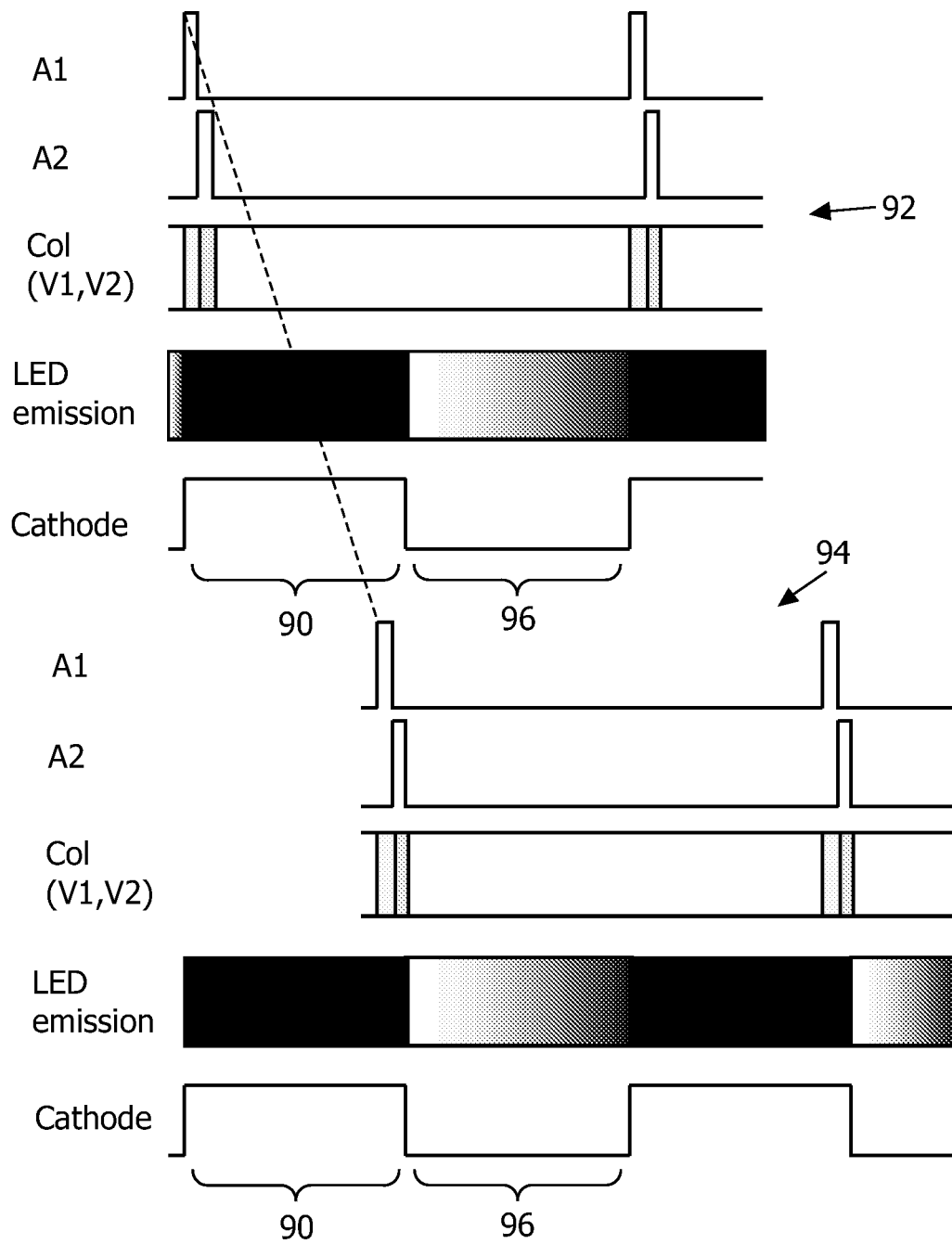


FIG. 9

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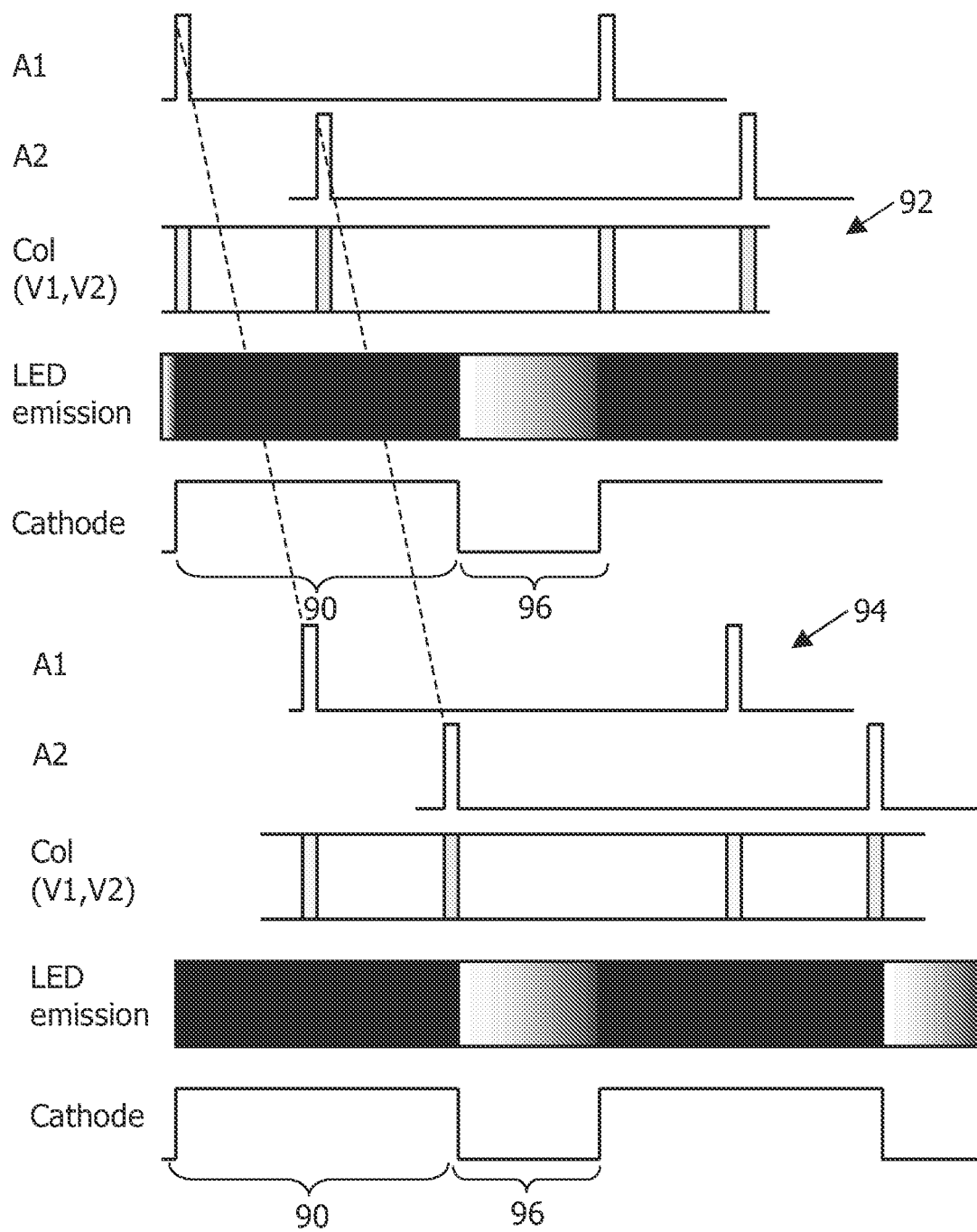


FIG. 10

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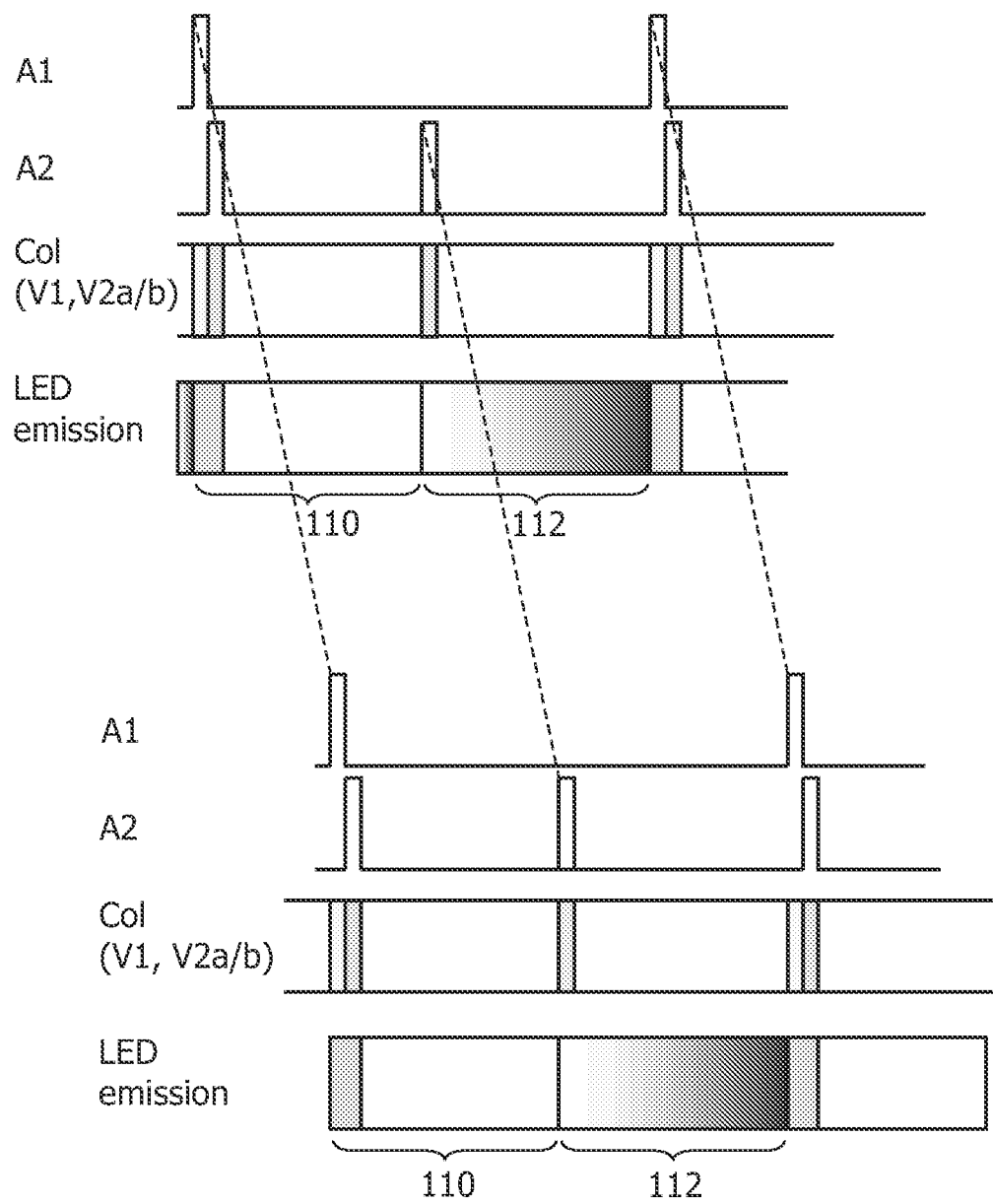


FIG. 11

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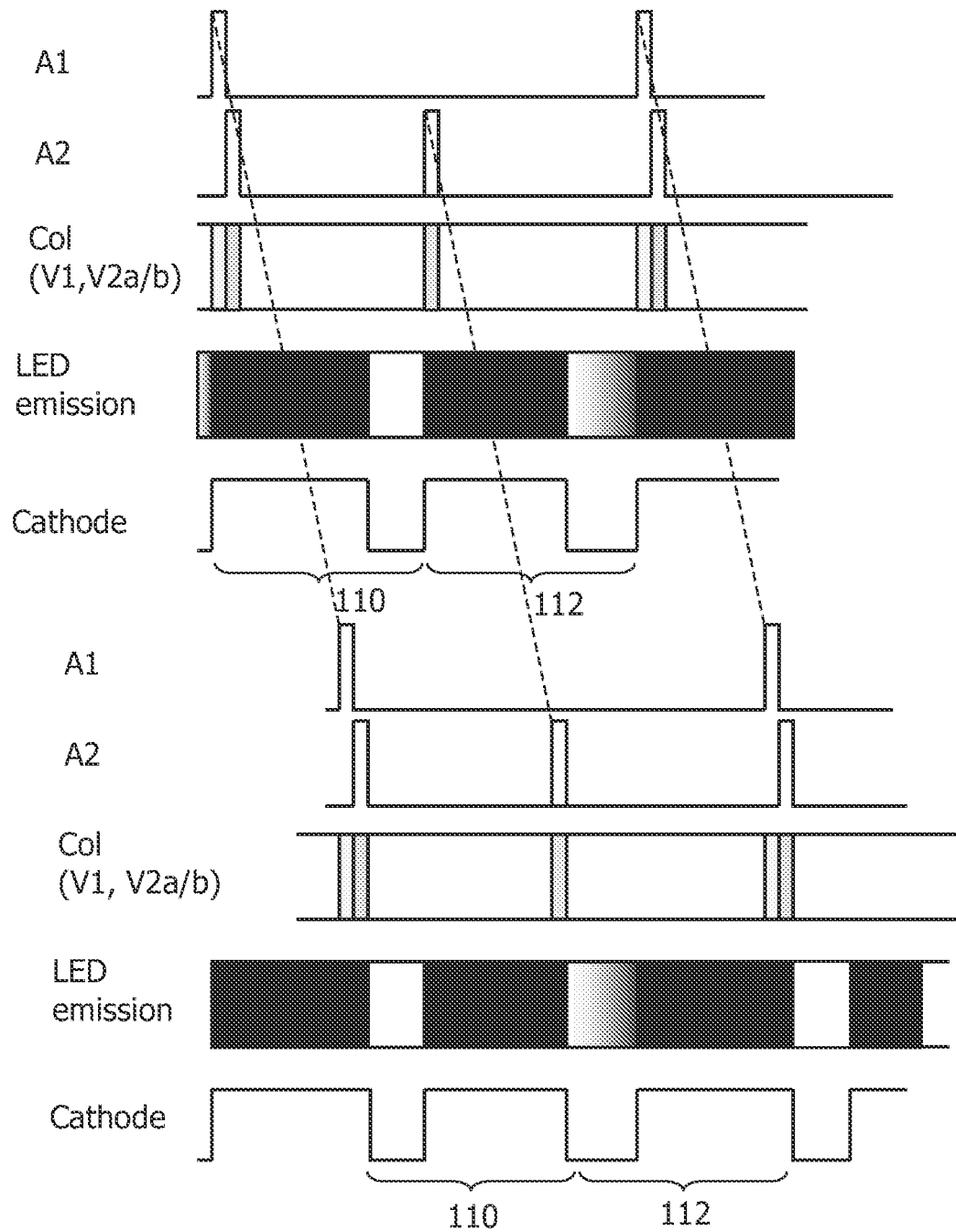


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No

PCT/IB2006/053643

A. CLASSIFICATION OF SUBJECT MATTER
INV. G09G3/32

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2005/091268 A (KONINKL PHILIPS ELECTRONICS NV [NL]; FISH DAVID A [GB]; DEANE STEVEN C) 29 September 2005 (2005-09-29) page 1, paragraph 1 page 4, line 1 - line 21 page 8, line 8 - line 21 page 9, line 31 - line 32 figures 1,6-9,13,14,20 -----	1-3,5, 16,18,19
P,X	US 2005/225683 A1 (NOZAWA TOSHIYUKI [JP]) 13 October 2005 (2005-10-13) paragraphs [0032], [0045] paragraphs [0066] - [0068] figures 3,9 -----	1-9,12, 13,16-19



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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O document referring to an oral disclosure, use, exhibition or other means

P document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

& document member of the same patent family

Date of the actual completion of the international search

8 February 2007

Date of mailing of the international search report

20/02/2007

Name and mailing address of the ISA/

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Authorized officer

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/IB2006/053643

Patent document cited in search report		Publication date		Patent family member(s)	Publication date
WO 2005091268	A	29-09-2005	EP	1728238 A1	06-12-2006
US 2005225683	A1	13-10-2005	JP	2005300897 A	27-10-2005

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发明人	GIRALDO, ANDREA KURT, RALPH		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3233 G09G3/2011 G09G3/2014 G09G3/2022 G09G3/22 G09G2300/0819 G09G2300/0852 G09G2300/0866 G09G2320/043 G09G2320/045 G09G2330/02 G09G2360/148		
优先权	2005109544 2005-10-13 EP		
外部链接	Espacenet		

摘要(译)

有源矩阵显示装置包括显示像素阵列，每个像素包括电流驱动的发光显示元件，用于驱动电流通过显示元件的驱动晶体管，与驱动晶体管串联的开关晶体管和光学反馈装置用于控制开关晶体管的栅极电压，从而能够控制关断开关晶体管的定时，以根据显示元件的光输出将显示元件与驱动晶体管隔离。该布置使用光学反馈装置来控制附加的开关晶体管，而不是控制驱动晶体管。因此简化了驱动晶体管的控制，并且附加的光控制用于与驱动晶体管串联的附加开关晶体管。