(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 950 364 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
27.03.2019 Bulletin 2019/13

(51) Int Cl.:
H01L 51/52 *(2006.01)* ***H01L 27/32*** *(2006.01)*

(21) Application number: **15169154.0**

(22) Date of filing: **26.05.2015**

(54) ORGANIC LIGHT EMITTING DISPLAY PANEL AND METHOD OF MANUFACTURING THE SAME

ORGANISCHE LICHTEMITTIERENDE ANZEIGETAFEL UND VERFAHREN ZUR HERSTELLUNG DAVON

PANNEAU D'AFFICHAGE ÉLECTROLUMINESCENT ORGANIQUE ET SON PROCÉDÉ DE FABRICATION

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

(30) Priority: **27.05.2014 KR 20140063963**

(43) Date of publication of application:
02.12.2015 Bulletin 2015/49

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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of the Korean Patent Application No. 10-2014-0063963 filed on May 27, 2014.

BACKGROUND

Field of the Invention

[0002] The present disclosure relates to an organic light emitting display panel and a method of manufacturing the same, and more particularly, to an organic light emitting display panel and a method of manufacturing the same, which use face seal technology for achieving narrow bezel configurations.

Discussion of the Related Art

[0003] Recently, flat panel displays (FPD) and other types of display apparatuses which have good characteristics such as thinness, lightness, and low power consumption are increasing in importance. Examples of display apparatuses include liquid crystal display (LCD) apparatuses, plasma display panels (PDPs), organic light emitting display (OLED) apparatuses, flexible displays, curved displays, etc. Recently, electrophoretic display (EPD) apparatuses are being used as well.

[0004] In particular, LCD apparatuses and an organic light emitting display apparatuses including thin film transistors (TFTs) are good in resolution, color display, and image quality, and thus are commercialized as display apparatuses for notebook computers, tablet computers, desktop computers, smartphones, and various other electronic devices.

[0005] Organic light emitting display (OLED) apparatuses are self-emitting apparatuses, and have low power consumption, a fast response time, high emission efficiency, high luminance, and a wide viewing angle. Therefore, the organic light emitting display apparatuses are attracting much attention as next-generation display apparatuses.

[0006] A lifetime of a panel for an organic light emitting display apparatus is determined based on certain factors, such as an operation lifetime and a shelf lifetime.

[0007] The operation lifetime denotes a period where maximum luminance is reduced when driving a device (for example, an organic light emitting diode (OLED)). The operation lifetime can be determined based on impurities contained in an organic material, an interface between the organic material and an electrode, a low glass transition temperature (Tg) of the organic material, and oxidization of a device (for example, an OLED) by oxygen and moisture.

[0008] The shelf lifetime denotes a period during which characteristics of an emission area is gradually reduced by moisture permeation into the organic material despite the device not being driven.

[0009] A lifetime of an OLED is determined by a shorter lifetime value among the operation lifetime and the shelf lifetime.

[0010] Moisture denotes that which is introduced in a process of manufacturing a device (for example, an OLED), and moisture which permeates from the exterior into the manufactured device. In some organic light emitting display apparatuses, face seal technology is used for minimizing the permeation of external moisture.

[0011] FIG. 1 is a cross-sectional view schematically illustrating a configuration of an organic light emitting display panel 10 having a face seal structure. FIGS. 2A and 2B are exemplary diagrams for describing a moisture permeation path based on a non-display area size in at organic light emitting display panel 10 having the face seal structure. The non-display area includes a bezel area.

[0012] Referring to FIG. 1, the organic light emitting display panel 10 includes a driving transistor Tdr which is on a first substrate 12, an OLED (denoted as "E") which is connected to a first driving electrode 14 of the driving transistor Tdr, a passivation layer 15 which covers a whole surface of the first substrate 12 including the OLED E, and a second substrate 17 which is provided on the passivation layer 15. In this case, the first substrate 12 is closely adhered to the second substrate 17 with the passivation layer 15 therebetween. In such organic light emitting display apparatus, the passivation layer 15 and the second substrate 17 cover the entire upper surface of the first substrate 12, and thus, even when external force or impact is applied to the organic light emitting display apparatus, the organic light emitting display panel 10 is not easily damaged.

[0013] However, in such organic light emitting display apparatus having the face seal structure, a moisture permeation path could occur due to interface imperfections or defects of a non-display area including a bezel area. In this case, as illustrated in FIG. 2A, moisture permeates into the OLED E via a bank 16 and a planarization layer 13, which are disposed at an outermost portion of the organic light emitting display panel 10, along a moisture permeation path R which starts from a side surface of the passivation layer 15.

[0014] Particularly, in a case of implementing a narrow bezel in an organic light emitting display apparatus, since an anti-moisture film such as a barrier film is not provided in a non-display area, allowing for a moisture permeation path up to a certain length or distance should be secured for maximally delaying the permeation of external moisture.

[0015] However, as illustrated in FIG. 2B, in the organic light emitting display apparatus having the face seal structure, as the non-display area is reduced, the moisture permeation path R becomes shorter.

[0016] Therefore, a probability that moisture permeates into the OLED E via the bank 16 and the planarization layer 13 which are disposed at the outermost portion

of the organic light emitting display panel 10 becomes higher.

[0017] Due to the permeation of moisture, a moisture permeability of the OLED E can worsen, and a lifetime of the OLED (E) is shortened. For this reason, the lifetime of an organic light emitting display apparatus is shortened.

[0018] US 2010/171138 A1 describes light-emitting elements in which an insulating layer serves as a partition and has a convex portion, wherein the convex portion is embedded in a resin film such that the resin film covers an entire surface of the insulating layer and an entire surface of a second electrode. Furthermore, an additional insulating layer made from an inorganic compound is formed over the second electrode, serves as a protective layer of the light-emitting element, and is provided in order to prevent entry of moisture or damages to the electroluminescent layer.

[0019] US 2003/201443 A1 describes a method for manufacturing a light-emitting device including an anode, banks, an organic compound layer, a cathode, and an additional layer covering all the structures of the light-emitting device in the display area and the non-display area of the device.

[0020] US 2006/132033 A1 describes a method of manufacturing an organic EL display, wherein the organic EL display includes a frame-shaped sealing resin layer which is formed such that the sealing resin layer surrounds the organic EL elements. Furthermore, the organic EL display includes a first electrode and partition insulating layers formed on a passivation layer. The sealing resin layer is formed along peripheries of the array substrate and the sealing substrate to form the frame shape, thereby forming a closed space between the substrates and covers portions of the passivation film which are not covered by the partition insulating layer.

SUMMARY

[0021] Accordingly, the present disclosure is directed to provide an apparatus, an organic light emitting display panel and a method of manufacturing the same that substantially obviate one or more problems due to limitations and disadvantages explained above.

[0022] An aspect of the present disclosure is directed to provide an organic light emitting display panel which includes an anti-moisture unit formed on a planarization layer so as to cover a non-display area and a second bank disposed between the non-display area and a display area.

[0023] Additional advantages and features of the present disclosure will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the present disclosure. The objectives and other advantages of the present disclosure may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0024] To achieve these and other advantages and in accordance with the purpose of the present disclosure, as embodied and broadly described herein, in accordance with various embodiments there is provided an apparatus according to claim 1.

[0025] Further embodiments of the invention are described in the dependent claims.

[0026] It is to be understood that both the foregoing general description and the following detailed description of the present disclosure are exemplary and explanatory and are intended to provide further explanation of the present disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The accompanying drawings, which are included to provide a further understanding of the present disclosure and are incorporated in and constitute a part of this disclosure, illustrate embodiments of the present disclosure and together with the description serve to explain the principle of the present disclosure. In the drawings:

FIG. 1 is a cross-sectional view schematically illustrating a configuration of an organic light emitting display panel having a face seal structure;

FIGS. 2A and 2B are exemplary diagrams for describing a moisture permeation path based on a non-display area size in the organic light emitting display panel having the face seal structure;

FIG. 3 is an exemplary diagram illustrating a configuration of an organic light emitting display apparatus including an organic light emitting display panel according to an exemplary embodiment of the present disclosure;

FIG. 4 is an exemplary diagram for describing an organic light emitting display panel according to an exemplary embodiment of the present disclosure; and

FIGS. 5A to 5F are exemplary diagrams for describing a method of manufacturing an organic light emitting display panel according to an exemplary embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE INVENTION

[0028] Reference will now be made in detail to the exemplary embodiments of the present disclosure, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0029] Hereinafter, embodiments of the present disclosure will be described in detail with reference to the accompanying drawings.

[0030] FIG. 3 is an exemplary diagram illustrating a configuration of an organic light emitting display appara-

tus including an organic light emitting display panel according to an exemplary embodiment of the present disclosure.

[0031] As illustrated in FIG. 3, the organic light emitting display apparatus including the organic light emitting display panel according to an exemplary embodiment of the present disclosure includes: a panel 100 where a plurality of pixels (P) 110 are respectively provided at or near intersection areas of a plurality of gate lines GL1 to GLg and a plurality of data lines DL1 to DLd; a gate driver 200 that sequentially supplies a scan pulse to the gate lines GL1 to GLd formed in the panel 100; a data driver 300 that respectively supplies data voltages to the data lines DL1 to DLd formed in the panel 100; and a timing controller 400 that controls a function of the gate driver 200 and a function of the data driver 300.

[0032] In the panel 100, the plurality of pixels (P) 110 may be respectively provided in a plurality of areas defined by intersections of the plurality of gate lines GL and the plurality of data lines DL.

[0033] Each of the plurality of pixels 110 may include an organic light emitting diode (OLED), which emits light, and a driver that drives the OLED.

[0034] First, the OLED may be configured in a top emission type where the light emitted from the OLED passes through through an upper substrate, or may be configured in a bottom emission type where the light emitted from the OLED passes through a lower substrate.

[0035] Second, the driver may be connected to a data line DL and a gate line GL which correspond to the driver. The driver may include a driving transistor, a switching transistor, and a storage capacitor, which are used to drive the OLED.

[0036] An anode of the OLED may be connected to a first power source, and a cathode of the OLED may be connected to a second power source. The OLED may emit light having certain luminance in response to a current supplied from the driving transistor.

[0037] When the scan pulse is supplied through the gate line GL, the driver may control an amount of current supplied to the OLED according to a data voltage supplied through the data line DL.

[0038] To this end, the driving transistor may be connected between the first power source and the OLED, and the switching transistor may be connected to the driving transistor, the data line DL, and the gate line GL.

[0039] The timing controller 400 outputs a gate control signal GCS for controlling the gate driver 200 and a data control signal DCS for controlling the data driver 300 by using a vertical sync signal, a horizontal sync signal, and a clock which are supplied from an external system.

[0040] The timing controller 400 samples input image data received from the external system, realigns the sampled image data, and supplies realigned digital image data to the data driver 300.

[0041] That is, the timing controller 400 realigns the input image data supplied from the external system, and supplies the realigned digital image data to the data driver 300. Also, the timing controller 400 generates the gate control signal GCS for controlling the gate driver 200 and the data control signal DCS for controlling the data driver 300 by using the vertical sync signal, the horizontal sync signal, and the clock signal which are supplied from the external system, and respectively transfers the gate control signal GCS and the data control signal DCS to the gate driver 200 and the data driver 300. Here, the vertical sync signal, the horizontal sync signal, and the clock signal are simply referred to as timing signals.

[0042] To this end, particularly, the timing controller 400 includes: a receiver that receives the input image data and the signals from the external system; an image data processor that realigns the input image data received from the receiver so as to match the panel 100, and generates the realigned digital image data; a control signal generator that generates the gate control signal GCS for controlling the gate driver 200 and the data control signal DCS for controlling the data driver 300 by using the signals received from the receiver; and a transferor that respectively outputs the control signals, generated by the control signal generator, to the gate driver 200 and the data driver 300, and outputs the image data, generated by the image data processor, to the data driver 300.

[0043] The data driver 300 converts the image data, input from the timing controller 400, into analog data voltages, and respectively supplies data voltages of one horizontal line to the data lines at every one horizontal period where the scan pulse is supplied to a corresponding gate line. That is, the data driver 300 converts the image data into the data voltages by using gamma voltages supplied from a gamma voltage generator, and respectively outputs the data voltages to the data lines.

[0044] That is, the data driver 300 shifts a source start pulse SSP from the timing controller 400 according to a source shift clock SSC to generate a sampling signal. The data driver 300 latches the image data, input according to the source shift clock SSC, according to the sampling signal, and converts the image data into the data voltages. Then, the data driver 300 respectively supplies the data voltages to the data lines in units of a horizontal line in response to a source output enable signal SOE.

[0045] To this end, the data driver 300 may include a shift register, a latch, a digital-to-analog converter (DAC), and an output buffer.

[0046] The shift register outputs the sampling signal by using data control signals received from the timing controller 400.

[0047] The latch latches the digital image data which are sequentially received from the timing controller 400, and then simultaneously outputs the latched image data to the DAC.

[0048] The DAC converts the image data, transferred from the latch, into the data voltages, and outputs the data voltages. That is, the DAC converts the image data into the data voltages by using the gamma voltages supplied from the gamma voltage generator, and respectively outputs the data voltages to the data lines.

[0049] The output buffer respectively outputs the data voltages, transferred from the DAC, to the data lines DL of the panel 100 according to the source output enable signal SOE transferred from the timing controller 400.

[0050] The gate driver 200 sequentially supplies the scan pulse to the gate lines GL1 to GLg of the panel 100 in response to the gate control signal input from the timing controller 400. Therefore, a plurality of switching transistors which are respectively formed in a plurality of sub-pixels 110 on a corresponding horizontal line to which the scan pulse is applied are turned on, and an image may be output to each of the sub-pixels 110.

[0051] That is, the gate driver 200 shifts a gate start pulse GSP transferred from the timing controller 400 according to a gate shift clock GSC to sequentially supply the scan pulse having a gate-on voltage to the gate lines GL1 to GLg. Also, during the other period where the scan pulse is not supplied, the gate driver 200 supplies a gate-off voltage to the gate lines GL1 to GLg.

[0052] The gate driver 200 may be provided independently from the panel 100, and may be configured in a type which is electrically connected to the panel 100 by various manners. However, the gate driver 200 may be configured in a gate-in-panel (GIP) type which is equipped in the panel 100. In this case, a gate control signal for controlling the gate driver 200 may include a start signal VST and a gate clock GCLK.

[0053] Moreover, hereinabove, it has been described that the data driver 300, the gate driver 200, and the timing controller 400 are separately provided, but at least one among the data driver 300 and the gate driver 200 may be provided as one body with the timing controller 400. Hereinafter, also, a generic name for the gate driver 200, the data driver 300, and the timing controller 400 is a panel driver.

[0054] FIG. 4 is an exemplary diagram for describing an organic light emitting display panel 100 according to an exemplary embodiment of the present disclosure.

[0055] As illustrated in FIG. 4, the organic light emitting display panel 100 includes a first substrate 120, a plurality of driving transistors Tdr which are formed on the first substrate 120, a planarization layer 123 which covers the driving transistors Tdr, a first bank 161 which is formed on the planarization layer 123 and in a display area where the driving transistors Tdr are formed and divides a plurality of pixels, a second bank 162 which is formed on the planarization layer 123 and divides the display area and a non-display area which is disposed outside the display area, an anti-moisture unit 155 which is formed on the planarization layer 123 to cover the non-display area and the second bank 162, a plurality of OLEDs E which are respectively formed in the plurality of pixels and emit light by the respective driving transistors Tdr, a passivation layer 150 which is formed on the anti-moisture unit 155 and the OLEDs E, and a second substrate 170 which covers the passivation layer 150.

[0056] A semiconductor layer 130 which is divided into a first area 130a including pure polysilicon and two second areas 130b on which impurities are doped, a gate insulation layer 121, a gate 145, an interlayer dielectric 122, and a driving thin film transistor (hereinafter referred to as a driving transistor) Tdr including first and second driving electrodes 141 and 142 may be formed on the first substrate 120. Here, the first driving electrode 141 may be connected to one of the two second areas 130b of the semiconductor layer 130, and the second driving electrode 142 may be connected to the other of the two second areas 130b.

[0057] The planarization layer 123 may include a contact hole 125 which exposes the first driving electrode 141, and may be disposed on the first and second driving electrodes 141 and 142.

[0058] A bank 163 which separates the plurality of pixels is disposed on the planarization layer 123. In this case, the bank 163 is formed in the display area where the driving transistors Tdr are formed, and includes the first bank 161 which separates the pixels and the second bank 162 which separates the display area and the non-display area disposed outside the display area.

[0059] The planarization layer 123 and the bank 163 may be each formed of, for example, an organic material such as polyimide, polyamide, acryl resin, or benzo cyclo butane (BCB), but are not limited thereto. In general, such materials may have poor anti-moisture ability.

[0060] The anti-moisture unit 155 which covers the non-display area and the second bank 162 is formed on the planarization layer 123 on which the first and second banks 161 and 162 are formed.

[0061] In this case, as illustrated in FIG. 4, the anti-moisture unit 155 may be formed to cover an entire portion of the planarization layer 123 which is exposed at the non-display area. That is, the anti-moisture unit 155 may cover all a side surface and a plane of the planarization layer 123. In other words, the anti-moisture unit 155 may cover the exposed portion of the planarization layer at the non-display area.

[0062] Moreover, as illustrated in FIG. 4, the anti-moisture unit 155 does not cover an entire portion of the second bank 162 but covers only a portion of the second bank 162 corresponding to the non-display area. That is, the second bank 162 may be formed to overlap an edge of a first electrode 147 of the OLED E, and in this case, the anti-moisture unit 155 may not be formed on a portion of the second bank 162 overlapping the edge of the first electrode 147.

[0063] Moreover, the anti-moisture unit 155 may be formed of an inorganic thin layer.

[0064] The OLED E which emits light by the driving transistor Tdr formed in each of the plurality of pixels includes the first electrode 147, an organic emission layer 148, and a second electrode 149. Here, the first electrode 147 is formed in the display area and on the planarization layer 123. In this case, the first electrode 147 may be electrically connected to the first driving electrode 141 of the driving transistor Tdr in each of a plurality of pixel areas. The organic emission layer 148 is formed on the

first electrode 147. The second electrode 149 is formed on the organic emission layer 148 and the bank 163.

[0065] The passivation layer 150 may be formed on the anti-moisture unit 155 and the OLEDs E.

[0066] The passivation layer 150 formed on the anti-moisture unit 155 may include a first passivation layer 151, which is formed on the anti-moisture unit 155, and one or more layers which are formed on the first passivation layer 151. The first passivation layer 151 may be formed of the same material as that of the anti-moisture unit 155, but is not limited thereto.

[0067] When the anti-moisture unit 155 is formed of the same material as that of the first passivation layer 151, adhesiveness between interfaces is better than a case where the anti-moisture unit 155 and the first passivation layer 151 are formed of different materials.

[0068] In an exemplary embodiment, the passivation layer 150 including two layers (for example, the first passivation layer 151 and a second passivation layer 152) is described as an example of the present disclosure. The second substrate 170, which is opposite to the first substrate 120 and covers the passivation layer 150, may be provided on the passivation layer 150. The second passivation layer 152 may include an organic layer, which is formed on the first passivation layer 151, and an inorganic layer which is formed on the organic layer. Also, the second passivation layer 152 may include three or more layers which include organic and inorganic layers.

[0069] As described above, the planarization layer 123 and the second bank 162, which are exposed at the non-display area, are protected by the anti-moisture unit 155, and thus, moisture permeation from the outside into the organic emission layer 148 of the OLED E, which is formed in the display area, through the planarization layer 123 or the second bank 162 is suppressed.

[0070] Moreover, the gate driver 200 including a transistor (for example, a driving transistor) covered by the planarization layer 123 may be provided in the non-display area. In this case, the gate driver 200 is protected by the anti-moisture unit 155.

[0071] In the non-display area, the gate driver 200 may be provided in a GIP type, and in addition, various elements may be provided. A plurality of thin film transistors may be provided in the gate driver 200 and the various elements. In this case, the gate driver 200 and the various elements may be covered by the planarization layer 123. Since the planarization layer 123 is protected by the anti-moisture unit 155, the gate driver 200 and the various elements are also protected by the anti-moisture unit 155. Therefore, moisture is suppressed from permeating into the gate driver 200 and the various elements, and thus, the lifetimes of the gate driver 200 and the various elements can be extended. Accordingly, the gate driver 200 and the various elements may be normally driven.

[0072] FIGS. 5A to 5F are exemplary diagrams for describing a method of manufacturing an organic light emitting display panel according to an exemplary embodiment of the present disclosure, and particularly, illustrate cross-sectional surfaces of the organic light emitting display panel in respective operations of the method of manufacturing the organic light emitting display panel according to an exemplary embodiment of the present disclosure.

[0073] Referring to FIGS. 5A to 5F, the method of manufacturing the organic light emitting display panel according to an exemplary embodiment of the present disclosure includes: forming the driving transistors Tdr on the first substrate 120; forming the planarization layer 123 which covers the driving transistors Tdr; forming the first bank 161, which is formed on the planarization layer 123 and in the display area where the driving transistors Tdr are formed and separates the plurality of pixels, and the second bank 162 which is formed on the planarization layer 123 and separates the display area and the non-display area which is disposed outside the display area; forming the anti-moisture unit 155 on the planarization layer 123 to cover the non-display area and the second bank 162; forming the plurality of OLEDs E which are respectively disposed in the plurality of pixels in the display area and emit light by the respective driving transistors Tdr; and forming a passivation layer 150, which is disposed on the anti-moisture unit 155 and the OLEDs E, and the second substrate 170 which covers the passivation layer 150.

[0074] Referring to FIG. 5A, the driving transistors Tdr respectively configuring the pixels may be formed on the first substrate 120. First, amorphous silicon or oxide semiconductor layer may be deposited on the first substrate 120. The amorphous silicon may be crystallized into polysilicon by irradiating a laser beam or performing thermal treatment. The semiconductor layer 130 may be formed by patterning the polysilicon.

[0075] Subsequently, the gate insulation layer 121 may be formed on the semiconductor layer 130 formed of the polysilicon. An inorganic insulating material such as oxide silicon (SiO_2) may be used as the gate insulation layer 121.

[0076] The gate 145 may be formed on the gate insulation layer 121. The gate 145 may be formed of a low-resistance metal material, for example, aluminum (Al), AlNd, copper (Cu), or a copper alloy. The gate 145 may be formed at a center portion of the semiconductor layer 130. The gate insulation layer 145 may be formed between the gate 145 and the semiconductor layer 130.

[0077] Subsequently, impurities (a triadic element or a pentad element) may be doped all over the first substrate 120. In this case, the gate 145 may be used as a blocking mask. Therefore, the impurities are prevented from being doped on a center area of the semiconductor layer 130 blocked by the gate 145. An area on which the impurities are not doped may be referred to as the first area 130a. The first area 130a may be formed of pure polysilicon. Also, except the first area 130a, an outer area of the semiconductor layer 130 on which the impurities are doped may be referred to as the second area 130b.

[0078] Finally, the interlay dielectric 122 may be

formed all over the first substrate 120 where the semiconductor layer 130 divided into the first and second areas 130a and 130b is formed. Subsequently, the interlayer dielectric 122 and the gate insulation layer 121 may be patterned simultaneously or in batches. At this time, an insulation layer contact hole 126 may be formed to expose the second area 130b.

[0079] The first driving electrode 141 and the second driving electrode 142, which contact the second area 130b through the insulation layer contact hole 126, may be formed on the interlayer dielectric 122.

[0080] Referring to FIG. 5B, the planarization layer 123 may be formed on the driving transistor Tdr. In this case, a contact hole 125 which exposes the first driving electrode 141 of the driving transistor Tdr may be provided on the planarization layer 123. The planarization layer 123 may be formed of, for example, an organic material such as polyimide, polyamide, acryl resin, BCB, or phenol resin. However, the present exemplary embodiment is not limited thereto.

[0081] Referring to FIG. 5C, a first electrode 147 connected to the first driving electrode 141 is formed on the planarization layer 123.

[0082] The first electrode 147 may act as an anode or a cathode depending on the type of the driving transistor Tdr. In FIG. 5C, the first electrode 147 may act as the anode of the OLED E and may be formed of a transparent conductive material (for example, indium-tin-oxide (ITO) or indium-zinc-oxide (IZO)) of which a work function value is large.

[0083] The first electrode 147 may be formed in all the pixels in common and may be patterned through a mask process.

[0084] The bank 163 is formed on the first electrode 147. As illustrated in FIG. 5C, the bank 163 is formed to surround each of the pixels and overlap an edge of the first electrode 147.

[0085] In this case, the bank 163 includes the first bank 161, which is formed on the planarization layer 123 and in the display area where the driving transistors Tdr are formed and divides the plurality of pixels, and the second bank 162 which is formed on the planarization layer 123 and separates the display area and the non-display area disposed outside the display area. In this case, the bank 163 may be formed of the same material as that of the planarization layer 123.

[0086] Referring to FIG. 5D, the anti-moisture unit 155 which covers the non-display area and the second bank 162 is formed on the planarization layer 123 on which the first bank 161 and the second bank 162 are formed. In this case, the anti-moisture unit 155 may cover all the side surface and plane of the planarization layer 123.

[0087] Moreover, as illustrated in FIG. 5D, the anti-moisture unit 155 does not cover an entire portion of the second bank 162 but covers only a portion of the second bank 162 corresponding to the non-display area. That is, the second bank 162 may be formed to overlap an edge of a first electrode 147 of the OLED E, and in this case, the anti-moisture unit 155 may not be formed on a portion of the second bank 162 overlapping the edge of the first electrode 147. As described above, the anti-moisture unit 155 is formed to be separated from, by a certain distance, the organic emission layer 148 of the OLED E which is formed later. Therefore, moisture is blocked without affecting an emission area of the OLED E.

[0088] In this case, the anti-moisture unit 155 may be formed of an inorganic thin layer.

[0089] Referring to FIG. 5E, the organic emission layer 148 is formed on the first electrode 147, and the second electrode 149 is formed on the organic emission layer 148 and the bank 163.

[0090] The organic emission layer 148 may be formed to have a structure of a hole transport layer/emission layer/electron transport layer or a structure of a hole injection layer/hole transport layer/emission layer/electron transport layer/electron injection layer. Furthermore, the organic emission layer 148 may further include a function layer for enhancing emission efficiency and/or a lifetime of the organic emission layer 148.

[0091] The second electrode 149 formed on the organic emission layer 148 may act as a cathode electrode when the first electrode 147 acts as an anode electrode.

[0092] In this case, as illustrated in FIG. 5E, the second electrode 149 is formed to overlap an edge of the anti-moisture unit 155. That is, the anti-moisture unit 155 may overlap an outermost portion of the second electrode 149 of the OLED E. As described above, moisture is more effectively blocked by minimizing an interval between the anti-moisture unit 155 and the second electrode 149. For example, the second electrode 149 may be formed to overlap an upper end of the anti-moisture unit 155, and thus, the permeation of moisture is more effectively prevented. The anti-moisture unit 155 is good in adhesiveness to the second bank 162 and the second electrode (a cathode) 149.

[0093] Moreover, the anti-moisture unit 155 is separated from the organic emission layer 148 of the OLED E by a certain distance. Accordingly, moisture is blocked without affecting the emission area of the OLED E.

[0094] The OLED E includes the first electrode 147, the organic emission layer 148, and the second electrode 149. The OLED E may emit light by the driving transistor Tdr which is formed in each of the pixels.

[0095] Referring to FIG. 5F, the passivation layer 150 may be formed on the anti-moisture unit 155 and the OLED E, and the second substrate 170 may be provided on the passivation layer 150.

[0096] The passivation layer 150 formed on the anti-moisture unit 155 may include one or more layers including the first passivation layer 151. In an exemplary embodiment, the passivation layer 150 including the two layers (for example, the first passivation layer 151 and the second passivation layer 152) is described as an example of the present disclosure.

[0097] The first passivation layer 151 may be formed on the anti-moisture unit 155 and the OLED E. The first

passivation layer 151 may be formed of the same material as that of the anti-moisture unit 155. The second passivation layer 152 may be formed on the first passivation layer 151. The second substrate 170, which is opposite to the first substrate 120 and covers the passivation layer 150, may be provided on the passivation layer 150. In this case, the second substrate 170 may be provided in a film and thin film encapsulation type. That is, the second substrate 170 may be adhered to the second passivation layer 152 in a film type, and in this case, the second substrate 170 may be deposited as a thin layer and may be formed on the second passivation layer 152.

[0098] The passivation layer 150 and the second substrate 170 protect the OLEDs E and the transistors (for example, the driving transistors) from an external impact.

[0099] In this case, the anti-moisture unit 155 protects the OLEDs E and the transistors (for example, the driving transistors) from moisture which permeates from an outermost portion of the planarization layer 123 and the second bank 162.

[0100] Moreover, since the anti-moisture unit 155 is formed, a plurality of lines which are formed in an outermost area of the organic light emitting display panel are protected.

[0101] Hereinabove, the anti-moisture unit may be applied to all organic light emitting display apparatuses which are driven in a top emission type or a bottom emission type.

[0102] Moreover, in a thin film transistor, the anti-moisture unit may be applied to a top gate type and a bottom gate type.

[0103] Moreover, the anti-moisture unit may be applied to all thin film transistor substrates using amorphous silicon, polysilicon, oxide, an organic material, etc.

[0104] Moreover, the present disclosure may be applied to general organic light emitting display apparatuses, and particularly, may be applied to organic light emitting display apparatuses where a narrow bezel is realized.

[0105] As described above, according to the exemplary embodiments of the present disclosure, since the anti-moisture unit is formed on the planarization layer to cover the non-display area and the second bank, moisture is prevented from penetrating into an OLED through the bank (i.e., the second bank) and the planarization layer which are disposed at an outermost portion of the organic light emitting display panel.

[0106] Moreover, according to the exemplary embodiments of the present disclosure, an organic light emitting display apparatus including a stable narrow bezel is implemented.

[0107] Moreover, according to the exemplary embodiments of the present disclosure, the plurality of lines which are disposed at the outermost portion of the organic light emitting display panel are protected.

[0108] Moreover, according to the exemplary embodiments of the present disclosure, since the anti-moisture unit is provided, a lifetime of the organic light emitting display panel extends.

[0109] The exemplary embodiments of the present invention can also be described as follows: an apparatus comprising a first electrode on a planarization layer, an organic emission layer on the first electrode, a first bank and a second bank on the planarization layer and configured to surround the organic emission layer and an anti-moisture unit on a portion of the planarization layer and on a portion of the second bank, a second electrode on the organic emission layer, the first bank and the second bank and a portion of the anti-moisture unit, wherein the portion of the anti-moisture unit is interposed between the portion of the second bank and the second electrode, wherein the anti-moisture unit is configured to suppress moisture permeation through the second bank and the planarization layer, wherein the first bank is disposed at a display area and the second bank is disposed at a bezel of a non-display area, wherein the anti-moisture unit covers only a first portion of a second bank corresponding to the non-display area such that it is separated from the organic emission layer.

[0110] A first portion of the second bank is covered with the anti-moisture unit, a second portion of the second bank is covered with the second electrode, and a third portion of the second bank is covered with the organic emission layer. The first bank is at a display area and the second bank is at a non-display area. The anti-moisture unit is configured to cover a side surface and a plane of the planarization layer exposed at the non-display area. The anti-moisture unit is formed of an inorganic material, wherein the planarization layer, the first bank and the second bank are formed of an organic material. A gate driver at the non-display area, wherein the gate driver is a gate-in-panel type and the planarization layer is extended to cover the gate driver. A passivation layer is placed on the anti-moisture unit and on the second electrode. The passivation layer comprises at least one passivation layer, wherein a first passivation layer among the at least one passivation layer is formed of the same material as that of the anti-moisture unit, wherein the first passivation layer is directly contacting the anti-moisture unit.

[0111] An organic light emitting display panel comprising a planarization layer configured to cover a plurality of driving transistors, a first bank on the planarization layer and in a display area having the plurality of driving transistors, and configured to separate a plurality of pixels, a second bank on the planarization layer and configured to separate the display area and a non-display area, an anti-moisture unit on the planarization layer and covering the non-display area and the second bank and a plurality of organic light emitting diodes (OLEDs) respectively in the plurality of pixels.

[0112] The anti-moisture unit is formed of an inorganic thin layer. A passivation layer, wherein the passivation layer on the anti-moisture unit comprises a first passivation layer on the anti-moisture unit and one or more layers on the first passivation layer, and the first passivation

layer is of the same material as a material of the anti-moisture unit. The anti-moisture unit covers a side surface and a plane of the planarization layer exposed at the non-display area. The gate driver including a plurality of transistors covered by the planarization layer is provided in the non-display area and is protected by the anti-moisture unit. The anti-moisture unit covers a region of the second bank corresponding to the non-display area and overlaps a cathode of the OLEDs.

Claims

1. An apparatus comprising:

a first electrode (147) on a planarization layer (123);
an organic emission layer (148) on the first electrode;
a first bank (161) and a second bank (162) on the planarization layer (123) and configured to surround the organic emission layer (148); and
an anti-moisture unit (155) on a portion of the planarization layer (123) and on a portion of the second bank (162),
a second electrode (149) on the organic emission layer (148), the first bank (161), the second bank (162) and a portion of the anti-moisture unit (155),
wherein the anti-moisture unit (155) is configured to suppress moisture permeation through the second bank (162) and the planarization layer (123),
wherein the first bank (161) is disposed at a display area and the second bank (162) is disposed at a bezel of a non-display area, the second bank (162) separating the display area and the non-display area,
wherein the anti-moisture unit (155) covers only a first portion of the second bank (162) corresponding to the non-display area such that it is separated from the organic emission layer (148),

characterized in that the portion of the anti-moisture unit (155) is interposed between the portion of the second bank (162) and the second electrode (149).

2. The apparatus of claim 1, wherein the second electrode is configured to seal the organic emission layer with an overlapping portion of the anti-moisture unit with the second electrode.

3. The apparatus of claim 1 or 2, wherein a second portion of the second bank (162) is covered with the second electrode (149), and a third portion of the second bank (162) is covered with the organic emission layer (148).

4. The apparatus of claim 3, wherein the anti-moisture unit (155) is configured to cover a side surface and a plane of the planarization layer (123) exposed at the non-display area.

5. The apparatus of claim 4, wherein the anti-moisture unit (155) is formed of an inorganic material, wherein the planarization layer (123), the first bank (161) and the second bank (162) are formed of an organic material.

6. The apparatus of claim 4 or 5, further comprising a gate driver (200) at the non-display area, wherein the gate driver (200) is a gate-in-panel type and the planarization layer (123) is extended to cover the gate driver.

7. The apparatus of claim 6, further comprising a passivation layer (150) on the anti-moisture unit (155) and on the second electrode (149).

8. The apparatus of claim 7, wherein the passivation layer (150) comprises at least one passivation layer, wherein a first passivation layer (151) among the at least one passivation layer is formed of the same material as that of the anti-moisture unit (155), wherein the first passivation layer (151) is directly contacting the anti-moisture unit (155).

9. An organic light emitting display panel (100) comprising an apparatus according to claim 1, wherein:

the planarization layer (123) is configured to cover a plurality of driving transistors (Tdr);
the first bank (161) on the planarization layer (123) is in a display area having the plurality of driving transistors (Tdr), and configured to separate a plurality of pixels (P);
the second bank (162) on the planarization layer (123) is configured to separate the display area and a non-display area;
the anti-moisture unit (155) on the portion of the planarization layer (123) and on the portion of the second bank (162) covers the non-display area; and
a plurality of organic light emitting diodes (OLEDs) are respectively in the plurality of pixels (P).

10. The organic light emitting display panel of claim 9, wherein the anti-moisture unit (155) is formed of an inorganic thin layer.

11. The organic light emitting display panel of claim 10, further comprising a passivation layer (150), wherein the passivation layer (150) on the anti-moisture unit

comprises a first passivation layer (151) on the anti-moisture unit (155) and one or more layers on the first passivation layer (151), and the first passivation layer (151) is of the same material as a material of the anti-moisture unit (155).

12. The organic light emitting display panel of any one of claims 9 to 11, wherein the anti-moisture unit (155) covers a side surface and a plane of the planarization layer (123) exposed at the non-display area.

13. The organic light emitting display panel of any one of claims 9 to 12, wherein a gate driver (200) including the plurality of driving transistors (Tdr) covered by the planarization layer (123) is provided in the non-display area and is protected by the anti-moisture unit (155).

14. The organic light emitting display panel of any one of claims 9 to 13, wherein the anti-moisture unit (155) covers a region of the second bank (162) corresponding to the non-display area and overlaps a cathode of the OLEDs.

Patentansprüche

1. Eine Vorrichtung, aufweisend:

eine erste Elektrode (147) auf einer Planarisierungsschicht (123);
eine organische Emissionsschicht (148) auf der ersten Elektrode;
einen ersten Damm (161) und einen zweiten Damm (162) auf der Planarisierungsschicht (123) und konfiguriert, die organische Emissionsschicht (148) zu umgeben; und
eine Anti-Feuchtigkeitseinheit (155) auf einem Teilbereich der Planarisierungsschicht (123) und auf einem Teilbereich des zweiten Damms (162),
eine zweite Elektrode (149) auf der organischen Emissionsschicht (148), dem ersten Damm (161), dem zweiten Damm (162) und einem Teilbereich der Anti-Feuchtigkeitseinheit (155),
wobei die Anti-Feuchtigkeitseinheit (155) konfiguriert ist, Feuchtigkeitsdurchdringung durch den zweiten Damm (162) und die Planarisierungsschicht (123) zu unterdrücken,
wobei der erste Damm (161) in einem Anzeigegebiet angeordnet ist und der zweite Damm (162) an einer Einfassung eines Nicht-Anzeigegebiets angeordnet ist, wobei der zweite Damm (162) das Anzeigegebiet und das Nicht-Anzeigegebiet trennt,
wobei die Anti-Feuchtigkeitseinheit (155) nur einen ersten Teilbereich des zweiten Damms (162), der zu dem Nicht-Anzeigegebiet korrespondiert, so bedeckt, dass er von der organischen Emissionsschicht (148) getrennt ist,

dadurch gekennzeichnet, dass der Teilbereich der Anti-Feuchtigkeitseinheit (155) zwischen den Teilbereich des zweiten Damms (162) und die zweite Elektrode (149) eingefügt ist.

2. Die Vorrichtung gemäß Anspruch 1, wobei die zweite Elektrode konfiguriert ist, die organische Emissionsschicht mit einem überlappenden Teilbereich der Anti-Feuchtigkeitseinheit mit der zweiten Elektrode zu versiegeln.

3. Die Vorrichtung gemäß Anspruch 1 oder 2, wobei ein zweiter Teilbereich des zweiten Damms (162) mit der zweiten Elektrode (149) bedeckt ist und ein dritter Teilbereich des zweiten Damms (162) mit der organischen Emissionsschicht (148) bedeckt ist.

4. Die Vorrichtung gemäß Anspruch 3, wobei die Anti-Feuchtigkeitseinheit (155) konfiguriert ist, eine Seitenfläche und eine Ebene der Planarisierungsschicht (123), die in dem Nicht-Anzeigegebiet freiliegt, zu bedecken.

5. Die Vorrichtung gemäß Anspruch 4, wobei die Anti-Feuchtigkeitseinheit (155) aus einem anorganischen Material ausgebildet ist, wobei die Planarisierungsschicht (123), der erste Damm (161) und der zweite Damm (162) aus einem organischen Material ausgebildet sind.

6. Die Vorrichtung gemäß Anspruch 4 oder 5, ferner einen Gate-Treiber (200) in dem Nicht-Anzeigegebiet aufweisend, wobei der Gate-Treiber (200) ein Gate-in-Panel-Typ ist und die Planarisierungsschicht (123) so ausgedehnt ist, dass der Gate-Treiber bedeckt ist.

7. Die Vorrichtung gemäß Anspruch 6, ferner eine Passivierungsschicht (150) auf der Anti-Feuchtigkeitseinheit (155) und auf der zweiten Elektrode (149) aufweisend.

8. Die Vorrichtung gemäß Anspruch 7, wobei die Passivierungsschicht (150) mindestens eine Passivierungsschicht aufweist, wobei eine erste Passivierungsschicht (151) unter der mindestens einen Passivierungsschicht aus dem gleichen Material wie das der Anti-Feuchtigkeitseinheit (155) ausgebildet ist, wobei die erste Passivierungsschicht (151) direkt die Anti-Feuchtigkeitseinheit (155) kontaktiert.

9. Ein organisches lichtemittierendes Anzeige-Panel (100), eine Vorrichtung gemäß Anspruch 1 aufweisend, wobei:

die Planarisierungsschicht (123) konfiguriert ist, eine Vielzahl von Treibertransistoren (Tdr) zu bedecken;
der erste Damm (161) auf der Planarisierungsschicht (123) in einem Anzeigegebiet ist, das die Vielzahl von Treibertransistoren (Tdr) hat, und konfiguriert ist, eine Vielzahl von Pixeln (P) zu trennen;
der zweite Damm (162) auf der Planarisierungsschicht (123) konfiguriert ist, das Anzeigegebiet und ein Nicht-Anzeigegebiet zu trennen;
die Anti-Feuchtigkeitseinheit (155) auf dem Teilbereich der Planarisierungsschicht (123) und auf dem Teilbereich des zweiten Damms (162) das Nicht-Anzeigegebiet bedeckt; und
eine Vielzahl von organischen lichtemittierenden Dioden (OLEDs) jeweils in der Vielzahl von Pixeln (P) sind.

10. Das organische lichtemittierende Anzeige-Panel gemäß Anspruch 9, wobei die Anti-Feuchtigkeitseinheit (155) aus einer anorganischen Dünnschicht ausgebildet ist.

11. Das organische lichtemittierende Anzeige-Panel gemäß Anspruch 10, ferner eine Passivierungsschicht (150) aufweisend, wobei die Passavierungsschicht (150) auf der Anti-Feuchtigkeitseinheit eine erste Passivierungsschicht (151) auf der Anti-Feuchtigkeitseinheit (155) und eine oder mehr Schichten auf der ersten Passivierungsschicht (151) aufweist und die erste Passivierungsschicht (151) aus dem gleichen Material ist wie ein Material der Anti-Feuchtigkeitseinheit (155).

12. Das organische lichtemittierende Anzeige-Panel gemäß einem der Ansprüche 9 bis 11, wobei die Anti-Feuchtigkeitseinheit (155) eine Seitenfläche und eine Ebene der Planarisierungsschicht (123), die in dem Nicht-Anzeigegebiet freiliegt, bedeckt.

13. Das organische lichtemittierende Anzeige-Panel gemäß einem der Ansprüche 9 bis 12, wobei ein Gate-Treiber (200), der die durch die Planarisierungsschicht (123) bedeckte Vielzahl von Treibertransistoren (Tdr) enthält, in dem Nicht-Anzeigegebiet bereitgestellt ist und durch die Anti-Feuchtigkeitseinheit (155) geschützt ist.

14. Das organische lichtemittierende Anzeige-Panel gemäß einem der Ansprüche 9 bis 13, wobei die Anti-Feuchtigkeitseinheit (155) einen zu dem Nicht-Anzeigegebiet korrespondierenden Bereich des zweiten Damms (162) bedeckt und eine Kathode der OLEDs überlappt.

Revendications

1. Appareil comprenant:

une première électrode (147) sur une couche de planarisation (123) ;
une couche d'émission organique (148) sur la première électrode ;
un premier banc (161) et un second banc (162) sur la couche de planarisation (123) et configurés pour entourer la couche d'émission organique (148) ; et
une unité anti-humidité (155) sur une partie de la couche de planarisation (123) et sur une partie du second banc (162),
une seconde électrode (149) sur la couche d'émission organique (148), le premier banc (161), le second banc (162) et une partie de l'unité anti-humidité (155),
dans lequel l'unité anti-humidité (155) est configurée pour supprimer la perméation à l'humidité par le biais du second banc (162) et de la couche de planarisation (123),
dans lequel le premier banc (161) est disposé au niveau d'une zone d'affichage et le second banc (162) est disposé au niveau d'une facette d'une zone de non-affichage, le second banc (162) séparant la zone d'affichage et la zone de non-affichage,
dans lequel l'unité anti-humidité (155) recouvre uniquement une première partie du second banc (162) qui correspond à la zone de non-affichage de sorte qu'elle soit séparée de la couche d'émission organique (148),
caractérisé en ce que la partie de l'unité anti-humidité (155) est interposée entre la partie du second banc (162) et la seconde électrode (149).

2. Appareil selon la revendication 1, dans lequel la seconde électrode est configurée pour fermer la couche d'émission organique avec une partie de chevauchement de l'unité anti-humidité avec la seconde électrode.

3. Appareil selon la revendication 1 ou 2, dans lequel une seconde partie du second banc (162) est recouverte par la seconde électrode (149), et une troisième partie du second banc (162) est recouverte par la couche d'émission organique (148).

4. Appareil selon la revendication 3, dans lequel l'unité anti-humidité (155) est configurée pour recouvrir une surface latérale et un plan de la couche de planarisation (123) exposé au niveau de la zone de non-affichage.

5. Appareil selon la revendication 4, dans lequel l'unité

anti-humidité (155) est formée d'un matériau inorganique, dans lequel la couche de planarisation (123), le premier banc (161) et le second banc (162) sont formés d'un matériau organique.

6. Appareil selon la revendication 4 ou 5, comprenant en outre un excitateur de grille (200) au niveau de la zone de non-affichage, dans lequel l'excitateur de grille (200) est de type « grille dans un panneau » et la couche de planarisation (123) s'étend afin de recouvrir l'excitateur de grille.

7. Appareil selon la revendication 6, comprenant en outre une couche de passivation (150) sur l'unité anti-humidité (155) et sur la seconde électrode (149).

8. Appareil selon la revendication 7, dans lequel la couche de passivation (150) comprend au moins une couche de passivation, dans lequel une première couche de passivation (151) parmi l'au moins une couche de passivation est formée du même matériau que celui de l'unité anti-humidité (155), dans lequel la première couche de passivation (151) est directement en contact avec l'unité anti-humidité (155).

9. Panneau d'affichage électroluminescent organique (100) comprenant un appareil selon la revendication 1, dans lequel :

la couche de planarisation (123) est configurée pour recouvrir une pluralité de transistors d'excitation (Tdr) ;
le premier banc (161) sur la couche de planarisation (123) se trouve dans une zone d'affichage qui possède la pluralité de transistors d'excitation (Tdr), et est configuré pour séparer une pluralité de pixels (P) ;
le second banc (162) sur la couche de planarisation (123) est configuré pour séparer la zone d'affichage et une zone de non-affichage ;
l'unité anti-humidité (155) sur la partie de la couche de planarisation (123) et sur la partie du second banc (162) recouvre la zone de non-affichage ; et
une pluralité de diodes électroluminescentes organiques (OLED) se trouve respectivement dans la pluralité de pixels (P).

10. Panneau d'affichage électroluminescent organique selon la revendication 9, dans lequel l'unité anti-humidité (155) est formée d'une couche inorganique fine.

11. Panneau d'affichage électroluminescent organique selon la revendication 10, comprenant en outre une couche de passivation (150), la couche de passivation (150) sur l'unité anti-humidité comprenant une première couche de passivation (151) sur l'unité anti-humidité (155) et une ou plusieurs couche(s) sur la première couche de passivation (151), et la première couche de passivation (151) étant du même matériau qu'un matériau de l'unité anti-humidité (155).

12. Panneau d'affichage électroluminescent organique selon l'une quelconque des revendications 9 à 11, dans lequel l'unité anti-humidité (155) recouvre une surface latérale et un plan de la couche de planarisation (123) exposé au niveau de la zone de non-affichage.

13. Panneau d'affichage électroluminescent organique selon l'une quelconque des revendications 9 à 12, dans lequel un excitateur de grille (200) comprenant la pluralité de transistors d'excitation (Tdr) recouverts par la couche de planarisation (123) est prévu dans la zone de non-affichage et est protégé par l'unité anti-humidité (155).

14. Panneau d'affichage électroluminescent organique selon l'une quelconque des revendications 9 à 13, dans lequel l'unité anti-humidité (155) recouvre une région du second banc (162) qui correspond à la zone de non-affichage, et chevauche une cathode des OLED.

FIG. 1
(RELATED ART)

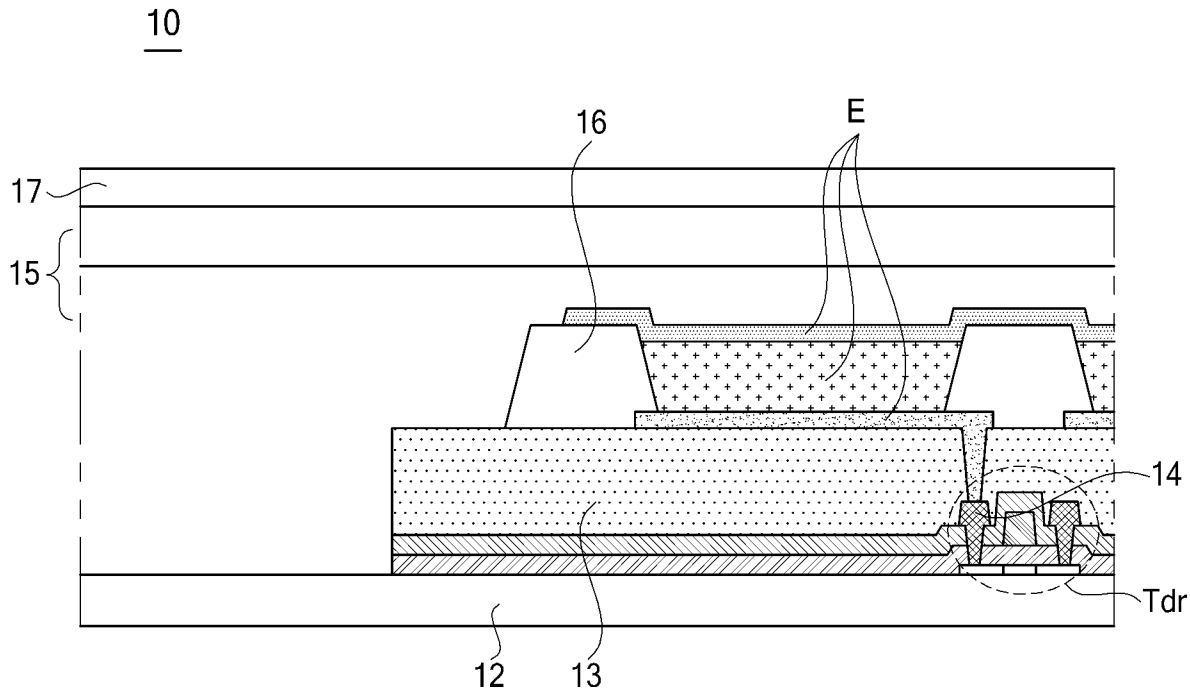


FIG. 2A
(RELATED ART)

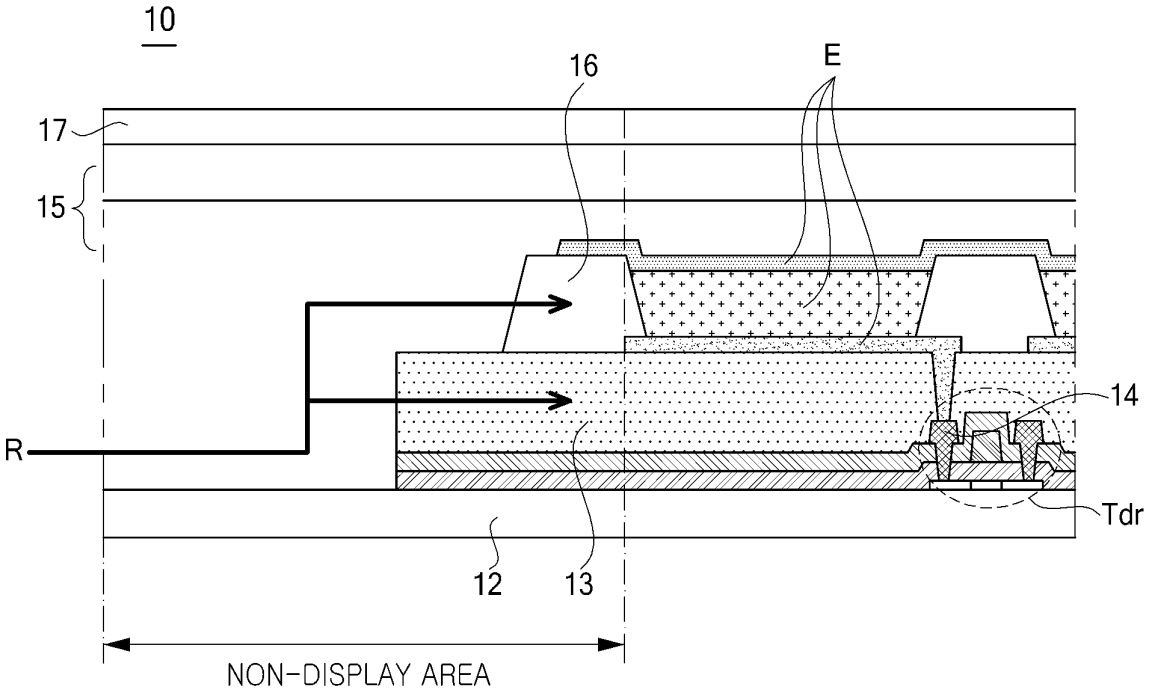


FIG. 2B
(RELATED ART)

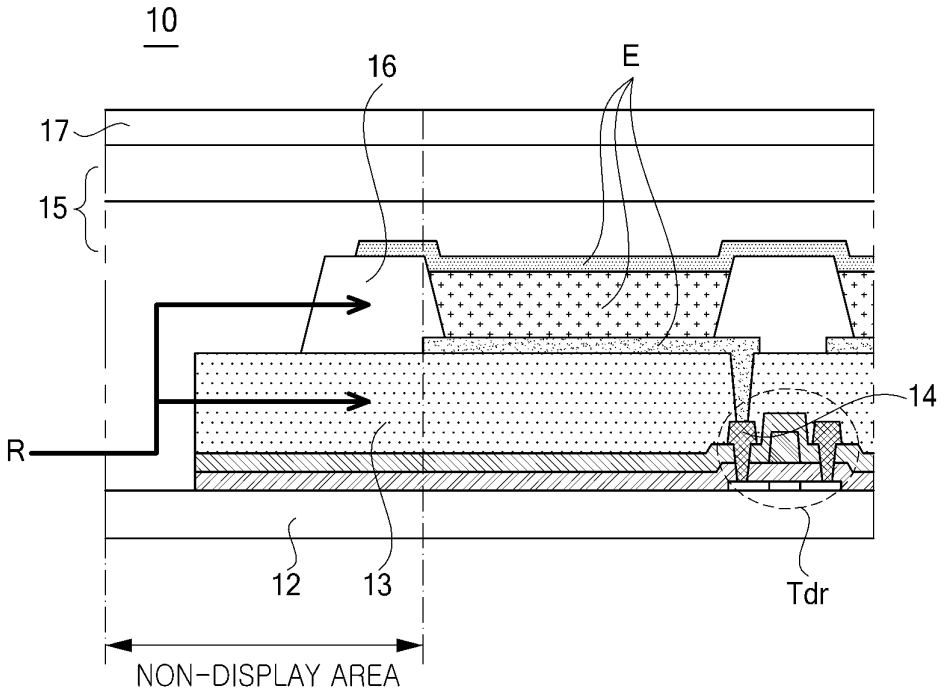


FIG. 3

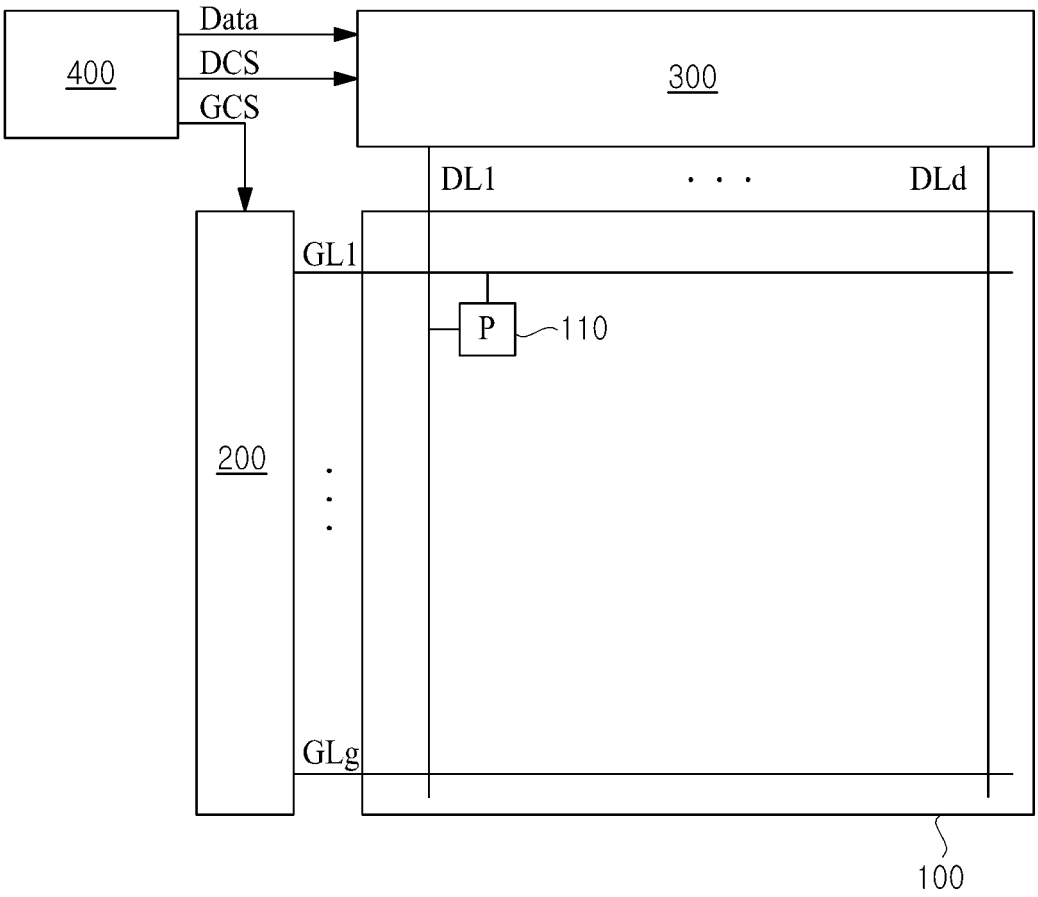


FIG. 4

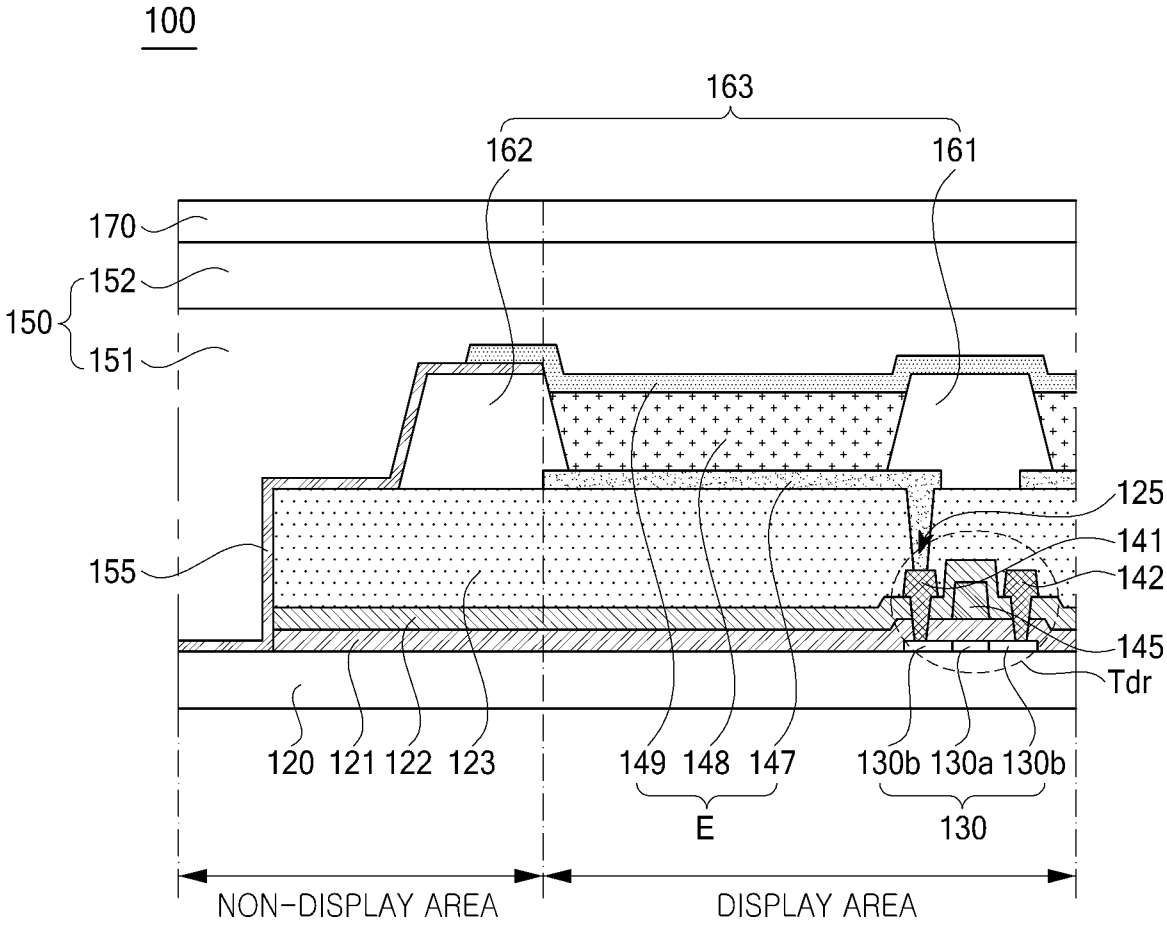

100
163
162
161
170
152
150
151
155
125
141
142
145
Tdr
120
121
122
123
149
148
147
130b
130a
130b
E
130
NON-DISPLAY AREA
DISPLAY AREA

FIG. 5A

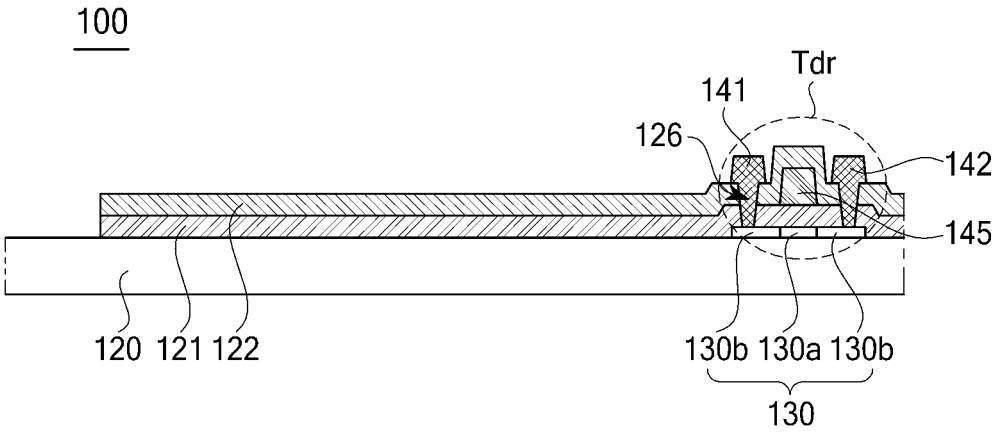

100
Tdr
141
126
142
145
120
121
122
130b
130a
130b
130

FIG. 5B

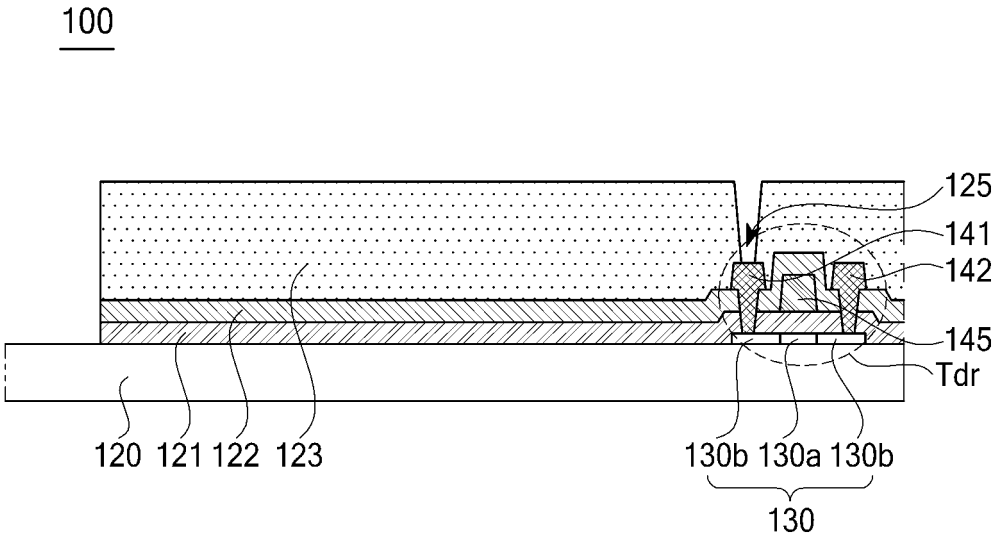

100
125
141
142
145
Tdr
120
121
122
123
130b
130a
130b
130

FIG. 5C

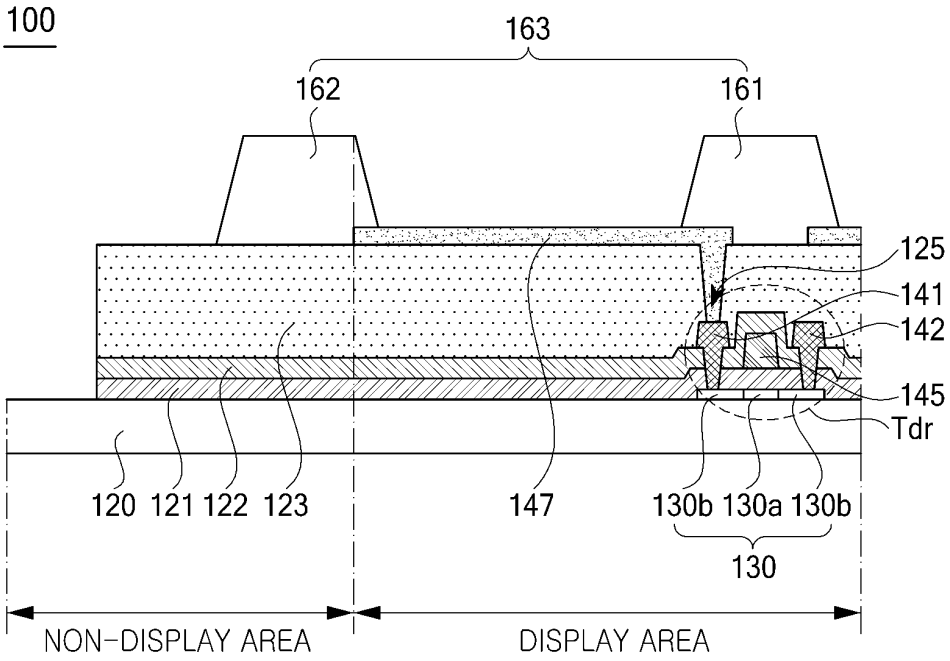

100
163
162
161
125
141
142
145
Tdr
120
121
122
123
147
130b
130a
130b
130
NON-DISPLAY AREA
DISPLAY AREA

FIG. 5D

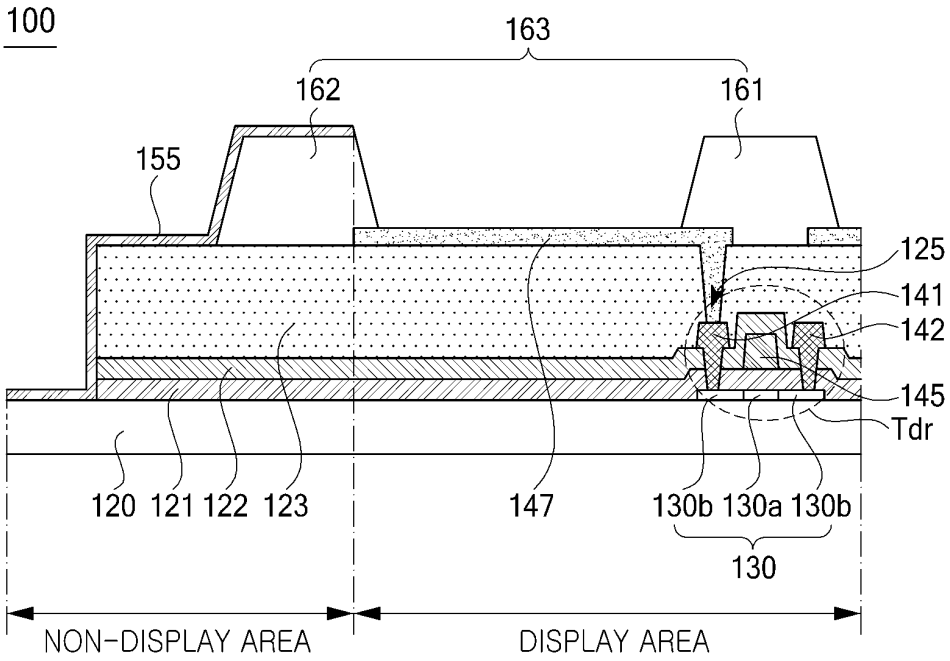

100
163
162
161
155
125
141
142
145
Tdr
120
121
122
123
147
130b
130a
130b
130
NON-DISPLAY AREA
DISPLAY AREA

FIG. 5E

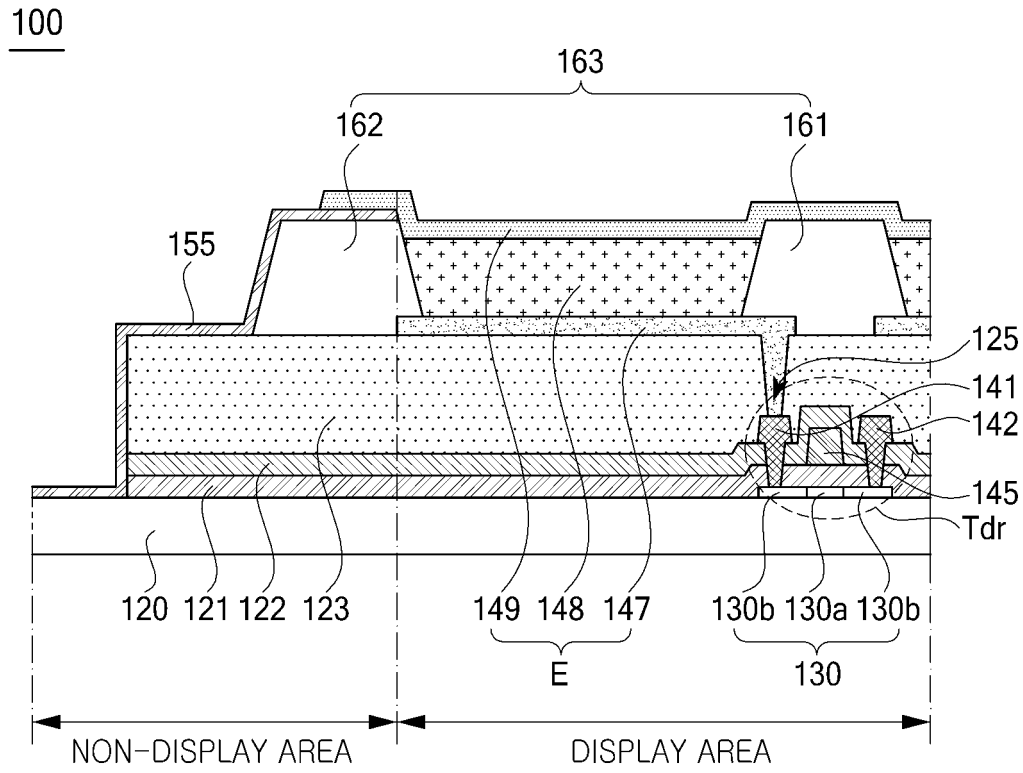
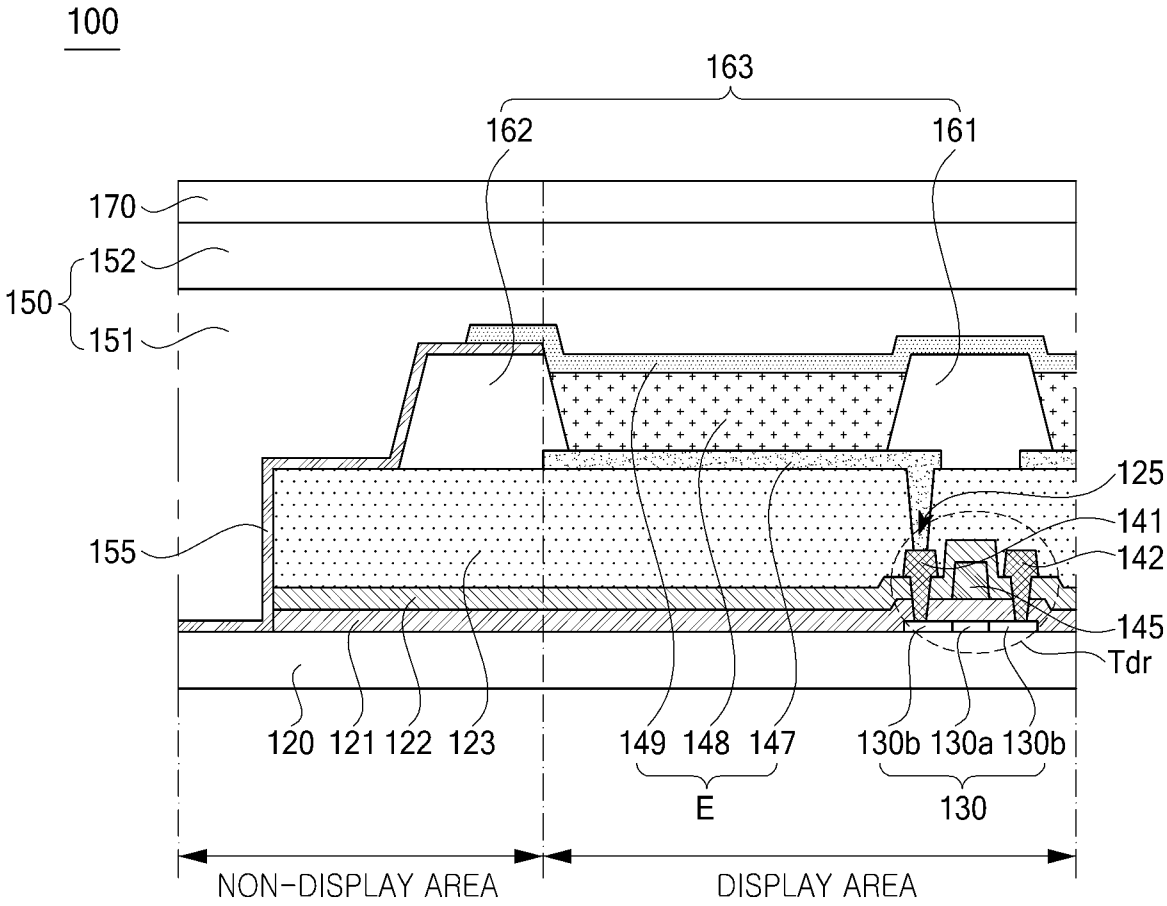

100
163
162
161
155
125
141
142
145
Tdr
120
121
122
123
149
148
147
130b
130a
130b
E
130
NON-DISPLAY AREA
DISPLAY AREA

FIG. 5F


100
163
162
161
170
152
150
151
155
125
141
142
145
Tdr
120
121
122
123
149
148
147
130b
130a
130b
E
130
NON-DISPLAY AREA
DISPLAY AREA

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- US 2010171138 A1 **[0018]**
- US 2003201443 A1 **[0019]**
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专利名称(译)	有机发光显示面板及其制造方法		
公开(公告)号	EP2950364B1	公开(公告)日	2019-03-27
申请号	EP2015169154	申请日	2015-05-26
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IPC分类号	H01L51/52 H01L27/32		
CPC分类号	H01L27/3244 H01L51/5246 H01L51/5253 H01L27/3246 H01L27/3258 H01L51/5237 H01L51/5221 H01L51/524		
优先权	1020140063963 2014-05-27 KR		
其他公开文献	EP2950364A1		
外部链接	Espacenet		

摘要(译)

一种装置，包括平坦化层（123）上的第一电极（147），第一电极上的有机发光层（148），平坦化层（123）上的第一堤岸（161）和第二堤岸（162）以及被配置为在平坦化层（123）的一部分和第二隔堤（162）的一部分上围绕有机发射层（148）和防潮单元（155），其中防潮单元（155）是配置为通过所述第二组（162）和平坦化层（123）以抑制湿气渗透。

FIG. 1
(RELATED ART)