



(51) International Patent Classification:
H01L 27/32 (2006.01) *G09G 3/00* (2006.01)
G01R 31/28 (2006.01)

[US/US]; c/o 343 State Street, Rochester, NY 14650 (US).

(21) International Application Number:
PCT/US2010/044085

(74) Agents: **GOODELL, Robert, J.** et al.; Morgan, Lewis & Bockius LLP, 1111 Pennsylvania Avenue, NW, Washington, DC 20004 (US).

(22) International Filing Date:
2 August 2010 (02.08.2010)

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
12/544,286 20 August 2009 (20.08.2009) US

(71) Applicant (*for all designated States except US*): **GLOBAL OLED TECHNOLOGY LLC** [US/US]; 1209 Orange Street, Wilmington, DE 19801 (US).

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **COK, Ronald, S.** [US/US]; c/o 343 State Street, Rochester, NY 14650 (US). **HAMER, John, W.** [CA/US]; c/o 343 State Street, Rochester, NY 14650 (US). **MATTERN, Michael, W.**

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU,

[Continued on next page]

(54) Title: OPTICALLY TESTING CHIPLETS IN DISPLAY DEVICE

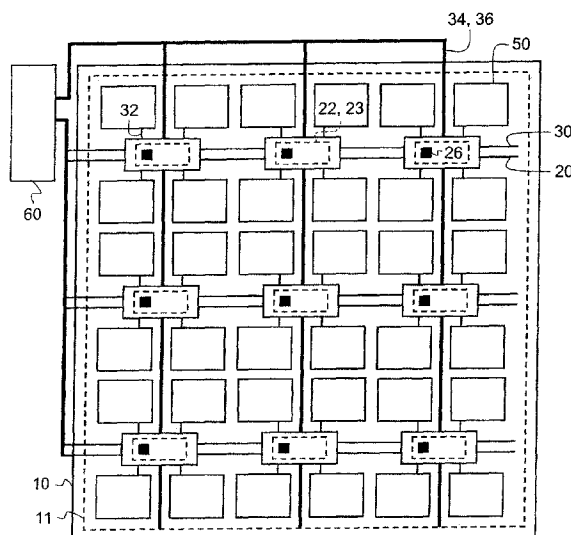


FIG. 1

(57) Abstract: A method of making a display includes providing a display substrate having a plurality of control electrodes in a display area; locating a plurality of chiplets responsive to a controller to provide current to the control electrodes, each duplet having a separate substrate, at least one pixel connection pad electrically connected to a control electrode, and one or more test light emitters formed in the chiplet responsive to the current provided on the control electrodes to emit light; controlling the chiplets to pass current through one or more of the test light emitters formed in the chiplet to emit light; detecting the light emitted by the test light emitters to determine faulty chiplets or chiplet interconnections; replacing or repairing the faulty chiplets or chiplet interconnections; and forming an organic light emitting diode over the substrate in the display area connected to the control electrodes.



LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, **Published:**

SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, — *with international search report (Art. 21(3))*
GW, ML, MR, NE, SN, TD, TG).

OPTICALLY TESTING CHIPLETS IN DISPLAY DEVICE

CROSS REFERENCE TO RELATED APPLICATION

Reference is made to commonly-assigned U.S. Patent Application
5 Serial No. 12/191,478 filed August 14, 2008, entitled "OLED Device With Embedded Chip Driving" by Dustin L. Winters et al, the disclosure of which is incorporated herein..

FIELD OF THE INVENTION

The present invention relates to display devices having a substrate
10 with distributed, independent chiplet control elements and optically testing such chiplets.

BACKGROUND OF THE INVENTION

Flat-panel display devices are widely used in conjunction with computing devices, in portable devices, and for entertainment devices such as
15 televisions. Such displays typically employ a plurality of pixels distributed over a substrate to display images. Each pixel incorporates several, differently colored light-emitting elements commonly referred to as sub-pixels, typically emitting red, green, and blue light, to represent each image element. Pixels and sub-pixels are not distinguished herein; all light-emitting elements are called pixels. A variety
20 of flat-panel display technologies are known, for example plasma displays, liquid crystal displays, and light-emitting diode displays. Active-matrix elements are not necessarily limited to displays and can be distributed over a substrate and employed in other applications requiring spatially distributed control.

Light-emitting diodes (LEDs) incorporating thin films of light-emitting materials forming light-emitting elements have many advantages in a
25 flat-panel display device and are useful in optical systems. U.S. Patent No. 6,384,529 to Tang et al. shows an organic LED color display that includes an array of organic LED light-emitting elements. Alternatively, inorganic materials can be employed and can include phosphorescent crystals or quantum dots in a
30 polycrystalline semiconductor matrix. Other thin films of organic or inorganic materials can also be employed to control charge injection, transport, or blocking to the light-emitting-thin-film materials, and are known in the art. The materials

are placed upon a substrate between electrodes, with an encapsulating cover layer or plate. Light is emitted from a pixel when current passes through the light-emitting material. The frequency of the emitted light is dependent on the nature of the material used. In such a display, light can be emitted through the substrate (a bottom emitter) or through the encapsulating cover (a top emitter), or both.

LED devices can include a patterned light-emissive layer wherein different materials are employed in the pattern to emit different colors of light when current passes through the materials. Alternatively, one can employ a single emissive layer, for example, a white-light emitter, together with color filters for forming a full-color display, as is taught in U.S. Patent No. 6,987,355 by Cok. It is also known to employ a white sub-pixel that does not include a color filter, for example, as taught in U.S. Patent No. 6,919,681 by Cok et al. A design employing an unpatterned white emitter has been proposed together with a four-color pixel including red, green, and blue color filters and sub-pixels and an unfiltered white sub-pixel to improve the efficiency of the device (see, e.g. U.S. Patent No. 7,230,594 to Miller, et al).

Two different methods for controlling the pixels in a flat-panel display device are generally known: active-matrix control and passive-matrix control. In an active-matrix device, control elements are distributed over the flat-panel substrate. Typically, each sub-pixel is controlled by one control element and each control element includes at least one transistor. For example, in a simple active-matrix organic light-emitting (OLED) display, each control element includes two transistors (a select transistor and a power transistor) and one capacitor for storing a charge specifying the brightness of the sub-pixel. Each light-emitting element typically employs an independent control electrode and a common electrode.

Prior-art active-matrix control elements typically include thin-film semiconductor materials, such as silicon, formed into transistors and capacitors through photolithographic processes. The thin-film silicon can be either amorphous or polycrystalline. Thin-film transistors made from amorphous or polycrystalline silicon are relatively larger and have lower performance than conventional transistors made from crystalline silicon wafers. Moreover, such

thin-film devices typically exhibit local or large-area non-uniformity that results in perceptible non-uniformity in a display employing such materials. While improvements in manufacturing and materials processes are made, the manufacturing processes are expensive and thin-film device performance
5 continues to be lower than the performance of crystalline silicon devices.

Matsumura et al discuss crystalline silicon substrates used with LCD displays in U.S. Patent Application Publication No. 2006/0055864. Matsumura describes a method for selectively transferring and affixing pixel-control devices made from first semiconductor substrates onto a second planar
10 display substrate. Wiring interconnections within the pixel-control device and connections from busses and control electrodes to the pixel-control device are shown. However, there is no teaching of improving the aperture ratio of a display, reducing the cost of such pixel-control devices in cooperation with a display device, or testing the pixel-control devices.

15 Electronic device testing is well known in the prior art. For example, U.S. Patent No. 6,028,441 describes self-testing routines in an LED display device by monitoring current use by the LEDs. U.S. Patent 5,369,357 describes an optically operated test structure for a CCD imager for testing the modulation transfer function for the CCD. Electrical testing methods for OLED
20 devices are described in U.S. Patent Application Publication 2007/0046581 and in U.S. Patent No. 6,995,519.

Yields are important in manufacturing low-cost flat-panel displays. It is important, therefore, that any flaws in the manufacturing process be detected as early as possible so as to repair the flaws or discard the flawed devices without
25 incurring any further manufacturing expense. In the prior art, flat-panel displays are tested after manufacture and repaired, if necessary. By testing displays during the manufacturing process, the cost of repair is reduced and the manufacturing yields improved. It is also important to test devices in an efficient way. In particular, displays with many pixels (e.g. high-definition televisions) can take a
30 long time to sequentially test each pixel. Therefore, test methods that can be implemented quickly are useful in the manufacturing process.

There is a need, therefore, for improving the performance of active-matrix light-emissive displays and testing such displays in an efficient and effective manner, in a short period of time, during or after manufacture, in order to improve the manufacturing yield of the active-matrix light-emissive displays.

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SUMMARY OF THE INVENTION

The present invention includes a method of making a display, comprising:

- (a) providing a display substrate having a display area and a plurality of control electrodes in the display area;
- 10 (b) locating a plurality of chiplets responsive to a controller to provide current to the control electrodes, each chiplet having a chiplet substrate separate from the display substrate, at least one pixel connection pad electrically connected to a control electrode, and one or more test light emitters formed in the chiplet responsive to the current provided on the control electrodes to emit light;
- 15 (c) controlling the chiplets to pass current through one or more of the test light emitters formed in the chiplet to emit light from the chiplet;
- (d) detecting the light emitted by the test light emitters to determine faulty chiplets or chiplet interconnections;
- (e) replacing or repairing the faulty chiplets or chiplet
- 20 interconnections; and
- (f) forming an organic light emitting diode over the substrate in the display area connected to the control electrodes.

Another aspect of the invention is a display, comprising:

- (a) a display substrate having a display area, and a plurality of
- 25 chiplets having a substrate independent of the display substrate located over the display substrate in the display area, each chiplet having at least one connection pad, at least one pixel control circuit, and at least one pixel test circuit;
- (b) a plurality of pixels located in the display area, each pixel including a control electrode, a second electrode, and at least one layer of light-
- 30 emitting material located between the control electrode and second electrode, wherein the pixel control circuit is connected to the control electrode for driving the control electrode causing the light-emitting material to emit light;

(c) a controller connected to one or more chiplets for providing external control signals to the chiplet; and

(d) wherein the pixel test circuit includes one or more test light emitters responsive to the external control signals, the test light emitters emitting
5 light independently of the layer of light-emitting material.

The present invention has the advantage that it improves the performance of control elements in a flat-panel substrate and provides an efficient way to test chiplets and electrical connections. The invention is particularly useful during fabrication of OLED devices including chiplets to ensure that the
10 chiplets are operating properly prior to the fabrication of the OLED layers in the device.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a display schematic according to an embodiment of the present invention;

15 FIG. 2 is a schematic of a portion of a display according to an embodiment of the present invention;

FIG. 3 is a cross section of a chiplet according to an embodiment of the present invention;

FIGS. 4A-4C are schematics of various pixel and test light emitter driving circuits according to alternative embodiments of the present invention;

20 FIG. 5 is a schematic of a pixel and test light emitter driving circuit according to another embodiment of the present invention;

FIG. 6 is a flow diagram of a method of the present invention;

FIG. 7 is a schematic of a pixel and test light emitter driving
25 circuits according to another embodiment of the present invention;

FIG. 8 is a partial cross section of a display and chiplet according to an embodiment of the present invention;

FIG. 9 is a schematic of a pixel group according to an embodiment of the present invention;

30 FIG. 10 is a flow diagram of a method of the present invention; and

FIG. 11 is a system diagram of display with test light emitters and an electronic camera according to a method of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to schematic FIG. 1 and cross-section FIG. 8, a display, according to one embodiment of the present invention, includes a display substrate 10 having a display area 11. A plurality of pixels 50 are located in the display area 11, each pixel 50 including a control electrode 12, a second electrode 16, and at least one layer of light-emitting material 14 located between the control electrode 12 and second electrode 16 that emits light in response to a current provided by the control electrode 12 and the second electrode 16. A plurality of chiplets 20 having a chiplet substrate 28 independent of the display substrate 10 are located over the display substrate 10 in the display area 11, each chiplet 20 having at least one connection pad 24, at least one pixel control circuit 22, and at least one pixel test circuit 23. The pixel control circuit 22 is connected to the control electrode 12 through an electrical connection 32 for driving the control electrode 12 and the layer of light-emitting material 14 to emit light. The pixel control circuit 22 is responsive to external control signals 30, 34, 36 from a controller 60 connected to one or more chiplets 20 that provides external control signals to the chiplet 20. The pixel test circuit 23 includes one or more test light emitters 26 responsive to the external control signals 34, 36, the test light emitters 26 emit light independently of the layer of light-emitting material 14 and second electrode 16.

As used herein, the light-emitting pixels are area emitters, employing layers of material coated over a substrate and driven by electrodes coated over and under the layers of material. The light-emitting material layers are not crystalline or formed in silicon. In contrast, the test light emitters can be conventional inorganic diodes formed in a crystalline material, such as silicon, that emit light from a small, point source.

FIG. 2 illustrates a more detailed portion of an embodiment of the present invention. Referring to FIG. 2, the test light emitter 26 is provided for each pixel 50 on the substrate 10 in the display area 11. Pixel test circuits 23 in each chiplet 20 drives the test light emitters 26 to emit light in response to external control signals such as, for example, control signals 36, data signals 34, or select signals 30. Each pixel 50 can be driven by pixel control circuit 22 with electrical

connections 32 connecting the pixel 50 to the chiplet 20 through connection pads 24. The test light emitters 26 can be responsive to current provided to its associated pixel 50.

As shown in FIG. 8, according to one active-matrix embodiment of the present invention having the chiplet 20 control device, each pixel 50 can have an independently controlled control electrode 12, the second electrode 16 can be common to multiple pixels 50, and the pixel control circuit 22 provides active-matrix control to the pixels 50. As is also shown in FIG. 8, the pixel control circuit 22 can drive more than one pixel 50. The connection pad 24 on the chiplet 20 can connect directly to a control electrode 12 (as shown) or through an electrical connection 32. In an alternative embodiment of the present invention illustrated in FIG. 9, one or more pixel control circuits 22 can provide passive-matrix control to a plurality of groups 52 of pixels 50. Such passive-matrix-controlled pixel groups 52 can be formed by the overlap of independent orthogonal column and row electrodes oriented in different directions that can correspond to electrodes 12 and 16. Pixel control circuits 22, for example in chiplets 20, can provide drive currents to activate the column and row electrodes 12, 16 to drive current through the pixels 50. Connection pads 24 can connect the chiplets 20 to the electrodes 12, 16. FIG. 8 is a cross section taken along line A, A' of FIG. 9.

The pixel control circuit 22 of various embodiments can be implemented in thin-film circuits on a substrate. However, such circuits are large and have relatively lower performance than circuits formed in crystalline silicon. Therefore, in an embodiment of the present invention, the pixel control circuits 22 are formed in chiplets 20 having separate substrates 28 that are adhered to the display substrate 10. Referring to FIG. 8 in more detail, the chiplet 20 having a separate chiplet substrate 28 is adhered to the substrate 10 and buried with an adhesion planarization layer 18. The chiplet 20 includes pixel control circuit 22. First electrodes 12 are electrically connected to connection pads 24 formed on the chiplet 20. Light-emitting material layer 14 is located over the first electrodes 12 and second electrodes 16 formed over the light-emitting material layer 14. The light-emitting material layer 14 can include multiple layers of light-emitting

material as well as various charge-control layers as are known in the organic and inorganic light-emitting diode art. The electrodes 12, 16 and layer(s) of light-emitting material 14 form a light-emitting diode 15.

FIG. 3 shows a cross section of the chiplet 20 taken from lines B, B' in FIG. 2, according to an embodiment of the present invention. The chiplet 20 is adhered to the substrate 10 with an adhesive and planarizing layer 18, for example including resin. Internal electrical connections 44 such as wires can connect the connection pads 24 within the chiplet 20 and pixel control circuit 22 can be used to respond to external signals 30, 34, and 36 to drive electrical connections 32 connected to pixels 50 and to drive the test light emitters 26 formed in the chiplet 20. Signals 30, 34, 36 can be connected over the top of a chiplet 20 or electrically connected through the chiplet 20 (as shown for select signal 30).

As shown in FIG. 1, the test light emitter 26 is formed in each chiplet 20 and is associated with each pixel test circuit 23. In this configuration, the test light emitter 26 can be responsive to current provided to more than one pixel 50, for example the pixels 50 connected to the same chiplet 20, controlled through the pixel control circuit 22. In one embodiment of the present invention, the test light emitter 26 sequentially responds to current provided to each of the pixels 50 driven by the pixel control circuit 22 in one chiplet 20.

The pixel test circuitry 23 can drive the test light emitters 26 in a variety of ways according to a variety of embodiments of the present invention. For example, as shown in FIG. 4A, the test light emitter 26 can be connected in parallel with the light emitting diode 15 so that whenever the light emitting diode 15 is driven by driving transistor 56, both the light emitting diode 15 and the test light emitter 26 will emit light. A display driving transistor 56 is responsive to a charge stored in a storage capacitor 61 that is deposited by external select signal 30 and data signal 34 through a control transistor 54.

Alternatively, as shown in FIG. 4B, the test light emitter 26 can be driven by the test control transistor 58 responsive to current provided to at least one pixel. The test control transistor 58 can be connected to the output of the driving transistor 56 and controlled by a test signal 57 so that, with the provision

of the test signal 57, current can flow from the driving transistor 56 through the test light emitter 26. The driving transistor 56 is responsive to a charge stored in storage capacitor 61 that is deposited by external select signal 30 and data signal 34 through control transistor 54.

5 Referring to FIG. 4C, a plurality of test signals can control a corresponding plurality of test control transistors 58 whose output is connected in a wired OR configuration. If any of the test control transistors 58 is turned on by test signal 57, test light emitter signal P4 conducts current through test light emitter 26. Similar circuits, each having a separate test signal 57 and test control
10 transistor 58, are connected to test light emitter signals P1, P2, and P3 so that upon the application of the test signal 57, the corresponding test control transistor 58 is activated, and the corresponding test light emitter signal conducts current through the test light emitter 26. Thus, a single test light emitter 26 can be responsive to a plurality of pixel control circuits 22, either together or independently, depending
15 on the test signals 57. The driving transistor 56 is responsive to a charge stored in storage capacitor 61 that is deposited by external select signal 30 and data signal 34 through transistor 54.

Referring to FIG. 5, a test light driving transistor 59 can drive the test light emitter 26 with an independently controlled current by connecting the
20 output of the test control transistor 58 to the gate of the test light driving transistor 59. This prevents current intended for the light-emitting diode 15 from being used to drive the test light emitter 26. Note that the amount of current driven through the test light emitter 26 can be controlled and correspond to the current driven through the light-emitting diode 15, so that the test light emitter 26 can provide a
25 range of light emission corresponding to the range of light emission of the light-emitting diode 15, enabling a wider variety of test capabilities. The driving transistor 56 is responsive to a charge stored in storage capacitor 61 that is deposited by external select signal 30 and data signal 34 through transistor 54.

In one embodiment of the present invention, the test light emitter
30 26 can be formed in a chiplet having a silicon substrate with doped or undoped areas. Therefore, the test light emitter 26 can be constructed as an inorganic light emitting diode that provides an inorganic point-source light emitter, for example a

conventional light-emitting diode formed in crystalline semiconductor material, such as silicon. As shown in FIG. 7, the test light emitter 26 can be a light-emitting NPN bipolar transistor 27. The NPN bipolar transistor 27 can include an emitter-base junction and the circuit can include a structure that provides a non-destructive reverse breakdown voltage across the emitter-base junction to cause the transistor to emit light. Because the transistor is formed on and in the surface of the chiplet, light emitted by the transistor can visibly escape from the chiplet.

Referring to FIG. 6 the test light emitters 26 can be employed, according to an embodiment of the present invention, in a method of making a display. A display substrate is provided (Step 100), and a plurality of chiplets responsive to a controller to provide current to a plurality of control electrodes located (Step 105) over the substrate in the display area. Each chiplet can have a chiplet substrate separate from the display substrate and at least one pixel connection pad can be electrically connected (Step 110) to a control electrode and one or more test light emitters formed in the chiplet that is responsive to the current provided on the control electrodes to emit light. The chiplets are controlled (Step 115) to pass current through one or more of the test light emitters formed in the chiplet to emit light from the chiplet. According to one embodiment of the present invention and as shown in FIG. 6, the chiplets can be controlled to emit light simultaneously from all of the test light emitters. Alternatively, the test light emitters can be controlled individually in sequence, for example as shown in FIG. 10. Referring to FIG. 10, the Step 115 of controlling the test light emitters can be performed in a series of steps in which a pixel counter number is first set (Step 116) to zero, the pixel corresponding to the pixel counter controlled to emit light, the pixel number is incremented (Step 118) and tested (Step 119). If all of the pixels are tested, the process of FIG. 10 completes; if not, the next pixel is tested.

The light emitted by the test light emitters can be detected (Step 120) to determine (Step 125) faulty chiplets or faulty chiplet interconnections. For example, as shown in FIG. 11, the substrate 10 with test light emitters 26 distributed thereon can be imaged by an electronic camera 70 (Step 120 of FIG. 6). The image can then be analyzed (Step 125 of FIG. 6) to determine any faults

in the test light emitters, chiplets, or chiplet interconnections, for example by the controller 60 or a separate computer system (not shown). Returning to FIG. 6, the faulty chiplets or faulty chiplet interconnections are replaced or repaired (Step 130). The process can return to Step 115 to confirm that the repairs are correct and complete. At this point in the process, a functioning backplane is constructed.

At least one layer of light-emitting material is deposited (Step 135) over the control electrodes and a second electrode formed (Step 140) over the one or more layers of light-emitting material. The control electrode, at least one layer of light-emitting material, and the second electrode form a light-emitting pixel responsive to current provided by the control electrode and the second electrode. The display is then operated (Step 145) by controlling the chiplets with the controller to drive the control electrodes to provide current through the light-emitting layer so that the pixels emit light.

In one embodiment of the present invention, the light from the test light emitter is detected by employing an image sensor to form an image of the display area while the test light emitters are controlled to emit light (FIG. 11). The test light emitters can be controlled to emit light simultaneously or, alternatively, the test light emitters can be controlled to emit light sequentially (FIG. 10). In yet another embodiment of the present invention, the test light emitters can be controlled to emit light at a luminance corresponding to the luminance desired for the pixels. The image or images formed of the test light emitters can be analyzed to determine faults using mathematical and image analysis software.

Chiplets can have a single row or multiple rows of connection pads along a relatively long side of the chiplet longer than a relatively shorter neighboring side. Chiplets can be connected to an external controller through a buss or through multiple busses. The busses can be serial, parallel, or point-to-point busses and can be digital or analog. A buss is connected to the chiplets to provide signals, such as power, ground, clock, data, or select signals. More than one buss separately connected to one or more controllers or chiplets can be employed.

In operation, a controller receives and processes an information signal according to the needs of the display device and transmits the processed signal and control information to each chiplet in the device. The processed signal includes luminance information for each light-emitting pixel element. The
5 luminance information can be stored in an analog or digital storage element corresponding to each light-emitting pixel element. The chiplets then activate the pixel electrodes to which they are connected. At the same time, or in response to a test signal, the test light emitters are illuminated through the circuitry and an image of the light-emission from the test light emitters is formed. The image is
10 analyzed to determine faults in the display device. Repairs can be made to correct the faults. If the light emitting diode is not yet constructed, it can then be constructed and the display device completed and put into operation.

Additional busses can supply a variety of signals, including timing (e.g. clock) signals, data signals, select signals, power connections, or ground
15 connections. The signals can be analog or digital, for example digital addresses or data values. Analog data values can be supplied as charge or voltage. The storage registers can be digital (for example including flip-flops) or analog (for example including capacitors for storing charge).

In one embodiment of the present invention, the display device is
20 an OLED display. The controller can be implemented as a chiplet and affixed to the substrate. The controller can be located on the periphery of the substrate, or can be external to the substrate and include a conventional integrated circuit.

According to various embodiments of the present invention, the chiplets can be constructed in a variety of ways, for example with one or two rows
25 of connection pads along a long dimension of a chiplet. Interconnection busses and wires can be formed from various materials and use various methods for deposition on the device substrate. For example, interconnection busses and wires can be metal, either evaporated or sputtered, for example aluminum or aluminum alloys, magnesium, or silver. Alternatively, the interconnection busses and wires
30 can be made of cured conductive inks or metal oxides. In one cost-advantaged embodiment, the interconnection busses and wires are formed in a single layer.

The present invention is particularly useful for multi-pixel device embodiments employing a large device substrate, e.g. glass, plastic, or foil, with a plurality of chiplets arranged in a regular arrangement over the device substrate. Each chiplet can control a plurality of pixels formed over the device substrate according to the circuitry in the chiplet and in response to control signals. Individual pixel groups or multiple pixel groups can be located on tiled elements, which can be assembled to form the entire display.

According to the present invention, chiplets provide distributed pixel control elements over a substrate. A chiplet is a relatively small integrated circuit compared to the device substrate and includes a circuit including wires, connection pads, passive components such as resistors or capacitors, or active components such as transistors or diodes, formed on an independent substrate. Chiplets are manufactured separately from the display substrate and then applied to the display substrate. The chiplets are preferably manufactured using silicon or silicon on insulator (SOI) wafers using known processes for fabricating semiconductor devices. Each chiplet is then separated prior to attachment to the device substrate. The crystalline base of each chiplet can therefore be considered a substrate separate from the device substrate and over which the chiplet circuitry is disposed. A plurality of chiplets therefore has a corresponding plurality of substrates separate from the device substrate and each other. In particular, the independent substrates are separate from the substrate on which the pixels are formed and the areas of the independent, chiplet substrates, taken together, are smaller than the device substrate.

Chiplets can have a crystalline substrate to provide higher performance active components than are found in, for example, thin-film amorphous or polycrystalline silicon devices. Chiplets can have a thickness preferably of 100 μm or less, and more preferably 20 μm or less. This facilitates formation of the adhesive and planarization material over the chiplet that can then be applied using conventional spin- or curtain-coating techniques. According to one embodiment of the present invention, chiplets formed on crystalline silicon substrates are arranged in a geometric array and adhered to a device substrate with adhesion or planarization materials. Connection pads on the surface of the

chipselets are employed to connect each chipset to signal wires, power busses and electrodes to drive pixels. Chipsets can control at least four pixels.

Since the chipsets are formed in a semiconductor substrate, the circuitry of the chipset can be formed using modern lithography tools. With such tools, feature sizes of 0.5 microns or less are readily available. For example, modern semiconductor fabrication lines can achieve line widths of 90 nm or 45 nm and can be employed in making the chipsets of the present invention. The chipset, however, also requires connection pads for making electrical connections to the wiring layer provided over the chipsets once assembled onto the display substrate. The connection pads must be sized based on the feature size of the lithography tools used on the display substrate (for example 5 μm) and the alignment of the chipsets to the wiring layer (for example $\pm 5\mu\text{m}$). Therefore, the connection pads can be, for example, 15 μm wide with 5 μm spaces between the pads. This shows that the pads will generally be significantly larger than the transistor circuitry formed in the chipset.

The pads can generally be formed in a metallization layer on the chipset over the transistors. It is desirable to make the chipset with as small a surface area as possible to enable a low manufacturing cost.

By employing chipsets with independent substrates (e.g. including crystalline silicon) having circuitry with higher performance than circuits formed directly on the substrate (e.g. amorphous or polycrystalline silicon), a device with higher performance is provided. Since crystalline silicon has not only higher performance but much smaller active elements (e.g. transistors), the circuitry size is much reduced. A useful chipset can also be formed using micro-electro-mechanical (MEMS) structures, for example as described in "A novel use of MEMs switches in driving AMOLED", by Yoon, Lee, Yang, and Jang, Digest of Technical Papers of the Society for Information Display, 2008, 3.4, p. 13.

The device substrate can include glass and the wiring layers made of evaporated or sputtered metal or metal alloys, e.g. aluminum or silver, formed over a planarization layer (e.g. resin) patterned with photolithographic techniques known in the art. The chipsets can be formed using conventional techniques well established in the integrated circuit industry.

The present invention can be employed in devices having a multi-pixel infrastructure. In particular, the present invention can be practiced with LED devices, either organic or inorganic, and is particularly useful in information-display devices. In a preferred embodiment, the present invention is employed in
5 a flat-panel OLED device composed of small-molecule or polymeric OLEDs as disclosed in, but not limited to U.S. Patent No. 4,769,292, to Tang et al., and U.S. Patent No. 5,061,569 to VanSlyke et al. Inorganic devices, for example, employing quantum dots formed in a polycrystalline semiconductor matrix (for example, as taught in U.S. Patent Application Publication No. 2007/0057263 by
10 Kahen), and employing organic or inorganic charge-control layers, or hybrid organic/inorganic devices can be employed. Many combinations and variations of organic or inorganic light-emitting displays can be used to fabricate such a device, including active-matrix displays having a top-emitter architecture or having a bottom-emitter architecture.

15 The invention has been described in detail with particular reference to certain preferred embodiments thereof, but it should be understood that variations and modifications can be effected within the spirit and scope of the invention.

PARTS LIST

A, A'	cross section line
B, B'	cross section line
P1, P2, P3, P4	test light emitter signal
10	substrate
11	display area
12	electrode
14	light-emitting material layer
15	light emitting diode
16	electrode
18	adhesive and planarization layer
20	chiplet
22	pixel control circuit
23	pixel test circuit
24	connection pad
26	test light emitter
27	light-emitting transistor
28	chiplet substrate
30	select signal
32	electrical connection
34	data signal
36	control signal
44	chiplet internal electrical connection
50	pixel
52	pixel group
54	control transistor
56	display driving transistor
57	test signal
58	test control transistor
59	test light driving transistor
60	controller

Parts List cont'd

61	storage capacitor
70	electronic camera
100	provide display step
105	locate chiplets step
110	form connections step
115	control chiplets step
116	set pixel number step
117	emit test light step
118	increment pixel number step
119	pixel count test step
120	detect light step
125	determine faults step
130	repair faults step
135	deposit OLED material step
140	form second electrode step
145	operate display step

CLAIMS:

1. A display, comprising:
 - (a) a display substrate having a display area, and a plurality of chiplets having a substrate independent of the display substrate located over the display substrate in the display area, each chiplet having at least one connection pad, at least one pixel control circuit, and at least one pixel test circuit;
 - (b) a plurality of pixels located in the display area, each pixel including a control electrode, a second electrode, and at least one layer of light-emitting material located between the control electrode and second electrode, wherein the pixel control circuit is connected to the control electrode for driving the control electrode causing the light-emitting material to emit light;
 - (c) a controller connected to one or more chiplets for providing external control signals to the chiplet; and
 - (d) wherein the pixel test circuit includes one or more test light emitters responsive to the external control signals, the test light emitters emitting light independently of the layer of light-emitting material.
2. The display of claim 1, wherein each pixel has an independently controlled control electrode, the second electrode is common, and the pixel control circuit provides active-matrix control to the pixel.
3. The display of claim 1, wherein the pixel control circuit drives more than one pixel.
4. The display of claim 1, wherein the control electrodes and the second electrodes of a group of pixels form an array of row and column electrodes, each row and column electrode oriented in a different direction, the pixels defined by the overlapping of the control and second electrodes, and one or more of the pixel control circuits provide a passive-matrix control to the group of pixels.
5. The display of claim 1, including means for driving a test light emitter from each pixel responsive to current provided to that pixel.
6. The display of claim 1, including means for driving a test light emitter from each pixel control circuit.

7. The display of claim 1, including means for driving one test light emitter responsive to current provided to more than one pixel.

8. The display of claim 1, wherein each pixel test circuit includes a transistor for driving the test light emitter in response to current
5 provided to at least one pixel.

9. The display of claim 1, wherein the test control circuit further includes a test signal that controls the test light emitter.

10. The display of claim 1, wherein the chiplet substrate is silicon.

11. The display of claim 1, wherein the test light-emitter is an inorganic point-source emitter.

12. A method of making a display, comprising:

(a) providing a display substrate having a display area and a plurality of control electrodes in the display area;

15 (b) locating a plurality of chiplets responsive to a controller to provide current to the control electrodes, each chiplet having a chiplet substrate separate from the display substrate, at least one pixel connection pad electrically connected to a control electrode, and one or more test light emitters formed in the chiplet responsive to the current provided on the control electrodes to emit light;

20 (c) controlling the chiplets to pass current through one or more of the test light emitters formed in the chiplet to emit light from the chiplet;

(d) detecting the light emitted by the test light emitters to determine faulty chiplets or chiplet interconnections;

25 (e) replacing or repairing the faulty chiplets or chiplet interconnections; and

(f) forming an organic light emitting diode over the substrate in the display area connected to the control electrodes.

13. The method of claim 12, wherein step f) includes forming at least one layer of light-emitting material over the control electrodes and forming a second electrode over the one or more layers of light-emitting material, wherein the control electrode, at least one layer of light-emitting material and
5 second electrode form a light-emitting pixel responsive to current provided by the control electrode and the second electrode.

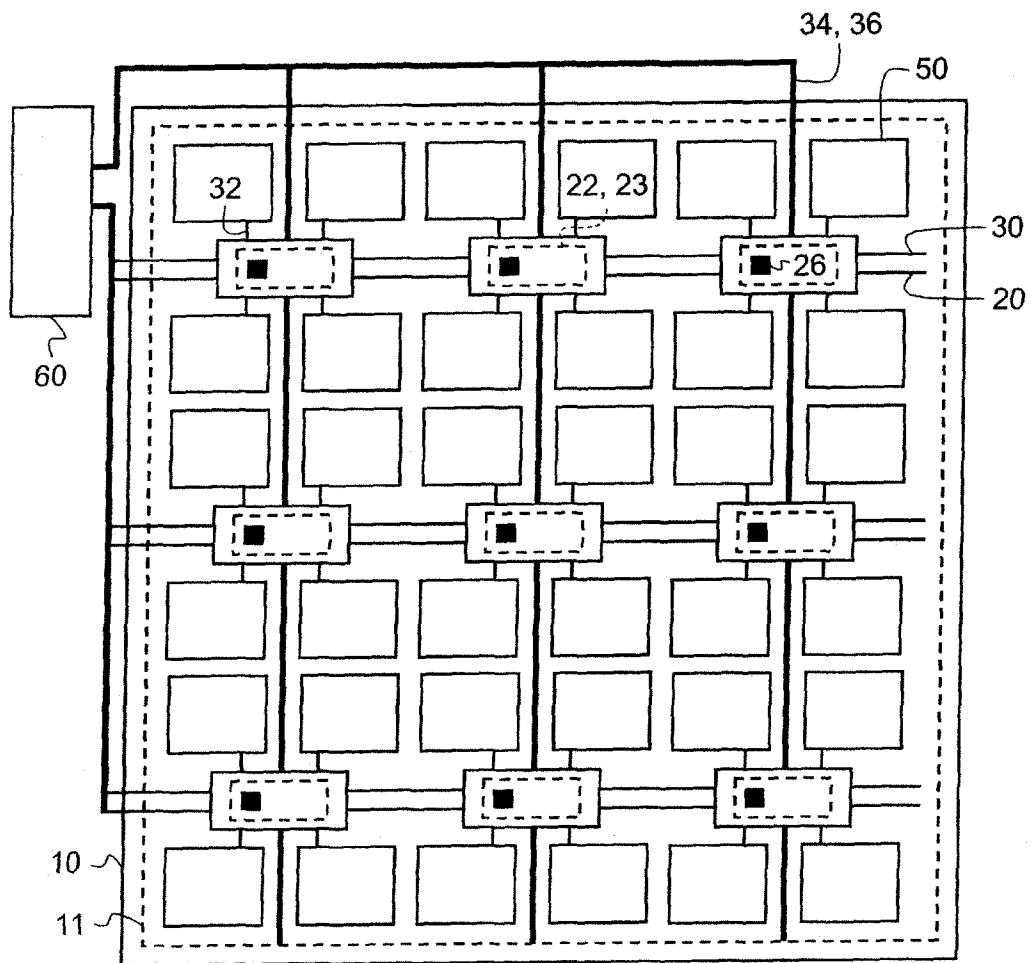
14. The method of claim 12 wherein the light is detected by employing an image sensor to form an image of the display area while the test light emitters are controlled to emit light.

10 15. The method of claim 12, further including the step of controlling the test light emitters to emit light simultaneously.

16. The method of claim 12, further including the step of controlling the test light emitters to emit light sequentially.

17. A chiplet, comprising:
15 (a) a chiplet substrate less than 40 microns thick;
(b) a pixel control circuit formed on or in the chiplet substrate and a pixel test circuit formed on or in the chiplet substrate;
(c) a plurality of connection pads formed over the chiplet substrate and electrically connected to the pixel control circuit;
20 (d) wherein the pixel control circuit responds to signals transmitted through a first connection pad to form a pixel driving signal connected to a second connection pad different from the first connection pad; and
(e) wherein the pixel test circuit is responsive to the pixel driving signal and includes one or more test light emitters, the test light emitter
25 emitting light in response to the pixel driving signal.

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**FIG. 1**

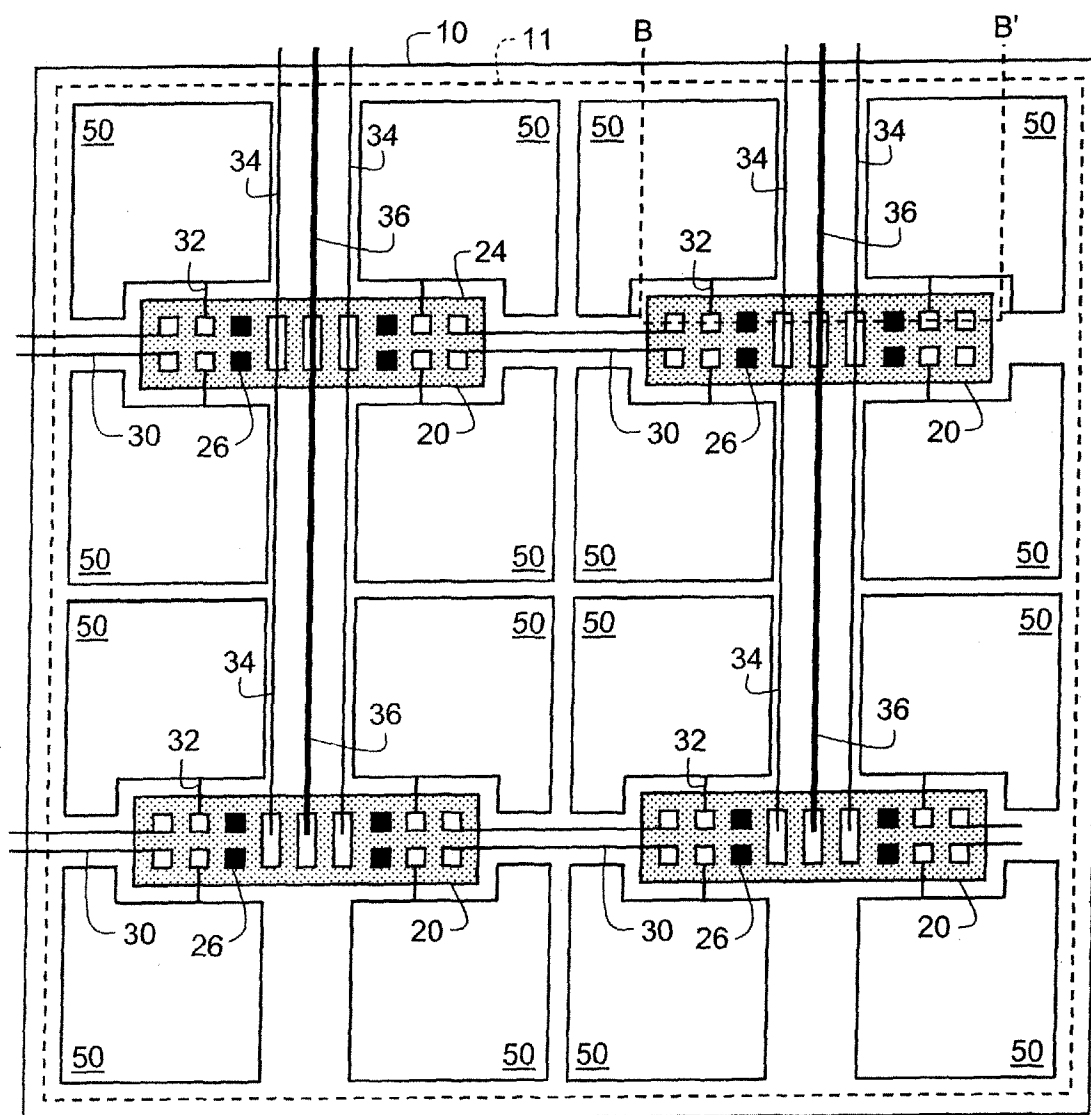


FIG. 2

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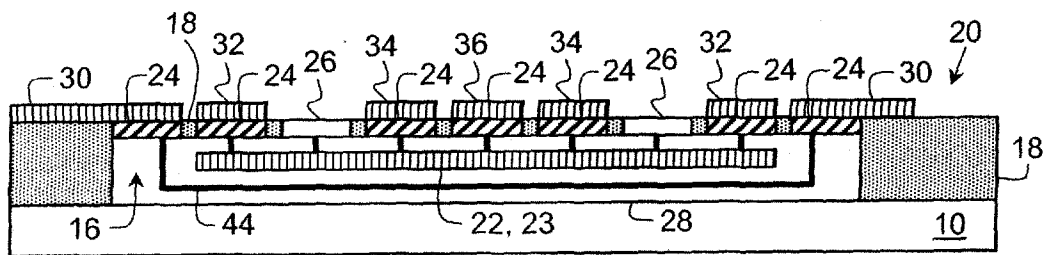
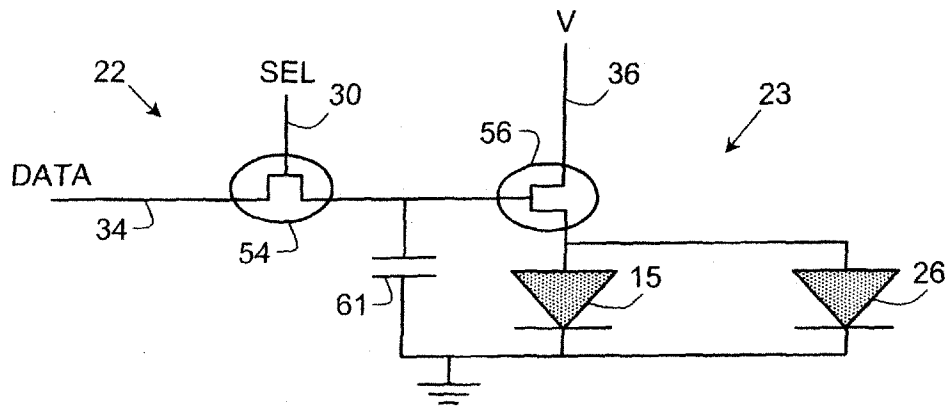
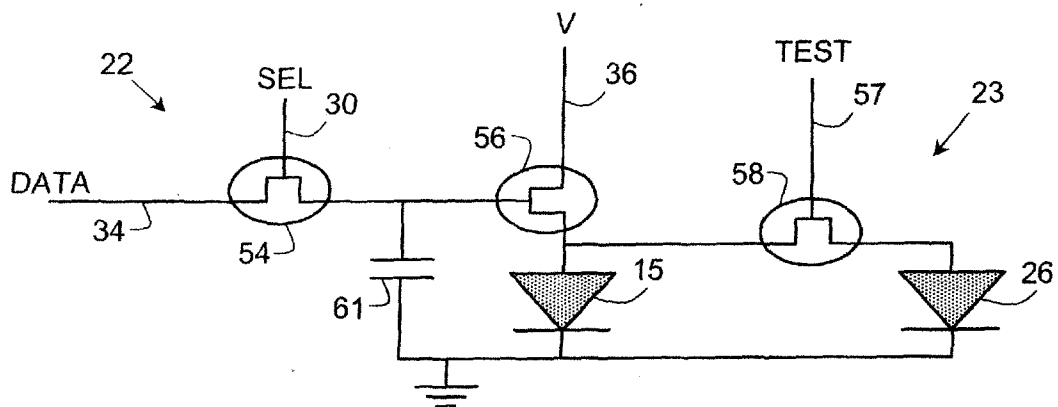
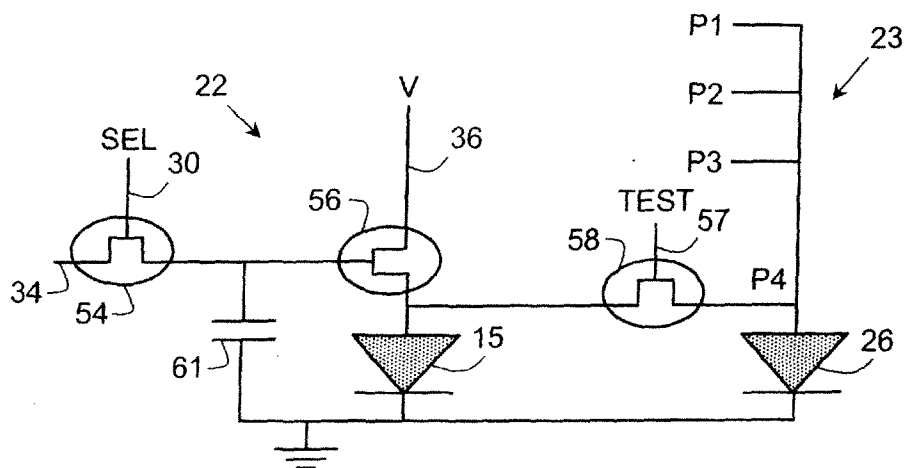
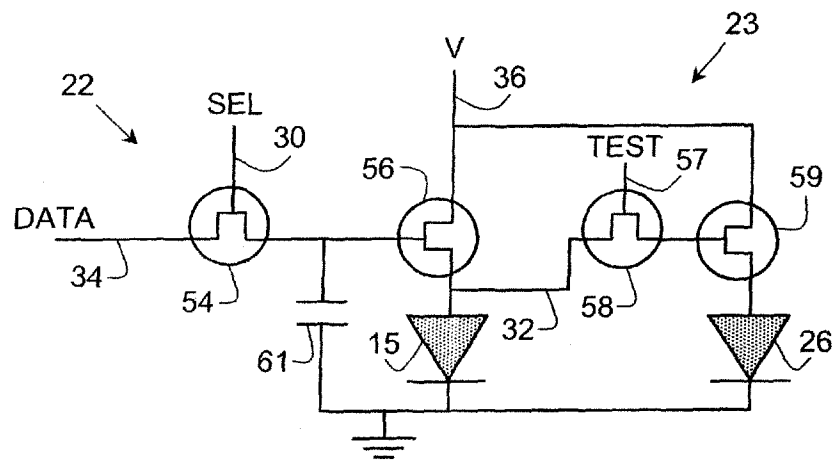


FIG. 3

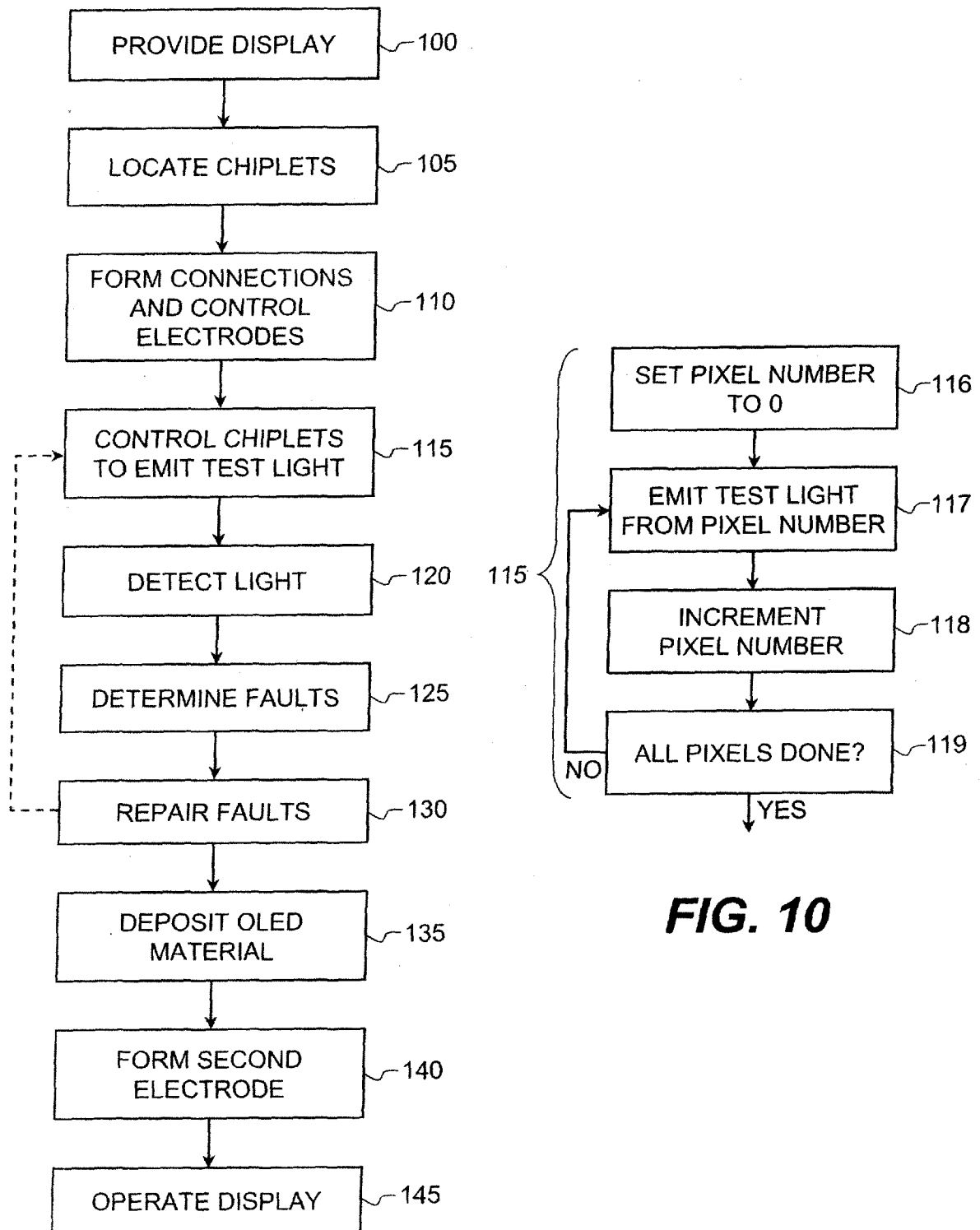
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**FIG. 4A****FIG. 4B****FIG. 4C**

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**FIG. 5**

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**FIG. 6****FIG. 10**

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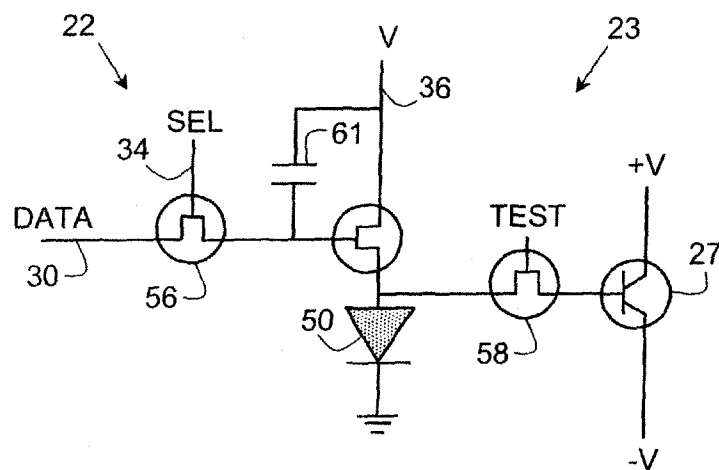


FIG. 7

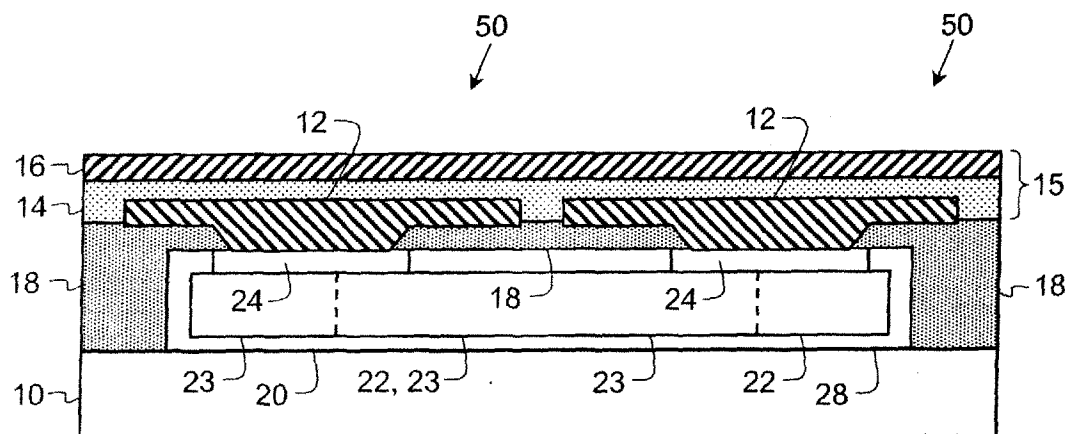


FIG. 8

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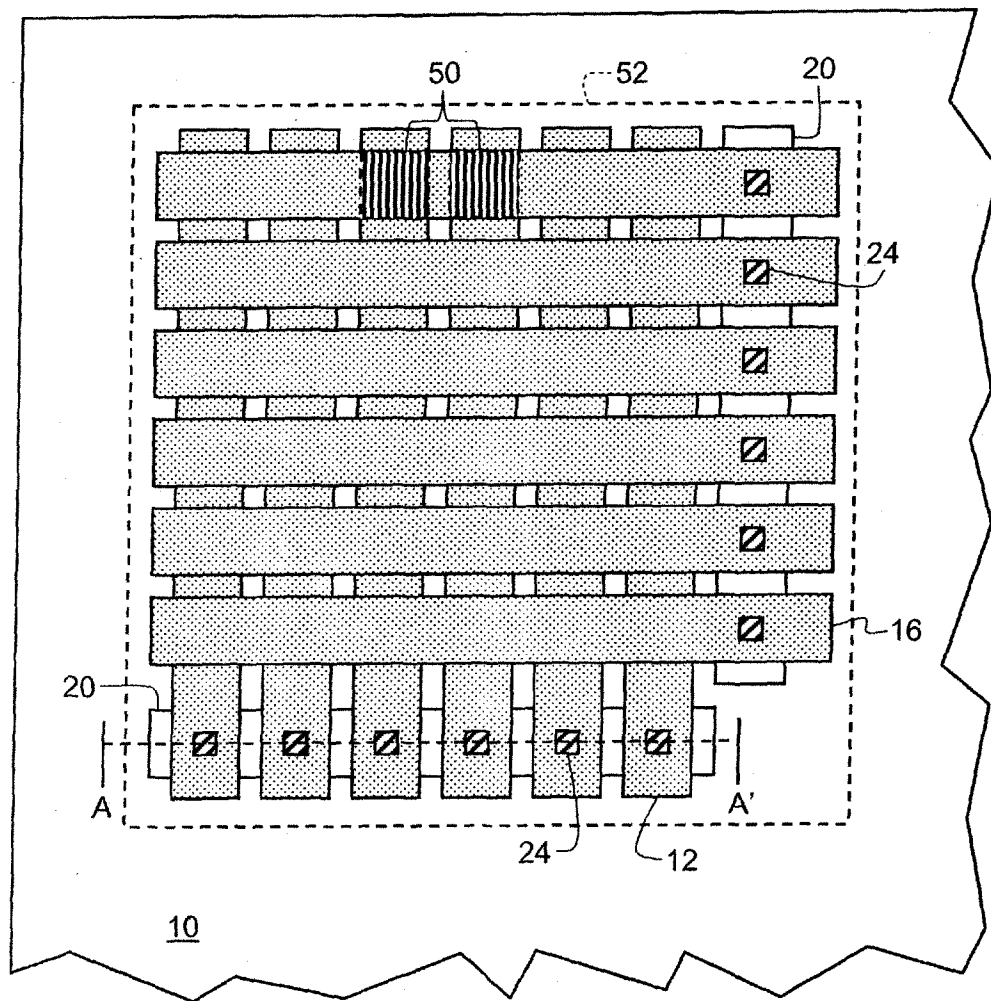
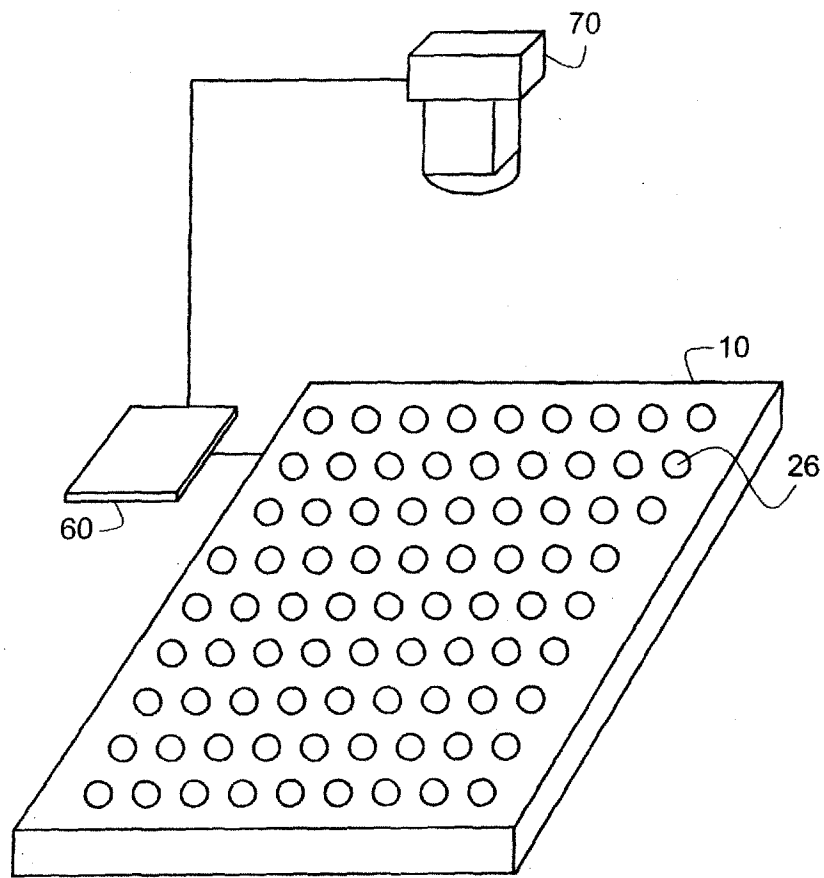


FIG. 9

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**FIG. 11**

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/044085

A. CLASSIFICATION OF SUBJECT MATTER INV. H01L27/32 G01R31/28 G09G3/00 ADD.		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) H01L G01R G09G G02F		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/032637 A1 (IMAMURA YOICHI [JP]) 19 February 2004 (2004-02-19) paragraphs [0004], [0006] - [0010] paragraphs [0166] - [0170], [174], [0176], [0179] paragraphs [0190], [0202]	1-17
Y	US 2006/055864 A1 (MATSUMURA HIDEKI [JP] ET AL) 16 March 2006 (2006-03-16) paragraphs [0002], [0006], [0018], [0035], [0120]	1-17
Y	US 2003/153105 A1 (BURCH KENNETH R [US]) 14 August 2003 (2003-08-14) paragraphs [0021], [0022]	1-17
-/--		
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents : "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. "&" document member of the same patent family		
Date of the actual completion of the international search 13 October 2010		Date of mailing of the international search report 21/10/2010
Name and mailing address of the ISA/ European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016		Authorized officer Faou, Marylène

INTERNATIONAL SEARCH REPORT

International application No

PCT/US2010/044085

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 00/49658 A1 (ALIEN TECHNOLOGY CORP [US]; SMITH JOHN S [US]) 24 August 2000 (2000-08-24) pages 3,4,8 pages 37-39	1-17
A	US 2008/142805 A1 (KOYAMA JUN [JP]) 19 June 2008 (2008-06-19) paragraphs [0031], [0034]	1-17

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2010/044085

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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US 2008142805 A1	19-06-2008	NONE	

专利名称(译)	在显示设备中光学测试小芯片		
公开(公告)号	EP2467875A1	公开(公告)日	2012-06-27
申请号	EP2010740484	申请日	2010-08-02
[标]申请(专利权)人(译)	全球OLED TECH		
申请(专利权)人(译)	全球OLED科技有限责任公司		
当前申请(专利权)人(译)	全球OLED科技有限责任公司		
[标]发明人	COK RONALD S HAMER JOHN W MATTERN MICHAEL W		
发明人	COK, RONALD, S. HAMER, JOHN, W. MATTERN, MICHAEL, W.		
IPC分类号	H01L27/32 G01R31/28 G09G3/00 G09G3/20 G09G3/3208		
CPC分类号	H01L27/3255 G09G3/006 G09G3/2085 G09G3/3208 G09G2330/12 H01L27/3276		
优先权	12/544286 2009-08-20 US		
其他公开文献	EP2467875B1		
外部链接	Espacenet		

摘要(译)

一种制造显示器的方法，包括在显示区域中提供具有多个控制电极的显示基板；响应于控制器定位多个小芯片以向控制电极提供电流，每个小芯片具有单独的基板，至少一个像素连接焊盘电连接到控制电极，并且小芯片中形成的一个或多个测试光发射器响应于控制电极上提供的电流发光；控制小芯片以使电流通过小芯片中形成的一个或多个测试光发射器以发光；检测测试光发射器发出的光，以确定有缺陷的小芯片或小芯片互连；更换或修理有缺陷的小芯片或小芯片互连；在连接到控制电极的显示区域中，在基板上形成有机发光二极管。