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(54) **ELECTROLUMINESCENT DISPLAY DEVICE**

(57) An electroluminescent display device includes a substrate including a plurality of pixel regions; a plurality of light emitting diodes spaced apart from each other on the substrate and corresponding to the plurality of pixel regions, respectively; encapsulation films respectively covering the plurality of light emitting diodes and having a first refractive index; a first partition wall disposed between the encapsulation films corresponding to a boundary between the plurality of pixel regions and having a

second refractive index lower than the first refractive index; and a color filter layer disposed on the encapsulation films and the first partition wall, wherein the color filter layer includes a plurality of color filter patterns having a third refractive index and a second partition wall disposed between the plurality of color filter patterns and having a fourth refractive index lower than the third refractive index.

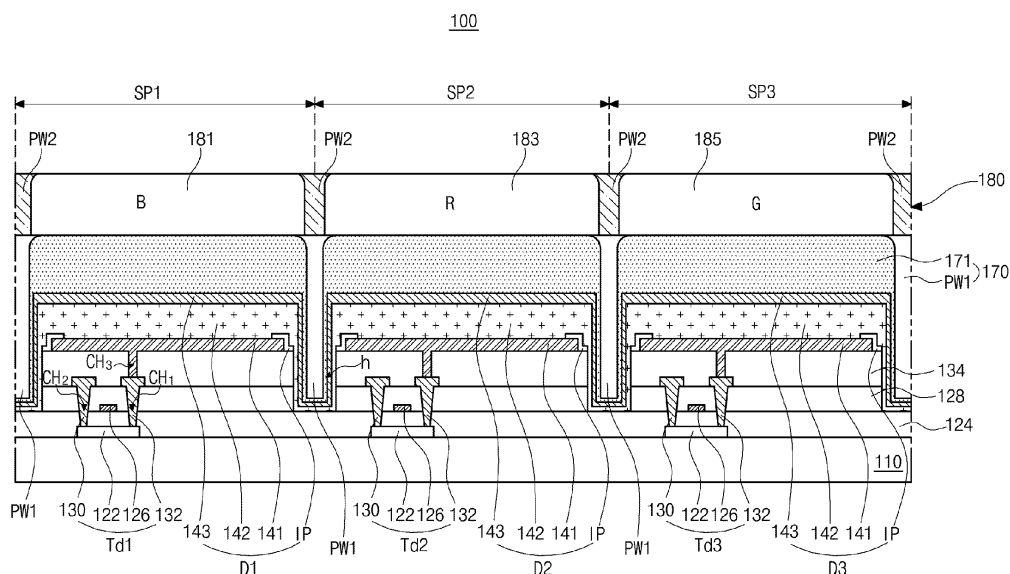


FIG. 2

Description

[0001] This application claims the priority of Korean Patent Application No. 10-2017-0166006, filed on December 5, 2017, in the Korean Intellectual Property Office.

BACKGROUND

1. Technical Field

[0002] The present disclosure relates to an electroluminescent display device.

2. Discussion of the Related Art

[0003] In recent years, flat panel displays having excellent characteristics such as being thin, lightweight, and having low power consumption have been widely developed and applied to various fields.

[0004] Among the flat panel displays, an electroluminescent display device is a device in which electrical charge carriers are injected into a light-emitting layer formed between a cathode, which is an electron-injecting electrode, and an anode, which is a hole-injecting electrode, such that excitons are formed, and then radiative recombination of the excitons occurs, thereby emitting light.

[0005] The electroluminescent display device can be formed using a flexible substrate such as plastic because it is self-luminous, and has excellent contrast ratios. Further the electroluminescent display device has a response time of several micro seconds, and there are advantages in displaying moving images. The electroluminescent display device also has wide viewing angles and is stable under low temperatures. Since the electroluminescent display device is driven by a low voltage of direct current DC 5V to 15V, it is easy to design and manufacture driving circuits.

[0006] Recently, as the size of substrates has been increased and display devices have evolved to have a high resolution, a pixel pitch has been decreased, and color mixture has become a problem.

SUMMARY

[0007] Accordingly, embodiments of the present disclosure are directed to an electroluminescent display device that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

[0008] It is an object of the present disclosure to provide an electroluminescent display device with high resolution in which a partition wall having a low refractive index is disposed so that light extraction efficiency is improved and color mixture is prevented, preferably in which a first partition wall and a second partition wall having a relatively low refractive index are disposed so

that light extraction efficiency is improved and color mixture is prevented.

[0009] The object is solved by the features of the independent claims. Preferred embodiments are given in the dependent claims.

[0010] To achieve the above-described object, the present disclosure provides an electroluminescent display device that includes a substrate including a plurality of pixel regions; a plurality of light emitting diodes spaced apart from each other on the substrate and corresponding to the plurality of pixel regions, respectively; encapsulation film respectively covering the plurality of light emitting diodes and having a first refractive index; a first partition wall disposed between the encapsulation film corresponding to a boundary between the plurality of pixel regions and having a second refractive index lower than the first refractive index.

[0011] In some embodiments, a color filter layer is disposed on the encapsulation film and the first partition wall, wherein the color filter layer includes a plurality of color filter patterns having a third refractive index and a second partition wall disposed between the plurality of color filter patterns and having a fourth refractive index lower than the third refractive index.

[0012] In some embodiments, the second partition wall is disposed corresponding to the first partition wall.

[0013] In some embodiments, the plurality of color filter patterns are disposed to correspond to the plurality of light emitting diodes, respectively.

[0014] In some embodiments, a middle portion of each of the first partition wall and the second partition wall has a bar shape.

[0015] Preferably, an upper portion of each of the first partition wall and the second partition wall has a width which progressively increases upward.

[0016] In some embodiments, a width of the middle portion of each of the first partition wall and/or the second partition wall is in a range of 2 μm to 3 μm .

[0017] In some embodiments, a height of each of the first partition wall and/or the second partition wall is in a range of 7 μm to 9 μm .

[0018] In some embodiments, each of the second refractive index and/or the fourth refractive index is in a range of 1.0 to 1.55.

[0019] In some embodiments, the color filter layer further includes a scattering layer disposed on an upper surface of each of the plurality of color filter patterns.

[0020] In some embodiments, an edge of each of the plurality of color filter patterns is curved.

[0021] In some embodiments, each of the plurality of light emitting diodes includes: a first electrode disposed on a passivation layer; an insulating pattern configured to cover an edge of the first electrode; a light-emitting layer disposed on the first electrode and the insulating pattern; and a second electrode disposed on the light-emitting layer.

[0022] In some embodiments, the electroluminescent display device further includes an interlayer insulating

layer disposed under the passivation layer.

[0023] In some embodiments, the passivation layer and the interlayer insulating layer are separated for each pixel region by the first partition wall.

[0024] In some embodiments, the light emitting diodes are partitioned by holes in the passivation layer and the interlayer insulating layer.

[0025] In some embodiments, an encapsulation layer includes the encapsulation film having the first refractive index and the first partition wall having a second refractive index lower than the first refractive index.

[0026] In some embodiments, wherein a hole has different portions and configured to partition the pixel regions in the interlayer insulating layer and the passivation layer, wherein a width of a first portion is larger than a width of a second portion.

[0027] It is to be understood that both the foregoing general description and the following detailed description are by example and explanatory, and are intended to provide further explanation of the present disclosure as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The accompanying drawings, which are included to provide a further understanding of the present disclosure and which are incorporated in and constitute a part of this specification, illustrate embodiments of the present disclosure and together with the description serve to explain various principles of the present disclosure. In the drawings:

FIG. 1 is a circuit diagram illustrating a single pixel region of an electroluminescent display device according to the present disclosure.

FIG. 2 is a cross-sectional view schematically illustrating an electroluminescent display device according to a first embodiment of the present disclosure.

FIG. 3 is an enlarged view of a portion of an electroluminescent display device according to the first embodiment of the present disclosure.

FIG. 4 is a cross-sectional view schematically illustrating an electroluminescent display device according to a second embodiment of the present disclosure.

FIG. 5 is an enlarged view of a portion of the electroluminescent display device according to the second embodiment of the present disclosure.

FIG. 6 is a graph schematically illustrating light extraction efficiency according to refractive indices of first and second partition walls according to the first and second embodiments of the present disclosure.

DETAILED DESCRIPTION

[0029] Hereinafter, exemplary embodiments of the present disclosure will be described with reference to the accompanying drawings.

<First embodiment>

[0030] FIG. 1 is a circuit diagram illustrating a single pixel region of an electroluminescent display device according to the present disclosure.

[0031] As illustrated in FIG. 1, the electroluminescent display device according to the embodiment of the present disclosure includes a gate line GL, a data line DL, a switching thin film transistor Ts, a driving thin film transistor Td, a storage capacitor Cst and a light-emitting diode D. The gate line GL and the data line DL cross each other to define a pixel region SP. The switching thin film transistor Ts, the driving thin film transistor Td, the storage capacitor Cst and the light-emitting diode D are formed in the pixel region SP.

[0032] More specifically, a gate electrode of the switching thin film transistor Ts is connected to the gate line GL and a source electrode of the switching thin film transistor Ts is connected to the data line DL. A gate electrode of the driving thin film transistor Td is connected to a drain electrode of the switching thin film transistor Ts, and a source electrode of the driving thin film transistor Td is connected to a high voltage supply VDD. An anode of the light-emitting diode D is connected to a drain electrode of the driving thin film transistor Td, and a cathode of the light-emitting diode D is connected to a low voltage supply VSS. The storage capacitor Cst is connected to the gate electrode and the drain electrode of the driving thin film transistor Td.

[0033] The electroluminescent display device is driven to display an image. For example, when the switching thin film transistor Ts is turned on by a gate signal applied through the gate line GL, a data signal from the data line DL is applied to the gate electrode of the driving thin film transistor Td and an electrode of the storage capacitor Cst through the switching thin film transistor Ts.

[0034] When the driving thin film transistor Td is turned on by the data signal, an electric current flowing through the light-emitting diode D is controlled, thereby displaying an image. The light-emitting diode D emits light due to the current supplied through the driving thin film transistor Td from the high voltage supply VDD.

[0035] That is, the amount of the current flowing through the light-emitting diode D is proportional to the magnitude of the data signal, and the intensity of light emitted by the light-emitting diode D is proportional to the amount of the current flowing through the light-emitting diode D. Thus, pixel regions SP show different gray levels depending on the magnitude of the data signal, and as a result, the electroluminescent display device displays an image.

[0036] The storage capacitor Cst maintains charges corresponding to the data signal for a frame when the switching thin film transistor Ts is turned off. Accordingly, even if the switching thin film transistor Ts is turned off, the storage capacitor Cst allows the amount of the current flowing through the light-emitting diode D to be constant and the gray level shown by the light-emitting diode D to

be maintained until a next frame.

[0037] A transistor and/or a capacitor other than the switching and driving thin film transistors Ts and Td and the storage capacitor Cst may be further added in the pixel region SP.

[0038] FIG. 2 is a cross-sectional view schematically illustrating an electroluminescent display device according to a first embodiment of the present disclosure.

[0039] As illustrated in FIG. 2, an electroluminescent display device 100 according to the first embodiment of the present disclosure may include a substrate 110, thin film transistors Td1, Td2, and Td3 and light emitting diodes D1, D2, and D3 respectively formed in pixel regions SP1, SP2, and SP3 disposed on the substrate 110, an encapsulation layer 170 disposed on the light emitting diodes D1, D2, and D3, and a color filter layer 180 disposed on the encapsulation layer 170.

[0040] That is, the thin film transistors Td1, Td2, and Td3 and the light emitting diodes D1, D2, and D3 may be respectively formed in the pixel regions SP1, SP2, and SP3 on the substrate 110, which is also referred to as a lower substrate, a thin film transistor (TFT) substrate, or a backplane.

[0041] In this case, each of the pixel regions SP1, SP2, and SP3 refers to a unit in which a specific type of color filter pattern among color filter patterns 181, 183, and 185 is formed and thus a specific color may be emitted.

[0042] For example, the pixel regions SP1, SP2, and SP3 may include a blue pixel region SP1, a red pixel region SP2, and a green pixel region SP3, but are not limited thereto, and may further include a white pixel region.

[0043] Specifically, a semiconductor layer 122 may be formed in each of the pixel regions SP1, SP2, and SP3. A gate insulating layer 124 may be formed on the semiconductor layer 122 substantially all over the substrate 110 including the pixel regions SP1, SP2, and SP3. The semiconductor layer 122 may include an active area which is formed of an intrinsic semiconductor material and disposed at the center of the semiconductor layer 122, and a source area and a drain area which are formed of an impurity-doped semiconductor material and respectively formed at left and right positions of the active area.

[0044] A gate electrode 126 is formed on the gate insulating layer 124 corresponding to the semiconductor layer 122, and an interlayer insulating layer 128 is formed on the gate electrode 126. The interlayer insulating layer 128 and the gate insulating layer 124 may include first and second contact holes CH1 and CH2 configured to respectively expose the source area and the drain area of the semiconductor layer 122.

[0045] A source electrode 132 and a drain electrode 130 spaced apart from each other are formed on the interlayer insulating layer 128 corresponding to the semiconductor layer 122, and the source electrode 132 and the drain electrode 130 may be respectively connected to the source area and the drain area of the semiconduc-

tor layer 122 through the first and second contact holes CH1 and CH2.

[0046] In this case, the semiconductor layer 122, the gate electrode 126, the source electrode 132, and the drain electrode 130 formed in each of the pixel regions SP1, SP2, and SP3 may constitute each of the thin film transistors Td1, Td2, and Td3.

[0047] Although coplanar type thin film transistors Td1, Td2, and Td3 have been illustrated in FIG. 2 as an example, embodiments are not limited thereto, and staggered type thin film transistors may also be formed.

[0048] Although only the driving thin film transistors Td1, Td2, and Td3 are illustrated in FIG. 2, a plurality of thin film transistors such as the switching thin film transistor Ts of FIG. 2 having the same structure as the driving thin film transistors Td1, Td2, and Td3 may be formed in a single pixel region.

[0049] Although not illustrated in Fig. 2, a gate line GL of FIG. 1, a data line DL of FIG. 1 and a power line crossing each other to define the pixel regions SP1, SP2, and SP3 may be formed. The switching thin film transistor Ts of FIG. 1 may be connected to the gate line GL of FIG. 1 and the data line DL of FIG. 1, and each driving thin film transistor Td1, Td2, and Td3 may be connected to the switching thin film transistor Ts of FIG. 1 and the power line.

[0050] A passivation layer 134 is formed on each of the thin film transistors Td1, Td2, and Td3. The passivation layer 134 may include a third contact hole CH3 configured to expose the source electrode 132.

[0051] An overcoat layer may be disposed on the passivation layer 134. In this case, the passivation layer 134 and the overcoat layer may include the third contact hole CH3 exposing the source electrode 132.

[0052] Here, holes h configured to partition the pixel regions SP1, SP2, and SP3 may be formed in the passivation layer 134 and the interlayer insulating layer 128. That is, the light emitting diodes D1, D2, and D3 may be partitioned by the holes h in the passivation layer 134 and the interlayer insulating layer 128 so that the light emitting diodes D1, D2, and D3 respectively correspond to the pixel regions SP1, SP2, and SP3. The light emitting diodes D1, D2, and D3 may be spaced apart from each other and respectively disposed in the pixel regions SP1, SP2, and SP3.

[0053] Although the holes h are illustrated as being formed in the passivation layer 134 and the interlayer insulating layer 128 in FIG. 2, this is merely an example. The electroluminescent display device 100 may have various other structures in which holes h capable of partitioning the light emitting diodes D1, D2, and D3 corresponding to the pixel regions SP1, SP2, and SP3 are formed.

[0054] Such holes h may be formed by performing a light-exposing process using a photo mask and a development process.

[0055] A first electrode 141 may be disposed on the passivation layer 134.

[0056] In this case, the first electrode 141 may be an anode or cathode for supplying one of holes or electrons to a light-emitting layer 142.

[0057] A case in which the first electrode 141 of the electroluminescent display device 100 according to the first embodiment of the present disclosure is an anode will be described as an example.

[0058] The first electrode 141 may be formed as a single layer of a transparent conductive material such as indium tin oxide (ITO). Alternatively, the first electrode 141 may be formed of a conductive material with relatively high reflectance such as a laminated structure of aluminum and titanium (Ti/Al/Ti), a laminated structure of A1 and ITO (ITO/Al/ITO), an APC alloy, and a laminated structure of the APC alloy and ITO (ITO/APC/ITO) in order to obtain a micro cavity effect. The APC alloy refers to an alloy of silver (Ag), palladium (Pd), and copper (Cu).

[0059] The first electrode 141 may be connected to the source electrode 132 of each of the thin film transistors Td1, Td2, and Td3 through the third contact hole CH3 formed in the passivation layer 134 and may be separately formed in each of the pixel regions SP1, SP2, and SP3.

[0060] Although the electroluminescent display device 100 according to the first embodiment of the present disclosure has been described by assuming that the thin film transistors Td1, Td2, and Td3 are N-type thin film transistors and the first electrode 141 is connected to the source electrode 132, embodiments are not limited thereto. When the thin film transistors Td1, Td2, and Td3 are P-type thin film transistors, the first electrode 141 may be connected to the drain electrode 130.

[0061] An insulating pattern IP configured to cover an edge of the first electrode 141 may be disposed on the first electrode 141. That is, the insulating pattern IP may be disposed to cover a side surface and a portion of an upper surface of the first electrode 141.

[0062] The insulating pattern IP may be formed of silicon oxide, but embodiments are not limited thereto.

[0063] In this case, the insulating pattern IP may mitigate a step difference of the first electrode 141 and improve current efficiency. That is, when forming the light-emitting layer 142 on the first electrode 141, the light-emitting layer 142 is formed to have a relatively small thickness on a stepped area of the first electrode 141 so that a current which does not contribute to emission is prevented from being focused.

[0064] The light-emitting layer 142 may be disposed on the first electrode 141 and the insulating pattern IP.

[0065] In this case, the light-emitting layer 142 may emit white light. For example, the light-emitting layer 142 may have a tandem white structure in which a plurality of light-emitting layers are stacked to emit white light. For example, the light-emitting layer 142 may include a first light-emitting layer configured to emit blue light and a second light-emitting layer disposed on the first light-emitting layer and configured to emit light having a color

which turns white when mixed with blue. The second light-emitting layer may be a light-emitting layer configured to emit yellow-green light. However, embodiments are not limited thereto, and a light-emitting layer 142 configured to emit one of blue light, red light, and green light may be disposed in each of the pixel regions SP1, SP2, and SP3.

[0066] A luminescent material of the light-emitting layer 142 may be an organic luminescent material having a refractive index of about 1.8 or higher or an inorganic luminescent material such as a quantum dot.

[0067] Also, the light-emitting layer 142 may be disposed in a shape which follows the morphology of the entire surfaces of the pixel regions SP1, SP2, and SP3.

[0068] That is, the light-emitting layer 142 may be disposed in a shape which follows the morphology of the first electrode 141 and the insulating pattern IP formed in each of the pixel regions SP1, SP2, and SP3 and the holes h formed in the passivation layer 134 and the interlayer insulating layer 128.

[0069] A second electrode 143 for supplying one of electrons or holes to the light-emitting layer 142 may be disposed on the light-emitting layer 142.

[0070] Here, the second electrode 143 may be a cathode or an anode.

[0071] A case in which the second electrode 143 of the electroluminescent display device 100 according to the first embodiment of the present disclosure is a cathode will be described as an example.

[0072] In this case, the second electrode 143 is formed along the morphology of the light-emitting layer 142. That is, the second electrode 143 may be formed to cover the light-emitting layer 142 along the shape of the light-emitting layer 142.

[0073] The second electrode 143 may be formed of a transparent conductive material such as ITO and IZO capable of transmitting light or may be formed of a semi-transmissive conductive material such as magnesium (Mg), silver (Ag), or an alloy of Mg and Ag.

[0074] Accordingly, the first electrode 141, the insulating pattern IP, the light-emitting layer 142, and the second electrode 143 may overlap with each other and form each of the light emitting diodes D1, D2, and D3, and the light emitting diodes D1, D2, and D3 may be spaced apart from each other and be disposed corresponding to the pixel regions SP1, SP2, and SP3, respectively.

[0075] The encapsulation layer 170 may be disposed on the light emitting diodes D1, D2, and D3 formed corresponding to the pixel regions SP1, SP2, and SP3, respectively.

[0076] The encapsulation layer 170 of the electroluminescent display device 100 according to the first embodiment of the present disclosure may include an encapsulation film 171 having a first refractive index and a first partition wall PW1 having a second refractive index lower than the first refractive index.

[0077] In this case, the encapsulation film 171 may be formed along the morphology of the light emitting diodes

D1, D2, and D3 formed to corresponding to the pixel regions SP1, SP2, and SP3, respectively. That is, the encapsulation film 171 may be formed along the morphology of the second electrode 143 disposed at the uppermost portions of the light emitting diodes D1, D2, and D3.

[0078] Due to the encapsulation film 171 being disposed along the morphology of the second electrode 143, a groove may be formed in the encapsulation film 171 corresponding to a boundary between the pixel regions SP1, SP2, and SP3.

[0079] In this case, the encapsulation film 171 may be formed of an inorganic film and/or may have a multilayer structure.

[0080] For example, the encapsulation film 171 may include at least one layer formed of silicon nitride, aluminum nitride, zirconium nitride, titanium nitride, hafnium nitride, tantalum nitride, silicon oxide, aluminum oxide, or titanium oxide.

[0081] The first partition wall PW1, which is bar-shaped, may be disposed in the groove of the encapsulation film 171 corresponding to the boundary between the pixel regions SP1, SP2, and SP3.

[0082] Although a width of an upper portion of the first partition wall PW1 is illustrated in the drawings as progressively increasing, this is merely an example, and the first partition wall PW1 may have the same width throughout.

[0083] The first partition wall PW1 may be an organic material having the second refractive index lower than the first refractive index of the encapsulation film 171. For example, the first refractive index may be in a range of 1.56 to 1.85, and the second refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0084] Due to the first partition wall PW1 having a refractive index lower than that of the encapsulation film 171, light that is incident obliquely on the encapsulation film 171 from the light-emitting layer 142 of the light emitting diodes D1, D2, and D3 may be reflected by the first partition wall PW1 and be output to upper areas of the corresponding pixel regions SP1, SP2, and SP3. Accordingly, light extraction efficiency of the electroluminescent display device 100 may be improved, and color mixture may be prevented.

[0085] In addition, permeation of oxygen or moisture into the light-emitting layer 142 and the second electrode 143 may be more effectively prevented by the encapsulation films 171 and the first partition walls PW1 disposed between the encapsulation films 171 configured to cover the light emitting diodes D1, D2, and D3.

[0086] The color filter layer 180 may be disposed on the encapsulation layer 170.

[0087] In this case, the color filter layer 180 may include the color filter patterns 181, 183, and 185 formed corresponding to the pixel regions SP1, SP2, and SP3, respectively, and a bar-shaped second partition wall PW2 disposed between the color filter patterns 181, 183, and 185.

[0088] Although a width of an upper portion of the second partition wall PW2 is illustrated in the drawings as progressively increasing, this is merely an example, and the second partition wall PW2 may have the same width throughout.

[0089] The color filter patterns 181, 183, and 185 may have a third refractive index, and the second partition wall PW2 may have a fourth refractive index lower than the third refractive index.

[0090] In this case, the third refractive index may be in a range of 1.6 to 1.85, and the fourth refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0091] The second partition wall PW2 may be formed of silicon oxide, but embodiments are not limited thereto.

[0092] Due to the second partition wall PW2 having a refractive index lower than that of the color filter patterns 181, 183, and 185, light that is incident obliquely on the color filter patterns 181, 183, and 185 from the light-emitting layer 142 of the light emitting diodes D1, D2, and D3 may be reflected by the second partition wall PW2 and be output to upper areas of the corresponding pixel regions SP1, SP2, and SP3. Accordingly, a problem in which color mixture occurs in a viewing angle direction may be prevented.

[0093] Further, since the second partition wall PW2 between the color filter patterns 181, 183, and 185 has a relatively fine width, an emissive area may be increased in comparison to a conventional case in which a black matrix is disposed.

[0094] Particularly, the second partition wall PW2 of the electroluminescent display device according to the first embodiment of the present disclosure may be formed corresponding to the first partition wall PW1. That is, the first partition wall PW1 and the second partition wall PW2 may be disposed to be parallel to each other in a first direction perpendicular to the substrate 110.

[0095] Due to the first partition wall PW1 and the second partition wall PW2 being disposed to be parallel to each other in the first direction, light that is output from the light emitting diodes D1, D2, and D3 respectively formed in the pixel regions SP1, SP2, and SP3 may be output to upper areas of the corresponding pixel regions SP1, SP2, and SP3. Accordingly, light extraction efficiency may be improved, and color mixture may be effectively prevented.

[0096] FIG. 3 is an enlarged view of a portion of an electroluminescent display device according to the first embodiment of the present disclosure.

[0097] As illustrated in FIG. 3, the electroluminescent display device 100 of FIG. 2 according to the first embodiment of the present disclosure may include a substrate 110 of FIG. 2, light emitting diodes D disposed on the substrate 110 of FIG. 2, an encapsulation layer 170 disposed on the light emitting diodes D, and a color filter layer 180 disposed on the encapsulation layer 170.

[0098] An interlayer insulating layer 128 and a passivation layer 134 may be disposed between the substrate

110 of FIG. 2 and the light emitting diodes D.

[0099] In this case, since holes h configured to partition pixel regions SP are formed in the passivation layer 134 and the interlayer insulating layer 128, the light emitting diodes D may be formed corresponding to the pixel regions SP.

[0100] That is, due to the holes h formed in the passivation layer 134 and the interlayer insulating layer 128, a bank layer which is formed in a conventional electroluminescent display device in order to partition pixel regions SP may be omitted, and a process may be simplified.

[0101] A first electrode 141 may be disposed on the passivation layer 134, and an insulating pattern IP configured to cover an edge of the first electrode 141 may be disposed on the first electrode 141.

[0102] When forming a light-emitting layer 142 on the first electrode 141 using the insulating pattern IP, the light-emitting layer 142 is formed to have a relatively small thickness on a stepped area of the first electrode 141 so that a current which does not contribute to emission is prevented from being focused, and current efficiency is improved.

[0103] The light-emitting layer 142 may be disposed on the first electrode 141 and the insulating pattern IP.

[0104] In this case, the light-emitting layer 142 may be disposed in a shape which follows the morphology of the first electrode 141, the insulating pattern IP, and the holes h formed in the passivation layer 134 and the interlayer insulating layer 128.

[0105] A second electrode 143 may be disposed on the light-emitting layer 142.

[0106] In this case, the second electrode 143 may be disposed in a shape which follows the morphology of the light-emitting layer 142.

[0107] Accordingly, the first electrode 141, the insulating pattern IP, the light-emitting layer 142, and the second electrode 143 may form the light emitting diodes D, and adjacent light emitting diodes D may be spaced apart from each other and be disposed corresponding to the pixel regions SP.

[0108] The encapsulation layer 170, which includes an encapsulation film 171 having a first refractive index and a first partition wall PW1 having a second refractive index lower than the first refractive index, may be disposed on the light emitting diodes D.

[0109] Particularly, the encapsulation film 171 may be formed along the morphology of the light emitting diodes D. That is, the encapsulation film 171 may be formed along the morphology of the second electrode 143 disposed at the uppermost portions of the light emitting diodes D.

[0110] Due to the encapsulation film 171 being disposed along the morphology of the second electrode 143, the electroluminescent display device 100 may have a structure in which the encapsulation film 171 covers each of the light emitting diodes D, and thus permeation of oxygen or moisture into the light-emitting layer 142 and

the second electrode 143 may be more effectively prevented.

[0111] In this case, the encapsulation film 171 may be formed of an inorganic film and/or may have a multilayer structure.

[0112] The first partition wall PW1 may be disposed in the groove of the encapsulation film 171 corresponding to the boundary between the pixel regions SP.

[0113] A middle portion of the first partition wall PW1 may have a bar shape, and an upper portion of the first partition wall PW1 may have a shape in which a width progressively increases upward. However, this is merely an example, and the first partition wall PW1 may be formed such that the upper portion and the middle portion have the same width.

[0114] In this case, a width d1 of the middle portion of the first partition wall PW1 may be in a range of 2 μm to 3 μm . The width of the upper portion of the first partition wall PW1 may be larger than or equal to the width d1 of the middle portion of the first partition wall PW1. However, embodiments are not limited thereto, and the widths of the upper portion and the middle portion of the first partition wall PW1 may be modified in various ways according to the size, resolution, and the like of the pixel regions SP.

[0115] Also, a height H1 of the first partition wall PW1 may be in a range of 7 μm to 9 μm , but embodiments are not limited thereto. The height H1 may be modified in various ways according to a thickness or the like of the passivation layer 134, the interlayer insulating layer 128, and the light emitting diodes D.

[0116] The passivation layer 134 and the interlayer insulating layer 128 may be separated corresponding to the pixel regions SP by the first partition wall PW1.

[0117] In this case, the first partition wall PW1 may be an organic material having a second refractive index lower than the first refractive index of the encapsulation film 171. For example, the first refractive index may be in a range of 1.6 to 1.85, and the second refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0118] Due to the first partition wall PW1 having a refractive index lower than that of the encapsulation film 171, light that is incident obliquely on the encapsulation film 171 from the light-emitting layer 142 of the light emitting diodes D may be reflected by the first partition wall PW1 and be output to upper areas of the corresponding pixel regions SP. Accordingly, light extraction efficiency of the electroluminescent display device 100 may be improved, and color mixture may be prevented.

[0119] By forming the first partition wall PW1 between the encapsulation films 171 configured to cover the light emitting diodes D, efficiency of preventing permeation of oxygen or moisture into the light-emitting layer 142 and the second electrode 143 may be further improved.

[0120] The color filter layer 180 may be disposed on the encapsulation layer 170.

[0121] In this case, the color filter layer 180 may include

color filter patterns 181, 183, and 185 formed corresponding to the pixel regions SP and a second partition wall PW2 formed between the color filter patterns 181, 183, and 185.

[0122] That is, the color filter patterns 181, 183, and 185 may be disposed corresponding to the light emitting diodes D.

[0123] Consequently, when white light is output from the light emitting diodes D, the white light may be converted into specific colored light through the color filter patterns 181, 183, and 185.

[0124] Here, edges of the color filter patterns 181, 183, and 185 may be curved.

[0125] Further, when lights of different wavelength bands are output from the light emitting diodes D, the color filter patterns 181, 183, and 185 may be disposed corresponding to the light emitting diodes D so that the lights of different wavelength bands are prevented from being mixed and causing a blurring phenomenon and a ghost phenomenon.

[0126] The color filter patterns 181, 183, and 185 may have a third refractive index, and the second partition wall PW2 may have a fourth refractive index lower than the third refractive index.

[0127] In this case, the third refractive index may be in a range of 1.6 to 1.85, and the fourth refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0128] A middle portion of the second partition wall PW2 may have a bar shape, and an upper portion of the second partition wall PW2 may have a shape in which a width progressively increases upward.

[0129] A width d2 of the middle portion of the second partition wall PW2 may be in a range of 2 μm to 3 μm . The width of the upper portion of the second partition wall PW2 may be larger than or equal to the width d2 of the middle portion of the second partition wall PW2. However, embodiments are not limited thereto.

[0130] Also, a height H2 of the second partition wall PW2 may be in a range of 7 μm to 9 μm , but embodiments are not limited thereto. The height H2 may be modified in various ways according to a thickness or the like of the color filter patterns 181, 183, and 185.

[0131] The second partition wall PW2 may be formed of silicon oxide, but embodiments are not limited thereto. The second partition wall PW2 may also be formed of an air gap.

[0132] Due to the second partition wall PW2 having a refractive index lower than that of the color filter patterns 181, 183, and 185, light that is incident obliquely on the color filter patterns 181, 183, and 185 from the light-emitting layer 142 of the light emitting diodes D may be reflected by the second partition wall PW2 and be output to upper areas of the corresponding pixel regions SP. Accordingly, a problem in which color mixture occurs in a viewing angle direction may be prevented.

[0133] Further, since the second partition wall PW2 between the color filter patterns 181, 183, and 185 has a

relatively fine width d2, an emissive area may be increased in comparison to the conventional case in which a black matrix is disposed.

[0134] A scattering layer SL may be disposed on an upper surface of each of the color filter patterns 181, 183, and 185.

[0135] In this case, the scattering layer SL may be a concavo-convex pattern formed on the upper surface of each of the color filter patterns 181, 183, and 185, but embodiments are not limited thereto. The scattering layer SL may also be formed of a material layer including beads.

[0136] Accordingly, light that passes through the color filter patterns 181, 183, and 185 and is output to the outside may be scattered in various directions.

[0137] Particularly, by scattering a portion of light L3, which is incident vertically on the color filter patterns 181, 183, and 185 at a boundary between the pixel regions SP, toward the second partition wall PW2, perception of lattices that may occur due to the fine second partition wall PW2 being viewed as a black area may be prevented when one views an image in a state in which one's eyes are close to a screen, such as when one views an image using a virtual reality (VR) device.

[0138] Particularly, the second partition wall PW2 of the electroluminescent display device 100 according to the first embodiment of the present disclosure may be formed corresponding to the first partition wall PW1.

[0139] That is, the first partition wall PW1 and the second partition wall PW2 may be disposed to be parallel to each other in a first direction 1A perpendicular to the substrate 110.

[0140] Due to the first partition wall PW1 and the second partition wall PW2 being disposed to be parallel to each other in the first direction 1A, light that is output from the light emitting diodes D respectively formed in the pixel regions SP may be output to upper areas of the corresponding pixel regions SP. Accordingly, light extraction efficiency may be improved, and color mixture may be effectively prevented.

<Second embodiment>

[0141] Hereinafter, detailed descriptions of configurations identical or similar to those of the first embodiment may be omitted.

[0142] FIG. 4 is a cross-sectional view schematically illustrating an electroluminescent display device according to a second embodiment of the present disclosure.

[0143] As illustrated in FIG. 4, an electroluminescent display device 200 according to the embodiment of the present disclosure may include a substrate 210, thin film transistors Td1, Td2, and Td3 and light emitting diodes D1, D2, and D3 respectively formed in pixel regions SP1, SP2, and SP3 disposed on the substrate 210, an encapsulation layer 270 disposed on the light emitting diodes D1, D2, and D3, and the color filter layer 280 disposed on the encapsulation layer 270.

[0144] That is, the thin film transistors Td1, Td2, and Td3 and the light emitting diodes D1, D2, and D3 may be respectively formed in the pixel regions SP1, SP2, and SP3 on the substrate 210, which is also referred to as a lower substrate, a thin film transistor (TFT) substrate, or a backplane.

[0145] In this case, the pixel regions SP1, SP2, and SP3 may include a blue pixel region SP1, a red pixel region SP2, and a green pixel region SP3, but are not limited thereto, and may further include a white pixel region.

[0146] A semiconductor layer 222 may be formed in each of the pixel regions SP1, SP2, and SP3. A gate insulating layer 224 may be formed on the semiconductor layer 222 substantially all over the substrate 110 including the pixel regions SP1, SP2, and SP3.

[0147] A gate electrode 226 is formed on the gate insulating layer 224 corresponding to the semiconductor layer 222, and an interlayer insulating layer 228 is formed on the gate electrode 226. The interlayer insulating layer 228 and the gate insulating layer 224 may include first and second contact holes CH1 and CH2 configured to respectively expose the source area and the drain area of the semiconductor layer 222.

[0148] A source electrode 232 and a drain electrode 230 spaced apart from each other are formed on the interlayer insulating layer 228 corresponding to the semiconductor layer 222, and the source electrode 232 and the drain electrode 230 may be respectively connected to the source area and the drain area of the semiconductor layer 222 through the first and second contact holes CH1 and CH2.

[0149] In this case, the semiconductor layer 222, the gate electrode 226, the source electrode 232, and the drain electrode 230 formed in the pixel regions SP1, SP2, and SP3 may constitute the thin film transistors Td1, Td2, and Td3.

[0150] A passivation layer 234 is formed on each of the thin film transistors Td1, Td2, and Td3. The passivation layer 234 may include a third contact hole CH3 configured to expose the source electrode 232.

[0151] In this case, in the electroluminescent display device 200 according to the second embodiment of the present disclosure, holes h1 and h2 configured to partition the pixel regions SP1, SP2, and SP3 may be formed in the interlayer insulating layer 228 and the passivation layer 234. That is, the light emitting diodes D1, D2, and D3 may be partitioned by the holes h1 and h2 in the interlayer insulating layer 228 and the passivation layer 234 so that the light emitting diodes D1, D2, and D3 respectively correspond to the pixel regions SP1, SP2, and SP3. The light emitting diodes D1, D2, and D3 may be spaced apart from each other and respectively disposed in the pixel regions SP1, SP3, and SP3.

[0152] Particularly, in the electroluminescent display device 200 according to the second embodiment of the present disclosure, a width of a portion of the hole h1 formed in the interlayer insulating layer 228 may be larger

than a width of a portion of the hole h1 formed in the passivation layer 234.

[0153] That is, the electroluminescent display device 200 has an under-cut form in which the width of the interlayer insulating layer 228 is smaller than the width of the passivation layer 234 disposed in each of the pixel regions SP1, SP2, and SP3.

[0154] Also, a first electrode 241 configured to cover an upper surface and a side surface of the passivation layer 234 may be disposed.

[0155] The first electrode 241 may be connected to the source electrode 232 of each of the thin film transistors Td1, Td2, and Td3 through the third contact hole CH3 formed in the passivation layer 234 and may be separately formed in each of the pixel regions SP1, SP2, and SP3.

[0156] Since the interlayer insulating layer 228 and the passivation layer 234 of the electroluminescent display device 200 according to the second embodiment of the present disclosure have the under-cut form, the first electrode 241 separately formed in each of the pixel regions SP1, SP2, and SP3 may be formed by one process so that the process may be simplified.

[0157] An insulating pattern IP configured to cover a side surface and a portion of an upper surface of the first electrode 241 may be disposed.

[0158] The insulating pattern IP may be formed of silicon oxide, but embodiments are not limited thereto.

[0159] In this case, the insulating pattern IP may mitigate a step difference of the first electrode 241 and improve current efficiency. That is, when forming a light-emitting layer 242 on the first electrode 241, the light-emitting layer 242 is formed to have a relatively small thickness on a stepped area of the first electrode 241 so that a current which does not contribute to emission is prevented from being focused.

[0160] The light-emitting layer 242 configured to cover the first electrode 241 and the insulating pattern IP may be disposed.

[0161] In this case, since the interlayer insulating layer 228 and the passivation layer 234 of the electroluminescent display device 200 according to the second embodiment of the present disclosure have the under-cut form, the light-emitting layer 242 separately formed in each of the pixel regions SP1, SP2, and SP3 may be formed by one process.

[0162] In this case, the light-emitting layer 242 may emit white light, but embodiments are not limited thereto. A light-emitting layer 242 configured to emit one of blue light, red light, and green light may be disposed in each of the pixel regions SP1, SP2, and SP3.

[0163] A luminescent material of the light-emitting layer 242 may be an organic luminescent material having a refractive index of about 1.8 or higher or an inorganic luminescent material such as a quantum dot.

[0164] A second electrode 243 configured to cover an upper surface and a side surface of the light-emitting layer 242 may be disposed.

[0165] Although the second electrode 243 is illustrated as if the second electrode 243 is formed separately in each of the pixel regions SP1, SP2, and SP3 in FIG. 4, the second electrodes 243 may be connected to each other in a cross-sectional view taken along a direction perpendicular to that of the cross-sectional view illustrated in FIG. 4.

[0166] Accordingly, the first electrode 241, the insulating pattern IP, the light-emitting layer 242, and the second electrode 243 form each of the light emitting diodes D1, D2, and D3, and the light emitting diodes D1, D2, and D3 may be spaced apart from each other and be disposed corresponding to the pixel regions SP1, SP2, and SP3, respectively.

[0167] The encapsulation layer 270 may be disposed on the light emitting diodes D1, D2, and D3 formed corresponding to the pixel regions SP1, SP2, and SP3, respectively.

[0168] The encapsulation layer 270 of the electroluminescent display device 200 according to the second embodiment of the present disclosure may include an encapsulation film 271 having a first refractive index and a first partition wall PW1 having a second refractive index lower than the first refractive index.

[0169] In this case, the encapsulation film 271 may be disposed in the form in which the encapsulation film 271 covers each of the light emitting diodes D1, D2, and D3 formed corresponding to each of the pixel regions SP1, SP2, and SP3.

[0170] In this case, the encapsulation film 271 may be formed of an inorganic film and/or have a multilayer structure.

[0171] A residual layer OM may be present between the light emitting diodes D1, D2, and D3.

[0172] In this case, the residual layer OM is formed from materials, which are to be used in forming the light emitting diodes D1, D2, and D3 and the encapsulation film 271, remaining in the hole h1 of the interlayer insulating layer 228.

[0173] The first partition wall PW1 may be disposed between the encapsulation films 271 corresponding to the boundary between the pixel regions SP1, SP2, and SP3.

[0174] Although a middle portion of the first partition wall PW1 is illustrated as having a bar shape and an upper portion of the first partition wall PW1 is illustrated as having a shape in which a width progressively increases in the drawings, this is merely an example. The first partition wall PW1 may be formed such that the upper portion and the middle portion have the same width.

[0175] Also, a lower portion of the first partition wall PW1 of the electroluminescent display device 200 according to the second embodiment of the present disclosure may be formed to have a width larger than that of the middle portion, and a lower surface of the first partition wall PW1 may contact the residual layer OM.

[0176] The first partition wall PW1 may be an organic material having a second refractive index lower than the

first refractive index of the encapsulation film 271. For example, the first refractive index may be in a range of 1.6 to 1.85, and the second refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0177] Due to the first partition wall PW1 having a refractive index lower than that of the encapsulation film 271, light that is incident obliquely on the encapsulation film 271 from the light-emitting layer 242 of the light emitting diodes D1, D2, and D3 may be reflected by the first partition wall PW1 and be output to upper areas of the corresponding pixel regions SP1, SP2, and SP3. Accordingly, light extraction efficiency of the electroluminescent display device 200 may be improved, and color mixture may be prevented.

[0178] In addition, permeation of oxygen or moisture into the light-emitting layer 242 and the second electrode 243 may be more effectively prevented by the encapsulation films 271 and the first partition wall PW1 disposed between the encapsulation films 271 configured to cover the light emitting diodes D1, D2, and D3.

[0179] By the width of the lower portion of the first partition wall PW1 being formed larger than the width of the middle portion thereof and the lower surface of the first partition wall PW1 having a structure in which the lower surface contacts the residual layer OM, efficiency of preventing permeation of oxygen and moisture may be further improved.

[0180] The color filter layer 280 may be disposed on the encapsulation layer 270.

[0181] In this case, the color filter layer 280 may include color filter patterns 281, 283, and 285 formed corresponding to the pixel regions SP1, SP2, and SP3, respectively, and second partition walls PW2 formed between the color filter patterns 281, 283, and 285.

[0182] In this case, edges of the color filter patterns 281, 283, and 285 may be curved.

[0183] The color filter patterns 281, 283, and 285 may have a third refractive index, and the second partition wall PW2 may have a fourth refractive index lower than the third refractive index.

[0184] In this case, the third refractive index may be in a range of 1.6 to 1.85, and the fourth refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0185] The second partition wall PW2 may be formed of silicon oxide, but embodiments are not limited thereto.

[0186] Due to the second partition wall PW2 having a refractive index lower than that of the color filter patterns 281, 283, and 285, light that is incident obliquely on the color filter patterns 281, 283, and 285 from the light-emitting layer 242 of the light emitting diodes D1, D2, and D3 may be reflected by the second partition wall PW2 and be output to upper areas of the corresponding pixel regions SP1, SP2, and SP3. Accordingly, a problem in which color mixture occurs in a viewing angle direction may be prevented.

[0187] Further, since the second partition wall PW2 be-

tween the color filter patterns 281, 283, and 285 has a relatively fine width, an emissive area may be increased in comparison to a conventional case in which a black matrix is disposed.

[0188] Particularly, the second partition wall PW2 of the electroluminescent display device 200 according to the second embodiment of the present disclosure may be formed corresponding to the first partition wall PW1.

[0189] That is, the first partition wall PW1 and the second partition wall PW2 may be disposed to be parallel to each other in a first direction perpendicular to the substrate 210.

[0190] Due to the first partition wall PW1 and the second partition wall PW2 being disposed to be parallel to each other in the first direction, light that is output from the light emitting diodes D1, D2, and D3 respectively formed in the pixel regions SP1, SP2, and SP3 may be output to upper areas of the corresponding pixel regions SP1, SP2, and SP3. Accordingly, light extraction efficiency may be improved, and color mixture may be effectively prevented.

[0191] FIG. 5 is an enlarged view of a portion of an electroluminescent display device according to the second embodiment of the present disclosure.

[0192] As illustrated in FIG. 5, the electroluminescent display device 200 of FIG. 4 according to the second embodiment of the present disclosure may include a substrate 210 of FIG. 4, light emitting diodes D disposed on the substrate 210 of FIG. 4, a encapsulation layer 270 disposed on the light emitting diodes D, and a color filter layer 280 disposed on the encapsulation layer 270.

[0193] An interlayer insulating layer 228 and a passivation layer 234 may be disposed between the substrate 210 of FIG. 4 and the light emitting diodes D.

[0194] In this case, since holes h1 and h2 configured to partition pixel regions SP are formed in the interlayer insulating layer 228 and the passivation layer 234, the light emitting diodes D may be spaced apart from each other and disposed in the pixel regions SP, respectively.

[0195] Due to the holes h1 and h2 formed in the passivation layer 234 and the interlayer insulating layer 228, a bank layer which is formed in a conventional electroluminescent display device in order to partition pixel regions SP may be omitted, and a process may be simplified.

[0196] The electroluminescent display device 200 has an under-cut form in which the width of the interlayer insulating layer 228 is smaller than the width of the passivation layer 234 disposed in each of the pixel regions SP.

[0197] Also, a first electrode 241 configured to cover an upper surface and a side surface of the passivation layer 234 may be disposed.

[0198] In this case, since the interlayer insulating layer 228 and the passivation layer 234 have the under-cut form, the first electrode 241 separately formed in each of the pixel regions SP may be formed by one process so that the process may be simplified.

[0199] An insulating pattern IP configured to cover a side surface and a portion of an upper surface of the first electrode 241 may be disposed.

[0200] When forming a light-emitting layer 242 on the first electrode 241 using such an insulating pattern IP, the light-emitting layer 242 is formed to have a relatively small thickness on a stepped area of the first electrode 241 so that a current which does not contribute to emission is prevented from being focused. Accordingly, current efficiency may be improved.

[0201] The light-emitting layer 242 configured to cover the first electrode 241 and the insulating pattern IP may be disposed.

[0202] In this case, since the interlayer insulating layer 228 and the passivation layer 234 of the electroluminescent display device 200 according to the second embodiment of the present disclosure have the under-cut form, the light-emitting layer 242 separately formed in each of the pixel regions SP may be formed by one process.

[0203] The second electrode 243 configured to cover an upper surface and a side surface of the light-emitting layer 242 may be disposed.

[0204] The first electrode 241, the insulating pattern IP, the light-emitting layer 242, and the second electrode 243 may form each of the light emitting diodes D, and the light emitting diodes D may be separated from each other and disposed corresponding to the pixel regions SP, respectively.

[0205] The encapsulation layer 270 may be disposed on the light emitting diodes D formed corresponding to the pixel regions SP, respectively.

[0206] In this case, the encapsulation layer 270 may include an encapsulation film 271 having a first refractive index and a first partition wall PW1 having a second refractive index lower than the first refractive index.

[0207] In this case, the encapsulation film 271 may be disposed in the form in which the encapsulation film 271 covers each of the light emitting diodes D formed corresponding to each of the pixel regions SP.

[0208] In this case, the encapsulation film 271 may be formed of an inorganic film and/or have a multilayer structure.

[0209] Since the encapsulation film 271 has a structure in which the encapsulation film 271 covers each of the light emitting diodes D, permeation of oxygen or moisture into the light-emitting layer 242 and the second electrode 243 may be more effectively prevented.

[0210] A residual layer OM may be present between the light emitting diodes D.

[0211] In this case, the residual layer OM is formed from materials, which are to be used in forming the light emitting diodes D and the encapsulation film 271, remaining in the hole h1 of the interlayer insulating layer 228.

[0212] The first partition wall PW1 may be disposed between the encapsulation films 271 corresponding to the boundary between the pixel regions SP.

[0213] Although a middle portion of the first partition wall PW1 is illustrated as having a bar shape and an

upper portion of the first partition wall PW1 is illustrated as having a shape in which a width progressively increases in the drawings, this is merely an example. The first partition wall PW1 may be formed such that the upper portion and the middle portion have the same width.

[0214] Also, a lower portion of the first partition wall PW1 of the electroluminescent display device 200 according to the second embodiment of the present disclosure may be formed to have a width larger than that of the middle portion, and a lower surface of the first partition wall PW1 may contact the residual layer OM.

[0215] In this case, a width d1 of the middle portion of the first partition wall PW1 may be in a range of 2 μm to 3 μm . The width of the upper portion of the first partition wall PW1 may be larger than or equal to the width d1 of the middle portion of the first partition wall PW1. However, embodiments are not limited thereto, and the size and form of the first partition wall PW1 may be modified in various ways according to the size, resolution, and the like of the pixel regions SP.

[0216] Also, a height H1 of the first partition wall PW1 may be in a range of 7 μm to 9 μm , but embodiments are not limited thereto. The height H1 may be modified in various ways according to a thickness or the like of the passivation layer 234, the interlayer insulating layer 228, and the light emitting diodes D.

[0217] In this case, the first partition wall PW1 may be an organic material having a second refractive index lower than the first refractive index of the encapsulation film 271. For example, the first refractive index may be in a range of 1.6 to 1.85, and the second refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0218] Due to the first partition wall PW1 having a refractive index lower than that of the encapsulation film 271, light that is incident obliquely on the encapsulation film 271 from the light-emitting layer 242 of the light emitting diodes D may be reflected by the first partition wall PW1 and be output upward. Accordingly, light extraction efficiency of the electroluminescent display device 200 may be improved, and color mixture may be prevented.

[0219] In addition, by forming the first partition wall PW1 between the encapsulation films 271 configured to respectively cover the light emitting diodes D, efficiency of preventing infiltration of oxygen and moisture into the light-emitting layer 242 and the second electrode 243 may be further improved.

[0220] Further, by the width of the lower portion of the first partition wall PW1 being formed larger than the width of the middle portion thereof and the lower surface of the first partition wall PW1 having a structure in which the lower surface contacts the residual layer OM, stability of the light emitting diodes D may be further improved.

[0221] The color filter layer 280 may be disposed on the encapsulation layer 270.

[0222] In this case, the color filter layer 280 may include color filter patterns 281, 283, and 285 formed corresponding to the pixel regions SP, respectively, and a sec-

ond partition walls PW2 formed between the color filter patterns 281, 283, and 285.

[0223] The color filter patterns 281, 283, and 285 may have a third refractive index, and the second partition wall PW2 may have a fourth refractive index lower than the third refractive index.

[0224] In this case, the third refractive index may be in a range of 1.6 to 1.85, and the fourth refractive index may be in a range of 1.0 to 1.55, but embodiments are not limited thereto.

[0225] A width d2 of a middle portion of the second partition wall PW2 may be in a range of 2 μm to 3 μm . The width of an upper portion of the second partition wall PW2 may be larger than or equal to the width d2 of the middle portion of the second partition wall PW2. However, embodiments are not limited thereto.

[0226] Also, a height H2 of the second partition wall PW2 may be in a range of 7 μm to 9 μm , but embodiments are not limited thereto. The height H2 may be modified in various ways according to a thickness or the like of the color filter patterns 281, 283, and 285.

[0227] The second partition wall PW2 may be formed of silicon oxide, but embodiments are not limited thereto. The second partition wall PW2 may also be formed of an air gap.

[0228] Due to the second partition wall PW2 having a refractive index lower than that of the color filter patterns 281, 283, and 285, light L2 that is incident obliquely on the color filter patterns 281, 283, and 285 from the light-emitting layer 242 of the light emitting diodes D may be reflected by the second partition wall PW2 and be output upward. Accordingly, a problem in which color mixture occurs in a viewing angle direction may be prevented.

[0229] Further, since the second partition wall PW2 between the color filter patterns 281, 283, and 285 has a relatively fine width d2, an emissive area may be increased in comparison to the conventional case in which a black matrix is disposed.

[0230] A scattering layer SL may be disposed on an upper surface of each of the color filter patterns 281, 283, and 285.

[0231] In this case, the scattering layer SL may be a concavo-convex pattern formed on the upper surface of each of the color filter patterns 281, 283, and 285, but embodiments are not limited thereto. The scattering layer SL may also be formed of a material layer including beads.

[0232] Accordingly, light that passes through the color filter patterns 281, 283, and 285 and is output to the outside may be scattered in various directions.

[0233] Particularly, by scattering a portion of light L3, which is incident vertically on the color filter patterns 281, 283, and 285 at a boundary between the pixel regions SP, toward the second partition wall PW2, perception of lattices that may occur due to the fine second partition wall PW2 being viewed as a black area may be prevented when one views an image in a state in which one's eyes are close to a screen, such as when one views an image

using a VR device.

[0234] Particularly, the second partition wall PW2 of the electroluminescent display device 200 of FIG. 5 according to the second embodiment of the present disclosure may be formed corresponding to the first partition wall PW1.

[0235] That is, the first partition wall PW1 and the second partition wall PW2 may be disposed to be parallel to each other in a first direction 1A perpendicular to the substrate 110.

[0236] Due to the first partition wall PW1 and the second partition wall PW2 being disposed to be parallel to each other in the first direction 1A, light that is output from the light emitting diodes D respectively formed in the pixel regions SP may be output to upper areas of the corresponding pixel regions SP. Accordingly, light extraction efficiency may be improved, and color mixture may be effectively prevented.

[0237] FIG. 6 is a graph schematically illustrating light extraction efficiency according to refractive indices of first and second partition walls according to the first and second embodiments of the present disclosure.

[0238] That is, FIG. 6 is a graph showing light extraction efficiency according to a change in refractive indices of first and second partition walls PW1 and PW2 of FIG. 5 when refractive indices of an encapsulation film 271 of FIG. 5 and color filter patterns 281, 283, and 285 of FIG. 5 are 1.7.

[0239] As illustrated in FIG. 6, it can be seen that light extraction efficiency increases as the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 decreases from 1.55 to 1.4.

[0240] That is, it is shown that light extraction efficiency is 47 when the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 are 1.55, light extraction efficiency is 51 when the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 are 1.5, light extraction efficiency is 55.5 when the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 are 1.45, and light extraction efficiency is 59 when the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 are 1.4.

[0241] Accordingly, it can be seen that light extraction efficiency is the highest when the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 are 1.4.

[0242] That is, a path of light that is obliquely output outward from light emitting diodes D may be adjusted through the first and second partition walls PW1 and PW2 of FIG. 5 and a largest amount of light may be output to the outside when the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 are 1.4.

[0243] Accordingly, light extraction efficiency may be further improved by setting the refractive indices of the first and second partition walls PW1 and PW2 of FIG. 5 of the electroluminescent display device 100 of FIG. 2 and the electroluminescent display device 200 of FIG. 4 according to the first and second embodiments of the

present disclosure to be 1.4.

[0244] In the present disclosure, a first partition wall having a low refractive index is disposed between light emitting diodes so that a path of light that is not output to the outside due to being totally reflected inside the light emitting diodes is changed and the light is allowed to be output to the outside. Accordingly, light extraction efficiency can be improved.

[0245] Further, a second partition wall having a low refractive index is disposed between color filter patterns so that a path of light that travels to an adjacent pixel region is changed and the light is allowed to be output to the corresponding pixel region. Accordingly, color mixture can be prevented.

Claims

1. An electroluminescent display device comprising:
 - a substrate (110, 210) including a plurality of pixel regions (SP);
 - a plurality of light emitting diodes (D) spaced apart from each other on the substrate (110, 210) and corresponding to the plurality of pixel regions (SP), respectively;
 - an encapsulation film (171, 271) respectively covering the plurality of light emitting diodes (D) and having a first refractive index;
 - a first partition wall (PW1) disposed between the encapsulation film (171, 271) corresponding to a boundary between the plurality of pixel regions (SP) and having a second refractive index lower than the first refractive index.
2. The electroluminescent display device of claim 1, further comprising a color filter layer (180, 280) disposed on the encapsulation film (171, 271) and the first partition wall (PW1), wherein the color filter layer (180, 280) includes a plurality of color filter patterns (181, 183, 185; 281, 283, 285) having a third refractive index and a second partition wall (PW2) disposed between the plurality of color filter patterns (181, 183, 185; 281, 283, 285) and having a fourth refractive index lower than the third refractive index.
3. The electroluminescent display device of claim 2, wherein the second partition wall (PW2) is disposed corresponding to the first partition wall (PW1).
4. The electroluminescent display device of claim 2 or 3, wherein the plurality of color filter patterns (181, 183, 185; 281, 283, 285) are disposed to correspond to the plurality of light emitting diodes (D), respectively.
5. The electroluminescent display device of any one of claims 1, 2, 3 or 4, wherein a middle portion of each

of the first partition wall (PW1) and/or the second partition wall (PW2) has a bar shape.

6. The electroluminescent display device of any one of the preceding claims, wherein an upper portion of each of the first partition wall (PW1) and the second partition wall (PW2) has a width which progressively increases upward. 5
7. The electroluminescent display device of claim 5 or 6, wherein 10
 - a width of the middle portion of each of the first partition wall (PW1) and/or the second partition wall (PW2) is in a range of 2 μm to 3 μm ;
 - and/or 15
 - a height of each of the first partition wall (PW1) and/or the second partition wall (PW2) is in a range of 7 μm to 9 μm .
8. The electroluminescent display device as claimed in any one of the preceding claims, wherein each of the second refractive index and/or the fourth refractive index is in a range of 1.0 to 1.55. 20
9. The electroluminescent display device as claimed in any one of the preceding claims, wherein the color filter layer (180, 280) further includes a scattering layer (SL) disposed on an upper surface of each of the plurality of color filter patterns (181, 183, 185; 281, 283, 285); and/or an edge of each of the plurality of color filter patterns (181, 183, 185; 281, 283, 285) is curved. 25 30
10. The electroluminescent display device as claimed in any one of the preceding claims, wherein each of the plurality of light emitting diodes (D) includes: 35
 - a first electrode (141, 241) disposed on a passivation layer (134, 234);
 - an insulating pattern (IP) configured to cover an edge of the first electrode (141, 241); 40
 - a light-emitting layer (142, 242) disposed on the first electrode (141, 241) and the insulating pattern (IP); and
 - a second electrode (143, 243) disposed on the light-emitting layer (142, 242). 45
11. The electroluminescent display device of claim 10, further including an interlayer insulating layer (128, 228) disposed under the passivation layer (134, 234), wherein the passivation layer (134, 234) and the interlayer insulating layer (128, 228) for each pixel region (SP) are separated by the first partition wall (PW1). 50
12. The electroluminescent display device as claimed in any one of the preceding claims, wherein two adjacent light emitting diodes (D1, D2, and D3) are par- 55

tioned by a hole (h) in the passivation layer (134) and the interlayer insulating layer (128).

13. The electroluminescent display device as claimed in any one of the preceding claims, wherein an encapsulation layer (170) includes the encapsulation film (171) having the first refractive index and the first partition wall (PW1) having a second refractive index lower than the first refractive index.
14. The electroluminescent display device as claimed in any one of the preceding claims, further comprising a hole (h) having different portions (h1) and (h2) configured to partition the pixel regions (SP1, SP2, SP3) in the interlayer insulating layer (228) and the passivation layer (234), wherein a width of a first portion (h1) is larger than a width of a second portion (h2).

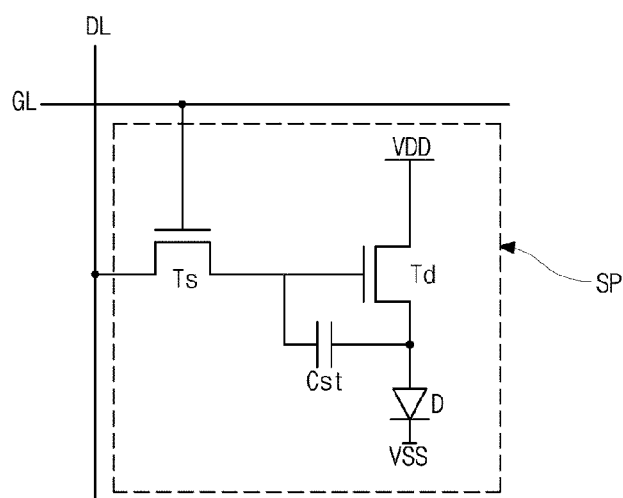


FIG. 1

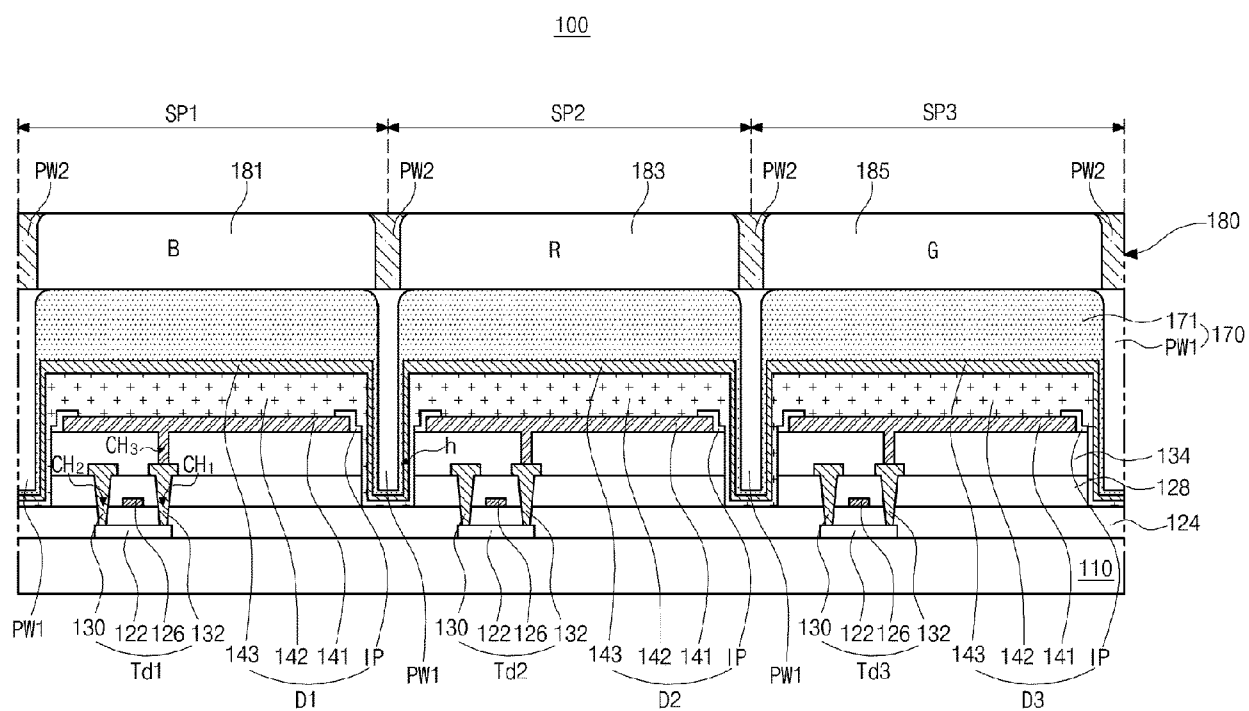


FIG. 2

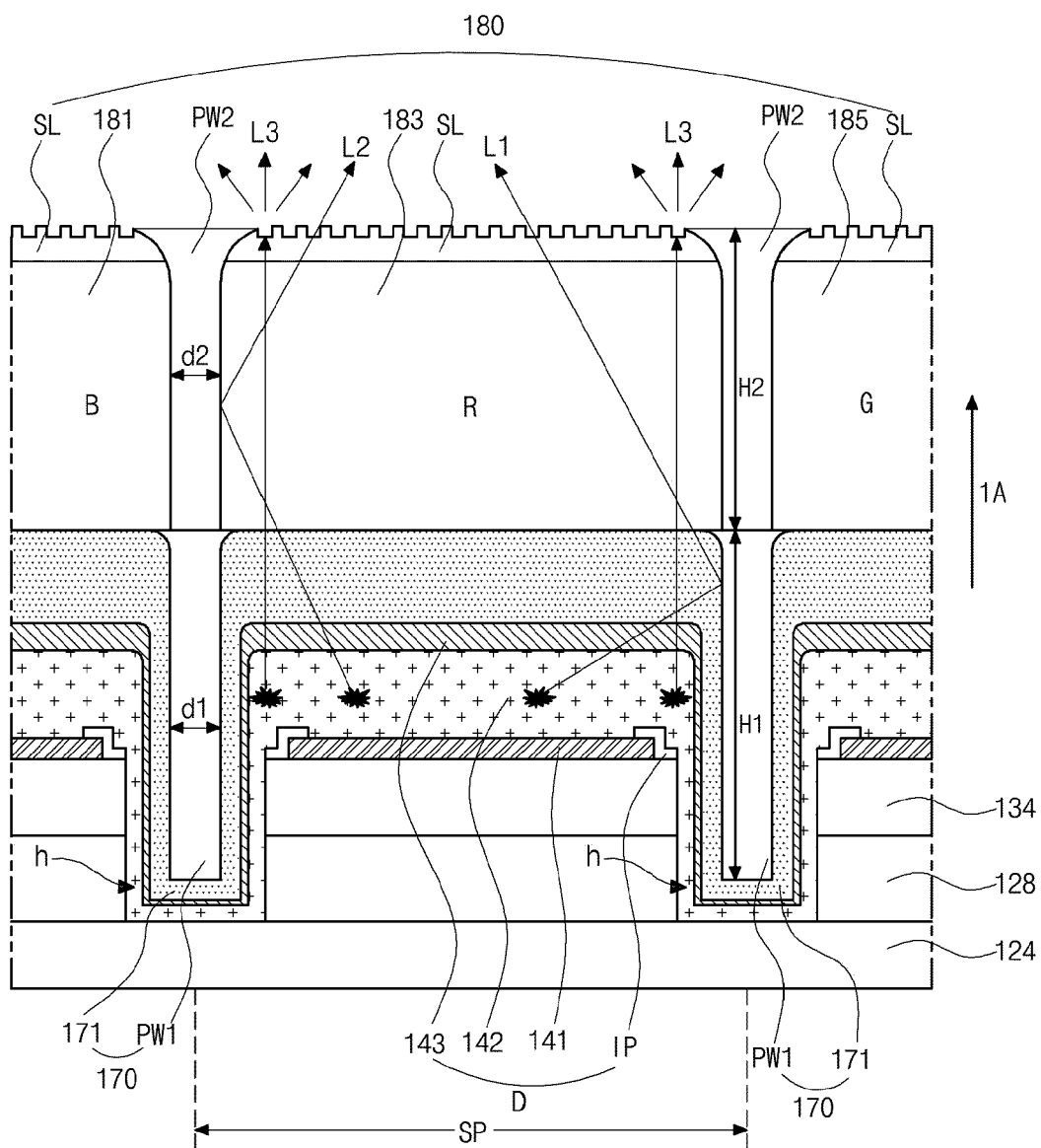


FIG. 3

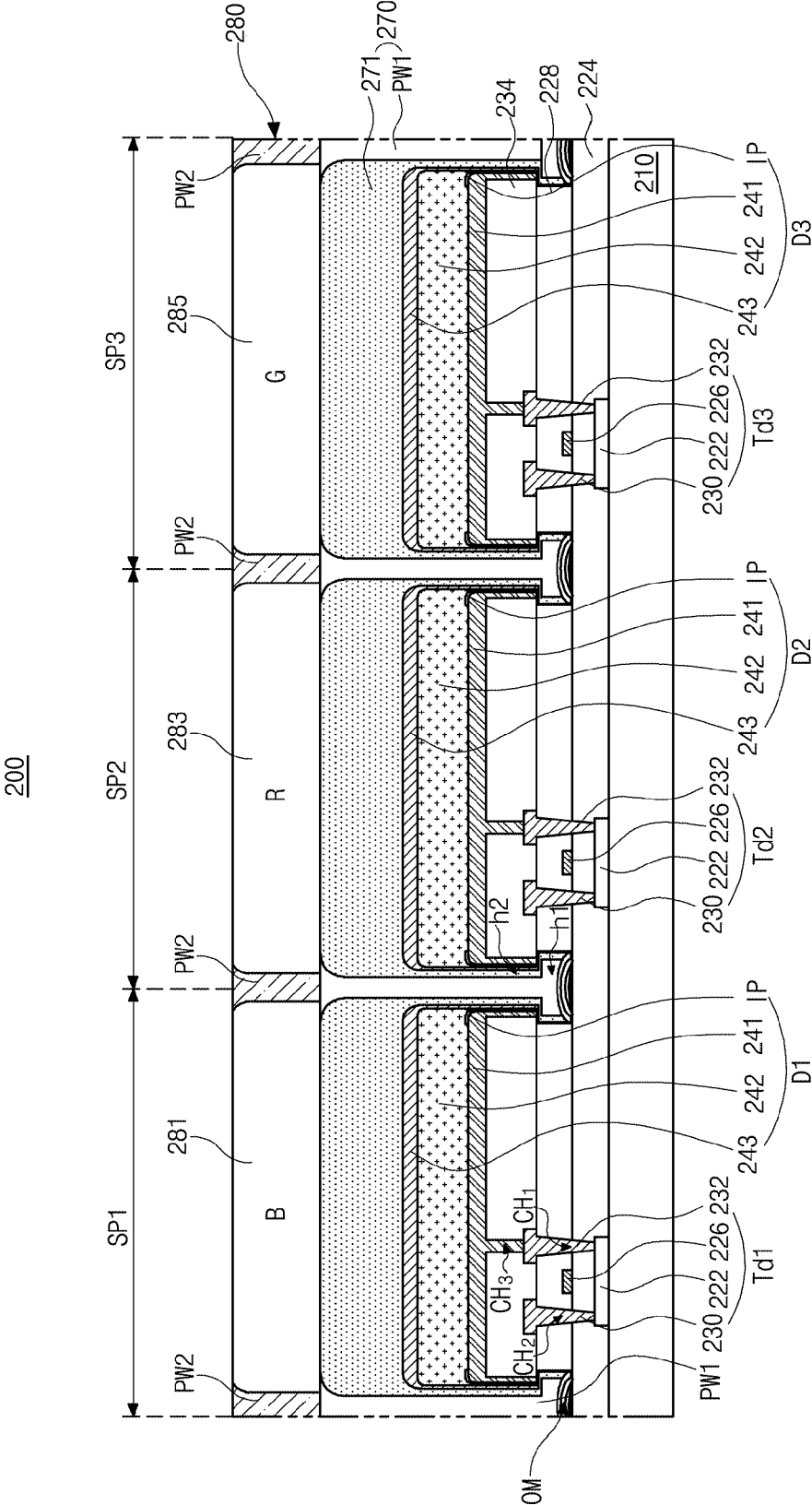


FIG. 4

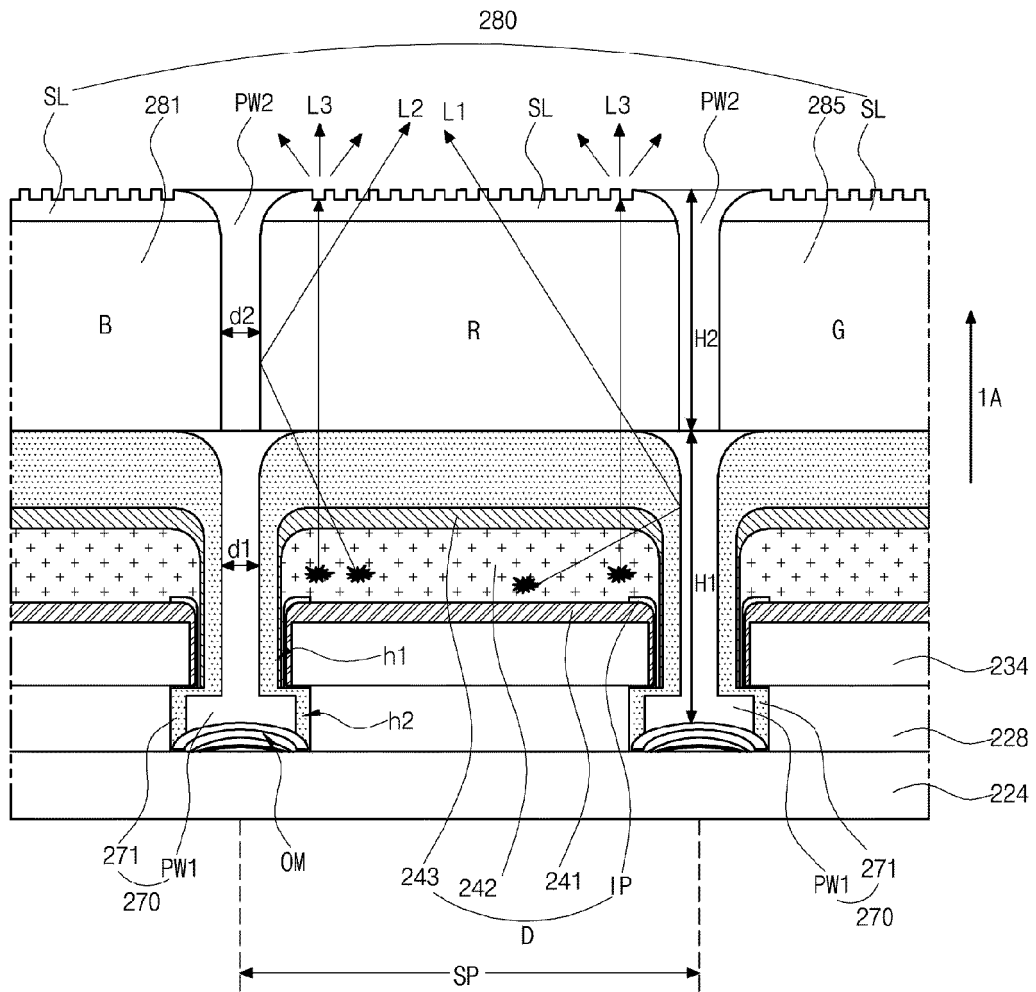


FIG. 5

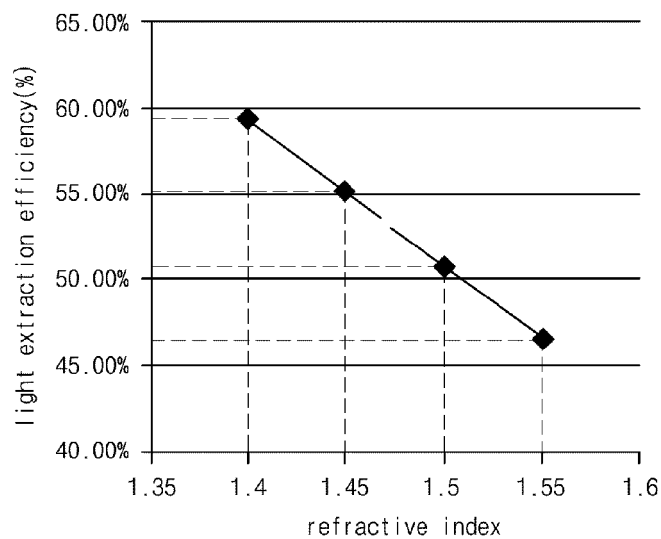


FIG. 6



EUROPEAN SEARCH REPORT

Application Number
EP 18 21 0235

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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X	US 2016/087245 A1 (PARK CHAN YOUNG [KR] ET AL) 24 March 2016 (2016-03-24) * paragraph [0038] - paragraph [0068]; figure 2 *	1	
X	US 2015/188092 A1 (PARK JAE-HYUN [KR] ET AL) 2 July 2015 (2015-07-02) * paragraph [0037] - paragraph [0038]; figures 4, 7 *	1	
X	US 2006/202613 A1 (KAWAGUCHI KOJI [JP] ET AL) 14 September 2006 (2006-09-14) * paragraph [0017] - paragraph [0060]; figure 1 *	1	
			TECHNICAL FIELDS SEARCHED (IPC)
			H01L
The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 9 April 2019	Examiner Bernabé Prieto, A
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

EPO FORM 1503 03/02 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 18 21 0235

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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专利名称(译)	电致发光显示装置		
公开(公告)号	EP3496176A1	公开(公告)日	2019-06-12
申请号	EP2018210235	申请日	2018-12-04
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	PARK HAN SUN BANG HYUNG SEOK PARK JI YEON		
发明人	LIM, HYEONG-JUN PARK, HAN-SUN BANG, HYUNG-SEOK PARK, JI-YEON		
IPC分类号	H01L51/52 H01L27/32		
CPC分类号	H01L27/322 H01L27/3244 H01L51/5268 H01L51/5271 H01L51/5275 H01L27/3211 H01L51/5012 H01L51/5206 H01L51/5221 H01L51/5256		
优先权	1020170166006 2017-12-05 KR		
其他公开文献	EP3496176B1		
外部链接	Espacenet		

摘要(译)

一种电致发光显示装置，包括：基板，包括多个像素区域；多个发光二极管，分别在基板上彼此隔开并对应于多个像素区域；封装膜分别覆盖多个发光二极管并具有第一折射率；第一分隔壁，设置在所述封装膜之间，对应于所述多个像素区域之间的边界，并且具有低于所述第一折射率的第二折射率；以及设置在所述封装膜和所述第一分隔壁上的滤色器层，其中所述滤色器层包括多个具有第三折射率的滤色器图案和设置在所述多个滤色器图案之间并具有第四折射率的第二分隔壁，所述第二分隔壁折射率低于第三折射率。

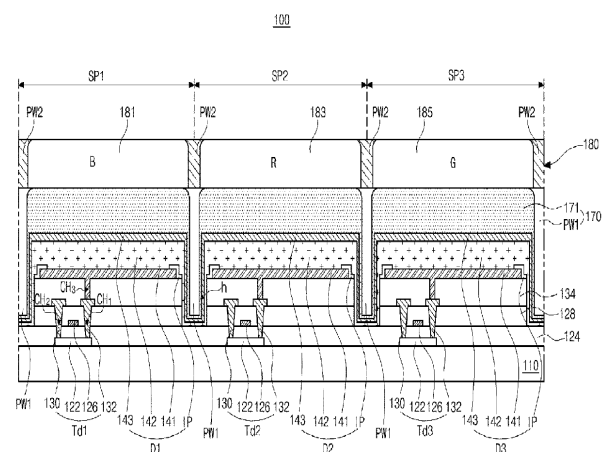


FIG. 2