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(54) **DISPLAY BACKPLATE AND MANUFACTURING METHOD THEREFOR, AND DISPLAY DEVICE**

(57) The present invention provides a display backplane and a manufacturing method thereof, as well as a display device. The display backplane comprising: a substrate; an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements formed on the substrate; and a heat insulation layer formed between the array of organic light emitting elements and the array of transistors, wherein the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements. The display backplane provided in the present invention can reduce the conduction of heat generated by the array of organic light emitting elements during lighting to the array of transistors, thus avoiding problems caused thereby such as uneven display.

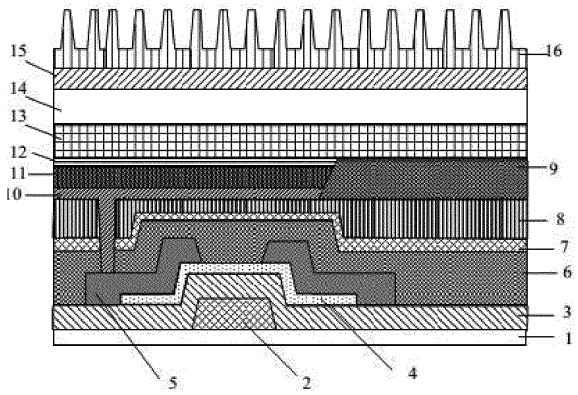

Fig. 1

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Description

Related Applications

[0001] The present application claims the benefit of Chinese Patent Application No. 201510111902.7, filed on March 13, 2015, the entire disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to the field of display technology, and in particular to a display backplane and a manufacturing method thereof, as well as a display device.

BACKGROUND ART

[0003] Oxide backplanes have attracted wide attention for their excellent performances. However, the performances of oxide backplanes are sensitive to factors such as heat and light, and this problem is even more prominent for an AMOLED display screen made of an oxide backplane. Since an active-matrix organic light-emitting diode (AMOLED) is driven by current, the temperature of the oxide backplane will easily rise during lightening, which influences the performances of the oxide backplane and thus gives rise to problems such as decreased display brightness, a shortened service lifetime and large-size unevenness of display brightness.

SUMMARY

[0004] In regard to defects in the prior art, one goal of the present invention is to reduce the influence of heat generated by the OLED on the display backplane.

[0005] The present invention provides a display backplane, comprising: a substrate; an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements formed on the substrate; and a heat insulation layer formed between the array of organic light emitting elements and the array of transistors, wherein the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements.

[0006] The above display backplane provided according to the present invention has a heat insulation layer formed between the array of organic light emitting elements and the array of transistors, wherein the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements. Thus, the conduction of heat generated by the array of organic light emitting elements during lighting to the array of transistors can be reduced, and accordingly problems caused thereby such as uneven display can be avoided.

[0007] According to embodiments of the present invention, the display backplane further comprises: a passivation layer formed between the array of organic light emitting elements and the array of transistors, wherein

the heat insulation layer is positioned between the passivation layer and the bottom electrode of the organic light emitting element in the array of organic light emitting elements; and

the passivation layer is provided with a passivation layer via hole formed therein, the position of which corresponds to that of the heat insulation layer via hole, and the drain of the transistor in the array of transistors is connected with the bottom electrode of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

[0008] Thus, mutual interferences between the array of organic light emitting elements and the array of transistors are avoided by taking advantage of the passivation layer. Moreover, the formation of a corresponding passivation layer via hole ensures the connection between the array of transistors and the array of organic light emitting elements.

[0009] According to embodiments of the present invention, the slope angle of the heat insulation layer via hole is smaller than or equal to 60° With such a slope angle, breakage of the bottom electrode of the organic light emitting element in the array of organic light emitting elements can be avoided. Furthermore, the slope angle of the heat insulation layer via hole is 40-60°.

[0010] According to embodiments of the present invention, the display backplane further comprises: a heat conduction layer formed on a side of the array of the organic light emitting elements away from the array of the transistors. With this heat conduction layer, heat generated by the organic light emitting elements during lighting can be effectively conducted in a direction opposite to the array of the transistors, and influence of the heat generated by the organic light emitting elements on the performance of the active layer is further reduced.

[0011] According to embodiments of the present invention, the display backplane further comprises: an encapsulation layer for encapsulating the substrate on which the array of organic light emitting elements and the array of transistors are formed, wherein the heat conduction layer is formed between the array of organic light emitting elements and the encapsulation layer.

[0012] According to embodiments of the present invention, the display backplane further comprises: a cover plate and a heat dissipation layer arranged on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is arranged between the heat dissipation layer and the encapsulation layer. Thereby, the dissipation of heat generated by the organic light emitting elements out from the display is further accelerated.

[0013] According to embodiments of the present invention, the heat dissipation layer comprises a heat dissipation sheet and a heat dissipation pin, the heat dissipation

pin being formed on a side of the heat dissipation sheet away from the cover plate.

[0014] The present invention further provides a method for manufacturing a display backplane, comprising:

forming on a substrate an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements; and

forming a heat insulation layer between the array of organic light emitting elements and the array of transistors, wherein

the heat insulation layer is provided with a heat insulation layer via hole formed therein, through which the array of transistors is connected with the array of organic light emitting elements.

[0015] In a manner similar to the effect of the above display backplane provided in the present invention, with a display backplane manufactured using the above method of the present invention, the conduction of heat generated by the array of organic light emitting elements during lighting to the array of transistors can be reduced, and accordingly problems caused thereby such as uneven display can be avoided.

[0016] According to embodiments of the present invention, the method further comprises: forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of transistors. Likewise, with this heat conduction layer, heat generated by the organic light emitting elements during lighting can be effectively conducted in a direction opposite to the array of the transistors, and influence of the heat generated by the organic light emitting elements on the performance of the active layer is further reduced.

[0017] According to embodiments of the present invention, the method further comprises: forming an encapsulation layer for encapsulating the substrate on which the array of organic light emitting elements and the array of transistors are formed; wherein

the step of forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of transistors comprises:

forming a heat conduction layer between the array of organic light emitting elements and the encapsulation layer.

[0018] According to embodiments of the present invention, the method further comprises: forming a cover plate and a heat dissipation layer on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is formed between the heat dissipation layer and the encapsulation layer. Likewise, with the heat dissipation layer, the dissipation of heat generated by the organic light emitting elements out from the display is further accelerated.

[0019] According to embodiments of the present invention, the method further comprises: forming a passivation layer between the array of organic light emitting elements and the array of transistors, wherein

the heat insulation layer is positioned between the passivation layer and the bottom electrode of the organic light emitting element in the array of organic light emitting elements; and

the passivation layer is provided with a passivation layer via hole formed therein, the position of which corresponds to that of the heat insulation layer via hole, and the drain of the transistor in the array of transistors is connected with the bottom electrode of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

[0020] Thus, mutual interferences between the array of organic light emitting elements and the array of transistors are avoided, and moreover, by taking advantage of a corresponding passivation layer via hole, the connection between the array of transistors and the array of organic light emitting elements is ensured.

[0021] Furthermore, the step of forming the heat insulation layer comprises:

coating a mixed material of a heat insulation material and a photoresist onto the passivation layer; and

exposing and developing the mixed material coated onto the passivation layer using a photolithography process, to form a heat insulation layer provided with a heat insulation layer via hole.

[0022] The present invention further provides a display device, comprising the above display backplane.

[0023] The technical problem solved by the display device and its related effects are the same as those of the display backplane and the manufacturing method thereof as mentioned above, so no more details shall be described herein for simplicity.

BRIEF DESCRIPTION OF DRAWINGS

[0024]

Fig. 1 is a schematic structural view of a display backplane provided according to embodiments of the present invention; and

Fig. 2 is a schematic view of a possible structure for the heat dissipation layer 16 in Fig. 1.

DETAILED DESCRIPTION OF EMBODIMENTS

[0025] To render the goal of the embodiments of the present invention, the technical solution and the advantages thereof even clearer, the technical solutions ac-

cording to embodiments of the present invention shall be described as follows in a clear and complete manner with reference to the drawings in the embodiments of the present invention. Obviously, the embodiments described here are only a part of the embodiments of the present invention, rather than all of them. Based on the embodiments of the present invention, all other embodiments obtained by those having ordinary skills in the art without inventive efforts, shall fall within the protection scope of the present invention.

[0026] The display backplane of the present invention comprises: a substrate, an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements formed on the substrate, and a heat insulation layer formed between the array of organic light emitting elements and the array of transistors, wherein the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements.

[0027] Since a heat insulation layer is formed between the array of organic light emitting elements and the array of transistors, and the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements, in this case, the conduction of heat generated by the array of organic light emitting elements during lighting to the array of transistors can be reduced, and accordingly problems caused thereby such as uneven display can be avoided.

[0028] Fig. 1 is a schematic structural view of a display backplane provided according to embodiments of the present invention, wherein the display backplane comprises:

glass substrate 1; a gate electrode pattern 2 formed on the glass substrate 1; a gate insulation layer 3 formed over the gate electrode pattern 2 and the glass substrate 1; an active layer pattern 4 formed over the gate insulation layer 3; a source-drain electrode pattern 5 formed over the active layer pattern 4; a passivation layer 6 formed over the active layer pattern 4 and the source-drain electrode pattern 5; a heat insulation layer 7 formed over the passivation layer 6; a resin layer 8 formed over the heat insulation layer 7; a pixel defining layer pattern 9, a bottom electrode pattern 10, a light emitting layer pattern 11 and a top electrode pattern 12 formed over the resin layer 8; a heat conduction layer 13 formed over the pixel defining layer pattern 9 and the top electrode pattern 12; an encapsulation layer 14 formed over the heat conduction layer 13; cover plate glass 15 formed on the encapsulation layer 14; and a heat dissipation layer 16 formed over the cover plate glass 15. In this case, the active layer pattern 4 can be formed from semiconductor materials such as metal oxides, polycrystalline silicon, amorphous silicon and the like; correspondingly, a passivation layer via hole, a heat insulation layer via hole and a resin layer via hole are formed respectively in the passivation layer 6, the heat insulation layer 7 and the resin layer 8, the positions of the passivation layer via hole, the heat insulation layer via hole and the resin layer via hole corresponding with each other, and the top electrode pattern 12 is connected with the source-drain electrode pattern 5 via the above via holes having corresponding positions. The gate electrode pattern 2, the gate insulation layer 3, the active layer pattern 4 and the source-drain electrode pattern 5 here together form an array of transistors, and the bottom electrode pattern 10, the light emitting layer pattern 11 and the top electrode pattern 12 together form an array of organic light emitting elements. Glass substrate 1 is an instance for the substrate. Besides, the substrate can be formed from materials such as transparent resin, quartz, sapphire and the like, which will not be limited in the present invention.

[0029] According to embodiments of the present invention, since the heat insulation layer 7 is formed between the passivation layer 6 and the bottom electrode pattern 10, the influence of heat generated by the organic light emitting elements during lighting on the performance of the array of transistors can be effectively avoided, and accordingly problems caused thereby such as uneven display brightness can be avoided. Meanwhile, according to embodiments of the present invention, since a heat conduction layer 13 is further formed over the top electrode pattern 12, heat generated by the organic light emitting elements during lighting can be effectively conducted in a direction opposite to the array of transistors, and hence the influence of heat generated by the organic light emitting elements during lighting on the performance of the active layer is further reduced. On the other hand, according to embodiments of the present invention, a heat dissipation layer 16 is further formed outside the cover plate glass 15, which can also further accelerate the dissipation of heat generated by the organic light emitting elements out form the display.

[0030] It should be noted that although Fig. 1 shows a situation where the heat insulation layer 7 is formed between the passivation layer 6 and the resin layer 8, the position of the heat insulation layer 7 is not limited thereto in an actual application. For example, the heat insulation layer can also be arranged between the resin layer 8 and the bottom electrode pattern 10, or the passivation layer 6 or the resin layer 8 can also be formed from a material having heat insulation function. As long as the heat insulation layer is arranged between the array of transistors and the array of organic light emitting elements such that respective solutions can all achieve the goal of reducing the influence of heat generated by the organic light emitting elements on the performance of the active layer, the corresponding technical solutions shall all fall within the protection scope of the present invention. In addition, structures such as a passivation layer, a resin layer and

a pixel defining layer pattern are not necessarily present as they can be added or deleted upon the actual or design need. In specific implementations, when only the heat insulation layer 7 is arranged without the heat conduction layer 13 and/or the heat dissipation layer 16 in Fig. 1, such a technical solution can also reduce to a certain degree the influence of heat generated by the organic light emitting elements on the performance of the active layer, so the corresponding technical solution shall also fall within the protection scope of the present invention.

[0031] In an actual application, the heat insulation layer 7 here can consist of one or more materials with a low thermal conductivity. For example, the material of the heat insulation layer can have a thermal conductivity of 0-0.5W/mK, such as polystyrene (the thermal conductivity of which is 0.08W/mK), polyethylene (the thermal conductivity of which is 0.3W/mK) and so on. The thickness of the heat insulation layer 7 can be 1-2μm. In specific implementations, the heat insulation layer 7 here can be made by coating, evaporation or the like.

[0032] In specific implementations, in order to avoid breakage of the bottom electrode pattern 10, the slope angle of the heat insulation layer via hole can be arranged as smaller than or equal to 60°. For instance, in WOLED + COA (White OLED + Color filter On Array), if the heat insulation layer 7 is arranged between the passivation layer 6 and a color film layer, the slope angle of the heat insulation layer via hole can be arranged as smaller than or equal to 60° if the heat insulation layer 7 is arranged over the resin layer 8 and d between the bottom electrode pattern 10, the slope angle of the heat insulation layer via hole can be arranged as between 40-60°. Besides, in a PLED structure (a P-type LED), the heat insulation layer 7 can be deposited between the passivation layer 6 and the bottom electrode pattern 10, wherein the slope angle of the via hole is 40-60°.

[0033] When the above display backplane is a bottom emission type display backplane, the light transmittance of the heat insulation layer 7 can be arranged as greater than or equal to 95% so as to ensure the transmittance of the display backplane.

[0034] The material of the heat conduction layer 13 may have a thermal conductivity of 100W/mK to 8000W/mK. For instance, it can consist of one or more materials with a high thermal conductivity, such as silver, copper, gold, aluminum, diamond, graphite, graphene, carbon nanotube and so on. The thickness of the heat conduction layer 13 can be 1-100μm. The above materials can be deposited over the top electrode pattern 12 by sputtering, evaporation, coating or the like to form the heat conduction layer 13.

[0035] In an actual application, the material of the heat dissipation layer 16 can have a thermal conductivity of greater than 100W/mK. For example, it can be one or more chosen from the following materials: silver, copper, gold, aluminum, diamond, graphite, grapheme, carbon nanotube and so on.

[0036] As shown in Fig. 2, the heat dissipation layer 16 has a heat dissipation sheet 16a and a heat dissipation pin 16b, the heat dissipation pin 16b being formed on a side of the heat dissipation sheet 16a away from the cover plate glass 14. Such a structure has a better heat dissipation effect.

[0037] In specific implementations, the heat dissipation pin here has a height of at least 1mm, and a width in a range of 1-5mm, and the distance between adjacent heat dissipation pins 16b can be in a range of 2-5mm.

[0038] In specific implementations, materials with a thermal conductivity of greater than 100W/mK can be chosen as the material of the heat dissipation layer, for example, one or more from the group consisting of silver, copper, gold, aluminum, diamond, graphite, grapheme, carbon nanotube and so on. The heat dissipation pin 16b may have different shapes and a larger surface area so as to dissipate heat more quickly. The heat dissipation pin 16b can be made by an etching process.

[0039] In specific implementations, the above display backplane can be either a bottom emission type display backplane or a top emission type display backplane. Fig. 1 shows a situation where it is a bottom emission type display backplane, the bottom electrode pattern 10 here can be an anode, and the corresponding top electrode pattern 12 is a cathode; or, the bottom electrode pattern 10 is a cathode, and the corresponding top electrode pattern 12 is an anode. Besides, the above display backplane can be a WOLED backplane, a PLED backplane and the like as mentioned above.

[0040] In specific implementations, the above heat insulation layer via hole, the passivation layer via hole and the resin layer via hole can be made by photolithography. Furthermore, the aperture of the heat insulation layer via hole can be arranged as greater than that of the passivation layer via hole, and the aperture of the resin layer can be arranged as greater than that of the heat insulation layer via hole.

[0041] In some applications, the above resin layer 8 is not an indispensable structure.

[0042] A further embodiment of the present invention also provides a method for manufacturing a display backplane, which method can be used for manufacturing any display backplane as mentioned above. The method can comprise: forming on a substrate an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements; and forming a heat insulation layer between the array of organic light emitting elements and the array of oxide transistors, wherein the heat insulation layer is provided with a heat insulation layer via hole formed therein, through which the array of oxide transistors is connected with the array of organic light emitting elements.

[0043] In specific implementations, the array of oxide transistors and the array of organic light emitting elements can be formed with reference to the prior art, and a heat insulation layer pattern can be formed between the array of oxide transistors and the array of organic light emitting elements which have been formed. Specif-

ically, a gate electrode pattern, a gate insulation layer, an oxide active layer pattern, a source-drain electrode pattern and a passivation layer can be formed on the substrate sequentially. Then a heat insulation layer pattern is formed over the passivation layer. After the formation of the heat insulation layer pattern, a resin layer, a bottom electrode pattern, a light emitting layer and a top electrode pattern are formed sequentially. If the display backplane to be manufactured is a top emission type display backplane, a reflective layer should also be formed prior to the formation of the gate electrode pattern.

[0044] In specific implementations, when the heat insulation layer pattern is formed directly on the passivation layer, the step of forming a heat insulation layer pattern and a passivation layer pattern can comprise:

forming a passivation layer;

mixing a heat insulation material with a photoresist in a certain proportion and then coating the mixture onto the passivation layer; and

exposing and developing the mixed material layer coated onto the passivation layer using a same mask plate by a photolithography process to form a pattern of the heat insulation layer via hole, and then forming a passivation layer via hole by dry etching.

[0045] The passivation layer via hole formed in the above manner can have a smaller slope angle, thereby avoiding breakage of the bottom electrode pattern.

[0046] Furthermore, the above method can further comprise: forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of oxide transistors. The heat conduction layer here can be formed on a surface of the top electrode pattern by sputtering, evaporation, coating or the like.

[0047] Furthermore, the above method can further comprise: forming an encapsulation layer for encapsulating the substrate on which the array of organic light emitting elements and the array of oxide transistors are formed.

[0048] Here, the step of forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of oxide transistors comprises:

forming a heat conduction layer between the array of organic light emitting elements and the encapsulation layer.

[0049] Furthermore, the method can further comprise: forming a cover plate and a heat dissipation layer on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is formed between the heat dissipation layer and the encapsulation layer.

[0050] In specific implementations, the heat dissipation layer here can be made from a thermally conductive material, and the structure of the heat dissipation layer formed here can be identical to that shown in Fig. 2. Here, the heat dissipation pin therein can be made by an etching process, and the height of the heat dissipation pin can be controlled by controlling the etching time.

[0051] It should be noted that although descriptions are provided in the above embodiments by taking the transistors in the display backplane as oxide transistors, in an actual application, the solution provided in the present invention can also achieve similar effects in a display backplane comprising transistors of other types. Therefore, the corresponding technical solutions shall also fall within the protection scope of the present invention.

[0052] A further embodiment of the present invention further provides a display device comprising any one of the above display backplanes. The display device can be any product or component having a display function, including: an OLED panel, a cell phone, a tablet computer, a television, a display, a notebook computer, a digital photo frame, a navigator and so on.

[0053] The above contents are only specific embodiments of the present invention, but the protection scope of the present invention shall not be limited thereto. Any modification or substitution easily conceivable for any one who is familiar with the art within the technical disclosure of the present invention shall be covered by the protection scope of the present invention. Therefore, the protection scope of the present invention should be subject to the protection scope of the claims.

Claims

1. A display backplane, comprising:

a substrate;
an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements formed on the substrate; and
a heat insulation layer formed between the array of organic light emitting elements and the array of transistors, wherein
the heat insulation layer is provided with a heat insulation layer via hole, through which the array of transistors is connected with the array of organic light emitting elements.

2. The display backplane according to claim 1, further comprising: a passivation layer formed between the array of organic light emitting elements and the array of transistors, wherein
the heat insulation layer is positioned between the passivation layer and the bottom electrode of the organic light emitting element in the array of organic light emitting elements; and
the passivation layer is provided with a passivation layer via hole formed therein, the position of which

corresponds to that of the heat insulation layer via hole, and the drain of the transistor in the array of transistors is connected with the bottom electrode of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

3. The display backplane according to claim 1 or 2, wherein the slope angle of the heat insulation layer via hole is smaller than or equal to 60°.

4. The display backplane according to claim 3, wherein the slope angle of the heat insulation layer via hole is 40-60°.

5. The display backplane according to claim 1, further comprising: a heat conduction layer formed on a side of the array of the organic light emitting elements away from the array of the transistors.

6. The display backplane according to claim 5, further comprising: an encapsulation layer for encapsulating the substrate on which the array of organic light emitting elements and the array of transistors are formed, wherein the heat conduction layer is formed between the array of organic light emitting elements and the encapsulation layer.

7. The display backplane according to claim 6, further comprising: a cover plate and a heat dissipation layer arranged on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is arranged between the heat dissipation layer and the encapsulation layer.

8. The display backplane according to claim 7, wherein the heat dissipation layer comprises a heat dissipation sheet and a heat dissipation pin, the heat dissipation pin being formed on a side of the heat dissipation sheet away from the cover plate.

9. A method for manufacturing a display backplane, comprising:

forming on a substrate an array of organic light emitting elements and an array of transistors for driving and controlling the array of organic light emitting elements; and
forming a heat insulation layer between the array of organic light emitting elements and the array of transistors, wherein
the heat insulation layer is provided with a heat insulation layer via hole formed therein, through which the array of transistors is connected with the array of organic light emitting elements.

10. The method according to claim 9, further comprising: forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of transistors.

11. The method according to claim 10, further comprising: forming an encapsulation layer for encapsulating the substrate on which the array of organic light emitting elements and the array of transistors are formed; wherein the step of forming a heat conduction layer on a side of the array of organic light emitting elements away from the array of transistors comprises:

forming a heat conduction layer between the array of organic light emitting elements and the encapsulation layer.

12. The method according to claim 11, further comprising:

forming a cover plate and a heat dissipation layer on a side of the encapsulation layer away from the array of organic light emitting elements, wherein the cover plate is formed between the heat dissipation layer and the encapsulation layer.

13. The method according to claim 9, further comprising: forming a passivation layer between the array of organic light emitting elements and the array of transistors, wherein
the heat insulation layer is positioned between the passivation layer and the bottom electrode of the organic light emitting element in the array of organic light emitting elements; and
the passivation layer is provided with a passivation layer via hole formed therein, the position of which corresponds to that of the heat insulation layer via hole, and the drain of the transistor in the array of transistors is connected with the bottom electrode of the organic light emitting element in the array of organic light emitting elements via the passivation layer via hole and the heat insulation layer via hole.

14. The method according to claim 13, wherein the step of forming the heat insulation layer comprises:

coating a mixed material of a heat insulation material and a photoresist onto the passivation layer; and
exposing and developing the mixed material coated onto the passivation layer using a photolithography process, to form a heat insulation layer provided with a heat insulation layer via hole.

15. A display device, comprising the display backplane according to any one of claims 1-8.

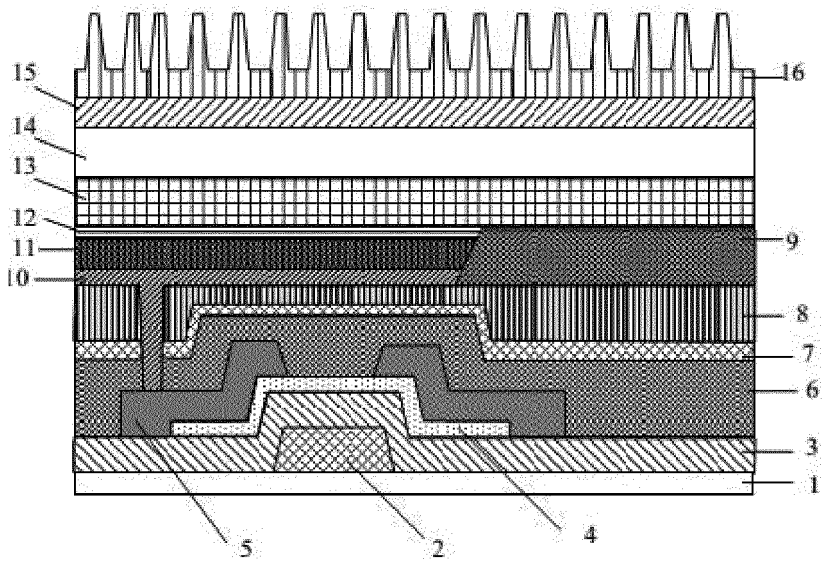

Fig. 1

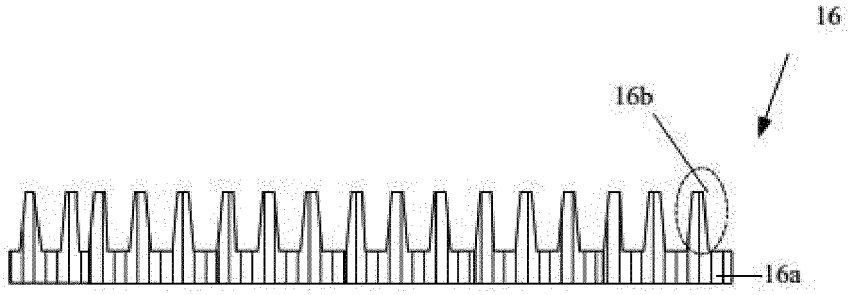

Fig. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2015/086869

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/12 (2006.01) i; H01L 27/32 (2006.01) i; H01L 21/77 (2006.01) i
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WPI, EPODOC, CNPAT, IEEE, CNKI: thermal insulation, contact hole, heat dissipation, display, transistor, array, organic, heat, thermal, hole, resist+

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 104659038 A (BOE TECHNOLOGY GROUP CO., LTD.), 27 May 2015 (27.05.2015), claims 1-14, and figures 1-2	1-15
X	US 2005087769 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.), 28 April 2005 (28.04.2005), description, paragraphs [0077]-[0140], and figures 1-2	1-6, 9-11, 13-15
Y	US 2005087769 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.), 28 April 2005 (28.04.2005), description, paragraphs [0077]-[0140], and figures 1-2	7-8, 12
Y	KR 20060118268 A (LG ELECTRONICS INC.), 23 November 2006 (23.11.2006), description, page 3, paragraph 8, and figure 1	7-8, 12
X	CN 103682143 A (SAMSUNG DISPLAY CO., LTD.), 26 March 2014 (26.03.2014), description, paragraphs [0051]-[0078], and figures 1-2	1-6, 9-11, 13-15
A	CN 104347819 A (LG DISPLAY CO., LTD.), 11 February 2015 (11.02.2015), the whole document	1-15

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 September 2015 (24.09.2015)	**03 November 2015 (03.11.2015)**
Name and mailing address of the ISA/CN: State Intellectual Property Office of the P. R. China No. 6, Xitucheng Road, Jimenqiao Haidian District, Beijing 100088, China Facsimile No.: (86-10) 62019451	Authorized officer **YAN, Miaoqing** Telephone No.: (86-10) **82245409**

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INTERNATIONAL SEARCH REPORT
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专利名称(译)	显示背板及其制造方法和显示装置		
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外部链接	Espacenet		

摘要(译)

本发明提供一种显示器背板及其制造方法，以及显示装置。显示器背板包括：基板;一系列有机发光元件和一系列晶体管，用于驱动和控制在基板上形成的有机发光元件阵列;在所述有机发光元件阵列与所述晶体管阵列之间形成隔热层，其中所述隔热层设置有隔热层通孔，所述晶体管阵列通过所述隔热层与所述有机发光阵列连接。元素。本发明提供的显示器背板可以减少在点亮晶体管阵列期间由有机发光元件阵列产生的热传导，从而避免由此引起的问题，例如不均匀显示。