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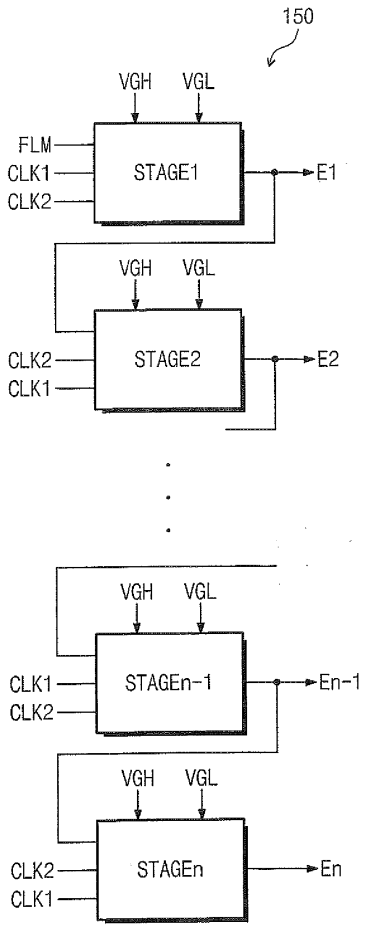
(54) Emission control driver and organic light emitting display device having the same

(57) An emission control driver includes stages sequentially outputting emission control signals through emission control lines. Each stage includes a first signal processor receiving a first voltage and generating first and second signals in response to first and second sub-control signals, a second signal processor receiving a second voltage having a level higher than a level of the first voltage and generating third and fourth signals in response to the third sub-control signal, the first signal, and the second signal, and a third signal processor receiving the first and second voltages and generating the emission control signal in response to the third and fourth signals. The first signal processor of each stage receives the emission control signal output from a previous stage as the first sub-control signal, and the first signal processor of a first stage among the stages receives a start signal as the first sub-control signal.

Fig. 3



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Description

BACKGROUND

1. Field

[0001] The present invention relates to an emission control driver and an organic light emitting display device having the same. More particularly, the present invention relates to an emission control driver capable of simplifying a configuration thereof and an organic light emitting display device having the emission control driver.

2. Description of the Related Art

[0002] In recent years, various display devices, such as liquid crystal display devices, organic light emitting display devices, electrowetting display devices, plasma display panels, electrophoretic display devices, etc., have been developed. Organic light emitting display devices display an image using an organic light emitting diode that generates light in association with a recombination between electrons and holes. Organic light emitting display devices have numerous advantages, e.g., fast response speed, low power consumption, etc.

[0003] Organic light emitting display devices include a plurality of pixels that displays the image, a scan driver that sequentially applies scan signals to the pixels, a data driver that applies data voltages to the pixels, and an emission control driver that applies emission control signals to the pixels. The pixels receive the data voltages in response to the scan signals. The pixels generate the light with a predetermined brightness corresponding to the data voltages to display the image. An emission time period of the pixels is controlled by the emission control signals. The emission control driver is initialized in response to initialization control signals and generates the emission control signals. However, simplification of the configuration of the emission control driver is desired.

SUMMARY

[0004] Embodiments of the inventive concept provide an emission control driver that includes a plurality of stages that sequentially outputs emission control signals through emission control lines. Each stage may include a first signal processor that receives a first voltage and generates a first signal and a second signal in response to a first sub-control signal and a second sub-control signal, a second signal processor that receives a second voltage having a level higher than a level of the first voltage and generates a third signal and a fourth signal in response to a third sub-control signal, the first signal, and the second signal, and a third signal processor that receives the first voltage and the second voltage and generates the emission control signal in response to the third signal and the fourth signal. The first signal processor of each stage receives the emission control signal output from a previous stage as the first sub-control signal, and the first signal processor of a first stage among the stages receives a start signal as the first sub-control signal.

[0005] The first signal processor of each of odd-numbered stages of the stages receives a first clock signal as the second sub-control signal, the second signal processor of each of the odd-numbered stages of the stages receives a second clock signal as a third sub-control signal, the first signal processor of each of even-numbered stages of the stages receives the second clock signal as the second sub-control signal, and the second signal processor of each of the even-numbered stages of the stages receives the first clock signal as the third sub-control signal.

[0006] The first and second clock signals have a same frequency and the second clock signal is obtained by shifting the first clock signal by a first duration corresponding to a half of a period of the first clock signal.

[0007] The start signal may be activated at a time point at which the first clock signal changes from a first level to a second level smaller than the first level, and the activation of the start signal is maintained during a second duration corresponding to four times of the first duration.

[0008] Each of the light emission control signals may have the level of the second voltage during a third duration corresponding to three times of the first duration, and the emission control signals are sequentially shifted by the first duration.

[0009] The first signal processor may include first, second, and third transistors. The first transistor has a gate terminal applied with the second sub-control signal and a source terminal applied with the first sub-control signal. The second transistor has a gate terminal connected to a drain terminal of the first transistor and a drain terminal applied with the second sub-control signal. The third transistor has a gate terminal applied with the second sub-control signal, a source terminal connected to a source terminal of the second transistor, and a drain terminal applied with the first voltage. The first signal is output from the source terminals of the second and third transistors, which are connected to each other, and the second signal is output from the drain terminal of the first transistor.

[0010] The second signal processor may include fourth, fifth, sixth, and seventh transistors and first and second capacitors. The fourth transistor has a gate terminal applied with the third sub-control signal and a drain terminal connected to a first node and the drain terminal of the first transistor. The first capacitor has a first electrode applied with the third sub-control signal and a second electrode connected to the drain terminal of the fourth transistor. The fifth transistor has a gate terminal connected to the source terminal of the third transistor and a second node, a source terminal applied with the second voltage, and a drain terminal connected to a source terminal of the fourth transistor. The sixth transistor has a gate terminal connected to the second node and a drain terminal applied with the third sub-control signal. The

second capacitor has a first electrode connected to the gate terminal of the sixth transistor and a second electrode connected to a source terminal of the sixth transistor. The seventh transistor has a gate terminal applied with the third sub-control signal, a source terminal connected to a third node, and a drain terminal connected to the source terminal of the sixth transistor. The third signal is applied to the third node, and the fourth signal is applied to the first node.

[0011] The third signal processor may include eighth, ninth, and tenth transistors and a third capacitor. The eighth transistor has a gate terminal connected to the first node, a source terminal applied with the second voltage, and a drain terminal connected to the third node. The third capacitor has a first electrode applied with the second voltage and a second electrode connected to the third node. The ninth transistor has a gate terminal connected to the third node, a source terminal applied with the second voltage, and a drain terminal connected to a corresponding emission control line. The tenth transistor has a gate terminal connected to the first node, a source terminal connected to the corresponding emission control line, and a drain terminal applied with the first voltage. The drain terminal of the ninth transistor and the source terminal of the tenth transistor are connected to a source terminal of a first transistor of a first signal processor of a next stage.

[0012] Embodiments of the inventive concept provide an organic light emitting display device that includes a display panel that includes a plurality of pixels each being connected to a corresponding scan line of scan lines, a corresponding data line of data lines, and a corresponding emission control line of emission control lines, a scan driver that sequentially applies scan signals to the pixels through the scan lines, a data driver that applies data voltages to the pixels through the data lines, and an emission control driver that includes a plurality of stages sequentially applying emission control signals to the pixels through the emission control lines. Each stage may include a first signal processor that receives a first voltage and generates a first signal and a second signal in response to a first sub-control signal and a second sub-control signal, a second signal processor that receives a second voltage having a level higher than a level of the first voltage, and generates a third signal and a fourth signal in response to a third sub-control signal, the first signal, and the second signal, and a third signal processor that receives the first voltage and the second voltage, and generates the emission control signal in response to the third signal and the fourth signal. The first signal processor of each stage receives the emission control signal output from a previous stage as the first sub-control signal, and the first signal processor of a first stage among the stages receives a start signal as the first sub-control signal.

[0013] Embodiments of the inventive concept provide an emission control driver that includes a plurality of stages that sequentially outputs emission control signals through emission control lines. Each stage may include a bi-directional driver that outputs a first input signal or a second input signal as a first sub-control signal in response to a first direction control signal and a second direction control signal, a first signal processor that receives a first voltage and generates a first signal and a second signal in response to the first sub-control signal and a second sub-control signal, a second signal processor that receives a second voltage having a level higher than a level of the first voltage and generates a third signal and a fourth signal in response to a third sub-control signal, the first signal, and the second signal, and a third signal processor that receives the first voltage and the second voltage and generates the emission control signal in response to the third signal and the fourth signal. The bi-directional driver receives the emission control signal output from a previous stage as the first input signal and the emission control signal output from a next stage as the second input signal, the bi-directional driver of a first stage among the stages receives a start signal as the first input signal, and the bi-directional driver of a last stage among the stages receives the start signal as the second input signal.

[0014] Embodiments of the inventive concept provide an emission control driver that includes a plurality of stages that sequentially outputs emission control signals through emission control lines. Each stage may include a bi-directional driver that outputs a first input signal or a second input signal as a first sub-control signal in response to a first direction control signal and a second direction control signal, a first signal processor that receives a first voltage and generates a first signal and a second signal in response to the first sub-control signal and a second sub-control signal, a second signal processor that receives a second voltage having a level higher than a level of the first voltage and generates a third signal, a fourth signal, and a carry signal in response to a third sub-control signal, the first signal, and the second signal, and a third signal processor that receives the first voltage and the second voltage and generates the emission control signal in response to the third signal and the fourth signal. The bi-directional driver receives the carry signal output from a previous stage as the first input signal and the carry signal output from a next stage as the second input signal, the bi-directional driver of a first stage among the stages receives a start signal as the first input signal, and the bi-directional driver of a last stage among the stages receives the start signal as the second input signal.

[0015] At least some of the above and other features of the invention are set out in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] Features of the invention will become apparent to those of ordinary skill in the art upon referring to the following description of embodiments of the invention with reference to the attached drawings in which:

[0017] FIG. 1 illustrates a block diagram of an organic light emitting display device according to an embodiment of the invention;

[0018] FIG. 2 illustrates an equivalent circuit diagram showing an example of one pixel of pixels shown in FIG. 1;

[0019] FIG. 3 illustrates a block diagram of an emission control driver shown in FIG. 1;

[0020] FIG. 4 illustrates a circuit diagram of stages of an emission control driver of an organic light emitting display device according to a first embodiment of the invention;

[0021] FIG. 5 illustrates a timing diagram of an operation of a first stage shown in FIG. 4;

[0022] FIGS. 6 and 7 illustrate circuit diagrams of stages of an emission control driver of an organic light emitting display device according to a second embodiment of the invention;

[0023] FIG. 8 illustrates a circuit diagram of stages of an emission control driver of an organic light emitting display device according to a third embodiment of the invention;

[0024] FIG. 9 illustrates a timing diagram of an operation of a first stage shown in FIG. 8; and

[0025] FIG. 10 illustrates a timing diagram of an operation of a second stage shown in FIG. 8.

DETAILED DESCRIPTION

[0026] Embodiments of the invention will now be described more fully hereinafter with reference to the accompanying drawings; however, the invention may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and convey implementations to those skilled in the art.

[0027] It will be understood that when an element or layer is referred to as being "on", "connected to" or "coupled to" another element or layer, it can be directly on, connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly on," "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present. Like numbers refer to like elements throughout. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0028] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings herein.

[0029] Spatially relative terms, such as "beneath", "below", "lower", "above", "upper" and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0030] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the embodiments. As used herein, the singular forms, "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "includes" and/or "including", when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0031] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0032] Hereinafter, embodiments will be explained in detail with reference to the accompanying drawings.

[0033] FIG. 1 illustrates a block diagram of an organic light emitting display device according to an embodiment of the invention. Referring to FIG. 1, an organic light emitting display device 100 includes a display panel 110, a timing controller 120, a scan driver 130, a data driver 140, and an emission control driver 150.

[0034] The display panel 110 includes a plurality of pixels PX11 to PXnm arranged in a matrix form. Each of the pixels PX11 to PXnm is connected to a corresponding scan line of scan lines S1 to Sn that extend in a row direction and a corresponding data line of data lines D1 to Dm crossing the scan lines S1 to Sn. In addition, each of the pixels PX11 to PXnm is connected to a corresponding emission control line of emission control lines E1 to En that extend substantially in parallel to the scan lines S1 to Sn.

[0035] The scan lines S1 to Sn are connected to the scan driver 130 to receive scan signals. The data lines D1 to Dm are connected to the data driver 140 to receive data voltages. The emission control lines E1 to En are connected to the emission control driver 150 to receive emission control signals. In the present embodiment, each of "n" and "m" is an integer number greater than zero (0).

[0036] The timing controller 120 may receive image signals, e.g., R, G, and B, and control signals from an external source (not shown), e.g., a system board. The control signals may include a horizontal synchronization signal Hsync, a vertical synchronization signal Vsync, and a main clock signal MCLK.

[0037] The timing controller 120 converts a data format of the image signals R, G, and B to a data format appropriate to an interface between the data driver 140 and the timing controller 120. The timing controller 120 provides the converted image signals R', G', and B' to the data driver 140.

[0038] The timing controller 120 generates a first control signal CONT1, a second control signal CONT2, and a third control signal CONT3 in response to the control signals. The first control signal CONT1, the second control signal CONT2, and the third control signal CONT3 are used to control operating timings of the scan driver 130, the data driver 140, and the emission control driver 150, respectively. The timing controller 120 applies the first, second, and third control signals CONT1, CONT2, and CONT3 to the scan driver 130, the data driver 140, and the emission control driver 150, respectively.

[0039] The scan driver 130 generates the scan signals in response to the first control signal CONT1. The scan signals are sequentially applied to the pixels PX11 to PXnm in the unit of row through the scan lines S1 to Sn. Accordingly, the pixels PX11 to PXnm are sequentially selected in the unit of row.

[0040] The data driver 140 generates the data voltages corresponding to the image signals R', G', and B' in response to the second control signal CONT2. The data voltages are applied to the pixels PX11 to PXnm respectively through the data lines D1 to Dm.

[0041] The third control signal CONT3 used to control the emission control driver 150 includes a plurality of sub-control signals. The sub-control signals may include a start signal FLM, a first clock signal CLK1, and a second clock signal CLK2.

[0042] The emission control driver 150 is applied with a first voltage VGL and a second voltage VGH having a voltage level higher than that of the fist voltage VGL. The emission control driver 150 generates the emission control signals in response to the third control signal CONT3. In detail, the emission control driver 150 generates the emission control signals using the start signal FLM, the first clock signal CLK1, the second clock signal CLK2, the first voltage VGL, and the second voltage VGH. The operation of the emission control driver 150 will be described in detail later. The emission control signals are applied to the pixels PX11 to PXnm through the emission control lines E1 to En.

[0043] The pixels PX11 to PXnm are applied with a first emission voltage ELVDD and a second emission voltage ELVSS. Each of the pixels PX11 to PXnm is applied with a corresponding data voltage of the data voltages through the corresponding data line of the data lines D1 to Dm in response to the corresponding scan signal provided through the corresponding scan line of the scan lines S1 to Sn. Each of the pixels PX11 to PXnm emits light at a brightness corresponding to the data voltage by using the first emission voltage ELVDD and the second emission voltage ELVSS. This will be described in detail later. An emission time period of each of the pixels PX11 to PXnm is controlled by the emission control signals.

[0044] The light emission driver 150 may generate the emission control signals using only the start signal FLM, the first clock signal CLK1, the second clock signal CLK2, the first voltage VGL, and the second voltage VGH. In other words, no additional control signals are required to initialize the emission control driver 150. Accordingly, the configuration of the emission control driver 150 may be simplifed.

[0045] FIG. 2 illustrates an equivalent circuit diagram showing an example of one pixel of the pixels shown in FIG. 1. Since the pixels PX11 to PXnm have the same configuration and function, only one pixel PXij has been shown in FIG. 2. Thus, hereinafter, an operation of one pixel PXij will be described in detail.

[0046] Referring to FIG. 2, the pixel PXij includes an organic light emitting diode OLED, a driving transistor T1, a capacitor Cst, a switching transistor T2, and an emission control transistor T3. The driving transistor T1 has a source terminal applied with the first emission voltage ELVDD, a drain terminal connected to a source terminal of the emission control transistor T3, and a gate terminal connected to a drain electrode of the switching transistor T2. The switching transistor T2 has a gate terminal connected to the corresponding scan line Si and a source terminal connected to the corresponding data line Dj.

[0047] The switching transistor T2 is turned on in response to the scan signal provided through the scan line Si. The turned-on switching transistor T2 receives the data voltage through the data line Dj and applies the data voltage to the gate terminal of the driving transistor T1.

[0048] The capacitor Cst has a first electrode connected to the source terminal of the driving transistor T1 and a second electrode connected to the gate terminal of the driving transistor T1. The capacitor Cst is charged with the data voltage applied to the gate terminal of the driving transistor T1 and maintains the charged data voltage after the switching transistor T2 is turned off.

[0049] The emission control transistor T3 has a gate terminal connected to the corresponding emission control line Ei and a drain terminal connected to an anode electrode of the organic light emitting diode OLED. The

emission control transistor T3 is turned on in response to the emission control signal provided through the emission control line Ei. The turned-on emission control transistor T3 transfers a current I_{OLED}, which flows through the driving transistor T1, to the organic light emitting diode OLED.

[0050] The organic light emitting diode OLED is applied with the second emission voltage ELVSS through a cathode electrode thereof. The organic light emitting diode OLED emits the light of various intensities in accordance with an amount of the current I_{OLED} provided from the driving transistor T1 through the emission control transistor T3.

[0051] FIG. 3 illustrates a block diagram showing the emission control driver shown in FIG. 1. Referring to FIG. 3, the emission control driver 150 includes a plurality of stages STAGE1 to STAGEn connected to each other one after another to sequentially output the emission control signals. The stages STAGE1 to STAGEn are connected to the emission control lines E1 to En, respectively, and sequentially output the emission control signals. The emission control signals overlap each other during a predetermined period. Hereinafter, the emission control signals output through the emission control lines E1 to En are referred to as first to n-th emission control signals.

[0052] Each of the stages STAGE1 to STAGEn receives the first voltage VGL and the second voltage VGH having the voltage level higher than that of the first voltage VGL. In addition, each of the stages STAGE1 to STAGEn receives the first clock signal CLK1 and the second clock signal CLK2.

[0053] Among the stages STAGE1 to STAGEn, a first stage STAGE1 is driven in response to the start signal FLM. In detail, the first stage STAGE1 receives the first voltage VGL and the second voltage VGH and generates the first emission control signal in response to the start signal FLM, the first clock signal CLK1, and the second clock signal CLK2. The first emission control signal is applied to the pixels arranged in a corresponding row through the first emission control line E1.

[0054] The stages STAGE2 to STAGEn are connected to each other one after another and are sequentially driven. In detail, a present stage is connected to an output terminal of a pervious stage and receives the emission control signal output from the previous stage. The present stage is driven in response to the emission control signal provided from the previous stage.

[0055] For instance, a second stage STAGE2 may receive the first emission control signal output from the first stage STAGE1 and is driven in response to the first emission control signal. In detail, the second stage STAGE2 receives the first voltage VGL and the second voltage VGH and generates the second emission control signal in response to the first emission control signal, the first clock signal CLK1, and the second clock signal CLK2. The second emission control signal is applied to the pixels arranged in a corresponding row through the second emission control line E2. The other stages STAGE3 to STAGEn are driven in the same way as the second stage STAGE2, and thus details thereof will not be repeated.

[0056] FIG. 4 illustrates a circuit diagram of stages of an emission control driver of an organic light emitting display device according to a first exemplary embodiment. FIG. 4 shows the circuit diagram of the first stage STAGE1 and the second stage STAGE2, but the stages STAGE1 to STAGEn have the same circuit configuration and function. Thus, hereinafter, the circuit configuration and the operation of the first stage STAGE1 will be described in detail, and the circuit configuration and the operation of the other stages STAGE2 to STAGEn will not be repeated in order to avoid redundancy. Referring to FIG. 4, each of the stages STAGE1 to STAGEn may include a first signal processor 151, a second signal processor 152, and a third signal processor 153.

[0057] The first signal processor 151 of each of the stages STAGE1 to STAGEn is applied with a first sub-control signal and a second sub-control signal. In detail, the first signal processor 151 of each of the stages STAGE2 to STAGEn receives the emission control signal output from the previous stage as the first sub-control signal. The first signal processor 151 of the first stage STAGE1 receives the start signal FLM as the first sub-control signal.

[0058] In addition, the first signal processor 151 of each of odd-numbered stages STAGE1, STAGE3, ..., and STAGEn-1 receives the first clock signal CLK1 as the second sub-control signal. The first signal processor 151 of each of even-numbered stages STAGE2, STAGE4, ..., and STAGEn receives the second clock signal CLK2 as the second sub-control signal.

[0059] Accordingly, the first signal processor 151 receives the first voltage VGL and generates a first signal CS1 and a second signal CS2 in response to the first and second sub-control signals. The first signal CS1 and the second signal CS2 are applied to the second signal processor 152.

[0060] The first signal processor 151 of the first stage STAGE1 receives the first voltage VGL and generates the first signal CS1 and the second signal CS2 in response to the start signal FLM and the first clock signal CLK1. The first signal processor 151 applies the first signal CS1 and the second signal CS2 to the second signal processor 152.

[0061] The first signal processor 151 includes first, second, third transistors M1, M2, and M3. The first, second, and third transistors M1, M2, and M3 may be PMOS transistors.

[0062] The first transistor M1 has a source terminal applied with the start signal FLM, a gate terminal applied with the first clock signal CLK1, and a drain terminal connected to a gate terminal of the second transistor M2.

[0063] The second transistor M2 has the gate terminal connected to the drain terminal of the first transistor M1, a source terminal connected to a source terminal of the third transistor M3, and a drain hsa applied with the first

clock signal CLK1.

[0064] The third transistor M3 has a gate terminal applied with the first clock signal CLK1 and connected to the drain terminal of the second transistor M2, a source terminal connected to the source terminal of the second transistor M2, and a drain terminal applied with the first voltage VGL.

[0065] The first signal CS1 is output from the source terminals of the second and third transistors M2 and M2, which are connected to each other. The second signal CS2 is output from the drain terminal of the first transistor M1.

[0066] The second signal processor 152 of each of the stages STAGE1 to STAGEn is applied with a third sub-control signal. In detail, the second signal processor 152 of each of the odd-numbered stages STAGE1, STAGE3, ..., and STAGEn-1 receives the second clock signal CLK2 as the third sub-control signal. The second signal processor 152 of each of the even-numbered stages STAGE2, STAGE4, ..., and STAGEn receives the first clock signal CLK1 as the third sub-control signal.

[0067] The second signal processor 152 receives the second voltage VGH and generates a third signal CS3 and a fourth signal CS4 in response to the third sub-control signal, the first signal CS1, and the second signal CS3. The third signal CS3 and the fourth signal CS4 are applied to the second signal processor 152.

[0068] The second signal processor 152 of the first stage STAGE1 receives the second voltage VGH and generates the third signal CS3 and the fourth signal CS4 in response to the first and second signals CS1 and CS2 from the first signal processor 151 and the second clock signal CLK2. The second signal processor 152 applies the third signal CS3 and the fourth signal CS4 to the third signal processor 153.

[0069] The second signal processor 152 includes fourth, fifth, sixth, and seventh transistors M4, M5, M6, and M7 and first and second capacitors C1 and C2. The fourth to seventh transistors M4 to M7 may be PMOS transistors.

[0070] The fourth transistor M4 has a gate terminal applied with the second clock signal CLK2, a drain terminal connected to a first node N1 and the gate terminal of the second transistor M2, and a source terminal connected to a drain terminal of the fifth transistor M5.

[0071] The first capacitor C1 has a first electrode applied with the second clock signal CLK2 and a second electrode connected to the drain terminal of the fourth transistor M4 and the first node N1.

[0072] The fifth transistor M5 has a gate terminal connected to the source terminal of the third transistor M3 and a second node N2, a source terminal applied with the second voltage VGH, and a drain terminal connected to the source terminal of the fourth transistor M4.

[0073] The sixth transistor M6 has a gate terminal connected to the second node N2, a source terminal connected to a drain terminal of the seventh transistor M7, and a drain terminal applied with the second clock signal CLK2.

[0074] The second capacitor C2 has a first electrode connected to the gate terminal of the sixth transistor M6 and a second electrode connected to the source terminal of the sixth transistor M6.

[0075] The seventh transistor M7 has a gate terminal applied with the second clock signal CLK2, a source terminal connected to a third node N3, and the drain terminal connected to the source terminal of the sixth transistor M6.

[0076] The third signal CS3 is applied to the third node N3 and the fourth signal CS4 is applied to the first node N1.

[0077] The third signal processor 153 of the first stage STAGE1 receives the first voltage VGL and the second voltage VGH, and generates the first emission control signal in response to the third signal CS3 and the fourth signal CS4 provided from the second signal processor 152. The first emission control signal is applied to the pixels through the first emission control line E1. The first emission control signal is applied to the first signal processor 151 of the second stage STAGE2.

[0078] The third signal processor 153 includes eighth, ninth, and tenth transistors M8, M9, and M10 and a third capacitor C3. The eight, ninth, and tenth transistors M8, M9, and M10 are PMOS transistors.

[0079] The eighth transistor M8 has a gate terminal connected to the first node N1, a source terminal applied with the second voltage VGH, and a drain electrode connected to the third node N3.

[0080] The third capacitor C3 has a first electrode applied with the second voltage VGH and a second electrode connected to the third node N3.

[0081] The ninth transistor M9 has a gate terminal connected to the third node N3, a source terminal applied with the second voltage VGH, and a drain terminal connected to the first emission control line E1.

[0082] The tenth transistor M10 has a gate terminal connected to the first node N1, a source terminal connected to the first emission control line E1, and a drain terminal applied with the first voltage VGL.

[0083] The drain terminal of the ninth transistor M9 and the source terminal of the tenth transistor M10 are connected to the source terminal of the first transistor M1 of the first signal processor 151 of the second stage STAGE2.

[0084] The operation of the first to tenth transistors M1 to M10 by the start signal FLM, the first clock signal CLK1, and the second clock signal CLK2 will be described in detail with reference to FIG. 5.

[0085] FIG. 5 illustrates a timing diagram showing the operation of the first stage shown in FIG. 4. Referring to FIG. 5, the first clock signal CLK1 and the second clock signal CLK2 have the same frequency. That is, the first and second clock signals CLK1 and CLK2 have the same first period T1. The second clock signal CLK2 is obtained by shifting the first clock signal CLK1 by a half of the first period T1 of the first clock signal CLK1. The shift period

between the first clock signal CLK1 and the second clock signal CLK2 is referred to as a first duration 1H.

[0086] The start signal FLM is applied to only the first stage STAGE1 and a high level duration of the start signal FLM is referred to as a second duration 4H. The second duration 4H is two times greater than the first period T1 of the first and second clock signals CLK1 and CLK2. That is, the second duration 4H is four times greater than the first duration 1H.

[0087] The start signal FLM changes from a low level to a high level when the first clock signal CLK1 changes from the high level to the low level. As described above, the start signal FLM maintains the high level during the second duration 4H after being changing from the low level to the high level. That is, the start signal FLM is activated when the first clock signal CLK1 changes from the high level to the low level, and the activated state of the start signal FLM is maintained during the second duration 4H.

[0088] Hereinafter, a high level of each signal is referred to as a first level and a low level, lower than the high level, of each signal is referred to as a second level. In addition, the first voltage VGL has the second level and the second voltage VGH has the first level.

[0089] The start signal FLM and the first clock signal CLK1 have the second level at a first time point t1 and the second clock signal CLK2 has the first level at the first time point t1.

[0090] The first clock signal CLK1 having the second level is applied to the gate terminal of the first transistor M1 and the gate terminal of the third transistor M3. Accordingly, the first and third transistors M1 and M3 are turned on.

[0091] The start signal FLM having the second level is applied to the gate terminal of the second transistor M2 and the first node N1 through the turned-on first transistor M1. Thus, the second transistor M2 is turned on and a voltage at the first node N1 has the second level.

[0092] The first clock signal CLK1 having the second level and the first voltage VGL are applied to the second node N2 respectively through the turned-on second transistor M2 and the turned-on third transistor M3. Therefore, a voltage at the second node N2 has the second level.

[0093] The second clock signal CLK2 having the first level is applied to the fourth transistor M4 and the seventh transistor M7. Thus, the fourth and seventh transistors M4 and M7 are turned off.

[0094] Since the voltage at the first node N1 has the second level, the eighth transistor M8 is turned on. The second voltage VGH is applied to the third node N3 through the turned-on eighth transistor M8. Accordingly, a voltage at the third node N3 has the first level. The third capacitor C3 is charged with the second voltage VGH. In other words, the third capacitor C3 is charged with the voltage having the first level. Since the voltage at the third node N3 has the first level, the ninth transistor M9 is turned off.

[0095] Since the voltage at the first node N1 has the second level, the tenth transistor M10 is turned on. Due to the turned-on tenth transistor M10, the first voltage VGL is applied to the first emission control line E1. Thus, the first emission control signal has the second level.

[0096] At a second time point t2, the start signal FLM has the second level and the first and second clock signals CLK1 and CLK2 have the first level. The first and third transistors M1 and M3 are turned off by the first clock signal CLK1 having the first level.

[0097] Since the voltage at the first node N1 is maintained at the second level, the second transistor M2 is turned on. The first clock signal CLK1 having the first level is applied to the second node N2 through the turned-on second transistor M2. Accordingly, the voltage at the second node N2 has the first level.

[0098] The voltage at the first node N1 has the second level, and thus the eighth and tenth transistors M8 and M10 are turned on. The second voltage VGH is applied to the third node N3 through the turned-on eighth transistor M8, so that the voltage at the third node N3 is maintained at the first level.

[0099] The ninth transistor M9 is turned off and the tenth transistor M10 is turned on since the voltage at the third node N3 has the first level and the voltage at the first node N1 has the second level. Accordingly, the first emission control signal is maintained at the second level.

[0100] At a third time point t3, the second clock signal CLK2 changes from the first level to the second level, and then changes from the second level to the first level again. Thus, an electric potential at the first node N1 is boot-strapped by a variation of electric potential of the second clock signal CLK2 due to the coupling of the first capacitor C1. That is, the first node N1, which has the voltage with the second level at the second time point t2, has a voltage of a third level lower than the second level in the second level period of the second clock signal CLK2 due to the coupling of the first capacitor C1. A conventional PMOS transistor has good drive characteristics as the level of the voltage applied to the PMOS transistor becomes low. Since the voltage at the first node N1 has the third level lower than the second level in the second level period of the second clock signal CLK2, the drive characteristics of the eighth and tenth transistors M8 and M10 may be improved. The first emission control signal is maintained at the second level.

[0101] At a fourth time point t4, the start signal FLM and the second clock signal CLK2 have the first level and the first clock signal CLK1 has the second level.

[0102] The first transistor M1 is turned on by the first clock signal CLK1 having the second level and the start signal FLM having the first level is applied to the first node N1. The voltage at the first node N1 has the first level, and thus the second and the tenth transistors M2 and M10 are turned off.

[0103] The third transistor M3 is turned on in response to the first clock signal CLK1 having the second level and the first voltage VGL is applied to the second node N2.

Thus, the voltage at the second node N2 has the second level.

[0104] The seventh transistor M7 is turned off in response to the second clock signal CLK2 having the first level. Since the voltage at the first node N1 has the first level, the eighth transistor M8 is turned off. The voltage at the third node N3 is maintained at the first level by the third capacitor C3. The voltage at the third node N3 is maintained at the first level, and thus the ninth transistor M9 is turned off. Therefore, the first emission control signal is maintained at the second level.

[0105] At a fifth time point t5, the start signal FLM and the first clock signal CLK1 have the first level, and the second clock signal CLK2 has the second level.

[0106] The first and third transistors M1 and M3 are turned off by the first clock signal CLK1 having the first level. Since the voltage at the first node N1 is maintained at the first level, the second, eighth, and tenth transistors M2, M8, and M10 are turned off.

[0107] The fourth and seventh transistors M4 and M7 are turned on in response to the second clock signal CLK2 having the second level. In addition, the voltage at the second node N2 has the second level, so that the fifth and sixth transistors M5 and M6 are turned on.

[0108] As the boot-strap described above, the electric potential of the second node N2 is boot-strapped by the variation of the electric potential of the second clock signal CLK2 due to the coupling of the second capacitor C2. That is, the voltage at the second node N2 has the third level lower than the second level in the second level period of the second clock signal CLK2.

[0109] The second clock signal CLK2 having the second level is applied to the third node N3 through the turned-on sixth and seventh transistors M6 and M7. Accordingly, the voltage at the third node N3 has the second level at the fifth time point t5. Since the voltage at the third node N3 has the second level, the ninth transistor M9 is turned on.

[0110] The first emission control signal is maintained at the first level since the ninth transistor M9 is turned on and the tenth transistor M10 is turned off.

[0111] At a sixth time point t6, the start signal FLM and the first clock signal CLK1 have the second level and the second clock signal CLK2 has the first level. According to the operation at the first time point t1, the first emission control signal has the second level at the sixth time point t6.

[0112] A duration in which the first emission control signal has the first level is referred to as a third duration 3H. The third duration 3H is three times greater than the first duration 1H.

[0113] The first emission control signal is applied to the pixels through the second stage STAGE2 and the first emission control line E1. The second stage STAGE2 generates the second emission control signal in response to the first emission control signal, the first clock signal CLK1, and the second clock signal CLK2.

[0114] The second emission control signal is output after being shifted by the first duration 1H with respect to the first emission control signal. In other words, the emission control signals output from the stages STAGE1 to STAGEn are sequentially shifted by the first duration 1H. In detail, the emission control signal output from the present stage is obtained by shifting the emission control signal output from the previous stage by the first duration 1 H.

[0115] Consequently, the emission control driver 150 of the organic light emitting display device according to the first exemplary embodiment receives the first voltage VGL and the second voltage VGH and generates the emission control signals in response to the start signal FLM, the first clock signal CLK1, and the second clock signal CLK2. Thus, the configuration of the emission control driver 150 may be simplified.

[0116] FIGS. 6 and 7 illustrate circuit diagrams of stages of an emission control driver of an organic light emitting display device according to a second embodiment of the invention.

[0117] FIG. 6 shows a first stage STAGE1 and a second stage STAGE2 and FIG. 7 shows an (n-1)th stage STAGEn-1 and an n-th stage STAGEn. However, the stages STAGE1 to STAGEn have the same circuit configuration and function. The stages shown in FIGS. 6 and 7 are driven in the same way as the stages shown in FIG. 4 except that the stages shown in FIGS. 6 and 7 include a bi-directional driver. Accordingly, hereinafter, different circuit configurations from those of the stages shown in FIG. 4 will be described.

[0118] Referring to FIGS. 6 and 7, the bi-directional driver 154 of each of the stages STAGE1 to STAGEn receives a first direction control signal BI_CTL and a second direction control signal BI_CTLB. The bi-directional driver 154 outputs a first input signal or a second input signal as a first sub-control signal in response to the first direction control signal BI_CTL and the second direction control signal BI_CTLB.

[0119] In detail, the bi-directional driver 154 of a present stage receives an emission control signal output from a previous stage as the first input signal and an emission control signal output from a next stage as the second input signal. In addition, the bi-directional driver 154 of the first stage STAGE1 receives the start signal FLM as the first input signal, and the n-th stage STAGEn receives the start signal FLM as the second input signal.

[0120] For instance, the first emission control signal output from the first stage STAGE1 is applied to the next stage, i.e., the second stage STAGE, since there is no previous stage of the first stage STAGE1. The second emission control signal output from the second stage STAGE2 is applied to the next stage, i.e., the third stage STAGE3, and the previous stage, i.e., the first stage STAGE1. The n-th emission control signal output from the n-th stage STAGEn is applied to the previous stage, i.e., the (n-1)th stage STAGEn-1, since there is no next stage of the n-th stage STAGEn. The (n-1)th emission control signal output from the (n-1)th stage STAGEn-1

is applied to the next stage, i.e., the n-th stage STAGEn, and the previous stage, i.e., the (n-2)th stage STAGEn-2.

[0121] The bi-directional driver 154 includes an eleventh transistor M11 and a twelfth transistor M12.

[0122] The eleventh transistor M11 includes a gate terminal applied with the first direction control signal BI_CTL and a source terminal applied with the first input signal. The twelfth transistor M12 includes a gate terminal applied with the second direction control signal BI_CTLB and a source terminal applied with the second input signal. Drain terminals of the eleventh and twelfth transistors M11 and M12 are connected to the source terminal of the first transistor M1 of the first signal processor 151.

[0123] In the first stage STAGE1, the gate terminal of the eleventh transistor M11 of the bi-directional driver 154 receives the first direction control signal BI_CTL and the source terminal of the eleventh transistor M11 of the bi-directional driver 154 receives the start signal FLM. The gate terminal of the twelfth transistor M12 receives the second direction control signal BI_CTLB and the source terminal of the twelfth transistor M12 receives the second emission control signal output from the second sage STAGE2. The drain terminals of the eleventh and twelfth transistors M11 and M12 are connected to the source terminal of the first transistor M1.

[0124] In the n-th stage STAGEn, the gate terminal of the eleventh transistor M11 of the bi-directional driver 154 receives the first direction control signal BI_CTL and the source terminal of the eleventh transistor M11 of the bi-directional driver 154 receives the (n-1)th emission control signal output from the (n-1)th stage STAGEn-1. The gate terminal of the twelfth transistor M12 receives the second direction control signal BI_CTLB and the source terminal of the twelfth transistor M12 receives the start signal FLM. The drain terminals of the eleventh and twelfth transistors M11 and M12 are connected to the source terminal of the first transistor M1.

[0125] In the other stages STAGE2 to STAGEn-1, the gate terminal of the eleventh transistor M11 of the bi-directional driver 154 receives the first direction control signal BI_CTL and the source terminal of the eleventh transistor M11 of the bi-directional driver 154 receives the emission control signal output from the previous stage. The gate terminal of the twelfth transistor M12 receives the second direction control signal BI_CTLB and the source terminal of the twelfth transistor M12 receives the emission control signal output from the next stage. The drain terminals of the eleventh and twelfth transistors M11 and M12 are connected to the source terminal of the first transistor M1.

[0126] The first direction control signal BI_CTL and the second direction control signal BI_CTLB have different levels from each other. For instance, when the first direction control signal BI_CTL has a first level (or a high level), the second direction control signal BI_CTLB has a second level (or a low level) lower than the first level.

[0127] When the first direction control signal BI_CTL has the second level, the eleventh transistor M11 of the bi-directional driver 154 of each of the stages STAGE1 to STAGEn is turned on and the twelfth transistor M12 of the bi-directional driver 154 of each of the stages STAGE1 to STAGEn is turned off. Accordingly, the start signal FLM is applied to the bi-directional driver 154 of the first stage STAGE1. In addition, the second emission control signal output from the first stage STAGE1 is applied to the second stage STAGE2. That is, the stages STAGE1 to STAGEn of the emission control driver according to the second exemplary embodiment are driven in the same way as the stages shown in FIG. 4. The emission control signals output from the stages STAGE I to STAGEn are sequentially applied to the pixels in the order from the first emission control signal to the n-th emission control signal. Accordingly, the pixels are driven in the order from the upper portion of the display panel 110 to the lower portion of the display panel 110.

[0128] In the case that the second direction control signal BI_CTLB has the second level, the eleventh transistor M11 of the bi-directional driver 154 of each of the stages STAGE1 to STAGEn is turned off and the twelfth transistor M12 of the bi-directional driver 154 of each of the stages STAGE1 to STAGEn is turned on. Accordingly, the start signal FLM is applied to the bi-directional driver 154 of the n-th stage STAGEn. In addition, the n-th emission control signal output from the n-th stage STAGEn is applied to the (n-1)th stage STAGEn-1. Therefore, the emission control signals output from the stages STAGE1 to STAGEn are sequentially applied to the pixels in the order from the n-th emission control signal to the first emission control signal. Accordingly, the pixels are driven in the order from the lower portion of the display panel 110 to the upper portion of the display panel 110.

[0129] The emission control driver of the organic light emitting display device according to this second embodiment of the invention receives the first voltage VGL and the second voltage VGH and generates the emission control signals in response to the start signal FLM, the first clock signal CLK1, and the second clock signal CLK2. Thus, the configuration of the emission control driver may be simplified.

[0130] FIG. 8 illustrates a circuit diagram of stages of an emission control driver of an organic light emitting display device according to a third embodiment of the invention. FIG. 8 shows a first stage STAGE1 and a second stage STAGE2 of an emission control driver. However, the stages STAGE1 to STAGEn have the same circuit configuration and function. Thus, hereinafter, the first stage STAGE1 will be described in detail and detailed descriptions of the other stages STAGE2 to STAGEn are omitted.

[0131] The stages shown in FIG. 8 are driven in the same way as the stages shown in FIGS. 6 and 7 except for a second signal processor 152a. Accordingly, hereinafter, different circuit configurations from those of the stages shown in FIGS. 6 and 7 will be described.

[0132] Referring FIG. 8, the bi-directional driver 154 of each of the stages STAGE1 to STAGEn receives a carry

signal CA output from a previous stage as a first input signal and a carry signal CA output from a next stage as a second input signal. In addition, the bi-directional driver 154 of the first stage STAGE1 receives a start signal FLM as the first input signal and the bi-directional driver 154 of the n-th stage STAGEn receives the start signal FLM as the second input signal.

[0133] The carry signal CA is output from the second signal processor 152a of each of the stages STAGE1 to STAGEn. In order to output the carry signal CA, the second signal processor 152 of each of the stages STAGE1 to STAGEn includes fourth to seventh transistors M4 to M7, first and second capacitors C1 and C2, and thirteenth and fourteenth transistors M13 and M14. The circuit configuration of the second signal processor 152a is the same as the second signal processor 152 shown in FIG. 4 except for the first capacitor C1, the thirteen transistor M13, and the fourteenth transistor M14. Thus, a connection between the first capacitor C1, the thirteenth transistor M13, and the fourteenth transistor M14 of the second signal processor 152 of the first stage STAGE1 will be described in detail.

[0134] The thirteenth transistor M13 has a gate terminal connected to the gate terminal of the fifth transistor M5 and the second node N2, a source terminal applied with the second voltage VGH, an a drain terminal connected to a fourth node N4.

[0135] The fourteenth transistor M14 has a gate terminal connected to the gate terminal of the fourth transistor M4, a source terminal connected to the fourth node N4, and a drain terminal applied with the second clock signal CLK2.

[0136] The first capacitor C1 has a first electrode connected to the gate terminal of the fourth transistor M4 and the gate terminal of the fourteenth transistor M14 and a second electrode connected to the fourth node N4.

[0137] A signal output from the fourth node N4 is defined as the carry signal CA and applied to the bi-directional driver 154 of the second stage STAGE2.

[0138] The carry signal CA of each of the stages STAGE1 to STAGEn is applied to the bi-directional driver 154 of each of the previous stage and the next stage. For instance, the carry signal CA output from the first stage STAGE1 is applied to the next stage, i.e., the bi-directional driver 154 of the second stage STAGE2, since the previous stage of the first stage STAGE1 does not exist. The carry signal CA output from the second stage STAGE2 is applied to the bi-directional driver 154 of the next stage, i.e., the third stage STAGE3, and to the bi-directional driver 154 of the previous stage, i.e., the first stage STAGE1.

[0139] The carry signal CA output from the n-th stage STAGEn is applied to the bi-directional driver 154 of the (n-1)th stage STAGEn-1 since the next stage of the n-th stage STAGEn does not exist. The carry signal CA output from the (n-1)th stage STAGEn-1 is applied to the bi-directional driver 154 of each of the n-th stage STAGEn and the (n-2)th stage STAGEn-2.

[0140] That is, each of the stages shown in FIG. 8 applies the carry signal CA to the previous and next stages thereof instead of the emission control signals used in the stages shown in FIGS. 6 and 7. Thus, the stages STAGE1 to STAGEn may be driven by using the carry signals rather than the emission control signals.

[0141] The output of the carry signal CA from the first stage STAGE1 by the thirteenth and fourteenth transistors M13 and M14 will be described in detail below with reference to FIG. 9. In addition, the second stage STAGE2 driven in response to the carry signal CA from the first stage STAGE1 will be described in detail later with reference to FIG. 10.

[0142] FIG. 9 illustrates a timing diagram showing the operation of the first stage shown in FIG. 8. Although not shown in FIG. 9, the first direction control signal BI_CTL has the second level and the second direction control signal BI_CTLB has the first level. That is, the stages STAGE1 to STAGEn are driven in the order from the upper portion of the display panel 110 to the lower portion of the display panel 110.

[0143] The signals shown in FIG. 9 have the same waveforms as those of the signals shown in FIG. 5 except that the voltage at the fourth node N4 is added as the carry signal CA. In other words, the first stage STAGE1 shown in FIG. 8 is driven in the same way as the first stage STAGE1 shown in FIG. 4 except that the first stage STAGE1 shown in FIG. 8 outputs the carry signal CA.

[0144] The first node N1 has the second or third level during a period except for a period N1_H in which the first node N1 has the first level. When the first node N1 has the second or third level, the fourteenth transistor M14 is turned on. That is, the second clock signal CLK2 is applied to the fourth node N4 during the period except for the period N1_H in which the first node N1 has the first level. Accordingly, the fourth node N4 has the same waveform as the second clock signal CLK2 during the period except for the period N1_H in which the first node N1 has the first level.

[0145] When the voltage at the first node N1 has the first level, the fourteenth transistor M14 is turned off. The voltage at the second node N2 is changed to the second level from the first level when the voltage at the first node N1 is changed to the first level from the second level. When the voltage at the second node N2 has the second level, the thirteenth transistor M13 is turned on. The second voltage VGH is applied to the fourth node N4 through the turned-on thirteenth transistor M13. Thus, the voltage at the fourth node N4 has the first level and is maintained at the first level while the thirteenth transistor M13 is turned on. That is, the voltage at the fourth node N4 is maintained at the first level during a period N2_L in which the voltage at the second node N2 has the second level.

[0146] When the fourteenth transistor M14 does not exist, the second clock signal CLK2 is continuously applied to the first capacitor C1. Accordingly, the first capacitor C1 is alternately and repeatedly charged with the first level and the second level. In this case, the second

clock signal CLK2 may be delayed due to the load of the first capacitor C1. That is, abnormal second clock signal CLK2 is applied to the second signal processor 152.

[0147] The fourteenth transistor M14 is turned off when the voltage at the first node N1 has the first level. When the fourteenth transistor M14 is turned off, the second clock signal CLK2 is not influenced by the third capacitor C3, and thus the delay of the second clock signal CLK2 may be prevented.

[0148] The thirteenth transistor M13 allows the fourth node N4 to be uniformly maintained when the fourteenth transistor M14 is turned off. In other words, when the fourteenth transistor M14 is turned off, the thirteenth transistor M13 is turned on, so that the voltage at the fourth node N4 is maintained at the first level.

[0149] The emission control driver of the organic light emitting display device according to this third embodiment generates the emission control signals using only the start signal FLM, the carry signal CA, the first clock signal CLK1, the second clock signal CLK2, and the second voltage VGH. That is, no additional control signals are required to initialize the emission control driver 150. Accordingly, the configuration of the emission control driver 150 may be simplified.

[0150] FIG. 10 illustrates a timing diagram showing the operation of the second stage shown in FIG. 8. Referring to FIG. 10, the voltage at the fourth node N4 of the first stage STAGE1is applied to the second stage STAGE2 as the carry signal CA. At a first time point t1, the carry signal CA and the second clock signal CLK2 have the second level and the first clock signal CLK1 has the first level.

[0151] The second clock signal CLK2 having the second level is applied to the gate terminal of the first transistor M1 and the gate terminal of the third transistor M3. Accordingly, the first and third transistors M1 and M3 are turned on.

[0152] The carry signal CA having the second level is applied to the gate terminal of the second transistor M2 and the first node N1 through the turned-on first transistor M1. Thus, the second transistor M2 is turned on and the voltage at the first node N1 has the second level.

[0153] The first clock signal CLK1 having the first level is applied to the fourth and seventh transistors M4 and M7. Therefore, the fourth and seventh transistors M4 and M7 are turned off.

[0154] Since the voltage at the first node N1 has the second level, the eighth transistor M8 is turned on. The second voltage VGH is applied to the third node N3 through the turned-on eighth transistor M8. Thus, the voltage at the third node N3 has the first level, and the ninth transistor M9 is turned off.

[0155] The voltage at the first node N1 has the second level, so that the tenth transistor M10 is turned on. Due to the turned-on tenth transistor M10, the first voltage VGL is applied to the first emission control line E1. Accordingly, the first emission control signal has the second level.

[0156] At a second time point t2, the carry signal CA, the first clock signal CLK1, and the second clock signal CLK2 have the first level. The first and third transistors M1 and M3 are turned off in response to the second clock signal CLK2 having the first level.

[0157] The voltage at the first node N1 is maintained at the second level, and thus the second transistor M2 is turned on. The first clock signal CLK1 having the first level is applied to the second node N2 through the turned-on second transistor M2. Accordingly, the voltage at the second node N2 has the first level.

[0158] Since the voltage at the first node N1 has the second level, the eighth and tenth transistors M8 and M10 are turned on. Thus, the second voltage VGH is applied to the third node N3 through the turned-on eighth transistor M8, so that the voltage at the third node N3 is maintained at the first level.

[0159] When the voltage at the third node N3 has the first level and the voltage at the first node N1 has the second level, the ninth transistor M9 is turned off and the tenth transistor M10 is turned on. Thus, the first emission control signal is maintained at the second level.

[0160] At a third time point t3, the variation of the electric potential of the first node N1, which is caused by the coupling of the first capacitor C1, is the same as described in FIG. 5.

[0161] At a fourth time point t4, the carry signal CA and the first clock signal CLK1 have the first level and the second clock signal CLK2 has the second level.

[0162] The first transistor M1 is turned on by the second clock signal CLK2 having the second level and the carry signal CA having the first level is applied to the first node N1. The voltage at the first node N1 has the first level. Since the voltage at the first node N1 has the first level, the second and tenth transistors M2 and M10 are turned off.

[0163] The third transistor M3 is turned on in response to the second clock signal CLK2 having the second level and the first voltage VGL is applied to the second node N2. Accordingly, the voltage at the second node N2 has the second level.

[0164] The seventh transistor M7 is turned off in response to the first clock signal CLK1 having the first level. Since the voltage at the first node N1 has the first level, the eighth transistor M8 is turned off. The voltage at the third node N3 is maintained at the first level by the third capacitor C3, and thus the ninth transistor M9 is turned off. As a result, the first emission control signal is maintained at the second level.

[0165] At a fifth time point t5, the carry signal CA and the second clock signal CLK2 have the first level and the first clock signal CLK1 has the second level.

[0166] The first and third transistors M1 and M3 are turned off in response to the second clock signal CLK2 having the first level. The voltage at the first node N1 is maintained at the first level. Thus, the second, eighth, and tenth transistors M2, M8, and M10 are turned off.

[0167] The fourth and seventh transistors M4 and M7

are turned on in response to the first clock signal CLK1 having the second level. In addition, since the voltage at the second node N2 has the second level, the fifth and sixth transistors M5 and M6 are turned on.

[0168] The second clock signal CLK2 having the second level is applied to the third node N3 through the turned-on sixth and seventh transistors M6 and M7. Thus, the voltage at the third node N3 has the second level at the fifth time point t5, so that the ninth transistor M9 is turned on. When the ninth transistor M9 is turned on and the tenth transistor M10 is turned off, the first emission control signal has the first level.

[0169] At a sixth time point t6, the carry signal CA and the second clock signal CLK2 have the second level and the first clock signal CLK1 has the first level. According to the operation at the first time point t1 as described above, the first emission control signal has the second level at the sixth time point t6.

[0170] As described above, the present stage generates the emission control signal in response to the first clock signal CLK1, the second clock signal CLK2, and the carry signal CA provided from the previous stage. In addition, the emission control signals output from the stages STAGE1 to STAGEn are sequentially shifted by the first duration 1H. As no additional control signals are required to initialize the emission control driver, the configuration of the emission control driver may be simplified.

[0171] Certain embodiments of the invention have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the scope of the present invention as set forth in the following claims.

Claims

1. An emission control driver, comprising:

a plurality of stages adapted to sequentially output emission control signals through emission control lines, each stage including:

a first signal processor adapted to receive a first voltage and generate first and second signals in response to first and second sub-control signals;

a second signal processor adapted to receive a second voltage having a level higher than a level of the first voltage and generate third and fourth signals in response to a third sub-control signal, the first signal, and the second signal; and

a third signal processor adapted to receive the first and second voltages and generate the emission control signal in response to the third and fourth signals,

wherein the first signal processor of each stage is adapted to receive the emission control signal output from a previous stage as the first sub-control signal, and the first signal processor of a first stage among the stages is adapted to receive a start signal as the first sub-control signal.

2. An emission control driver, comprising:

a plurality of stages adapted to sequentially output emission control signals through emission control lines, each stage including:

a bi-directional driver adapted to output a first input signal or a second input signal as a first sub-control signal in response to a first direction control signal and a second direction control signal;

a first signal processor adapted to receive a first voltage and generate a first signal and a second signal in response to the first sub-control signal and a second sub-control signal;

a second signal processor adapted to receive a second voltage having a level higher than a level of the first voltage and generate a third signal, a fourth signal and optionally a carry signal in response to a third sub-control signal, the first signal, and the second signal; and

a third signal processor adapted to receive the first voltage and the second voltage and generate the emission control signal in response to the third signal and the fourth signal,

wherein the bi-directional driver is adapted to receive the emission control signal or carry signal output from a previous stage as the first input signal and the emission control signal or carry signal output from a next stage as the second input signal, the bi-directional driver of a first stage among the stages is adapted to receive a start signal as the first input signal, and the bi-directional driver of a last stage among the stages is adapted to receive the start signal as the second input signal.

3. An emission control driver as claimed in claim 2,

wherein the bi-directional driver id adapted to apply the first input signal to the first signal processor in response to the first direction control signal that is activated, and apply the second input signal to the first signal processor in response to the second direction control signal that is activated.

4. An emission control driver as claimed in claim 3, wherein the bi-directional driver comprises:

an eleventh transistor having a gate terminal adapted to receive the first direction control signal and a source terminal adapted to receive the first input signal; and
a twelfth transistor having a gate terminal adapted to receive the second direction control signal, a source terminal adapted to receive the second input signal, and a drain terminal connected to a drain terminal of the eleventh transistor, wherein the first sub-control signal is adapted to receive the first signal processor through the drain terminals of the eleventh and twelfth transistors.

5. An emission control driver as claimed in any preceding claim, wherein:

the first signal processor of each of odd-numbered stages of the stages is adapted to receive a first clock signal as the second sub-control signal,
the second signal processor of each of the odd-numbered stages of the stages is adapted to receive a second clock signal as a third sub-control signal,
the first signal processor of each of even-numbered stages of the stages is adapted to receive the second clock signal as the second sub-control signal, and
the second signal processor of each of the even-numbered stages of the stages is adapted to receive the first clock signal as the third sub-control signal.

6. An emission control driver as claimed in claim 5, wherein the first signal processor comprises:

a first transistor having a gate terminal adapted to receive the second sub-control signal and a source terminal adapted to receive the first sub-control signal;
a second transistor having a gate terminal connected to a drain terminal of the first transistor and a drain terminal adapted to receive the second sub-control signal;
a third transistor having a gate terminal adapted to receive the second sub-control signal, a source terminal connected to a source terminal of the second transistor; and
a drain terminal adapted to receive the first voltage;
wherein the source terminals of the second and third transistors, which are connected to each other, are adapted to output the first signal and the drain terminal of the first transistor is adapted to output the second signal.

7. An emission control driver as claimed in claim 6, wherein the second signal processor comprises:

a fourth transistor having a gate terminal adapted to receive the third sub-control signal and a drain terminal connected to a first node and the drain terminal of the first transistor;
a first capacitor having a first electrode adapted to receive the third sub-control signal and a second electrode connected to the drain terminal of the fourth transistor;
a fifth transistor having a gate terminal connected to the source terminal of the third transistor and a second node, a source terminal adapted to receive the second voltage, and a drain terminal connected to a source terminal of the fourth transistor;
a sixth transistor having a gate terminal connected to the second node and a drain terminal adapted to receive the third sub-control signal;
a second capacitor having a first electrode connected to the gate terminal of the sixth transistor and a second electrode connected to a source terminal of the sixth transistor; and
a seventh transistor having a gate terminal adapted to receive the third sub-control signal, a source terminal connected to a third node, and a drain terminal connected to the source terminal of the sixth transistor, wherein the third node is adapted to receive the third signal and the first node is adapted to receive the fourth signal.

8. An emission control driver as claimed in claim 7, wherein the third signal processor comprises:

an eighth transistor having a gate terminal connected to the first node, a source terminal adapted to receive the second voltage, and a drain terminal connected to the third node;
a third capacitor having a first electrode adapted to receive the second voltage and a second electrode connected to the third node;
a ninth transistor having a gate terminal connected to the third node, a source terminal adapted to receive the second voltage, and a drain terminal connected to a corresponding emission control line; and
a tenth transistor having a gate terminal connected to the first node, a source terminal con-

nected to the corresponding emission control line, and a drain terminal adapted to receive the first voltage, wherein the drain terminal of the ninth transistor and the source terminal of the tenth transistor are connected to a source terminal of a first transistor of a first signal processor of a next stage.

9. An emission control driver as claimed in claim 6 when dependent upon claim 2, wherein the second signal processor comprises:

a fourth transistor having a gate terminal applied with the third sub-control signal and a drain terminal connected to a first node and the drain terminal of the first transistor;
a first capacitor having a first electrode connected to a fourth node and a second electrode connected to the drain terminal of the fourth transistor;
a fifth transistor having a gate terminal connected to the source terminal of the third transistor and a second node, a source terminal applied with the second voltage, and a drain terminal connected to a source terminal of the fourth transistor;
a sixth transistor having a gate terminal connected to the second node and a drain terminal applied with the third sub-control signal;
a second capacitor having a first electrode connected to the gate terminal of the sixth transistor and a second electrode connected to a source terminal of the sixth transistor;
a seventh transistor having a gate terminal applied with the third sub-control signal, a source terminal connected to a third node, and a drain terminal connected to the source terminal of the sixth transistor;
a thirteenth transistor having a gate terminal connected to the second node, a source terminal applied with the second voltage, and a drain terminal connected to the fourth node; and
a fourteenth transistor having a gate terminal connected to the second electrode of the first capacitor, a source terminal connected to the fourth node, and a drain terminal applied with the first clock signal, wherein the third signal is applied to the third node, the fourth signal is applied to the first node, and a voltage at the fourth node is output as the carry signal.

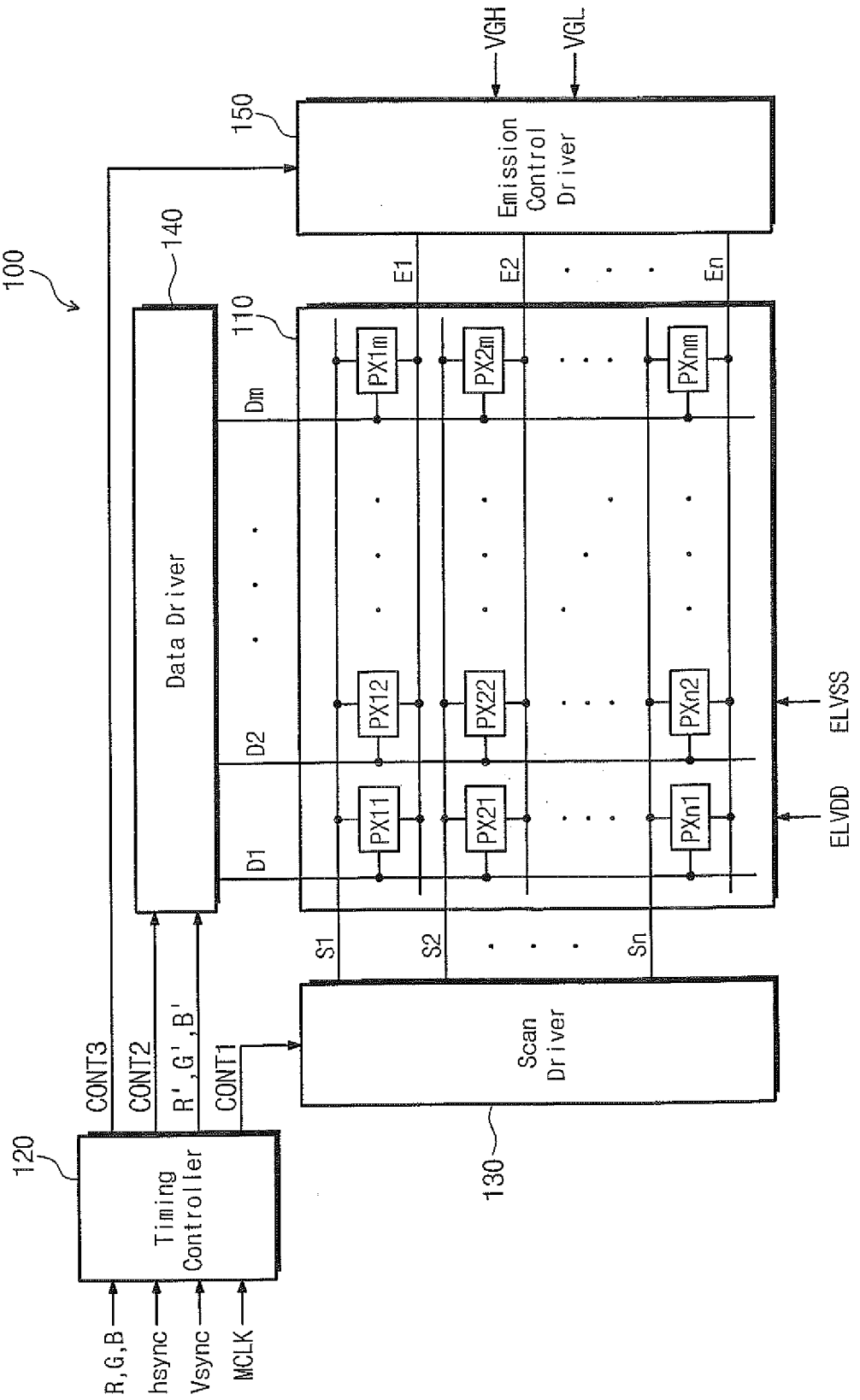
10. An organic light emitting display device, comprising:

a display panel that includes a plurality of pixels each being connected to a corresponding one of a plurality of scan lines, a corresponding one of a plurality of data lines, and a corresponding one of a plurality of emission control lines;
a scan driver adapted to sequentially apply scan signals to the pixels through the scan lines;
a data driver adapted to apply data voltages to the pixels through the data lines; and
an emission control driver according to one of claims 1 to 9.

11. An organic light emitting display device as claimed in claim 9, when the emission control driver is as set out in claim 2, wherein:

the said organic light emitting display device further comprises a timing controller;
the first and second clock signals have a same frequency,
the timing controller is adapted to obtain the second clock signal by shifting the first clock signal by a first duration corresponding to a half of a period of the first clock signal,
the timing controller is adapted to activate the start signal at a time point at which the first clock signal changes from a first level to a second level smaller than the first level, and
the timing controller is adapted to maintain the activation of the start signal during a second duration that is four times the first duration.

Fig. 1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Vsync
MCLK
CONT3
CONT2
R',G',B'
CONT1
140
Data Driver
150
Emission Control Driver
VGH
VGL
110
E1
E2
En
Dm
D2
D1
PX1m
PX2m
PXnm
PX12
PX22
PXn2
PX11
PX21
PXn1
ELVSS
ELVDD
S1
S2
Sn
130
Scan Driver

Fig. 2

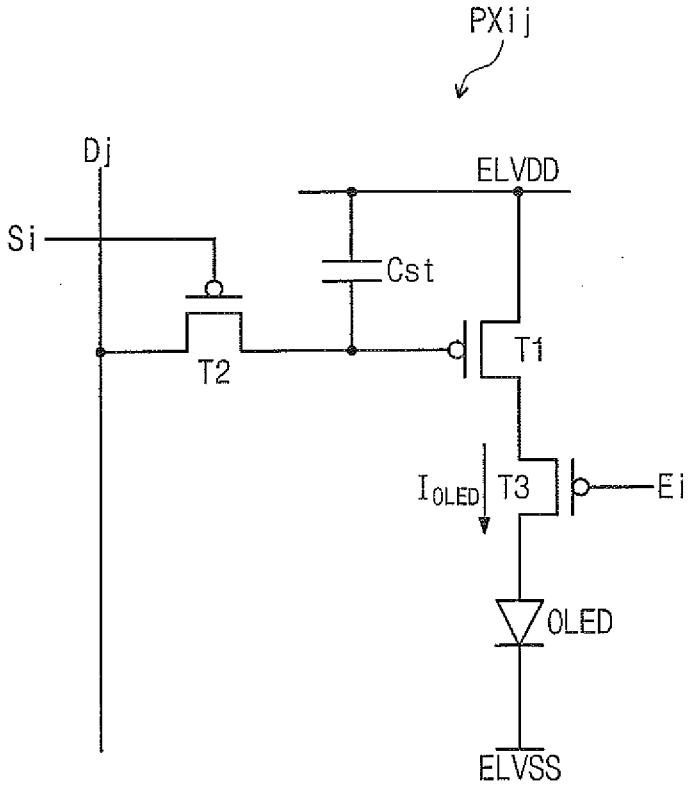
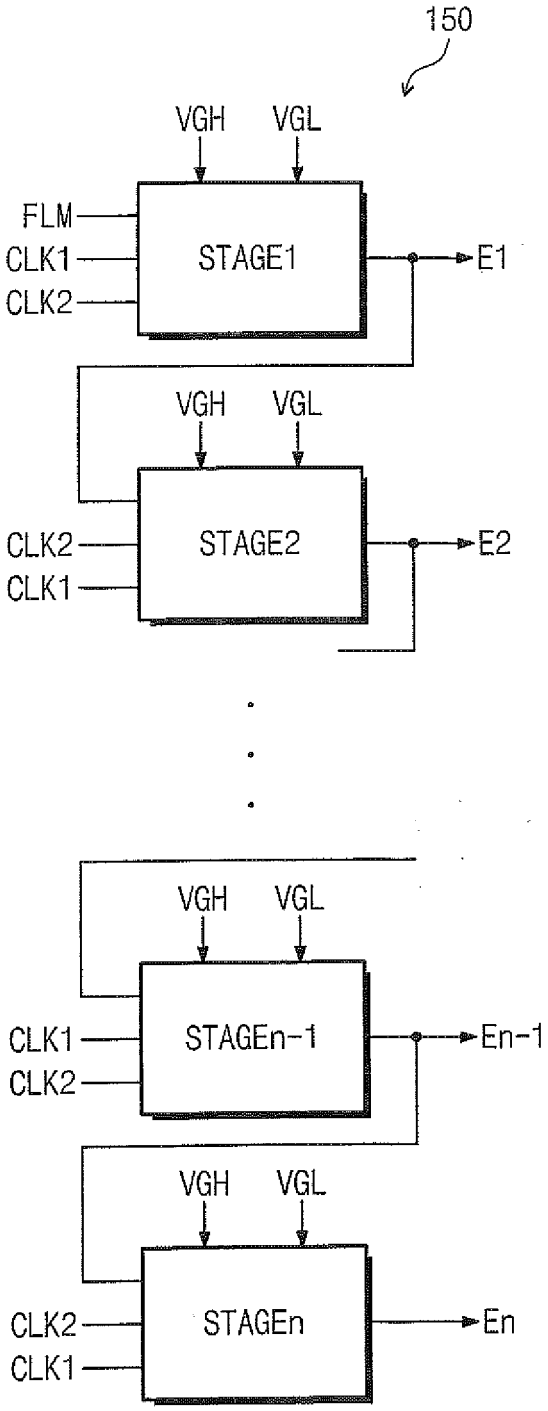


Fig. 3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VGL
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CLK2
STAGE1
E1
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VGL
CLK2
CLK1
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VGL
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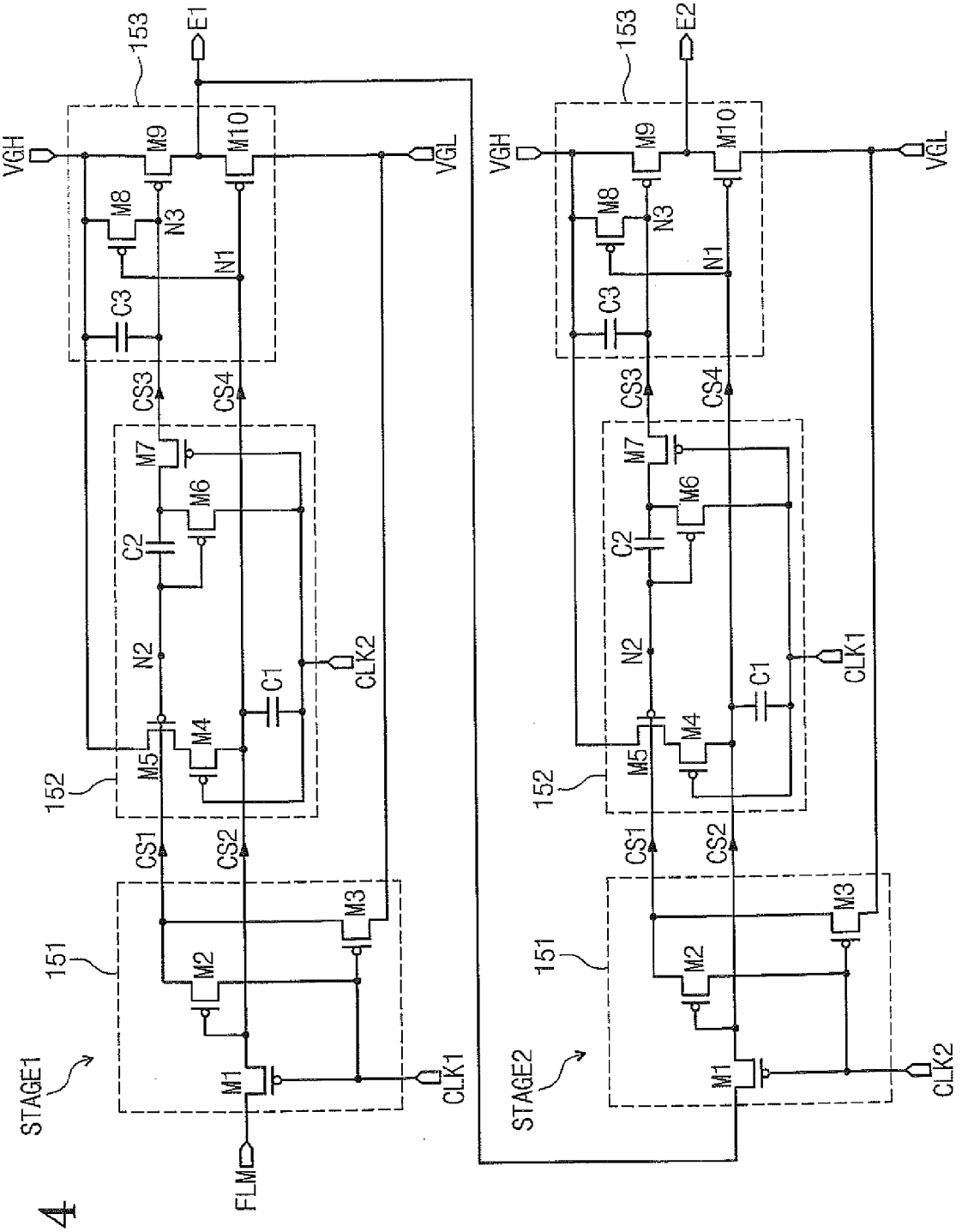
En-1
VGH
VGL
CLK2
CLK1
STAGEn
En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M7
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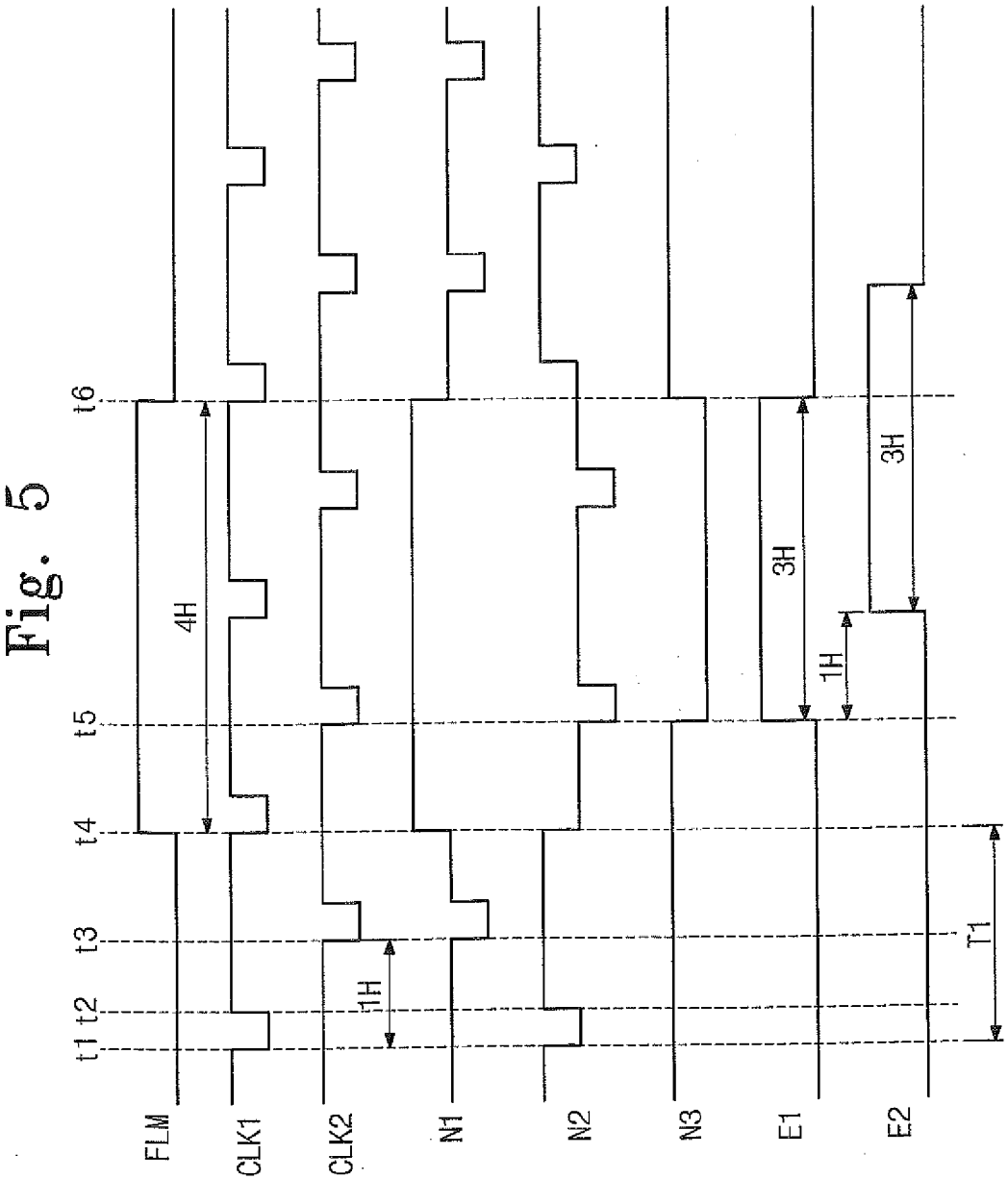
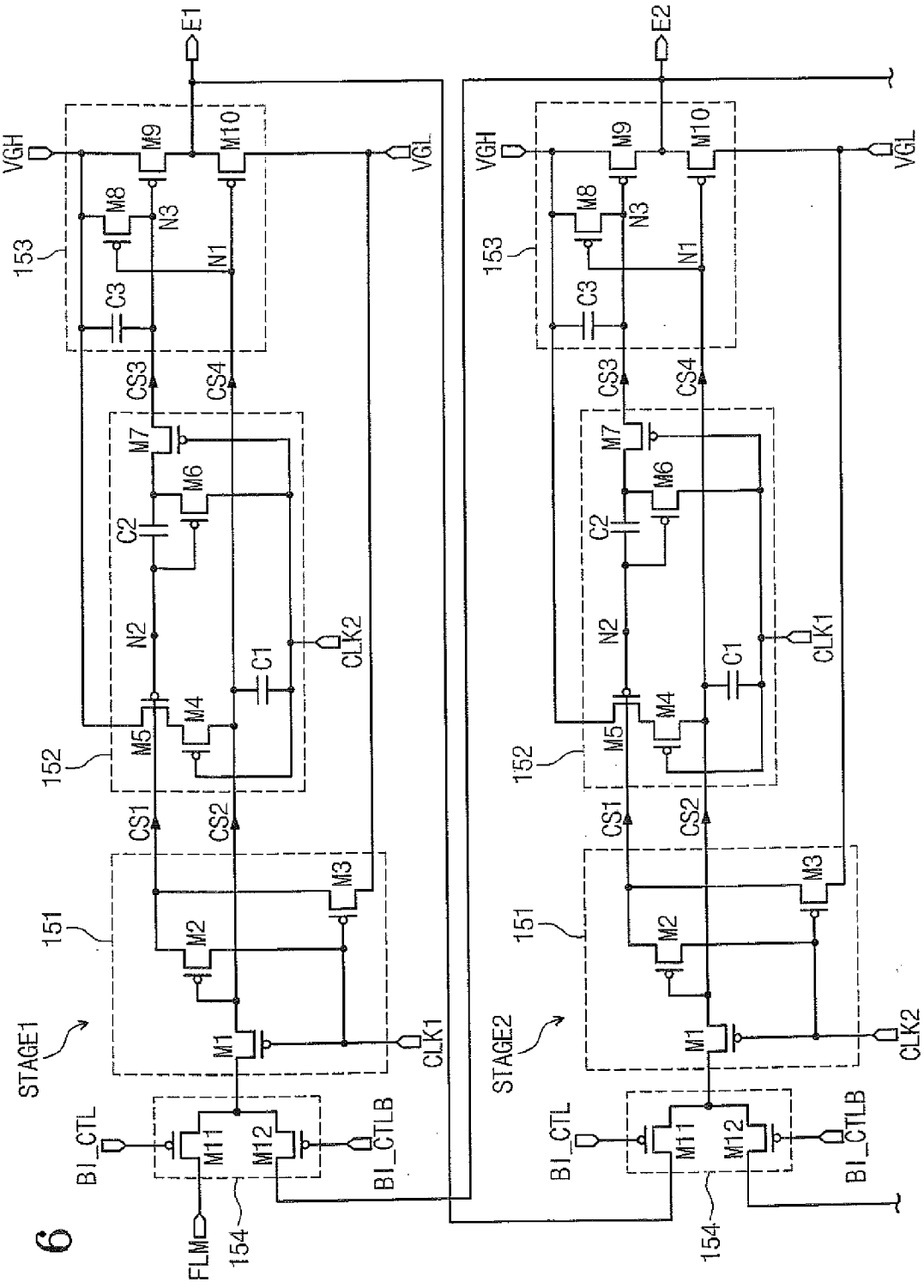
M10
C1
C2
C3
N1
N2
N3
CS1
CS2
CS3
CS4
CLK1
CLK2
FLM
STAGE1
STAGE2
151
152

Fig. 4

Fig. 5

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C1
C2
C3
N1
N2
N3
CS1
CS2
CS3
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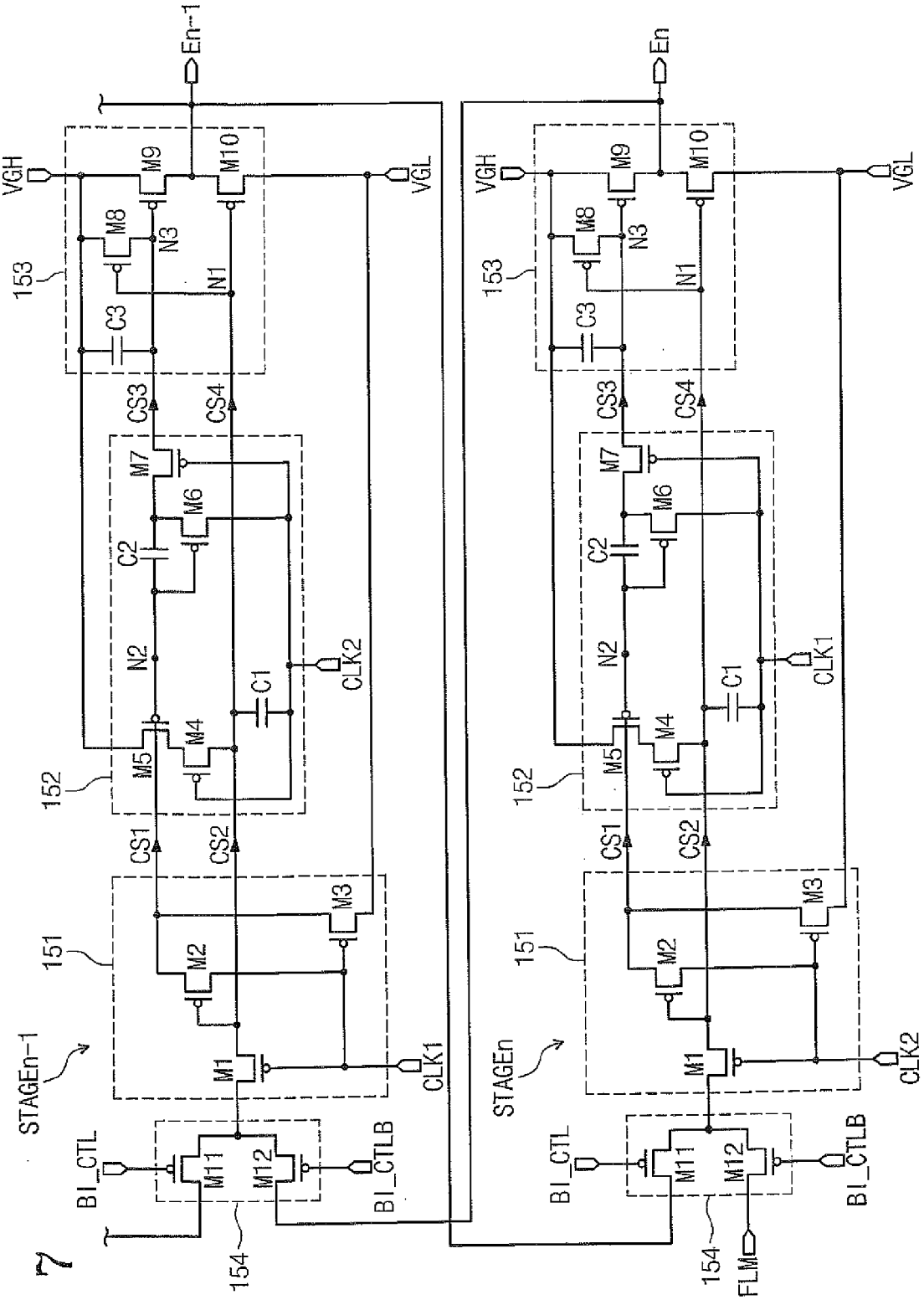
CLK1
CLK2
BI_CTL
BI_CTLB
FLM
STAGE1
STAGE2
151
152
153
154

Fig. 6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M6
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M10
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C1
C2
C3
N1
N2
N3
CS1
CS2
CS3
CS4
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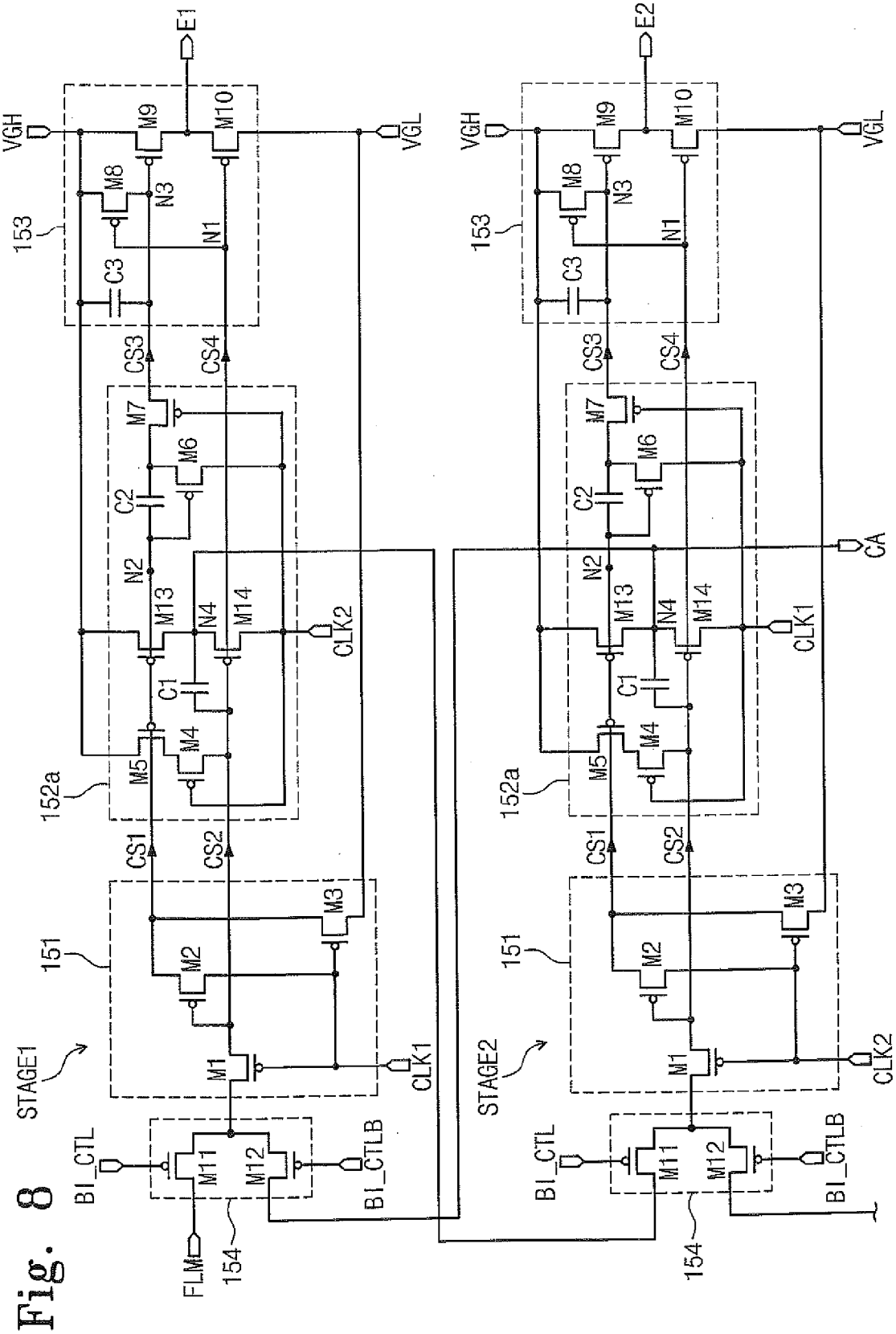
BI_CTLB
FLM
STAGEn-1
STAGEn
151
152
153
154

Fig. 7

Fig. 8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M4
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M6
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M9
M10
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M13
M14
C1
C2
C3
N1
N2
N3
N4
CS1
CS2
CS3
CS4
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CLK2
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BI_CTLB
FLM
STAGE1
STAGE2
151
152a
153
154

Fig. 9

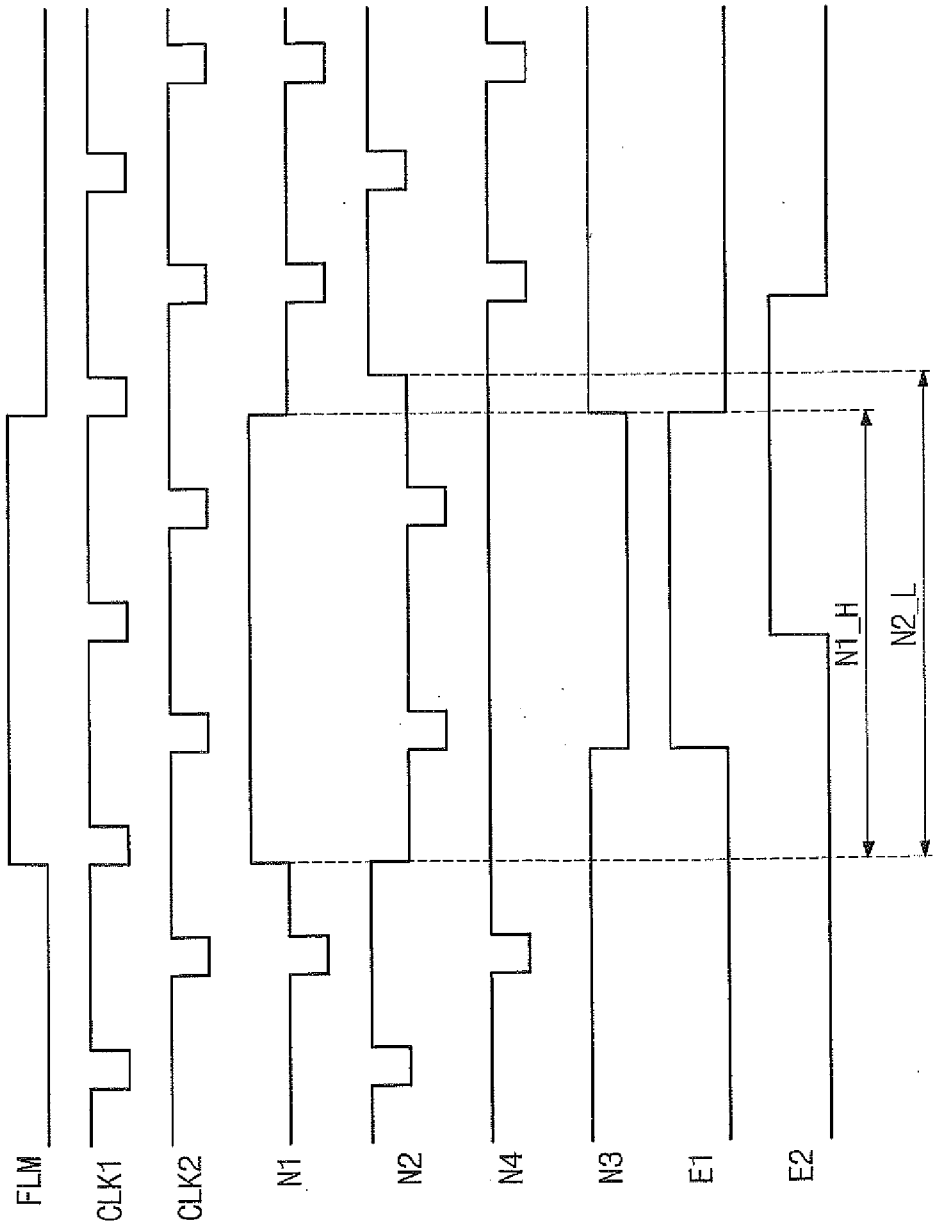
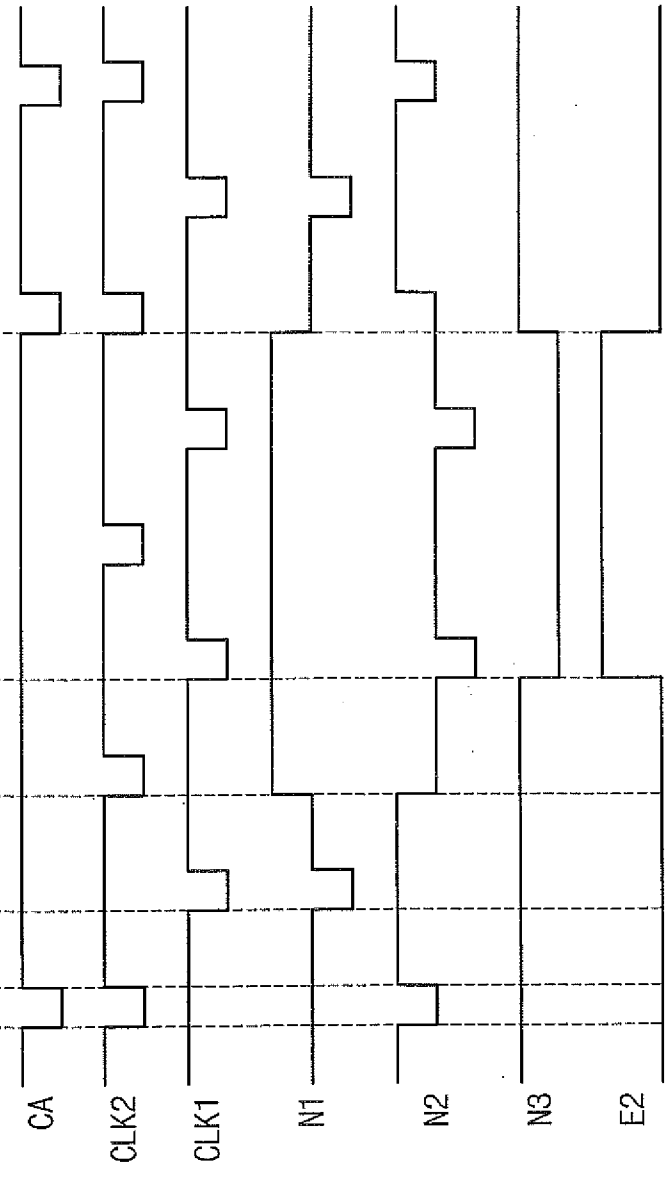


Fig. 10



专利名称(译)	发射控制驱动器和具有该发射控制驱动器的有机发光显示装置		
公开(公告)号	EP2701142A2	公开(公告)日	2014-02-26
申请号	EP2013178175	申请日	2013-07-26
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	JANG HWAN SOO		
发明人	JANG, HWAN SOO		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3266 G09G2230/00 G09G2300/0861 G09G2310/0202 G09G2310/0262 G09G2310/0283 G09G2310/0286 G09G3/2022 G09G3/3291		
优先权	1020120091442 2012-08-21 KR		
其他公开文献	EP2701142A3		
外部链接	Espacenet		

摘要(译)

发射控制驱动器包括通过发射控制线顺序输出发射控制信号的级。每级包括第一信号处理器，其接收第一电压并响应于第一和第二子控制信号产生第一和第二信号，第二信号处理器接收第二电压，该第二电压的电平高于第一电压的电平并产生第三电压。响应于第三和第四信号，第四信号响应第三子控制信号，第一信号和第二信号，第三信号处理器接收第一和第二电压，并响应第三和第四信号产生发射控制信号。每级的第一信号处理器接收从前一级输出的发射控制信号作为第一子控制信号，并且各级中的第一级的第一信号处理器接收作为第一子控制信号的起始信号。

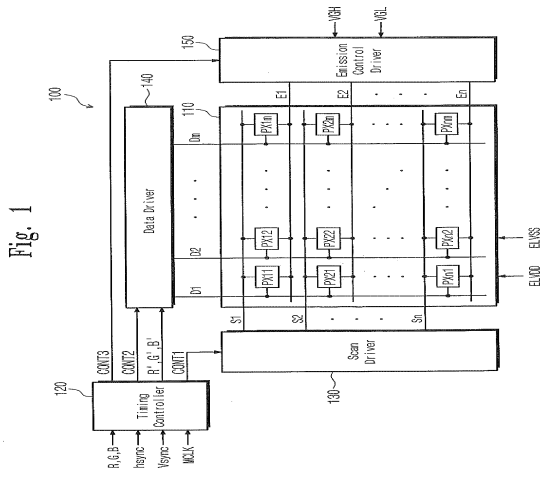


Fig. 1