(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) **EP 2 439 724 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
13.07.2016 Bulletin 2016/28

(21) Application number: **10783073.9**

(22) Date of filing: **04.03.2010**

(51) Int Cl.:
G09G 3/32 *(2006.01)* ***G09G 3/20*** *(2006.01)*

(86) International application number:
PCT/JP2010/001523

(87) International publication number:
WO 2010/140285 (09.12.2010 Gazette 2010/49)

(54) DISPLAY DEVICE AND DRIVE METHOD FOR DISPLAY DEVICE

ANZEIGEVORRICHTUNG UND ANTRIEBSVERFAHREN FÜR DIE ANZEIGEVORRICHTUNG

DISPOSITIF D'AFFICHAGE ET PROCÉDÉ DE COMMANDE POUR LE DISPOSITIF D'AFFICHAGE

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO SE SI SK SM TR

(30) Priority: **04.06.2009 JP 2009135286**

(43) Date of publication of application:
11.04.2012 Bulletin 2012/15

(73) Proprietor: **Sharp Kabushiki Kaisha**
Osaka-shi, Osaka 545-8522 (JP)

(72) Inventor: **KISHI, Noritaka**
Osaka-shi
Osaka 545-8522 (JP)

(74) Representative: **Goddar, Heinz J.**
Boehmert & Boehmert
Anwaltspartnerschaft mbB
Patentanwälte Rechtsanwälte
Pettenkoferstrasse 20-22
80336 München (DE)

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EP 2 439 724 B1

Printed by Jouve, 75001 PARIS (FR)

Description

Technical Field

[0001] The present invention relates to a display device and a drive method for driving the display device.

Background Art

[0002] In order to drive a light emitting element (such as organic EL, light emitting diodes etc.) controlled by an electric current, that is, to drive an electric current element, accurate control of the electric current to be supplied to the electric current element is required in a range from minute electric currents for low gray scales to large electric currents for high gray scales. If a conventional simple matrix drive is employed to an organic EL display device, high luminance drive is required especially in a high gray scale region due to a low duty ratio, thereby shortening a life of the organic EL display device. For this reason, an active matrix drive using TFT is mainly employed.

[0003] By utilizing a signal programmed in a selection period, the active matrix drive makes it possible to perform the driving in a hold mode in which light is emitted also during a non-selection period other than the selection period.

[0004] Recently, organic EL elements have been improved to be more efficient, thereby requiring that more minute electric current should be controlled more accurately at a higher speed. Various driving methods have been proposed, but none of them is a breakthrough solution. Thus, it is expected that a demand for a driving technique for coping with finer resolutions and gray scale increases will be higher.

[0005] Fig. 9 is a circuit diagram illustrating a conventional driving circuit described in JP 2003/195810 A. In the driving circuit illustrated in Fig. 9, a gate electrode of a transistor 10 is connected with a scanning line Xi, a drain electrode of the transistor 10 is connected with a drain electrode of a transistor 12. The drain electrode of the transistor 12 is connected with a power source line Vi. A gate electrode of the transistor 12 is connected with a source electrode of the transistor 10. A source electrode of the transistor 12 is connected with a drain electrode of a transistor 11 and with anodes of organic EL elements Ei and Ej. A gate electrode of the transistor 11 is connected with the scanning line Xi, and a source electrode of the transistor 11 is connected with a signal line Yj.

[0006] During a selection period, a power source signal voltage is applied on the power source line Vi. The power source signal voltage is equal to or lower than a reference potential

[0007] Vss. When the scanning line Xi becomes H (high) during the selection period, the transistors 10 to 12 are turned on. Meanwhile, a voltage across each organic EL element Ei and EJ becomes 0 or reversely biased. Thus, a programmed sink current Ij flows in a path indicated by the arrow α.

[0008] When the transistor 12 is turned on in the selection period, a gate-source voltage Vgs determined according to a driving capacity of the transistor 12 is applied on a capacitor 13. By this, an electric charge corresponding to the gate-source voltage Vgs is stored in the capacitor 13.

[0009] After that, in a non-selection period in which the scanning line Xi becomes L (low) after the selection period is ended, the capacitor 13 thus charged during the selection period applies a positive voltage across the gate and source of the transistor 12, thereby turning on only the transistor 12.

[0010] Moreover, a power source signal voltage to be applied on the power source line Vi during the non-selection period is a power source voltage Vdd that is sufficiently higher than the reference potential Vss. Thus, a forwardly biased voltage is applied on the organic EL elements Ei and Ej. The transistor 12 supplies the organic EL elements with a constant electric current whose ampere is equal to Ij. That is, it is possible to supply a constant electric current to the organic EL elements Ei and Ej even if the transistors 12 are uneven in terms of properties.

[0011] US 2009/002281 A1 shows an active matrix organic electroluminescence(EL) display that comprises plural selection and data lines mutually crossed, and a pixel circuit connected to the selection and data lines and having switching devices, a storage capacitor and an organic EL device. In a part of a period that the pixel circuit connected to the selection line is being selected, an applied first data signal is held as a voltage at the storage capacitor of the selected pixel circuit. After the selection signal applying, a first current according to the held voltage is supplied to the organic EL device, and this emits light at luminance according to the first current. In another part of the period, a second current according to an applied second data signal is supplied to the organic EL device of the selected pixel circuit, and this emits light at luminance according to the second current.

[0012] EP 1 424 680 A2 tries to accomplish improvement of overall display quality by employing drive modes depending upon display targets in an electro-optical device employing electro-optical elements for emitting light with a brightness corresponding to a driving current. When a first drive mode is selected as a drive mode, a drive mode selecting circuit 6 drives the electro-optical elements for a first light emitting time period shorter than a time period from a time point at which the scanning line corresponding to the pixel 2 in which data should be written is selected to a time point at which the scanning line is next selected. In addition, when a second drive mode other than the first drive mode is selected as a drive mode, the drive mode selecting circuit 6 drives the electro-optical element for a second light emitting time period longer than the first light emitting time period in the time period from a time point at which the scanning line corresponding to the pixel 2 in which data should be written is se-

lected to a time point at which the scanning line is next selected.

Summary of Invention

Technical Problem

[0013] The current programming in the driving circuit illustrated in Fig. 9 uses an electric current source as the signal source. However, it is difficult to realize an electric current source capable of controlling minute currents of an order of several ten nA. Further, in case where the programming is carried out with such a minute electric current as above, it is time-consuming to charge a parasite capacitor of lines or a pixel circuit with the minute electric current. As a result, a writing period will not be long enough.

[0014] On the other hand, in the driving circuit of Fig. 9, the programming the voltage by using a voltage source as the signal source does not have the problem of not enough writing time. However, the light emitting ampere becomes more minute in association with the improvement of the EL elements to be more efficient, such as development of fluorescent materials. Meanwhile, the driving transistor for converting a programming voltage into a light emitting current is a TFT. As a result of technical development to improve the TFT in mobility, the TFT has become able to provide a greater current amplitude from a smaller voltage change. As a result, it has become necessary to control a more minute voltage in order to control a more minute current. It is difficult to accurately supply such a minute voltage.

[0015] To overcome this problem, a technique may be sometimes adopted, in which black is inserted in a later half of a frame in order to increase luminance in a light emitting period. This is because the luminance seems to be identical apparently as long as luminance integral value is constant in a frame period.

[0016] However, the black insertion would not be sufficient to solve the difficulty of the current control. In such a case, it is necessary to perform control of a minute current of several 10 nA in the hold mode.

[0017] This current control converts a voltage value to a current value by using a driving TFT in a current pixel, so as to supply a control current to the EL element. However, an influence of uneven threshold among TFTs becomes greater in the minute current ranges. Therefore, it is considered that it will be difficult to provide a highly sensitive driving TFT for controlling such a minute current.

[0018] It is further known that, if the driving is carried out with further brighter instant luminance and a longer black period in order to overcome this drawback, it becomes necessary to significantly increase the brightness of the higher-side gray scales during the light emitting period, thereby resulting in a shorter light of the organic EL element.

[0019] The present invention was accomplished in view of the aforementioned problem and an object of the present invention is to provide a display device and a drive method for the display device, in each of which gray scale control can be performed more easily than conventional gray scale control, a longer life of the organic EL element can be achieved by lowering the instant luminance, and a lower power consumption can be achieved.

Solution to Problem

[0020] The invention is defined by the subject matter of the independent claims. Advantageous embodiments are subject to the dependent claims.

[0021] According to the present invention, if a pixel is to display in a lower-side gray scale, the pixel is driven in the impulse mode for attaining easy gray scale control, and if a pixel is to display in a higher-side gray scale, the pixel is driven in the hold mode for attaining a longer life.

[0022] With this, the first signal source supplies the light emitting signal in case the driving is carried out in the impulse mode. This allows the ampere value for the lowest gray scale
to be larger than conventional gray scale control, thereby making it possible to perform the gray scale control more easily than the conventional gray scale control.

[0023] Meanwhile, the second signal source supplies the light emitting signal in case the driving is carried out in the hold mode. This allows the ampere value for the highest gray scale to be smaller than the conventional gray scale control, thereby making it possible to prolong the life of the device.

[0024] Especially in a display device with high resolution, if the gray scale range driven in the impulse mode is small and the gray scale rage driven in the hold mode is large, the current control can be carried out by effectively utilizing the ranges of the gray scales.

[0025] Further, compared with the conventional art, the present invention has the following advantages. A first advantage is that it becomes unnecessary to change the timing of the data output, thereby making it possible to further simplify the configuration of the control circuit in the gate driver circuit. A second advantage is that it is possible to perform the light emission during the whole selection period, a longer life is achieved by reducing the instant luminance.

[0026] A third advantage is that the technology described in the present embodiment is useful in achieving lower power consumption. In the hold mode of the conventional driving circuit, the current is supplied to the organic EL element through the driving transistors continuously. If a driving transistor is driven in a saturation region, a voltage drop occurs across the driving transistor. The voltage drop causes an energy to be consumed in heat release rather than in the light emission, thereby wasting the energy. On the other hand, in the impulse mode, the light emission current is supplied via a switching element operating in a linear region, thereby reducing the power loss as small as possible. That is, compared

with the hold mode of the conventional driving circuit, it is possible to reduce the power loss in case where the driving is carried out in the impulse mode. Thus, it becomes possible to realize a display device whose power consumption is reduced.

Advantageous Effects of Invention

[0027] With the display device of claim 1 and the drive method of claim 10, it becomes possible to provide a display device and a drive method for the display device, in each of which gray scale control can be performed more easily than conventional gray scale control, a longer life of the device can be achieved by lowering the instant luminance, and a lower power consumption can be achieved.

Brief Description of Drawings

[0028]

Fig. 1 is a circuit diagram of a pixel circuit according to an Example of the present invention.
Fig. 2 is a timing chart showing operation of the pixel circuit according to the Example of the present invention.
Fig. 3 is a block diagram illustrating a display device according to the Example of the present invention.
Fig. 4 is a flowchart illustrating how driving only in a hold mode and driving both in an impulse mode and the hold mode are switched over according to an image source.
Fig. 5 is a circuit diagram of a pixel circuit according to another Example of the present invention.
Fig. 6 is a timing chart showing operation of the pixel circuit according to the another Example of the present invention.
Fig. 7 is a circuit diagram of a pixel circuit according to still another Example not forming part of the present invention.
Fig. 8 is a timing chart showing operation of the pixel circuit according to the still another Example not forming part of the present invention.
Fig. 9 is a circuit diagram of a conventional driving circuit described in JP 2003/195810 A.

Description of Embodiments

[0029] One embodiment of the present invention is described below, referring to Examples 1 to 2 and Figs. 1 to 6. To begin with, a configuration of a display device 1 according to the embodiment of the present invention.

[Configuration of Display Device]

[0030] Fig. 3 is a block diagram illustrating a configuration of the display device 1 according to the present embodiment. The display device 1 includes a source driver circuit 2 for driving a plurality of (an m number of) data signal lines S1, S2, ..., Sm, and a gate driver circuit 3 for controlling a plurality of (an n number of) scanning lines G1, G2, ..., Gn and a plurality of (an n number of) scanning lines R1, R2, ..., Rn, and a display section 4 having a plurality of (an m × n number of) pixels A11, ... , A1m, ... , An1, ... Anm, and a control circuit 5 for controlling the source driver circuit 2 and the gate driver circuit 3.

[0031] The source driver circuit 2 includes a shift register, a data latch section, and a switch section and is configured to supply a voltage signal or a current signal to a selected column. The gate driver circuit 3 includes a shift register, a data latch section, and a switch section, like the source driver circuit 2, and is configured to control the scanning
lines G1, G2, ..., Gn and the scanning lines R1, R2, ..., Rn. The gate driver circuit 3 is configured to supply a control signal to a selected row. The control circuit 5 is configured to output a control clock or a start pulse. The shift registers of the source driver circuit 2 and the gate driver circuit 3 are configured to output signals to select the column or row.

[0032] The display section 4 of the display device 1 includes the n number of scanning lines G1 to Gn, the m number of data signal lines S1 to Sm crossing the n number of scanning lines G1 to Gn, and the m × n number of pixels A11, ... , A1m, ... , An1, ... Anm, provided correspondingly to intersections between the n number of scanning lines G1 to Gn and the m number of data signal lines S1 to Sm. The pixels may be picture elements. The pixels A11, ..., A1m, ..., An1, ... Anm are provided in matrix, thereby constituting a pixel array. In the following, a direction in which the scanning lines are extended is referred to as a row direction, and a direction in which the data signal lines are extended is referred to as a column direction.

[0033] In Examples 1 to 2, pixel circuits of the pixels A11, ..., A1m, ..., An1, ... Anm are described in terms of their configuration and operation.

[Example 1]

[0034] Fig. 1 is a circuit diagram of a pixel circuit 6 according to Example 1. Fig. 2 is a timing chart illustrating an operation of the pixel circuit 6 according to Example 1. Firstly, a configuration of the pixel circuit 6 is explained below, referring to Fig. 1.

[0035] The pixel circuit 6 is a pixel circuit provided for a pixel Aij provided correspondingly to intersections between an i-th scanning line Gi and a j-th data signal line Sj and between an i-th scanning line Ri and the j-th data signal line Sj, where i = 1 to n and j = 1 to m.

[0036] The pixel circuit 6 includes an organic EL (Electro luminescence) diode element 7 (a element for emitting light at a luminance that is dependent on a current flowing the organic EL diode 7), a thin film transistor (TFT) T1 to T3, and a capacitor C. The TFT T1 to T3 may be N-

channel TFTs, so as to allow employ an amorphous silicon panel in the display device 1, which amorphous silicon panel has a difficulty of adopting P-channel TFTs.

[0037] In the pixel circuit 6, the TFT T1 has a gate connected to the i-th scanning line Gi. The TFT T2 has a gate connected to the i-th scanning line Ri. The TFT T3 has a gate connected with a source of the TFT T2 and one end of the capacitor C. The TFT T3 has a drain connected with a power source line Vp.

[0038] The TFT T3 has a source connected with a drain of the TFT T1, another end of the capacitor C, and an anode of the organic EL diode 7. The TFT T1 has a source connected with a j-th data signal line Sj.

[0039] A drain of the TFT T2 and a cathode of the organic EL diode 7 are electrically grounded.

[0040] The j-th data signal line Sj is connected with a programmed current source I1 for the lower-side gray scale display, in case where the pixel Aij is to display at a lower-side gray scale. On the other hand, the j-th data signal line Sj is connected with a programmed current source I2 for the higher-side gray scale display , in case where the pixel Aij is to display at a higher-side gray scale. Switching-over between connecting the j-th data signal line Sj with the current source I1 and connecting the j-th data signal line Sj with the current source I2 is performed by using a switch SW. The later-described source driver circuit 2 as illustrated in Fig. 3 includes the current sources I1 and I2, and the switch SW.

[0041] The operation of the pixel circuit 6 as such is explained below, referring to the timing charge of Fig. 2.

[0042] As a start of a "selection period" of a selected row, signal levels of the scanning lines Gi and Ri of the selected row are changed from L (low) to H (high). The signal levels change from H to L at an end of the selection period.

[0043] The pixel circuit 6 is driven in the impulse mode when the pixel Aij displays at a lower-side gray scale. That is, the pixel circuit 6 is driven to cause the organic EL diode 7 to emit light only during the selection period. More specifically, in Fig. 2, sourcing of the programmed current I is performed, that is, the j-th data signal line Sj is connected to the programmed current source I1 for the lower-side gray scale display.

[0044] In this case, a potential corresponding to the data of the data signal line Sj becomes positive, and a potential at the source of the TFT T1 is positive. Moreover, during the selection period, potentials at the TFTs T1 and T2 are turned on. Accordingly, the drain of the TFT T1, the another end of the capacitor C and the anode of the organic EL diode 7 become positive because they receive the positive potential from the source of the TFT T1. The gate of the TFT T3 and the one end of the capacitor C are electrically grounded to have a ground potential.

[0045] As a result of this, the organic EL diode 7 receives a forward biased voltage is applied, thereby the organic EL diode 7 is turned on. Moreover, a gate-source voltage Vgs of the TFT T3 becomes negative, thereby turning off the TFT T3.

[0046] Consequently, the programmed current I flows in a route as follows: an output terminal of the programmed current source I1 for the lower-side gray scale display → the data signal line Sj → the source of the TFT T1 → the drain of the TFT T1 → the anode of the organic EL diode 7 → the cathode of the organic EL diode 7. As a result, the organic EL diode 7 emits light.

[0047] Meanwhile, the TFT T1 does not start output of a drain current immediately in response to the change of the signal level of the scanning line Gi from L to H. It takes a delay time and a rising time for the drain current of the TFT T1 to reach its saturation. The delay time and the rising time will be explained later. Due to this feature of the TFT T1, a current waveform Eli of the organic EL diode 7 (i-th row) and a current waveform Eli-1 of the organic EL diode 7 (i-1th row) slowly raise during the delay time and the rising time.

[0048] The luminance of the light emission of the organic EL diode 7 is determined by an ampere value of the programmed current I set by the programmed current source I1 for the lower-side gray scale display. The ampere value of the programmed current I and the gray scale value are in a proportional relationship.

[0049] After the end of the selection period, the TFTs T1 and T2 are turned off, thereby not allowing the flow of the programmed current I. Moreover, the gate-source voltage Vgs of the TFT T3 becomes 0 or negative, thereby turning off the TFT T3. As a result, the organic EL diode 7 is turned off.

[0050] The TFT T1 is not turned off immediately in response to the change of the signal level of the scanning line Gi from H to L. It takes a delay time and a falling time for the TFT T1 to be turned off. Due to this feature of the TFT T1, a current waveform Eli of the organic EL diode 7 (i-th row) and a current waveform Eli-1 of the organic EL diode 7 of (i-1th row) slowly fall during the delay time and the falling time.

[0051] In the explanation above, the delay time is a time period from a time when an ideal pulse of the drain current of a TFT appears to a time when an amplitude of an actual pulse of the drain current becomes 10%, or a time period from the time when an amplitude of an actual pulse of the drain current becomes 10%, to a time when the amplitude becomes 0. Moreover, the rising time is a time period in which the amplitude becomes 90% from 10%. Further, the falling time is a time period in which the amplitude becomes 10% from 90%.

[0052] While the current waveform Eli in Fig. 2, is a current waveform of the pixel Aij controlled by the scanning lines Gi and Ri, it should be noted that not all the pixels controlled by the scanning lines Gi and Ri are driven in the impulse mode. Among the pixels associated with the data signal line Sj, there are pixels driven in the impulse mode and the pixels driven in the hold mode. In order to perform black insertion for the pixels driven in the hold mode, a black insertion period is provided in which the signal level of the scanning line Gi is set to L

and the signal level of the scanning line Ri is set to H.

[0053] Next, the pixel circuit 6 is driven in the hole mode when the pixel Aij displays at a higher-side gray scale. That is, the pixel circuit 6 is configured to cause the organic El diode 7 to emit the light not during the selection period but after the selection period. More specifically, the programmed current I' in Fig. 2 is sunk. That is, the j-th data signal line Sj is connected to the programmed current source I2 for the higher-side gray scale display.

[0054] In this case, the potential of the data signal line Sj is negative and the potential at the source of the TFT T1 is negative. Moreover, the TFTs T1 and T2 are turned of during the selection period. Accordingly, the drain of the TFT T1, the another end of the capacitor C and the anode of the organic EL diode 7 become negative because they receive the negative potential from the source of the TFT T1. The gate of the TFT T3 and the one end of the capacitor C are electrically grounded to have a ground potential.

[0055] As a result of this, the organic EL diode 7 receives a reverse biased voltage is applied, thereby the organic EL diode 7 is turned off. Moreover, the gate-source voltage Vgs of the TFT T3 becomes positive, thereby turning on the TFT T3.

[0056] Consequently, the programmed current I' flows in a route as follows: the power source line Vp → the drain of the TFT T3 → the source of the TFT T3 → the drain of the TFT T1 → the source of the TFT T1 → the data signal line Sj → an input terminal of the programmed current source I2 for the higher-side gray scale display → an output terminal of the programmed current source I2 for the higher-side gray scale display. The programmed current I' has an ampere value corresponding to the gray scale value. The ampere value of the programmed current I' is set by the programmed current source I2 for the higher-side gray scale display.

[0057] After the end of the selection period, the source potential of the TFT T3 is changed in accordance with the anode potential of the organic EL diode 7. Moreover, the gate potential of the TFT T3 follows the change of the source potential of the TFT T3 so as to keep the gate-source voltage Vgs of the TFT T3 constant. This is caused because the TFT T2 is turned off and thereby is in a floating state.

[0058] The gate-source voltage Vgs of the TFT T3 in the selection period is maintained even after the selection period because the capacitor C charged with the gate-source voltage Vgs during the selection period. Because of this the TFTs T1 and T2 are turned off after the selection period, while the TFT T3 is kept on after the selection period.

[0059] As a result, the programmed current I", whose ampere value is substantially identical with that of the programmed current I' flowing in the selection period, flows in a route as follows: the power source Vp → the drain of the TFT T3 → the source of the TFT T3 → the anode of the organic EL diode 7 → the cathode of the organic EL diode 7.

[0060] However, the TFT T1 is not turned off immediately in response to the change of the signal level of the scanning line Gi from H to L. It takes a delay time and a falling time of the TFT T1 to turn off. Thus, the current waveform E1i+1th of the organic EL diode 7 (i+ 1 th row) slowly falls during the delay time and the falling time.

[0061] In case where black is inserted after the end of the selection period, the signal level of the scanning line Gi is set to L and the signal level of the scanning line Ri is set to H. By this, the TFT T1 is turned off and the TFT T2 is turned on. Because the TFT T2 is turned on, the gate potential of the TFT T3 is grounded thereby turning off the TFT T3. Because the TFT T3 is turned off, the programmed current I" does not flow, thereby turning off the organic EL diode 7.

[0062] The TFT T3 is not turned off immediately in response to a change of the signal level of the scanning line Ri from L to H. It takes a delay time and a falling time for the drain current of the TFT T3 to turn off. Because of this, the current waveform Eli+1 of the organic EL diode 7 slowly falls during the delay time and the falling time.

[0063] In the pixel circuit 6 of Example 1, the direction of the programmed current I flowing in the date signal line Sj in the impulse mode and the direction of the programmed current I' flowing in the data signal line Sj in the hold mode are opposite with in each other along the data signal line Sj.

[0064] By this, it is possible to distinguish the impulse mode and the hold mode by referring to the direction of the programmed current.

[0065] Both in the impulse mode and hold mode, the data output can be in the same timing as the start and end of the selection period. Thus, it is not necessary to complicate the circuit for controlling the timing of the data output.

[0066] Further, the luminance of the EL element is controlled by the current directly flowing the EL element. Therefore, it is possible to attain uniform luminance distribution that is not influenced by unevenness (individual differences) of the driving TFTs used for driving the pixel circuit.

[0067] Note that the "Selection Period", "Frame Period", "Black Insertion Period" etc. in Fig. 2 are those of the i-th row.

[0068] The present invention proposes an arrangement in which, if the pixel Aij is to display at a lower-side gray scale, the pixel Aij is driven in the impulse mode for easy gray scale control and if the pixel Aij is to display at a higher-side gray scale, the pixel Aij is driven in the hold mode for longer life, where the whole gray scales are classified into the lower-side gray scales and the higher-side gray scales.

[0069] In Example 1, as illustrated in Table 1 below, the whole gray scales are 0 to 255 gray scales. For 0 to 32 gray scales, the driving is carried out in the impulse mode. For 33 and greater gray scales, the driving is carried out in "the hold mode in which black is inserted in 90% of one frame period".

[0070] For black, that is, 0 gray scale, the driving can be carried out either in the impulse mode or the hold mode.

Table 1

Ampere Value For Light Emission in Impulse/Hold mode * The hold mode is 90% black insertion hold mode in which the white current = 10 μA.		
Gray scales	Impulse (μA)	Hold (μA)
255	1076	10.0
128	540	0.0
64	270	2.5
33	139	1.29
32	135	1.25
16	68	0.63
8	34	0.31
4	17	0.16
2	8	0.08
1	4.2	0.04
* Assuming that the number of lines = 1080.		

[0071] In this driving method, the ampere value for the lowest gray scale is 4.2 μA, while the ampere value for the lowest gray scale was 40 nA if the driving for the lowest gray scale is carried out in the hold mode. This makes it easier to carry out the gray scale control.

[0072] In this driving method, the ampere value for the largest gray scale is 10 pA, while the ampere value for the largest gray scale was 1 mA or greater if the driving for the largest gray scale is carried out in the impulse mode. This provides a longer life than the conventional art.

[0073] Especially in a display device with high resolution, if the gray scale range driven in the impulse mode is small and the gray scale rage driven in the hold mode is large, the current control can be carried out by effectively utilizing the ranges of the gray scales. If the range of the gray scales driven in the impulse mode is larger, the ampere value necessary to perform the driving is increased and it becomes necessary to flow a large current instantly. Thus, it is not preferable that the range of the gray scales driven in the impulse mode is larger.

[0074] Further, compared with the conventional art, the present invention has the following advantages. A first advantage is that it becomes unnecessary to change the timing of the data output, thereby making it possible to further simplify the configuration of the control circuit in the gate driver circuit. A second advantage is that it is possible to perform the light emission during the whole selection period, a longer life is achieved by reducing the instant luminance.

[0075] A third advantage is that the technology described in the present embodiment is useful in achieving lower power consumption. In the hold mode of the conventional driving circuit, the current is supplied to the organic EL element through the driving transistors continuously. If a driving transistor is driven in a saturation region, a voltage drop occurs across the driving transistor. The voltage drop causes an energy to be consumed in heat release rather than in the light emission, thereby wasting the energy. On the other hand, in the impulse mode, the light emission current is supplied via a switching element operating in a linear region, thereby reducing the power loss as small as possible. That is, compared with the hold mode of the conventional driving circuit, it is possible to reduce the power loss in case where the driving is carried out in the impulse mode. Thus, it becomes possible to realize a display device whose power consumption is reduced.

[0076] The switching-over between the impulse mode and the hold mode may not be carried out based on the gray scales. For example, in a gray scale distribution for a first pattern for displaying a mainly-black-and-white display content such as text, the gray scale for displaying white and the gray scale for displaying black are more abundant than the other gray scales. In such a first pattern, the display quality deterioration due to the uneven gray scales is not significant. Thus, the pixel circuit is driven only in the hold mode irrespectively of the gray scales, so that the life of the organic EL element can be prolonged.

[0077] On the other hand, a gray scale distribution for a second pattern for displaying a content, such as photos and moving pictures, in which uneven gray scales causes display quality deterioration is a distribution ranged widely over the whole gray scales, for example. In such a second pattern, the pixel circuits are driven both in the impulse mode and the hold mode.

[0078] Fig. 4 illustrates one exemplary flow chart showing how to switch over, according to image sources, the driving method for driving only in the hold mode and the driving method for driving both in the impulse mode and the hold mode. That is, the display device 1 has means for analyzing an image signal, and is configured to switch over the two driving method based on whether an image to be displayed is a moving picture or not, how large an area of the black display, and whether the image to be displayed is mainly text or not.

[0079] In the flowchart in Fig. 4, whether the image signal is for a moving picture or not is determined at Step s1. If the image signal is for a moving picture (Yes at Step S1), the driving method for driving both in the impulse mode and the hold mode is employed.

[0080] If the image signal is not for a moving picture (No at Step s1), it is determined whether or not signals for intermediate-lengths accounts for 90% or more of the image signal (Step s2), in order to determine whether the area of the black display is large or small. If the signals for the intermediate-lengths accounts for less than 90%

of the image signal (No at Step s2), the driving method for driving only in the hold mode is employed.

[0081] If the signals for the intermediate-lengths accounts for 90% or more of the image signal (Yes at Step s2), then it is determined whether or not the image to be displayed based on the image signal is mainly text (Step s3). If the image to be displayed based on the image signal is mainly text (Yes at Step s3), the driving method for driving only in the hold mode is employed. If the image to be displayed based on the image signal is not mainly text (No at Step s3), the driving method for driving both in the impulse mode and the hold mode is employed.

[0082] As described above, the two driving methods can be selected only be switching over the signal current sources. Therefore, no special control is necessary to change the control every time the type of the image to be displayed is switched over.

[0083] As described above, the gray scale distribution of the gray scales constituting the image to be displayed can be the criterion to switch over the impulse mode and the hold mode, that is, to switch over whether to drive the pixel circuit 6 both in the impulse mode and the hold mode, or to drive only in the hold mode. The source driver circuit 2 may have the criterion, or the control circuit 5 may have the criterion.

[Example 2]

[0084] Another Example of the present invention is described below, referring to Figs. 5 and 6. Example 2 has a configuration identical with that of Example 1, except what is described herein. For the sake of easy explanation, members having functions like those of the members illustrated in the drawings for Example 1 are like numbered and their explanation is not repeated here.

[0085] Fig. 5 is a circuit diagram of a pixel circuit 8 according to Example 2. The pixel circuit 8 is different from the pixel circuit 6 of Example 1 in terms of the following point.

[0086] The pixel circuit 6 of Example 1, the drain of the TFT T2 is electrically grounded, and the drain of the TFT T3 is connected to the power source Vp.

[0087] On the other hand, the pixel circuit 8 of Example 2 is configured such that a drain of a TFT T2 and a drain of a TFT T3 are connected to a common power source line Pi, whose potential is, as illustrated in a timing charge of Fig. 6, a ground potential during the selection period, but is a potential Vp' during the non-selection period, where the potential Vp' is greater than the grounding potential.

[0088] With this configuration, the pixel circuit 8 is not only capable of operating in the same way as the pixel circuit 6 of Example 1, but also capable of commonly utilizing the common power source line Pi instead of separately using the power source line for the ground potential and the power source line for the potential Vp' greater than the ground potential. By this, it is possible to reduce the number of the power source lines by one per row.

[Example 3]

[0089] A comparative Example not forming part of the present invention is described below referring to Figs. 7 and 8. Example 3 has a configuration identical with those of Examples 1 and 2, except what is described herein. For the sake of easy explanation, members having functions like those of the members illustrated in the drawings for Example 1 or 2 are like numbered and their explanation is not repeated here.

[0090] Fig. 7 is a circuit diagram of a pixel circuit 9 according to Example 3. The pixel circuit 8 is different from the pixel circuit 6 of Example 1 in the following points.

[0091] In the pixel circuit 6 according to Example 1, the gate of the TFT T1 is connected to the i-th scanning line Gi, and the gate of the TFT T2 is connected to the i-th scanning line Ri.

[0092] On the other hand, the pixel circuit 9 of Example 3 is configured such that a gate of a TFT T1 and a gate of a TFT T2 are connected to an i-th scanning line Gi, commonly.

[0093] With this configuration, the pixel circuit 9 is not only capable of perform the same no-black-insertion operation which the pixel circuit 6 of Example 1 performs, but also capable of using the scanning line Gi commonly. By this, it is possible to reduce the number of the scanning line by one per row.

[0094] Fig. 8 is a timing chart illustrating an operation of the pixel circuit 9 according to Example 3. Unlike the timing chart of Fig. 3, the timing chart of Fig. 8 has no waveform of the scanning line Ri.

[0095] It should be noted that the pixel circuits 6, 8, and 9 of the present embodiment is applicable not only to an organic EL diode 7 but also to a semiconductor light emitting diode.

[0096] Moreover, the display device 1 may be configured such that the programmed current source I1 for the lower-side gray scale display and the programmed current source I2 for the higher-side gray scale display are current sources for outputting the currents in opposite directions.

[0097] Further, instead of the current sources I1 and I2, the display device 1 may use voltage sources one of which shows a positive voltage change in response to a gray scale change, and another one of which shows a negative voltage change in response to the gray scale change.

[0098] Further, the display device 1 may be configured such that the driving in the impulse mode is carried out for lower-side gray scales and the driving in the hold mode is carried out for higher-side gray scales, where the whole gray scales of the programmed current I or I' are classified into the lower-side gray scales and the higher-side gray scales.

[0099] Further, the display device 1 may be configured such that the lower-side gray scales are ranged from a lowest gray scale of the whole gray scales of the light emitting signal to a gray scale smaller than a 1/2 gray

scale which is a center gray scale at the middle of the whole gray scales of the programmed current I, and the higher-gray scales are ranged from the gray scale smaller than the 1/2 gray scale, to a highest gray scale of the whole gray scales of the light emitting signal.

[0100] Further, according to the display device 1 according to the present Example, the combinational use of the impulse mode and the hold mode provides a wider color reproducible range both on the lower-gray scale side and the higher-gray scale side. Therefore, the whole color reproducible range achieved by color combination can be dramatically widened.

(Summary]

[0101] The display device 1 may be configured such that: the plurality of scanning lines encompass a plurality of scanning lines G1, G2, ..., Gn, Gi and a plurality of scanning lines R1, R2, ..., Rn, Ri; the pixel circuit 6 includes a thin film transistor T1, a thin film transistor T2, a thin film transistor T3, and a capacitor C; the thin film transistor T1 has a gate connected with the scanning line Gi, and a source connected with the data signal line Sj; the thin film transistor T2 has a gate connected with the scanning line Ri, a drain being electrically grounded, and a source connected with a gate of the thin film transistor T3 and with one end of the capacitor C; the thin film transistor T3 has a drain connected with a power source line Vp, a source connected with a drain of the thin film transistor T1, with another end of the capacitor C, and with an anode of the organic EL diode 7; the organic EL diode 7 has a cathode being electrically grounded; the source driver circuit 3 has the programmed current source I1 for the lower-side gray scale display, the programmed current source I2 for the higher-side gray scale display, and a switch SW; and for the pixel All, ... A1m, ... An1, ..., Anm, or Aij displaying an image in the impulse mode, the switch SW connects a corresponding one of the data signal lines S1, S2, ..., Sm, Sj with the programmed current source I1, and for a pixel All, ... A1m, ... An1, ..., Anm, or Aij displaying an image in the hold mode, the switch SW connects a corresponding one of the data signal lines S1, S2, ..., Sm, Sj with the programmed current source I2.

[0102] In the selection period, the signal level of the scanning line Gi and the signal level of the scanning line Ri are at the high level. By this, in the impulse mode, the programmed current I is supplied in the following route: the programmed current source I1 for the lower-side gray scale display → the data signal line Sj → the source of the TFT T1 → the drain of the TFT T1 → the anode of the organic EL diode 7 → the cathode of the organic EL diode 7. Thereby, the organic EL diode 7 emits light.

[0103] In the hold mode, a reversely biased voltage is applied on the organic EL diode 7 during the selection period, thereby turning off the organic EL diode 7. Meanwhile, the gate-source voltage of the TFT T3 becomes positive, thereby turning on the TFT T3.

[0104] Therefore, the programmed current I' is supplied in the following route: the power source line Vp → the drain of the TFT T3 → the source of the TFT T3 → the drain of the TFT T1 → the source of the TFT T1 → the data signal line Sj → the programmed current source I2 for the higher-side gray scale display.

[0105] Because the capacitor C is charged with the gate-source voltage during the selection period of the TFT T3, the gate-source voltage of the TFT T3 during the selection period is maintained after the end of the selection period. Because of this, the TFT transistors T1 and T2 are turned off after the end of the selection period, but the TFT T3 is kept on after the end of the selection period.

[0106] Thus, the programmed current I", whose ampere value is substantially identical with that of the programmed current I', is supplied in the following route: the power source line Vp → the drain of the TFT T3 → the source of the TFT T3 → the anode of the organic EL diode 7 → the cathode of the organic EL diode 7.

[0107] In case black is inserted after the end of the selection period, the signal level of the scanning line Gi is low and the signal level of the scanning line Ri is high. By this, the TFT T1 is turned off and the TFT T2 is turned on. The TFT T3 is turned off, while the TFT T2 is turned on. The TFT T3 is turned off because the gate potential of the TFT T3 is electrically grounded by turning on the TFT T2. Because TFT T3 is turned off, the programmed current I" is not supplied, thereby turning off the organic EL diode 7.

[0108] Therefore, it becomes possible to arrange such that, in case where the gray scale of the programmed current I is a lower-side gray scale, the driving is carried out in the impulse mode, and in case where the gray scale of the programmed current I is a higher-side gray scale, the driving is carried out in the hold mode.

[0109] The display device 1 may be configured such that: the plurality of scanning lines encompass a plurality of scanning lines G1, G2, ..., Gn, Gi, and a plurality of scanning lines R1, R2, ..., Rn, Ri; the pixel circuit 8 includes a thin film transistor T1, a thin film transistor T2, a thin film transistor T3, and a capacitor C; the thin film transistor T1 has a gate connected with the scanning line Gi, and a source connected with the data signal line Sj; the thin film transistor T2 has a gate connected with the scanning line Ri, a drain being electrically connected to a common power source line Pi, and a source connected with a gate of the thin film transistor T3 and with one end of the capacitor C; the thin film T3 transistor has a drain connected with the common power source line Pi, a source connected with a drain of the thin film transistor T1, with another end of the capacitor C, and with an anode of the organic EL diode 7; the organic EL diode 7 has a cathode being electrically grounded; the source driver circuit 3 has the programmed current source I1 for the lower-side gray scale display, the programmed current source I2 for the higher-side gray scale display, and a switch SW; for the pixel All, ..., A1m, ..., An1, ..., Anm, or Aij, displaying an image in the impulse mode, the switch

SW connects a corresponding one of the data signal lines S1, S2, ..., Sm, Sj, with the current source I1, and for the pixel A11, ..., A1m, ..., An1, ..., Anm, or Aij, displaying an image in the hold mode, the switch SW connects a corresponding one of the data signal lines S1, S2, ..., Sm, Sj, with the current source I2; and the common power source line Pi has a ground potential during the selection period, and an potential greater than the ground potential not during the selection period.

[0110] With this configuration, the pixel circuit 8 is not only capable of operating in the same way as the pixel circuit 6 configured such that the drain of the TFT T3 is connected to the power source line Vp, but also capable of commonly utilizing the common power source line Pi instead of separately using the power source line for the ground potential and the power source line for the potential Vp' greater than the ground potential. By this, it is possible to reduce the number of the power source lines by one per row.

[0111] According to Example 3 not forming part of the invention, the display device 1 may be configured such that: the pixel circuit 9 includes a thin film transistor T1, a thin film transistor T2, a thin film transistor T3, and a capacitor C; the thin film transistor T1 has a gate connected with the scanning line Gi, and a source connected with the data signal line Sj; the thin film transistor T2 has a gate connected with the scanning line Gi, a drain being electrically grounded, and a source connected with a gate of the thin film transistor T3 and with one end of the capacitor C; the thin film transistor T3 has a drain connected with a power source line Vp, a source connected with a drain of the thin film transistor T1, with another end of the capacitor C, and with an anode of the organic EL diode 7; the organic EL diode 7 has a cathode being electrically grounded; the source driver circuit 3 has the programmed current source I1 for the lower-side gray scale display, the programmed current source I2 for the higher-side gray scale display, and a switch SW; and for the pixel All, ..., A1m, ..., An1, ..., Anm, or Aij displaying an image in the impulse mode, the switch SW connects a corresponding one of the data signal lines S1, S2, ..., Sm, Sj with the programmed current source I1, and for the pixel All, ..., A1m, ..., An1, ..., Anm, or Aij displaying an image in the hold mode, the switching means connects a corresponding one of the data signal lines with the programmed current source I2.

[0112] As described above, the pixel circuit 9 is configured such that the gate of the TFT T1 and the gate of the TFT T2 are connected to the scanning line Gi, commonly.

[0113] With this configuration, the pixel circuit 9 is not only capable of perform the same no-black-insertion operation which the pixel circuit 6 or 8 using the scanning lines Gi and Ri performs, but also capable of using the scanning line Gi commonly. By this, it is possible to reduce the number of the scanning line by one per row.

[0114] The display device 1 may be configured such that the programmed current source I1 and the programmed current source I2 are current sources configured to output currents in opposite directions.

[0115] With this configuration, the current (the first current) flowing in the data signal lines S1, S2, ... Sm, Sj in the impulse mode flow in a direction opposite to that of the current (the second current) flowing in the data signal lines S1, S2, ... Sm, Sj in the hold mode. By this, it becomes possible to distinguish the impulse mode and the hold mode from each other. Thus, it becomes possible to continue the light emission until the end of the selection period even in case of the impulse mode.

[0116] Both in the impulse mode and hold mode, the data output can be in the same timing as the start and end of the selection period. Thus, it is not necessary to complicate the circuit for controlling the timing of the data output.

[0117] Further, the luminance of the organic EL element 7 is controlled by the current directly flowing the organic EL element 7. Therefore, it is possible to attain uniform luminance distribution that is not influenced by unevenness (individual differences) of the driving TFTs used for driving the pixel circuit.

[0118] The display device 1 may be configured such that the programmed current source I1 and the programmed current source I2 are voltage sources one of which shows a positive voltage change in response to a gray scale change, and another one of which shows a negative voltage change in response to the gray scale change.

[0119] The display device 1 may be configured such that the thin film transistor T1, the thin film transistor T2, and the thin film transistor T3 are N-channel thin film transistors.

[0120] This allows to employ an amorphous silicon panel in the display device 1, which amorphous silicon panel has a difficulty of adopting P-channel TFTs.

[0121] The display device 1 may be configured such that the driving in the impulse mode is carried out for lower-side gray scales and the driving in the hold mode is carried out for higher-side gray scales, where whole gray scales of the light emitting signal are classified into the lower-side gray scales and the higher-side gray scales.

[0122] In addition, the drive method for the display device may be arranged such that the step of driving in the impulse mode is carried out for lower-side gray scales and the step of driving in the hold mode is carried out for higher-side gray scales where the whole gray scales of the programmed currents I, I', and I" are classified into the lower-side gray scales and the higher-side gray scales.

[0123] The display device 1 may be configured such that the lower-side gray scales are ranged from a lowest gray scale of the whole gray scales of the programmed currents I, I', and I", to a gray scale smaller than a 1/2 gray scale which is a center gray scale at the middle of the whole gray scales of the programmed currents I, I', and I", and the higher-gray scales are ranged from the

gray scale smaller than the 1/2 gray scale, to a highest gray scale of the whole gray scales of the programmed currents I, I', and I".

[0124] In addition, the drive method for the display device may be arranged such that the lower-side gray scales are ranged from a lowest gray scale of the whole gray scales of the programmed currents I, I', and I" to a gray scale smaller than a 1/2 gray scale which is a center gray scale at the middle of the whole gray scales of the programmed currents I, I', and I", and the higher-gray scales are ranged from the gray scale smaller than the 1/2 gray scale, to a highest gray scale of the whole gray scales of the programmed currents I, I', and I".

[0125] Further, the display device 1 may be configured such that the source driver circuit 3 has a criterion on whether to drive the pixel circuits 6 both in the impulse mode and the hold mode, or to drive the pixel circuits 6 only in the hold mode, where the criterion is based on a distribution of gray scale values constituting the image.

[0126] For example, in a gray scale distribution for a first pattern for displaying a mainly-black-and-white display content such as text, the gray scale for displaying white and the gray scale for displaying black are more abundant than the other gray scales. In such a first pattern, the display quality deterioration due to the uneven gray scales is not significant. In this case, it is possible to drive the pixel circuit 6 only in the hold mode, irrespectively of the gray scales, in order to achieve low power consumption.

[0127] On the other hand, a gray scale distribution for a second pattern for displaying a content, such as photos and moving pictures, in which uneven gray scales causes display quality deterioration is a distribution ranged widely over the whole gray scales, for example. In such a second pattern, the pixel circuit 6 is driven both in the impulse mode and the hold mode.

Industrial Applicability

[0128] The present invention makes it possible to perform the gray scale control more easily than conventional gray scale control, to prolong the life of the device by lowering the instant luminance, and to improve moving picture displaying performance. Thus, the present invention is suitably applicable to display devices for full-color image display operation.

Reference Signs List

[0129]

1: Display Device
2: Source Driver Circuit
3: Gate Driver Circuit
4: Display Section
5: Control Circuit
6, 8, 9: Pixel Circuit
7: Organic EL Diode (Element, Organic Electroluminescence Diode)
A11,...,A1m,...,An1,..., Anm, Aij: Pixels
C: Capacitor
G1, G2, ..., Gn, Gi: Scanning Lines (First Scanning Line)
R1, R2, ..., Rn, Ri: Scanning Lines (Second Scanning Line)
I: Programmed Current (Light Emitting Signal)
I': Programmed Current (Light Emitting Signal)
I": Programmed Current (Light Emitting Signal)
I1: Programmed Current Source for Lower-Side Gray Scale Display (First Signal Source)
I2: Programmed Current Source for Higher-Side Gray Scale Display (Second Signal Source)
Pi: Common Power Source Line
s1 to s3: Steps
S1, S2,....,Sm, Sj: Data Signal Lines
SW: Switch (Switch Means)
T1: Thin Film Transistor (First Thin Film Transistor)
T2: Thin Film Transistor (Second Thin Film Transistor)
T3: Thin Film Transistor (Third Thin Film Transistor)
Vgs: Gate-Source Voltage
Vp: Power Source Line
Vp': Potential Greater than Ground Potential

Claims

1. A display device (1) including:

a plurality of scanning lines (G1, G2, ...; R1, R2, ...) extended in one direction, wherein the plurality of scanning lines (G1, G2, ...; R1, R2, ...) encompass a plurality of first scanning lines (G1, G2, ...) and a plurality of second scanning lines (R1, R2, ...);
a plurality of data signal lines (S1, S2, ...) extended in another direction;
a source driver circuit (2) for driving the plurality of data signal lines;
a gate driver circuit (3) for controlling the plurality of scanning lines; and
a plurality of pixels, each pixel being provided correspondingly to each intersection between the plurality of scanning lines and the plurality of data signal lines, each pixel being provided with an element (7) for emitting light with luminance depending on an electric current supplied to the element (7), where a selection period of a pair of the first and the second scanning lines is a period in which both scanning lines of the pair are simultaneously selected by the gate driver circuit (3); and
a pixel circuit (6, 8, 9) per pixel, wherein the pixel circuit (6, 8, 9) is adapted to drive the element (7) in an impulse mode in which the element (7) emits the light only during the selection period

of the pair of the first and the second scanning lines to which the pixel circuit is connected, or in a hold mode in which the element (7) emits the light not during the selection period but after the selection period,
wherein the pixel circuit (6, 8, 9) includes a first thin film transistor (T1), a second thin film transistor (T2), a third thin film transistor (T3), and a capacitor (C);
wherein the first thin film transistor (T1) has a gate connected with a corresponding one of the first scanning lines (G1, G2, ...), and a source connected with a corresponding one of the data signal lines (S1, S2, ...);
wherein the second thin film transistor (T2) has a gate connected with a corresponding one of the second scanning lines (R1, R2, ...), a drain being electrically grounded, and a source connected with a gate of the third thin film transistor (T3) and with one end of the capacitor (C);
wherein the third thin film transistor (T3) has a drain connected with a power source line (Vp), a source connected with a drain of the first thin film transistor (T1), with another end of the capacitor (C), and with an anode of the element (7);
wherein the element (7) has a cathode being electrically grounded;
wherein the source driver circuit (2) is provided with switching means (SW), a first signal source (I1) for supplying a light emitting signal when the pixel circuit (6, 8, 9) is driven in the impulse mode, and a second signal source (I2) for supplying the light emitting signal when the pixel circuit (6, 8, 9) is driven in the hold mode, and
wherein the display device (1) is adapted to carry out the driving in the impulse mode for lower-side gray scales and to carry out the driving in the hold mode for higher-side gray scales, where whole gray scales of the light emitting signal are classified into the lower-side gray scales and the higher-side gray scales;

wherein

the first signal source (I1) and the second signal source (I2) are a first current source and second current source, respectively, and the first and second current sources are configured to output currents in opposite directions; and
wherein switching means (SW) is adapted to connect a corresponding one of the data signal lines with the first current source (I1) for the pixel displaying an image in the impulse mode, and to connect a corresponding one of the data signal lines with the second current source (I2) for the pixel displaying an image in the hold mode.

2. A display device as set forth in claim 1, wherein the drain of the second thin film transistor (T2) is connected to the power source line, a potential of which is 2 ground potential during the selection period and is 2 potential (Up') greater than the ground potential during the non-selection period.

3. The display device as set forth in claim 1 or 2, wherein the first thin film transistor (T1), the second thin film transistor, (T2), and the third thin film transistor (T3) are N-channel thin film transistors.

4. The display device as set forth in one of claims 1 to 3, wherein the lower-side gray scales are ranged from a lowest gray scale of the whole gray scales of the light emitting signal to a gray scale smaller than a 1/2 gray scale which is a center gray scale at the middle of the whole gray scales of the light emitting signal, and the higher-gray scales are ranged from the gray scale smaller than the 1/2 gray scale, to a highest gray scale of the whole gray scales of the light emitting signal.

5. The display device as set forth in claim 1, wherein the source driver circuit (2) is configured to drive the pixel circuits (6, 8, 9) both in the impulse mode and the hold mode or to drive the pixel circuits (6, 8, 9) only in the hold mode, based on a distribution of gray scale values constituting the image.

6. The display device as set forth in one of claims 1 to 5 wherein the element (7) is an organic electroluminescence diode.

7. The display device as set forth in one of claims 1 to 6, wherein the gate driver circuit (3) is adapted to provide, when carrying out the driving in the hold mode for higher-side gray scales, a black insertion period, in which the gate driver circuit (3) sets the signal level of the first scanning lines (G1, G2, ...) to a low signal level and sets the signal level of the second scanning lines (R1, R2, ...) to a high signal level.

8. The display device as set forth in one of claims 1 to 7, wherein a current is supplied to the element via the first thin film transistor (T1) being adapted to operate in a linear region in the impulse mode.

9. The display device as set forth in one of claims 1 to 8, wherein the display device is adapted to emit light in the impulse mode in a state where the third thin film transistor (T3) is turned off.

10. A method for driving the display device (1) according to one of claims 1 to 9, the drive method comprising:

driving a pixel circuit (6, 8, 9) of the pixels in the impulse mode for the lower-side gray scales or

in the hold mode for the higher side gray scales;
connecting, by the switching means (SW) of the display device (1), a corresponding one of the data signal lines with the first current source (II) for the pixel displaying an image in the impulse mode, and
connecting, by the switching means (SW) of the display device (1), a corresponding one of the data signal lines with the second current source (I2) for the pixel displaying an image in the hold mode, wherein the first and second current sources output currents in opposite directions.

11. The method as set forth in claim 10, wherein the lower-side gray scales are ranged from a lowest gray scale of the whole gray scales of the light emitting signal to a gray scale smaller than a 1/2 gray scale which is a center gray scale at the middle of the whole gray scales of the light emitting signal, and the higher-gray scales are ranged from the gray scale smaller than the 1/2 gray scale, to a highest gray scale of the whole gray scales of the light emitting signal.

12. The method as set forth in claim 10 or 11, wherein the element is an organic electroluminescence diode.

Patentansprüche

1. Anzeigevorrichtung (1), umfassend:

mehrere Scan-Leitungen (G1, G2, ...; R1, R2, ...), die sich in einer Richtung erstrecken, wobei die mehreren Scan-Leitungen (G1, G2, ...; R1, R2, ...) mehrere erste Scan-Leitungen (G1, G2, ...) und mehrere zweite Scan-Leitungen (R1, R2, ...) umfassen;
mehrere Datensignalleitungen (S1, S2, ...), die sich in einer anderen Richtung erstrecken;
eine Source-Treiberschaltung (2) zum Treiben der mehreren Datensignalleitungen;
eine Gate-Treiberschaltung (3) zum Steuern der mehreren Scan-Leitungen; und
mehrere Pixel, wobei jedes Pixel entsprechend jedem Schnittpunkt zwischen den mehreren Scan-Leitungen und den mehreren Datensignalleitungen bereitgestellt ist, wobei jedes Pixel mit einem Element (7) zum Emittieren von Licht mit einer Leuchtdichte versehen ist, die von einem elektrischen Strom abhängig ist, der dem Element (7) zugeführt wird, wobei eine Auswahlperiode eines Paars der ersten und der zweiten Scan-Leitungen eine Periode ist, in der beide Scan-Leitungen des Paars gleichzeitig von der Gate-Treiberschaltung (3) ausgewählt werden; und
eine Pixelschaltung (6, 8, 9) pro Pixel, wobei die Pixelschaltung (6, 8, 9) eingerichtet ist, das Element (7) in einem Impulsmodus zu treiben, in dem das Element (7) das Licht nur während der Auswahlperiode des Paars der ersten und der zweiten Scan-Leitungen emittiert, mit denen die Pixelschaltung verbunden ist, oder in einem Haltemodus, in dem das Element (7) das Licht nicht während der Auswahlperiode, sondern nach der Auswahlperiode emittiert,
wobei die Pixelschaltung (6, 8, 9) einen ersten Dünnfilmtransistor (T1), einen zweiten Dünnfilmtransistor (T2), einen dritten Dünnfilmtransistor (T3) und einen Kondensator (C) umfasst;
wobei der erste Dünnfilmtransistor (T1) ein Gate, das mit einer entsprechenden einen der ersten Scan-Leitungen (G1, G2, ...) verbunden ist, und eine Source, die mit einer entsprechenden einen der Datensignalleitungen (S1, S2, ...) verbunden ist, aufweist;
wobei der zweite Dünnfilmtransistor (T2) ein Gate, das mit einer entsprechenden einen der zweiten Scan-Leitungen (R1, R2, ...) verbunden ist, einen Drain, der elektrisch geerdet ist, und eine Source, die mit einem Gate des dritten Dünnfilmtransistors (T3) und mit einem Ende des Kondensators (C) verbunden ist, aufweist;
wobei der dritte Dünnfilmtransistor (T3) einen Drain, der mit einer Energiequellenleitung (Vp) verbunden ist, und eine Source, die mit einem Drain des ersten Dünnfilmtransistors (T1), mit einem anderen Ende des Kondensators (C) und mit einer Anode des Elements (7) verbunden ist, aufweist;
wobei das Element (7) eine Kathode aufweist, die elektrisch geerdet ist;
wobei die Source-Treiberschaltung (2) mit einem Schaltmittel (SW), einer ersten Signalquelle (I1) zum Zuführen eines lichtemittierenden Signals, wenn die Pixelschaltung (6, 8, 9) in dem Impulsmodus getrieben wird, und einer zweiten Signalquelle (12) zum Zuführen des lichtemittierenden Signals, wenn die Pixelschaltung (6, 8, 9) in dem Haltemodus getrieben wird, versehen ist; und
wobei die Anzeigevorrichtung (1) eingerichtet ist, das Treiben in dem Impulsmodus für tieferseitige Graustufen durchzuführen, und das Treiben in dem Haltemodus für höherseitige Graustufen durchzuführen, wobei die gesamten Graustufen des lichtemittierenden Signals in die tieferseitigen Graustufen und die höherseitigen Graustufen klassifiziert werden;
wobei die erste Signalquelle (I1) und die zweite Signalquelle (12) jeweils eine erste Stromquelle und zweite Stromquelle sind, und die erste und zweite Stromquelle ausgelegt sind, Ströme in entgegengesetzte Richtungen auszugeben; und

wobei das Schaltmittel (SW) eingerichtet ist, eine entsprechende eine der Datensignalleitungen mit der ersten Stromquelle (I1) für das Pixel zu verbinden, das ein Bild in dem Impulsmodus anzeigt, und eine entsprechende eine der Datensignalleitungen mit der zweiten Stromquelle (12) für das Pixel zu verbinden, das ein Bild in dem Haltemodus anzeigt.

2. Anzeigevorrichtung nach Anspruch 1, wobei der Drain des zweiten Dünnfilmtransistors (T2) mit der Energiequellenleitung verbunden ist, ein Potential von welcher während der Auswahlperiode ein Erdpotential ist und während der Nicht-Auswahlperiode ein Potential (Up'), das größer als das Erdpotential ist.

3. Anzeigevorrichtung nach Anspruch 1 oder 2, wobei der erste Dünnfilmtransistor (T1), der zweite Dünnfilmtransistor (T2) und der dritte Dünnfilmtransistor (T3) N-Kanal-Dünnfilmtransistoren sind.

4. Anzeigevorrichtung nach einem der Ansprüche 1 bis 3, wobei die tieferseitigen Graustufen von einer tiefsten Graustufe der gesamten Graustufen des lichtemittierenden Signals bis zu einer Graustufe reichen, welche kleiner ist als eine 1/2 Graustufe, die eine zentrale Graustufe in der Mitte der gesamten Graustufen des lichtemittierenden Signals ist, und die höherseitigen Graustufen von der Graustufe, welche kleiner ist als die 1/2 Graustufe, bis zu einer höchsten Graustufe der gesamten Graustufen des lichtemittierenden Signals reichen.

5. Anzeigevorrichtung nach Anspruch 1, wobei die Source-Treiberschaltung (2) ausgelegt ist, die Pixelschaltungen (6, 8, 9) sowohl in dem Impulsmodus als auch dem Haltmodus zu treiben, oder die Pixelschaltungen (6, 8, 9) nur in dem Haltemodus zu treiben, auf der Basis einer Verteilung von Graustufenwerten, die das Bild darstellen.

6. Anzeigevorrichtung nach einem der Ansprüche 1 bis 5, wobei das Element (7) eine organische Elektrolumineszenzdiode ist.

7. Anzeigevorrichtung nach einem der Ansprüche 1 bis 6, wobei die Gate-Treiberschaltung (3) eingerichtet ist, wenn das Treiben in dem Haltemodus für höherseitige Graustufen durchgeführt wird, eine schwarze Einfügeperiode bereitzustellen, in der die Gate-Treiberschaltung (3) den Signalpegel der ersten Scan-Leitungen (G1, G2, ...) auf einen tiefen Signalpegel setzt und den Signalpegel der zweiten Scan-Leitungen (R1, R2, ...) auf einen hohen Signalpegel setzt.

8. Anzeigevorrichtung nach einem der Ansprüche 1 bis 7, wobei ein Strom dem Element über den ersten Dünnfilmtransistor (T1) zugeführt wird, der eingerichtet ist, in einem linearen Gebiet in dem Impulsmodus zu arbeiten.

9. Anzeigevorrichtung nach einem der Ansprüche 1 bis 8, wobei die Anzeigevorrichtung eingerichtet ist, Licht in dem Impulsmodus in einem Zustand zu emittieren, wo der dritte Dünnfilmtransistor (T3) ausgeschaltet ist.

10. Verfahren zum Treiben der Anzeigevorrichtung (1) nach einem der Ansprüche 1 bis 9, wobei das Treibverfahren umfasst:

Treiben einer Pixelschaltung (6, 8, 9) der Pixel in dem Impulsmodus für die tieferseitigen Graustufen oder in dem Haltemodus für die höherseitigen Graustufen;
Verbinden, durch das Schaltmittel (SW) der Anzeigevorrichtung (1), einer entsprechenden einen der Datensignalleitungen mit der ersten Stromquelle (I1) für das Pixel, das ein Bild in dem Impulsmodus anzeigt; und Verbinden, durch das Schaltmittel (SW) der Anzeigevorrichtung (1), einer entsprechenden einen der Datensignalleitungen mit der zweiten Stromquelle (12) für das Pixel, das ein Bild in dem Haltemodus anzeigt,
wobei die erste und zweite Stromquelle Ströme in entgegengesetzte Richtungen ausgeben.

11. Verfahren nach Anspruch 10, wobei die tieferseitigen Graustufen von einer tiefsten Graustufe der gesamten Graustufen des lichtemittierenden Signals bis zu einer Graustufe reichen, welche kleiner ist als eine 1/2 Graustufe, die eine zentrale Graustufe in der Mitte der gesamten Graustufen des lichtemittierenden Signals ist, und die höherseitigen Graustufen von der Graustufe, welche kleiner ist als die 1/2 Graustufe, bis zu einer höchsten Graustufe der gesamten Graustufen des lichtemittierenden Signals reichen.

12. Anzeigevorrichtung nach Anspruch 10 oder 11, wobei das Element eine organische Elektrolumineszenzdiode ist.

Revendications

1. Dispositif d'affichage (1) incluant :

une pluralité de lignes de balayage (G1, G2, ... ; R1, R2, ...) étendue dans une direction, dans lequel la pluralité de lignes de balayage (G1, G2, ... ; R1, R2, ...) englobe une pluralité de premières lignes de balayage (G1, G2, ...) et une pluralité de secondes lignes de balayage (R1,

R2, ...) ;
une pluralité de lignes de signal de données (S1, S2, ...) étendue dans une autre direction ;
un circuit de commande de source (2) destiné à commander la pluralité de lignes de signal de données ;
un circuit de commande de grille (3) destiné à commander la pluralité de lignes de balayage ; et
une pluralité de pixels, chaque pixel étant fourni en correspondance avec chaque intersection entre la pluralité de lignes de balayage et la pluralité de lignes de signal de données, chaque pixel étant pourvu d'un élément (7) destiné à émettre de la lumière présentant une luminance qui est en fonction d'un courant électrique fourni à l'élément (7), où une période de sélection d'une paire des premières et secondes lignes de balayage correspond à une période dans laquelle les lignes de balayage de la paire sont simultanément sélectionnées par le circuit de commande de grille (3) ; et
un circuit de pixel (6, 8, 9) pour chaque pixel, dans lequel le circuit de pixel (6, 8, 9) est apte à commander l'élément (7) dans un mode d'impulsion dans lequel l'élément (7) émet de la lumière uniquement au cours de la période de sélection de la paire des premières et secondes lignes de balayage auxquelles est connecté le circuit de pixel, ou dans un mode de maintien dans lequel l'élément (7) émet de la lumière non pas au cours de la période de sélection, mais après la période de sélection ;
dans lequel le circuit de pixel (6, 8, 9) inclut un premier transistor à couches minces (T1), un deuxième transistor à couches minces (T2), un troisième transistor à couches minces (T3) et un condensateur (C) ;
dans lequel le premier transistor à couches minces (T1) présente une grille connectée à une ligne correspondante des premières lignes de balayage (G1, G2, ...), et une source connectée à une ligne correspondante des lignes de signal de données (SI, S2, ...) ;
dans lequel le deuxième transistor à couches minces (T2) présente une grille connectée à une ligne correspondante des secondes lignes de balayage (R1, R2, ...), un drain qui est électriquement mis à la terre, et
une source connectée à une grille du troisième transistor à couches minces (T3) et à une extrémité du condensateur (C) ;
dans lequel le troisième transistor à couches minces (T3) présente un drain connecté à une ligne de source d'alimentation (Vp), une source connectée à un drain du premier transistor à couches minces (T1), à une autre extrémité du condensateur (C) et à une anode de l'élément (7) ;
dans lequel l'élément (7) présente une cathode qui est électriquement mise à la terre ;
dans lequel le circuit de commande de source (2) est doté d'un moyen de commutation (SW), d'une première source de signal (I1) destinée à fournir un signal électroluminescent lorsque le circuit de pixel (6, 8, 9) est commandé dans le mode d'impulsion, et d'une seconde source de signal (I2) destinée à fournir le signal électroluminescent lorsque le circuit de pixel (6, 8, 9) est commandé dans le mode de maintien ; et
dans lequel le dispositif d'affichage (1) est apte à mettre en oeuvre la commande dans le mode d'impulsion pour des échelles de gris de côté inférieur et à mettre en oeuvre la commande dans le mode de maintien pour des échelles de gris de côté supérieur, où des échelles de gris entières du signal électroluminescent sont classées dans les échelles de gris de côté inférieur et les échelles de gris de côté supérieur ;
dans lequel :

la première source de signal (I1) et la seconde source de signal (I2) correspondent à une première source de courant et à une seconde source de courant, respectivement, et les première et seconde sources de courant sont configurées de manière à générer en sortie des courants dans des directions opposées ; et
dans lequel le moyen de commutation (SW) est apte à connecter une ligne correspondante des lignes de signal de données à la première source de courant (I1) pour le pixel affichant une image dans le mode d'impulsion, et à connecter une ligne correspondante des lignes de signal de données à la seconde source de courant (I2) pour le pixel affichant une image dans le mode de maintien.

2. Dispositif d'affichage selon la revendication 1, dans lequel le drain du deuxième transistor à couches minces (T2) est connecté à la ligne de source d'alimentation, dont un potentiel correspond à un potentiel de masse au cours de la période de sélection et correspond à un potentiel (Up') supérieur au potentiel de masse au cours de la période de non-sélection.

3. Dispositif d'affichage selon la revendication 1 ou 2, dans lequel le premier transistor à couches minces (T1), le deuxième transistor à couches minces (T2), et le troisième transistor à couches minces (T3) correspondent à des transistors à couches minces à canal N.

4. Dispositif d'affichage selon l'une quelconque des revendications 1 à 3, dans lequel les échelles de gris de côté inférieur varient d'une échelle de gris la plus faible des échelles de gris entières du signal électroluminescent à une échelle de gris inférieure à 1/2 échelle de gris qui correspond à une échelle de gris centrale au milieu des échelles de gris entières du signal électroluminescent, et dans lequel les échelles de gris plus élevées varient de l'échelle de gris inférieure à 1/2 échelle de gris à une échelle de gris la plus élevée des échelles de gris entières du signal électroluminescent.

5. Dispositif d'affichage selon la revendication 1, dans lequel le circuit de commande de source (2) est configuré de manière à commander les circuits de pixel (6, 8, 9) à la fois dans le mode d'impulsion et dans le mode de maintien, ou à commander les circuits de pixel (6, 8, 9) uniquement dans le mode de maintien, sur la base d'une répartition de valeurs d'échelles de gris constituant l'image.

6. Dispositif d'affichage selon l'une quelconque des revendications 1 à 5, dans lequel l'élément (7) est une diode électroluminescente organique.

7. Dispositif d'affichage selon l'une quelconque des revendications 1 à 6, dans lequel le circuit de commande de grille (3) est apte à fournir, lors de la mise en oeuvre de la commande dans le mode de maintien pour des échelles de gris de côté supérieur, une période d'insertion de noir, dans laquelle le circuit de commande de grille (3) définit le niveau de signal des premières lignes de balayage (G1, G2, ...) sur un niveau de signal faible, et définit le niveau de signal des secondes lignes de balayage (R1, R2, ...) sur un niveau de signal élevé.

8. Dispositif d'affichage selon l'une quelconque des revendications 1 à 7, dans lequel un courant est fourni à l'élément par l'intermédiaire du premier transistor à couches minces (T1) lequel est apte à opérer au sein d'une zone linéaire dans le mode d'impulsion.

9. Dispositif d'affichage selon l'une quelconque des revendications 1 à 8, dans lequel le dispositif d'affichage est apte à émettre de la lumière dans le mode d'impulsion, dans un état où le troisième transistor à couches minces (T3) est hors tension.

10. Procédé de commande du dispositif d'affichage (1) selon l'une quelconque des revendications 1 à 9, le procédé de commande comprenant les étapes ci-dessous consistant à :

commander un circuit de pixel (6, 8, 9) des pixels dans le mode d'impulsion pour les échelles de gris de côté inférieur, ou dans le mode de maintien pour les échelles de gris de côté supérieur ;
connecter, par le biais du moyen de commutation (SW) du dispositif d'affichage (1), une ligne correspondante des lignes de signal de données à la première source de courant (I1) pour le pixel affichant une image dans le mode d'impulsion ; et
connecter, par le biais du moyen de commutation (SW) du dispositif d'affichage (1), une ligne correspondante des lignes de signal de données à la seconde source de courant (I2) pour le pixel affichant une image dans le mode de maintien, dans lequel les première et seconde sources de courant génèrent en sortie des courants dans des directions opposées.

11. Procédé selon la revendication 10, dans lequel les échelles de gris de côté inférieur varient d'une échelle de gris la plus faible des échelles de gris entières du signal électroluminescent à une échelle de gris inférieure à 1/2 échelle de gris qui correspond à une échelle de gris centrale au milieu des échelles de gris entières du signal électroluminescent, et dans lequel les échelles de gris plus élevées varient de l'échelle de gris inférieure à 1/2 échelle de gris à une échelle de gris la plus élevée des échelles de gris entières du signal électroluminescent.

12. Procédé selon la revendication 10 ou 11, dans lequel l'élément est une diode électroluminescente organique.

FIG. 1

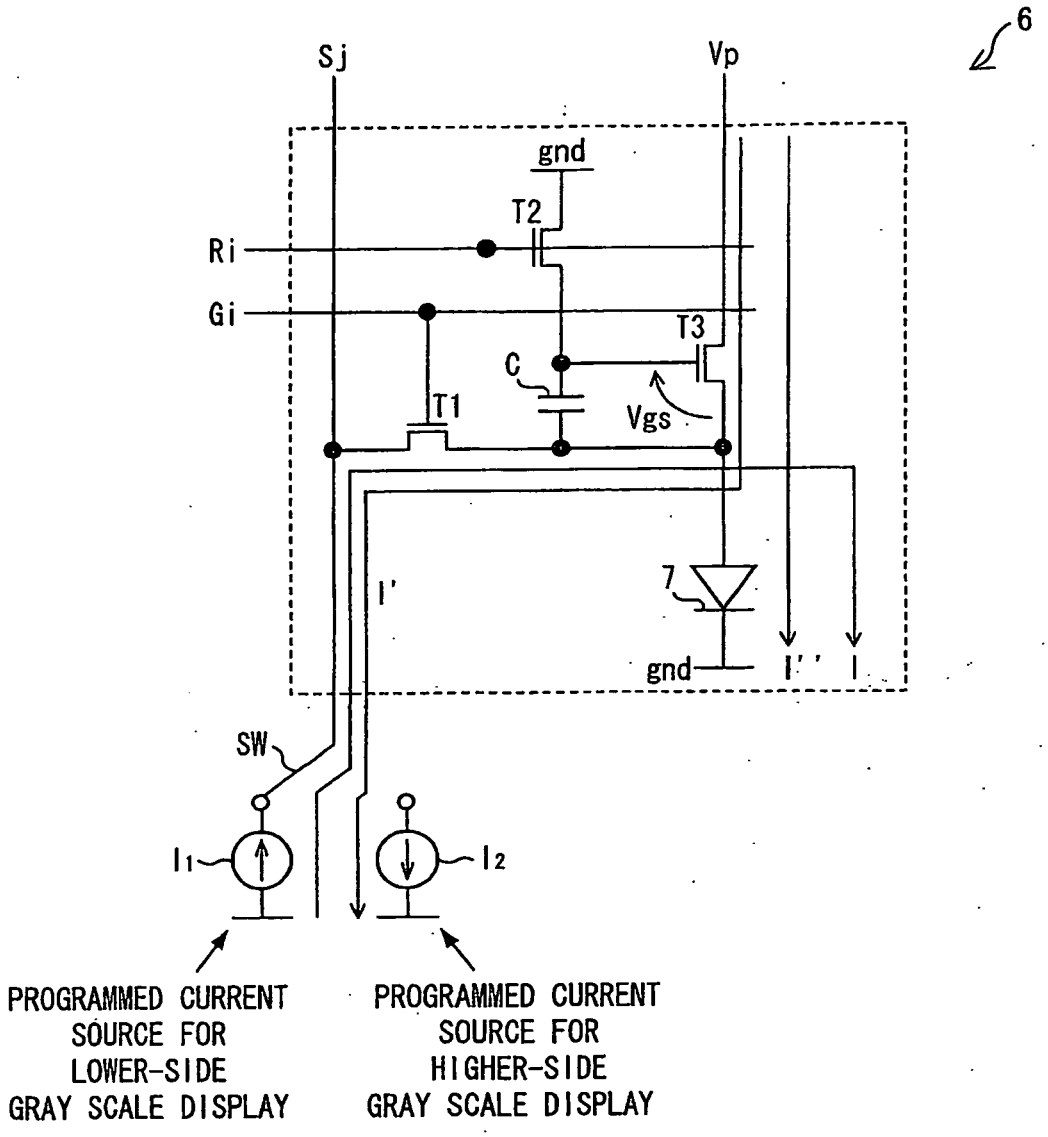

6
Sj
Vp
gnd
T2
Ri
Gi
T3
C
T1
Vgs
7
I'
gnd
I''
I
SW
I1
I2
PROGRAMMED CURRENT SOURCE FOR LOWER-SIDE GRAY SCALE DISPLAY
PROGRAMMED CURRENT SOURCE FOR HIGHER-SIDE GRAY SCALE DISPLAY

FIG. 2

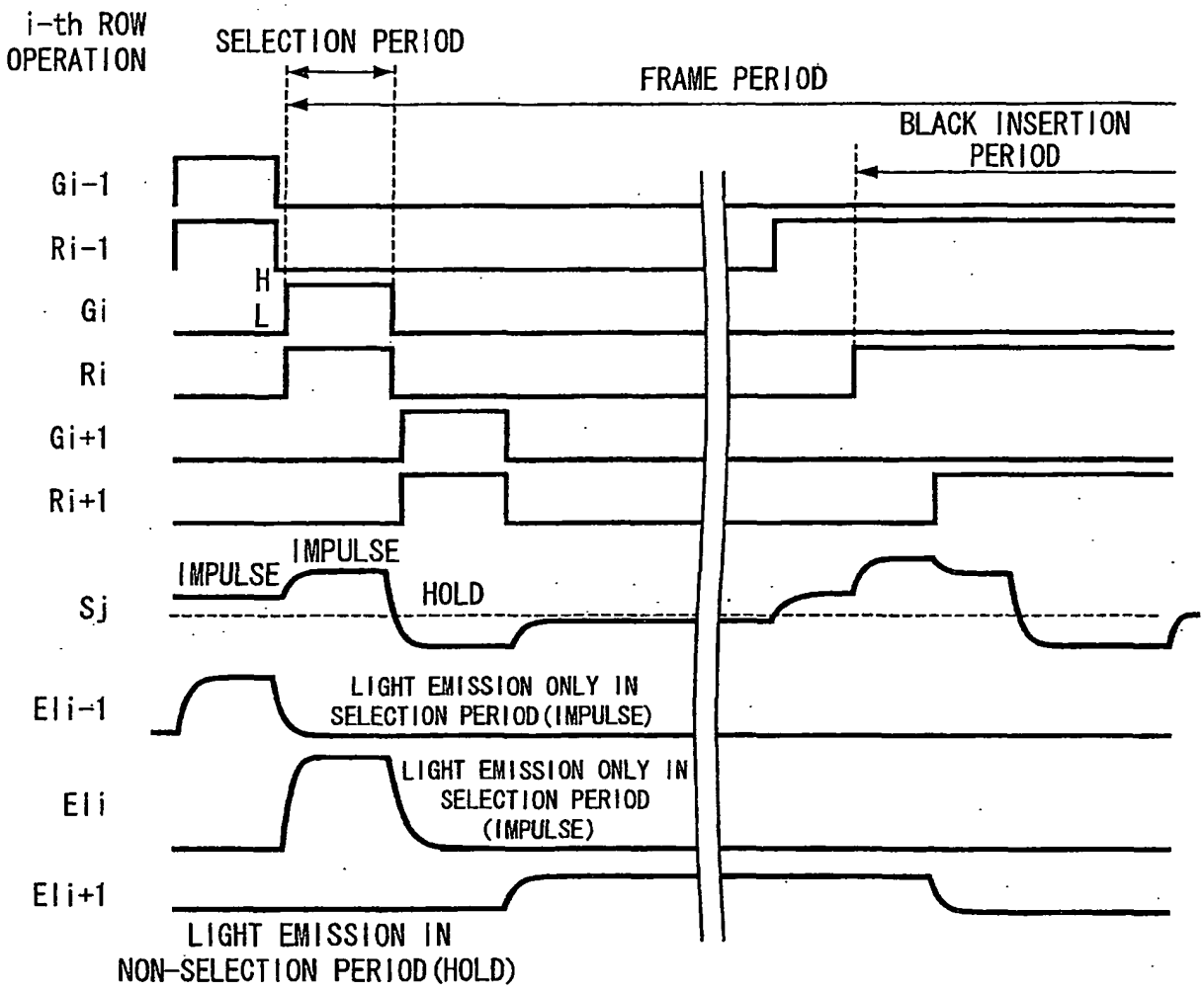

i-th ROW OPERATION
SELECTION PERIOD
FRAME PERIOD
BLACK INSERTION PERIOD
Gi-1
Ri-1
H
L
Gi
Ri
Gi+1
Ri+1
IMPULSE
IMPULSE
HOLD
Sj
LIGHT EMISSION ONLY IN SELECTION PERIOD(IMPULSE)
Eli-1
LIGHT EMISSION ONLY IN SELECTION PERIOD (IMPULSE)
Eli
Eli+1
LIGHT EMISSION IN NON-SELECTION PERIOD(HOLD)

FIG. 3

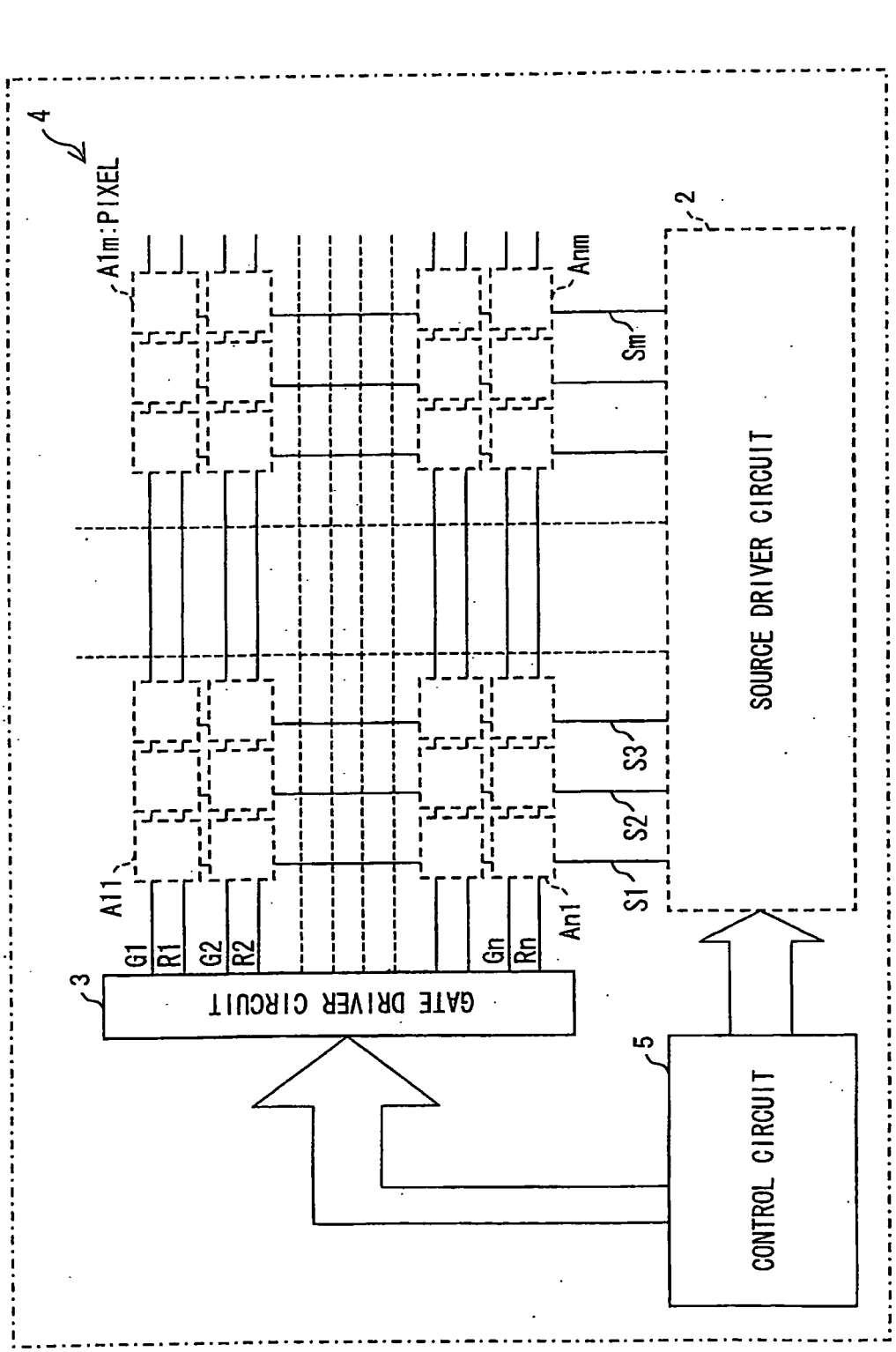

1
4
A1m:PIXEL
Anm
2
Sm
SOURCE DRIVER CIRCUIT
S3
S2
S1
A11
An1
G1
R1
G2
R2
Gn
Rn
3
GATE DRIVER CIRCUIT
5
CONTROL CIRCUIT

FIG. 4

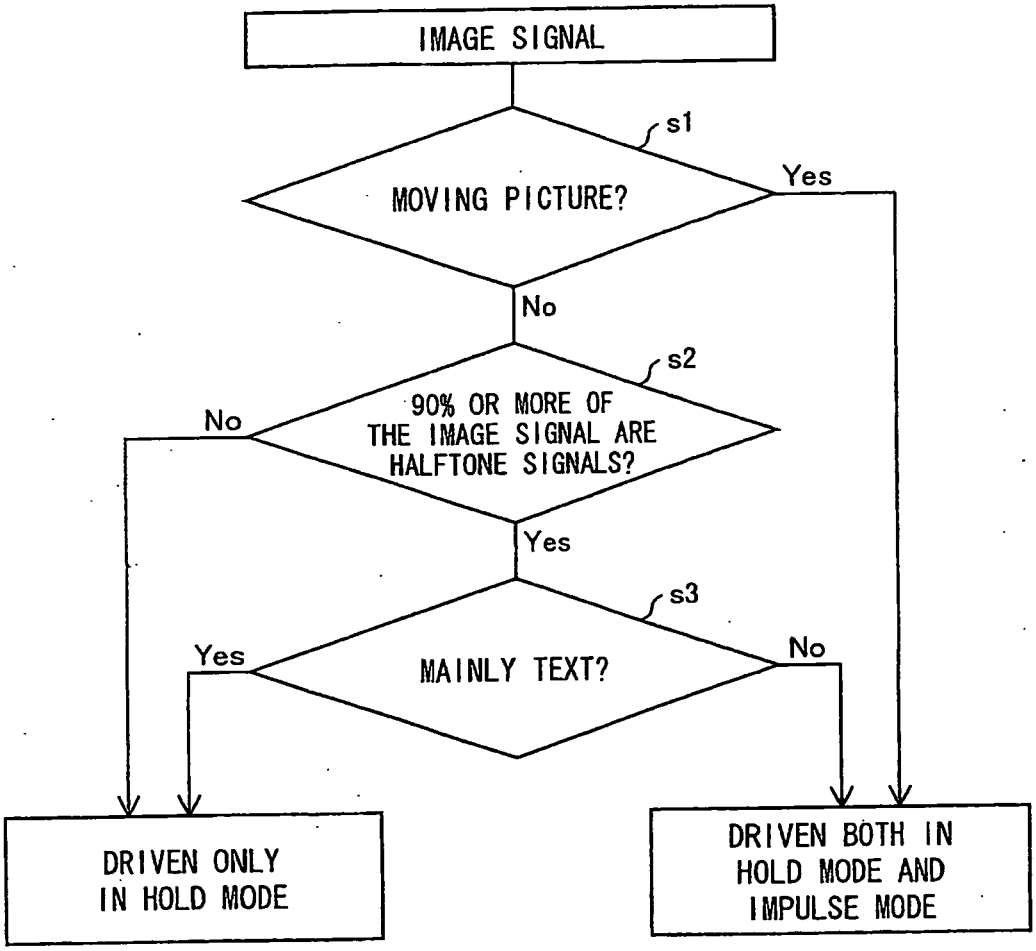


IMAGE SIGNAL
s1
MOVING PICTURE?
Yes
No
s2
90% OR MORE OF THE IMAGE SIGNAL ARE HALFTONE SIGNALS?
No
Yes
s3
MAINLY TEXT?
Yes
No
DRIVEN ONLY IN HOLD MODE
DRIVEN BOTH IN HOLD MODE AND IMPULSE MODE

FIG. 5

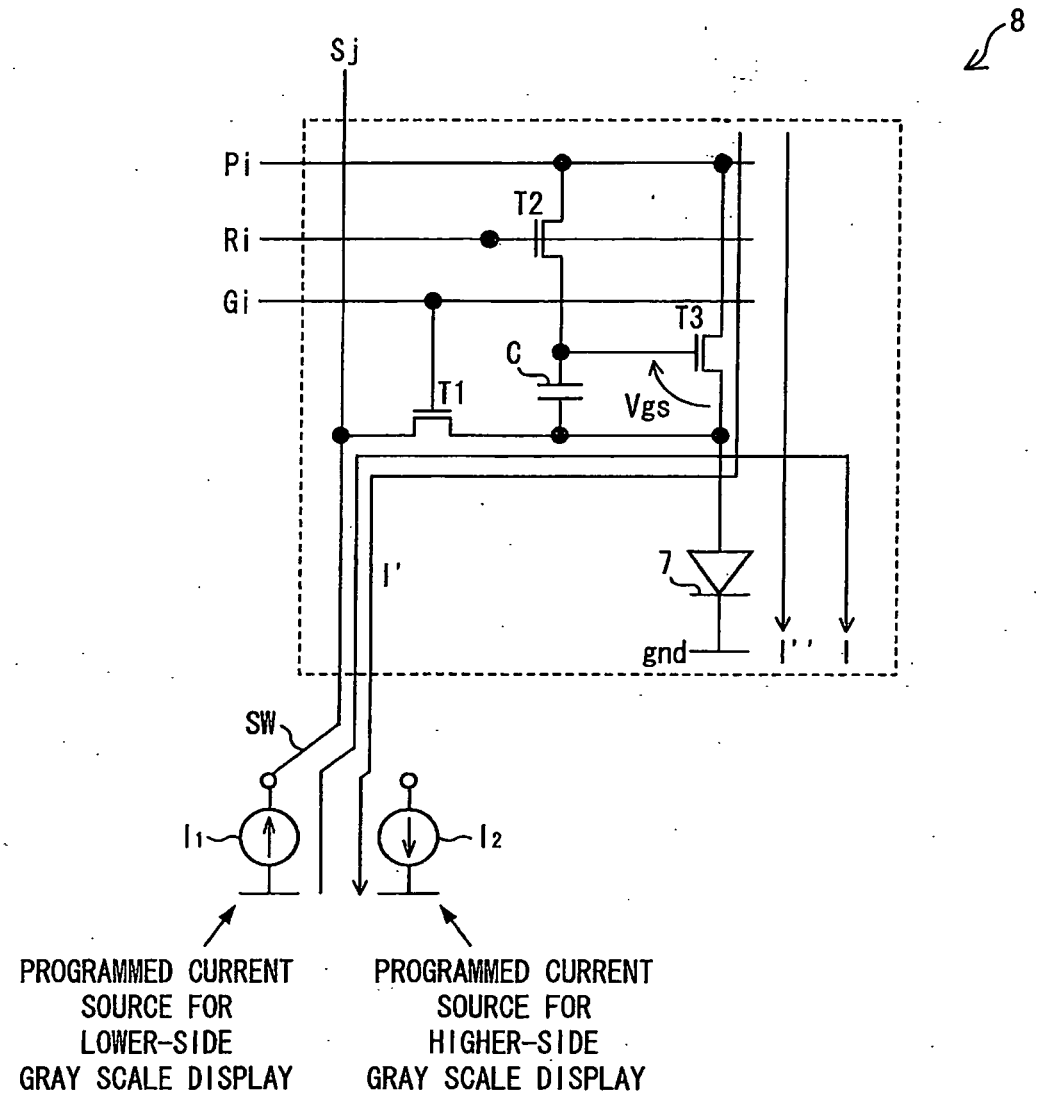

8
Sj
Pi
Ri
Gi
T2
T3
C
T1
Vgs
I'
7
gnd
I''
I
SW
I1
I2
PROGRAMMED CURRENT SOURCE FOR LOWER-SIDE GRAY SCALE DISPLAY
PROGRAMMED CURRENT SOURCE FOR HIGHER-SIDE GRAY SCALE DISPLAY

FIG. 6

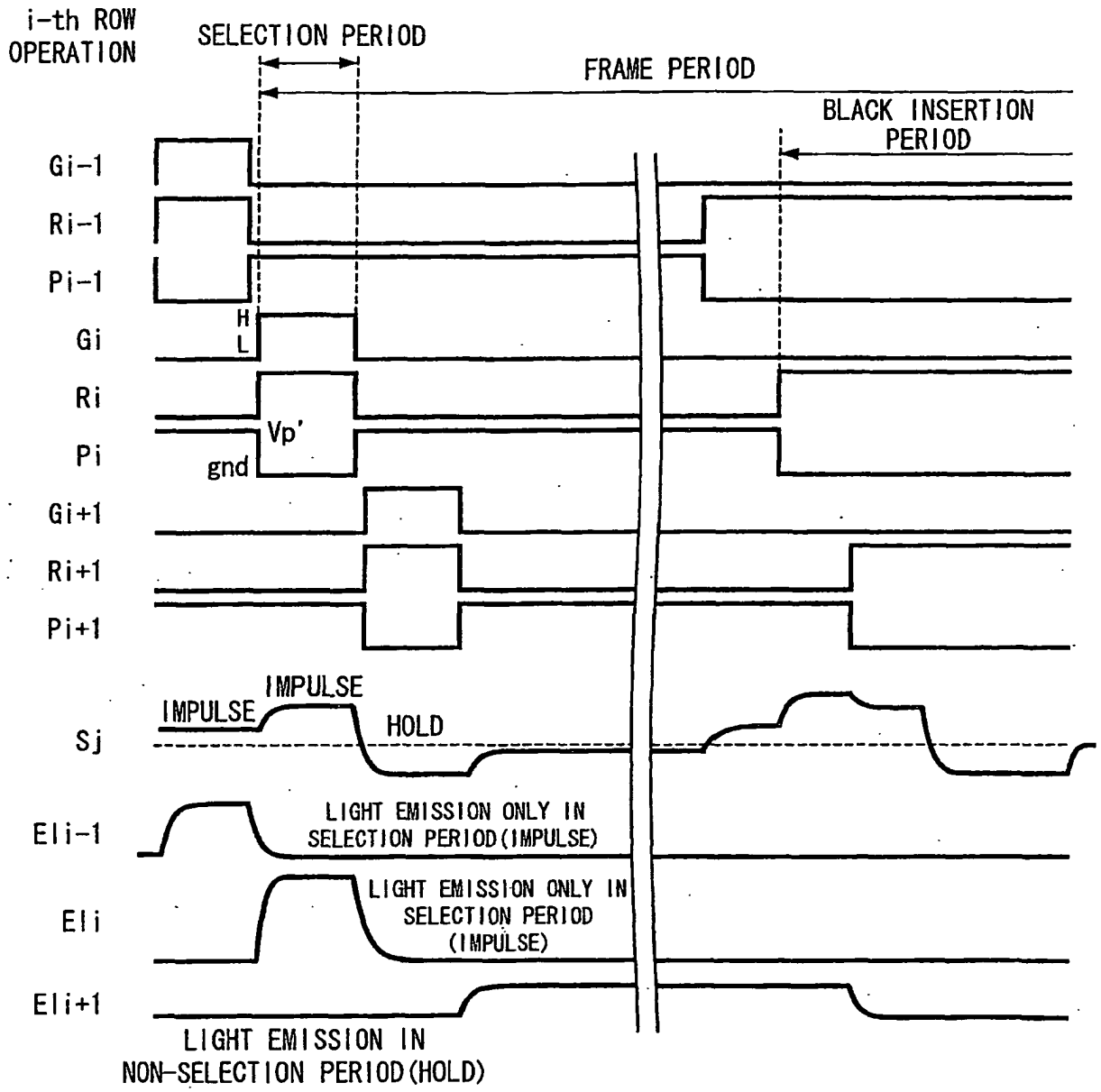

i-th ROW OPERATION
SELECTION PERIOD
FRAME PERIOD
BLACK INSERTION PERIOD
Gi-1
Ri-1
Pi-1
Gi
H
L
Ri
Vp'
Pi
gnd
Gi+1
Ri+1
Pi+1
IMPULSE
IMPULSE
HOLD
Sj
Eli-1
LIGHT EMISSION ONLY IN SELECTION PERIOD(IMPULSE)
Eli
LIGHT EMISSION ONLY IN SELECTION PERIOD (IMPULSE)
Eli+1
LIGHT EMISSION IN NON-SELECTION PERIOD(HOLD)

FIG. 7

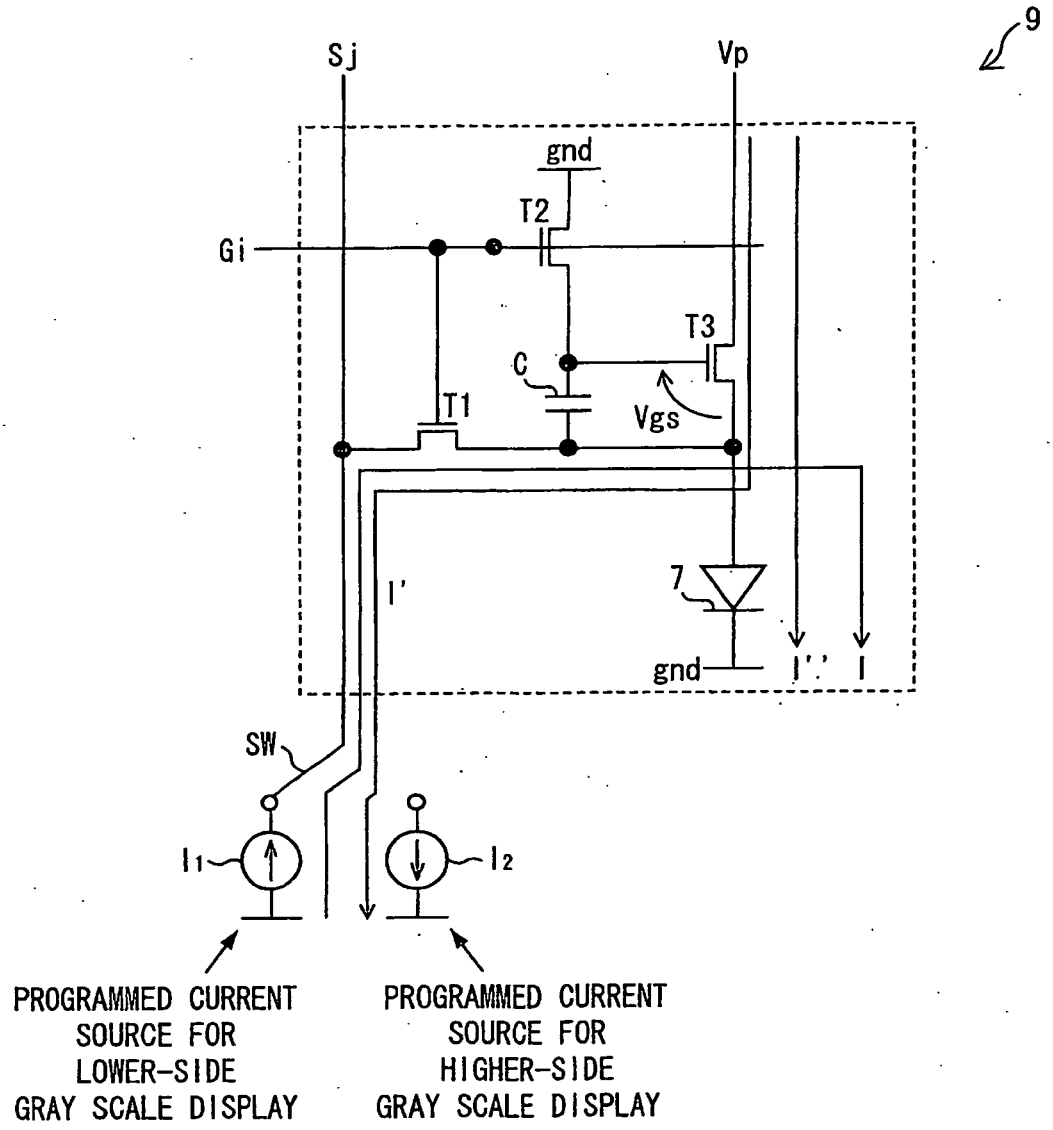

9
Sj
Vp
gnd
T2
Gi
T3
C
T1
Vgs
I'
7
gnd
I''
I
SW
I1
I2
PROGRAMMED CURRENT SOURCE FOR LOWER-SIDE GRAY SCALE DISPLAY
PROGRAMMED CURRENT SOURCE FOR HIGHER-SIDE GRAY SCALE DISPLAY

FIG. 8

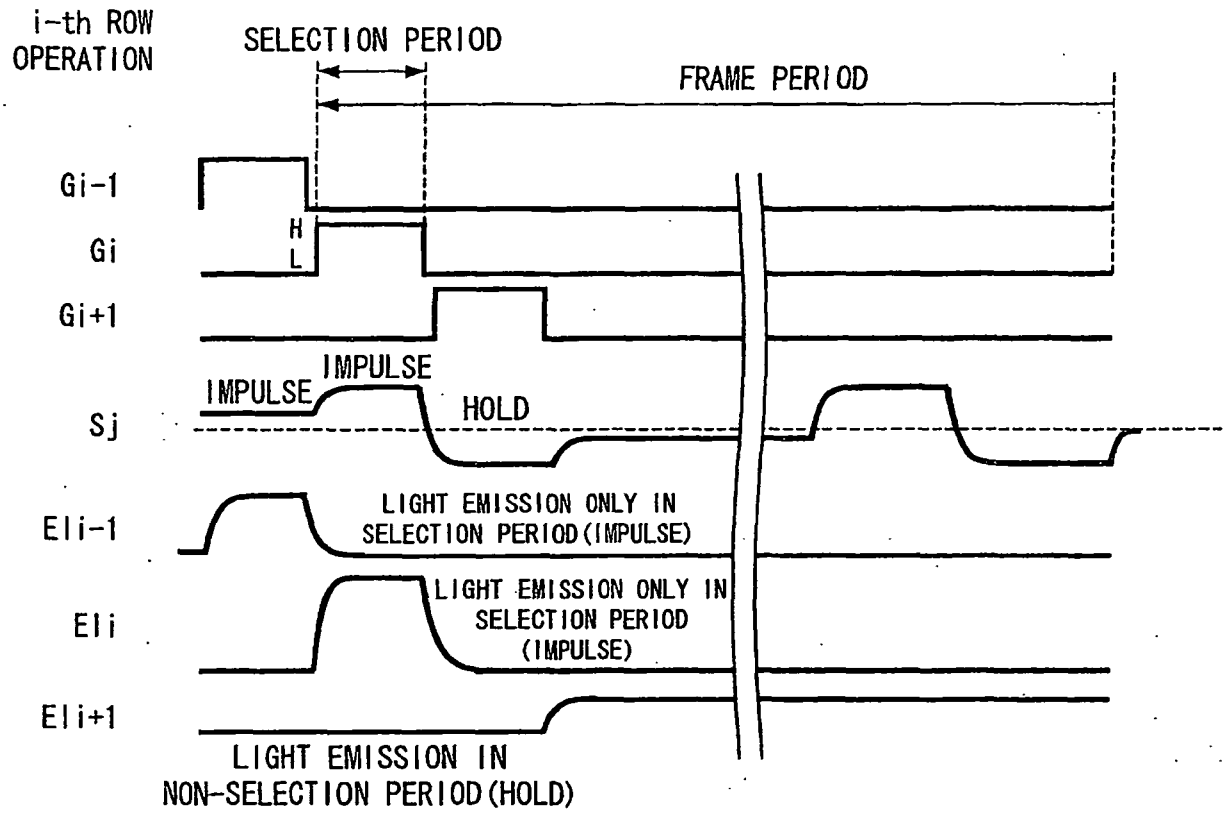
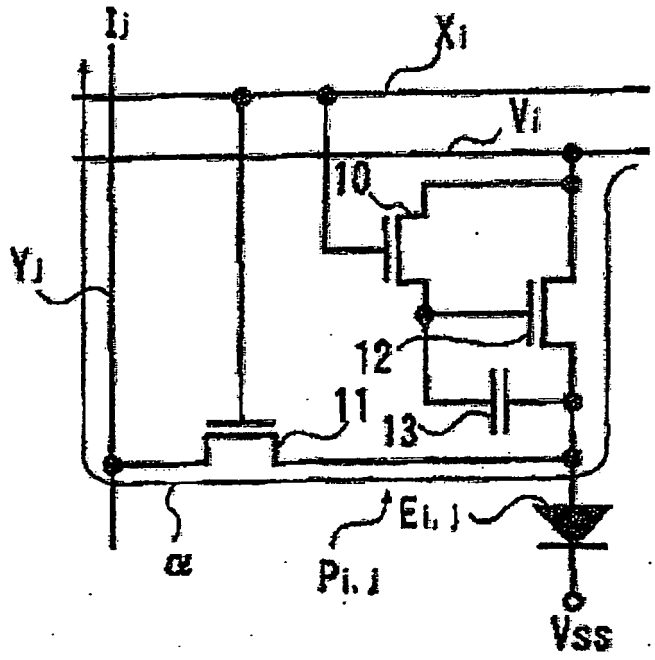

i-th ROW OPERATION
SELECTION PERIOD
FRAME PERIOD
Gi-1
Gi
H
L
Gi+1
IMPULSE
IMPULSE
HOLD
Sj
LIGHT EMISSION ONLY IN SELECTION PERIOD (IMPULSE)
Eli-1
LIGHT EMISSION ONLY IN SELECTION PERIOD (IMPULSE)
Eli
Eli+1
LIGHT EMISSION IN NON-SELECTION PERIOD (HOLD)

FIG. 9



REFERENCES CITED IN THE DESCRIPTION

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- EP 1424680 A2 **[0012]**

专利名称(译)	显示装置和显示装置的驱动方法		
公开(公告)号	EP2439724B1	公开(公告)日	2016-07-13
申请号	EP2010783073	申请日	2010-03-04
[标]申请(专利权)人(译)	夏普株式会社		
申请(专利权)人(译)	夏普株式会社		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	KISHI NORITAKA		
发明人	KISHI, NORITAKA		
IPC分类号	G09G3/32 G09G3/20		
CPC分类号	G09G3/3225 G09G3/2077 G09G3/3283 G09G2300/0842 G09G2320/0261 G09G2330/021		
优先权	2009135286 2009-06-04 JP		
其他公开文献	EP2439724A1 EP2439724A4		
外部链接	Espacenet		

摘要(译)

像素电路（6）以脉冲模式驱动，其中有机EL二极管（7）仅在选择周期期间发光，或者在保持模式下驱动，其中有机EL二极管（7）在选择期间不发光期间但在选择期后。此外，像素电路（6）具有用于下侧灰度级显示的编程电流源（I1）和用于高侧灰度级显示的编程电流源（I2），该像素电路（6）被提供有当在脉冲模式下驱动像素电路（6）时，来自编程电流源（I1）的编程电流（I），以及当像素电路（6）中来自编程电流源（I2）的编程电流（I'）在保持模式下被驱动。

FIG. 1