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(54) **Data driving integrated circuit (IC), light emitting display using the IC, and method of driving the light emitting display**

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(56) References cited:
EP-A1- 1 225 557
US-A1- 2003 011 314
US-A1- 2003 063 081
US-A1- 2004 100 430

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Description

CLAIM OF PRIORITY

[0001] This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. § 119 from an application for DATA INTEGRATED CIRCUIT AND DRIVING METHOD OF LIGHT EMITTING DISPLAY USING THE SAME earlier filed in the Korean Intellectual Property Office on the 24th of December 2004 and there duly assigned Serial No. 10-2004-0112530.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates to a data driving Integrated Circuit (IC), a light emitting display using the IC, and a method of driving the light emitting display, and more particularly, to a data driving IC to display an image with a desired brightness, a light emitting display using the IC, and a method of driving the light emitting display.

2. Related Art

[0003] Various flat panel displays have recently been developed as alternatives to a relatively heavy and bulky cathode ray tube (CRT) display. The flat panel display includes a liquid crystal display (LCD), a field emission display (FED), a plasma display panel (PDP), a light emitting display (OLED), etc.

[0004] Among the flat panel displays, the light emitting display can emit light for itself by electron-hole recombination. Such a light emitting display has advantages in that response time is relatively fast and power consumption is relatively low. Generally, the light emitting display employs a transistor provided in each pixel for supplying current corresponding to a data signal to a light emitting device, thereby allowing the light emitting device to emit light.

[0005] A light emitting display includes: a pixel portion having a plurality of pixels formed in a region defined by the intersections of scan lines and data lines; a scan driver to drive the scan lines; a data driver to drive the data lines; and a timing controller to control the scan driver and the data driver.

[0006] The timing controller generates a Data Control Signal (DCS) and a Scan Control Signal (SCS) corresponding to an external synchronization signal. The DCS and the SCS are supplied from the timing controller to the data driver and the scan driver, respectively. Furthermore, the timing controller supplies external data to the data driver.

[0007] The scan driver receives the scan control signal SCS from the timing controller. The scan driver generates scan signals on the basis of the scan control signal SCS and supplies the scan signals to the scan lines.

[0008] The data driver receives the DCS from the timing controller. The data driver generates data signals on the basis of the DCS and supplies the data signals to the data lines while synchronizing with the scan signals.

[0009] The display portion receives a first voltage ELVDD and a second voltage ELVSS from an external power source, and supplies them to the respective pixels. When the first voltage ELVDD and the second voltage ELVSS are supplied to the pixels, each pixel controls a current corresponding to the data signal to flow from a first voltage ELVDD to a second voltage ELVSS via the light emitting device, thereby emitting light corresponding to the data signal.

For example, US open-laid patent application 2003/011314 A1 discloses a display apparatus comprising a signal controller connected to data lines and feedback lines and adapted to measure a pixel current flowing in each pixel and to adjust the data accordingly. Furthermore, US open-laid patent application 2003/063081 A1 concerns a display apparatus comprising a light emitting device and a driving device for controlling a driving current flowing through the light emitting device for each pixel of the display apparatus.

[0010] That is, in such a light emitting display, each pixel emits light with predetermined brightness corresponding to the data signal, but cannot emit light with desired brightness because transistors provided in the respective pixels are different in threshold voltage from each other. Furthermore, in such a light emitting display, there is no method of measuring and controlling a real current flowing in each pixel in correspondence with the data signal.

European patent application 1 225 557 A1 discloses a method of driving a light emitting display comprising the steps of generating a gradation voltage, supplying the gradation voltage to a pixel, measuring a pixel current flowing in the pixel, comparing the measured current value with a target current value and adjusting a bit value of the data on the basis of the comparison.

SUMMARY OF THE INVENTION

[0011] Accordingly, it is an aspect of the present invention to provide a data driving integrated circuit according to claim 1 to display an image with desired brightness, a light emitting display using the data driving integrated circuit, and a method of driving the light emitting display. The invention is set forth in claims 1 and 8.

[0012] The foregoing and/or other aspects of the present invention can be achieved by providing a data driving integrated circuit, comprising: a shift register adapted to generate sampling signals in sequence; a latch adapted to store external data in response to the sampling signal; a register adapted to temporarily store the data stored in the latch; a voltage digital-analog converter adapted to generate a gradation voltage corresponding to the data stored in the register; a current digital-analog converter adapted to generate a gradation

current corresponding to the data stored in the register; a buffer adapted to supply the gradation voltage as a data signal to a pixel; and a data controller adapted to receive a pixel current flowing in the pixel in correspondence to the gradation voltage and fed back from the pixel and to adjust a bit value of the data stored in the register.

[0013] The data controller is preferably adapted to compare the pixel current with the gradation current, and to increase or decrease the bit value of the data stored in the register on the basis of compared results.

[0014] The data controller is preferably adapted to increase or decrease the bit value of the data by a previously set constant value.

[0015] The latch preferably comprises: a sampling latch adapted to store the data in sequence in response to the sampling signal; and a holding latch adapted to store the data stored in the sampling latch and at the same time to supply the stored data to the register.

[0016] The data controller preferably comprises j data controllers adapted to adjust the bit values of j data (where, j is a natural number).

[0017] Each data controller comprises: a comparator adapted to compare the pixel current with the gradation current; and a data adjuster adapted to adjust the bit value of the data stored in the register on the basis of control by the comparator.

[0018] The data adjuster is adapted to adjust the bit value of the data to make the pixel current equal to the gradation current.

[0019] The data driving integrated circuit preferably further comprises a selector arranged between the register and the current digital-analog converter.

[0020] The selector preferably comprises j switching devices, each switching device being adapted to be turned on for a first period of one horizontal period to supply the data from the register to the current digital-analog converter, and to be turned off for a second period of one horizontal period except for the first period to prevent the data having the adjusted bit value from the register being supplied to the current digital-analog converter.

[0021] The foregoing and/or other aspects of the present invention can also be achieved by providing a light emitting display, comprising: a plurality of scan lines; a plurality of data lines and feedback lines arranged to intersect the scan lines; a pixel portion including a plurality of pixels connected to the scan lines, the data lines and the feedback lines; a scan driver adapted to supply scan signals to the scan lines in sequence; and a data driver connected to the data line and the feedback lines and adapted to convert external data into a gradation voltage, and to supply the gradation voltage to the data line; wherein the data driver is adapted to receive a pixel current flowing in each pixel corresponding to the gradation voltage, and to adjust a bit value of the data in accordance with the received pixel current.

[0022] The data driver preferably comprises at least one data driving integrated circuit, each data driving integrated circuit comprising: a shift register adapted to generate sampling signals in sequence; a latch adapted to store external data in response to the sampling signal; a register adapted to temporarily store the data stored in the latch; a voltage digital-analog converter adapted to generate a gradation voltage corresponding to the data stored in the register; a current digital-analog converter adapted to generate a gradation current corresponding to the data stored in the register; a buffer adapted to supply the gradation voltage as a data signal to a pixel; and a data controller adapted to receive a pixel current flowing in the pixel in correspondence to the gradation voltage and fed back from the pixel and to adjust a bit value of the data stored in the register.

[0023] The data controller is preferably adapted to compare the pixel current with the gradation current, and to increase or decrease the bit value of the data stored in the register by a previously set constant value on the basis of compared results.

[0024] The data controller preferably comprises j data controllers adapted to adjust the bit values of j data (where, j is a natural number).

[0025] Each data controller comprises: a comparator adapted to compare the pixel current with the gradation current; and a data adjuster adapted to adjust the bit value of the data stored in the register on the basis of control by the comparator.

[0026] The data adjuster is adapted to adjust the bit value of the data to make the pixel current equal to the gradation current.

[0027] The foregoing and/or other aspects of the present invention can also be achieved by providing a method of driving a light emitting display according to claim 8, the method comprising: generating a gradation voltage and a gradation current corresponding to data; supplying the gradation voltage to pixels; comparing a pixel current flowing in one pixel in correspondence to the gradation voltage with the gradation current; and adjusting a bit value of the data on the basis of compared result.

[0028] Adjusting a bit value of the data on the basis of compared result preferably comprises increasing or decreasing the bit value of the data to equalize the pixel current with the gradation current.

[0029] Adjusting a bit value of the data on the basis of compared result preferably comprises increasing or decreasing the bit value of the data by a previously set constant value.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] A more complete appreciation of the present invention, and many of the attendant advantages thereof, will be readily apparent as the present invention becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings, in which like reference symbols indicate the same or similar components, wherein:

[0031] FIG. 1 is a view of a light emitting display;

[0032] FIG. 2 is a view of a light emitting display according to an embodiment of the present invention;

[0033] FIG. 3 is a block diagram of an embodiment of the data driving integrated circuit of FIG. 2;

[0034] FIG. 4 is a detailed block diagram of the data control block of FIG. 3;

[0035] FIG. 5 is a block diagram of a selector provided anterior to the current digital-analog converter of FIG. 2;

[0036] FIG. 6 is a view of a waveform of a selection signal supplied to the selector of FIG. 5; and

[0037] FIG. 7 is a circuit diagram of the comparator of FIG. 4.

DETAILED DESCRIPTION OF THE INVENTION

[0038] Referring to FIG. 1, a light emitting display includes: a pixel portion 30 having a plurality of pixels 40 formed in a region defined by the intersections of scan lines S 1 through Sn and data lines D 1 through Dm; a scan driver 10 to drive the scan lines S 1 through Sn; a data driver 20 to drive the data lines D 1 through Dm; and a timing controller 50 to control the scan driver 10 and the data driver 20.

[0039] The timing controller 50 generates a Data Control Signal (DCS) and a Scan Control Signal (SCS) corresponding to an external synchronization signal. The DCS and the SCS are supplied from the timing controller 50 to the data driver 20 and the scan driver 10, respectively. Furthermore, the timing controller 50 supplies external data to the data driver 20.

[0040] The scan driver 10 receives the scan control signal SCS from the timing controller 50. The scan driver 10 generates scan signals on the basis of the scan control signal SCS and supplies the scan signals to the scan lines S1 through Sn.

[0041] The data driver 20 receives the DCS from the timing controller 50. The data driver 20 generates data signals on the basis of the DCS and supplies the data signals to the data lines D1 through Dm while synchronizing with the scan signals.

[0042] The display portion 30 receives a first voltage ELVDD and a second voltage ELVSS from an external power source, and supplies them to the respective pixels 40. When the first voltage ELVDD and the second voltage ELVSS are supplied to the pixels 40, each pixel 40 controls a current corresponding to the data signal to flow from a first voltage ELVDD to a second voltage ELVSS via the light emitting device, thereby emitting light corresponding to the data signal.

[0043] That is, in such a light emitting display, each pixel 40 emits light with predetermined brightness corresponding to the data signal, but cannot emit light with desired brightness because transistors provided in the respective pixels 40 are different in threshold voltage from each other. Furthermore, in such a light emitting display, there is no method of measuring and controlling a real current flowing in each pixel 40 in correspondence with the data signal.

[0044] Hereinafter, exemplary embodiments according to the present invention are described with reference to the accompanying drawings, wherein the exemplary embodiments of the present invention have been provided to be readily understood by those skilled in the art.

[0045] FIG. 2 is a view of a light emitting display according to an embodiment of the present invention.

[0046] Referring to FIG. 2, a light emitting display according to an embodiment of the present invention includes: a pixel portion 130 having pixels 140 formed on a region intersected by scan lines S1 through Sn, data lines D 1 through Dm and feedback lines F 1 through Fm; a scan driver 110 to drive scan lines S1 through Sn; a data driver 120 to drive data lines D1 through Dm; and a timing controller to control the data driver 120.

[0047] The pixel portion 130 includes the plurality of the pixels 140 connected to the scan lines S 1 through Sn, the data lines D 1 through Dm and the feedback lines F1 through Fm. The scan lines S1 through Sn are formed horizontally and supply a scan signal to the pixels 140. The data lines D1 through Dm are formed vertically and supply a data signal to the pixels 140. The feedback lines F1 through Fm receive the pixel current from pixels 140 and supply to the data driver 120 in correspondence to the data signal. The feedback lines F1 through Fm are formed at the same direction (vertical direction) as the data lines D1 through Dm. The feedback lines F1 through Fm receive a current from the pixels 140 to which a data signal is currently being supplied. That is, the pixel current is generated by the pixels 140 currently receiving the scan signal, and is returned to the data driver 120 via the feedback lines F1 through Fm.

[0048] The first external voltage ELVDD and the second external voltage ELVSS are supplied to the pixels 140. When the first external voltage ELVDD and the second external voltage ELVSS are supplied to the pixels 140, each pixel 140 controls the pixel current corresponding to the data signal in the data lines D flowing from the first voltage ELVDD to the second voltage ELVSS via the light emitting device. Furthermore, a plurality of the pixels 140 supply the pixel current during a predetermined period of one horizontal period.

[0049] The timing controller 150 generates the data driving control signal DCS and scan driving control signal SCS in correspondence with the external synchronization signals. The data driving control signal DCS and the scan driving control signal SCS, which are generated in the timing controller 150, are respectively supplied to the data driver 120 and the scan driver 110. Furthermore, the timing controller 150 supplies the external data to the data driver 120.

[0050] The scan driver 110 receives the scan driving control signal SCS from the timing controller 150 and generates the scan signals, thereby supplying the scan signals to the scan lines S1 through Sn in sequence.

[0051] The data driver 120 receives the data driving control signal DCS from the timing controller 150 and

generates the data signals, thereby supplying the data signals to the data lines D1 through Dm while synchronizing with the scanning signal. The data driver 120 supplies a predetermined gradation voltage as a data signal to the data lines D.

[0052] Furthermore, the data driver 120 receives the pixel current from the pixels 140 via feedback lines F1 through Fm. The data driver 120 receives the pixel current and checks whether the intensity of pixel current corresponds to the data. For example, when the pixel current flowing in the pixel 140 should have an intensity of 10 microamperes corresponding to a bit value (or gradation value) of the data, the data driver 120 checks whether the pixel current supplied from the pixel 140 is 10 microamperes. When the desired current is not supplied to each pixel 140, the data driver 120 adjusts the bit value (or gradation value) of the data in order to cause the desired current to flow for each pixel 140. The data driver 120 comprises at least one data driving integrated circuit 129 having j channels (where, j is a natural number).

[0053] FIG. 3 is a block diagram of the data driving integrated circuit of FIG. 2.

[0054] Referring to FIG. 3, a data driving integrated circuit 129 comprises a shift register 200 to generate sampling signals sequentially; a sampling latch 210 to sequentially store data in response to the sampling signal; a holding latch 220 to temporally store the data of the sampling latch 210 and to transmit the data stored therein; a register 230 to temporally store the data transmitted from the holding latch 220; a data control block 240 to increase or decrease the bit value of the data stored in the register 230; a Voltage Digital-Analog Converter (VDAC) 250 to generate a gradation voltage Vdata corresponding to the bit value of the data Vdata stored in the register 230; a Current Digital-Analog Converter (IDAC) 260 to generate a gradation current Idata corresponding to the bit value of the data stored in the register 230; a buffer 270 to supply the gradation voltage Vdata supplied from the VDAC 250 to data lines D1 through Dj.

[0055] The shift register 200 receives a Source Shift Clock (SSC) and a Source Start Pulse (SSP) from the timing controller 150, and j sampling signals sequentially while shifting the source start pulse SSP per one cycle of the source shift clock SSC. The shift register 200 comprises j shift registers (2001 through 200j).

[0056] The sampling latch 210 stores the data Data in response to the sampling signals sequentially transmitted from the shift register 200. The sampling latch 210 comprises j sampling latches 2101 through 210j in order to store j data. Furthermore, each sampling latch 2101 through 210j has a size corresponding to the bit value of the data. For example, in the case of the data of k bits, each sampling latch 2101 through 210j is set to have a size corresponding to k bits.

[0057] The register 230 temporally stores the data supplied from the holding latch 220. The data stored in the register 230 is supplied to the data controller 240, the VDAC 250 and the IDAC 260. The register 230 comprises j registers 2301 through 230j each set to have a size corresponding to k bits.

[0058] The data control block 240 receives the gradation current Idata, the pixel current Ipixel and data Data, and compares the gradation current Idata with the pixel current Ipixel. Then, the data controller 240 adjusts the bit value of the data Data on the basis of the compared current difference. Preferably, the data controller 240 adjusts the bit value of the data in order to make the gradation current Idata equal to the pixel current Ipixel. The data adjusted in the data controller 240 (hereinafter referred to as "reset data") is returned to the register 230. The data controller 240 comprises j data controllers 2401 through 240j.

[0059] The VDAC 250 generates the gradation voltage Vdata corresponding to the bit value of the data Data or reset data, and supplies the gradation voltage Vdata to the buffer 270. The VDAC 250 generates j gradation voltage Vdata corresponding to j data (or reset data) transmitted from the register 230. TheVDAC 250 comprises j gradation voltage generators 2501 through 250j.

[0060] IDAC 260 generates the gradation current Idata corresponding to the bit value of the data Data, and supplies it to the data controller 240. IDAC 260 generates j gradation current Idata in correspondence to j data transmitted from the register 230. The IDAC 260 comprises j gradation current generators 2601 through 260j.

[0061] The buffer 270 supplies the gradation voltage supplied from the VDAC 250 to j data lines D1 through Dj. The buffer 270 comprises j buffers 2701 through 270j.

[0062] FIG. 4 is a detailed block diagram of the data controller of FIG. 3. For the sake of convenience, the jth data controller is illustrated.

[0063] Referring to FIG. 4, a data controller 240j of the present invention comprises a comparator 241 and a data adjuster 242.

[0064] The comparator 241 receives the gradation current Idata and the pixel current Ipixel from the gradation current generator 260j and the pixel 140, respectively. The pixel current Ipixel is supplied from the pixel 140 that is receiving the current gradation voltage Vdata (i.e., data signal). Then, the comparator 241 compares the pixel current Ipixel with the gradation current Idata, and supplies a first control signal or a second control signal to the data adjuster 242 on a basis of the compared result. For example, when the gradation current Idata is higher than the pixel current Ipixel, the comparator 241 generates the first control signal. On the other hand, when the gradation current Idata is lower than the pixel current Ipixel, the comparator 241 generates the second control signal.

[0065] The data adjuster 242 receives the data Data from the register 230j and stores it therein. Furthermore, the data adjuster 242 receives the first control signal or the second control signal from the comparator 241, and receives a constant value CN from the outside. Then, the data adjuster 242 increases or decreases the bit value

of the data Data by the constant value CN, thereby adjusting the data Data. The data Data adjusted by the data adjuster 242 is supplied to the register 230j.

[0066] The data controller operates as follows. The register 230j supplies the data Data from the holding latch 220j to the data adjuster 242, the gradation voltage generator 250j, and the gradation current generator 260j. The gradation voltage generator 250j receives the data Data, generates the gradation voltage Vdata corresponding to the bit value of the data Data, and supplies the gradation voltage Vdata to the buffer 270j. The gradation voltage Vdata is supplied from the buffer 270j to the pixel 140 via the data line Dj. The pixel 140 supplies the pixel current Ipixel corresponding to the data signal to the feedback lines Fj.

[0067] The gradation current generator 260j receives the data Data and generates the gradation current Idata corresponding to the bit value of the data Data. The gradation current Idata is supplied to the comparator 241. Then, the comparator 241 receives the pixel current Ipixel and the gradation current Idata from the feedback lines Fj and the gradation current generator 260j, respectively. The gradation current Idata is an ideal current to flow in the pixel 140 in correspondence to the data, and the pixel current Ipixel is an actual current flowing in the pixel 140. Then, the comparator 241 compares the pixel current Ipixel with the gradation current Idata, and generates the first control signal or the second control signal on the basis of the compared result, thereby supplying the first control signal or the second control signal to the data adjuster 242.

[0068] The data adjuster 242 receives the first control signal or the second control signal, and increases or decreases the stored data Data by the constant value CN, thereby generating the reset data Data. The reset data Data is supplied to the register 230j. The data adjuster 242 adjusts the bit value of the data Data to approximately equalize the pixel current Ipixel with the gradation current Idata. For example, in the case where the data adjuster 242 receives the first control signal, the data adjuster 242 decreases the bit value of the data Data by the constant value CN, thereby increasing the pixel current Ipixel. On the other hand, in the case where the data adjuster 242 receives the second control signal, the data adjuster 242 increases the bit value of the data Data by the constant value CN, thereby decreasing the pixel current Ipixel. The constant value CN has been previously set to a predetermined value.

[0069] The reset data Data is supplied from the data adjuster 242 to the register 230j. Then, the register 230j supplies the reset data Data to the gradation voltage generator 250j. Then, the gradation voltage generator 250j generates the gradation voltage Vdata using the reset data Data, and supplies the gradation voltage Vdata to the pixel 140 via the buffer 270j. The pixel 140 receives the gradation voltage Vdata and generates the pixel current Ipixel corresponding to the gradation voltage Vdata, thereby supplying the pixel current Ipixel to the comparator 241. Substantially, the aforesaid processes are repeated a predetermined number of times per horizontal period 1H, thereby controlling a desired pixel current Ipixel to flow in the pixel 140.

[0070] Referring to FIG. 4, the gradation current generator 260j can generate the gradation current Idata correspondence to the reset data Data. Actually, the gradation current Idata generated corresponding to the reset data is not an ideal current which should flow in the pixel 140. Therefore, when the gradation current Idata corresponding to the reset data Data is supplied to the comparator 141, an undesired pixel current Ipixel flows in the pixel 140. To solve this problem, a selector 255 can be additionally provided between the register 230 and IDAC 260 as shown in FIG. 5.

[0071] The selector 255 comprises switching devices SW1 provided corresponding to respective channels. For example, the selector 255 comprises j switch devices SW1. Referring to the FIG. 6, the switching device SW is turned on in response to a third control signal CS3 for a first period of one horizontal period, and turned off for the rest of one horizontal period, i.e., a second period. During the first period for turning on the switching device SW1, the IDAC 260 receives the data Data from the register 230. Furthermore, during the second period for storing the reset data in the register 230, the switching device SW1 is turned off. Thus, the IDAC 260 generates only the gradation current Idata corresponding to the data Data, and controls the pixel current Ipixel to flow in the pixel 140.

[0072] FIG. 7 is a circuit diagram of the comparator of FIG. 4. The comparator illustrated in FIG. 7 was disclosed by the Institute of Electrical and Electronics Engineers (IEEE) in 1992. However, the comparator according to an embodiment of the present invention is not limited to that proposed by the IEEE. Alternatively, various well-known comparators may be used in the present invention.

[0073] Referring to FIG. 7, the current corresponding to the difference between the pixel current Ipixel and the gradation current Idata is supplied to a second node N2. Then, the current is supplied from the second node N2 to gate terminals of a fourth transistor M4 and a fifth transistor M5 formed as an inverter. Then, either of the fourth transistor M4 or the fifth transistor M5 is turned on, thereby supplying a high voltage VDD or a low voltage GND to an output terminal. The voltage supplied to the output terminal is supplied to the gate terminals of the second and third transistors M2 and M3, thereby stably maintaining the voltage supplied to the output terminal.

[0074] As described above, the present invention provides a data driving integrated circuit, a light emitting display using the data driving integrated circuit, and a driving method thereof, which compares a gradation current corresponding to data with a pixel current flowing in a pixel, and adjusts a bit value of the data on the basis of the compared results so as to approximately equalize the pixel current with the gradation current, thereby display-

ing an image with a desired brightness. Particularly, according to an embodiment of the present invention, the bit value of the data is adjusted on the basis of the pixel current fed back from each pixel, so that an image is displayed with a desired brightness regardless of non-uniform threshold voltages between transistors.

[0075] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that modifications can be made to this embodiment without departing from the scope of the appended claims.

Claims

1. A data driving integrated circuit (129) for a light emitting display comprising a plurality of pixels (140), each pixel (140) comprising a light emitting device for emitting light by electron-hole combination and a transistor for supplying a pixel current corresponding to a data signal to the light emitting device, the data driving integrated circuit (129) comprising:

a shift register (200) adapted to generate sampling signals in sequence;
a latch (210, 220) adapted to store external data in response to the sampling signal;
a register (230) adapted to temporarily store the data stored in the latch (210, 220);
a voltage digital-analog converter (250) adapted to generate a gradation voltage corresponding to the data stored in the register (230); and
a buffer (270) adapted to supply the gradation voltage as the data signal to the transistor of a pixel (140),
characterized in that
the data driving integrated circuit (129) further comprises:

a current digital-analog converter (260) adapted to generate a gradation current corresponding to the data stored in the register (230); and
a data controller (240) adapted to receive the pixel current flowing via the light emitting device in the pixel (140) in correspondence to the data signal and fed back from the pixel (140) and to adjust a bit value of the data stored in the register (230),
wherein the data controller (240) comprises a comparator (241) adapted to compare the pixel current with the gradation current, and a data adjuster (242) adapted to increase or decrease the bit value of the data stored in the register (230) on the basis of the results of the comparison to make the pixel current equal to the gradation current.

2. The data driving integrated circuit according to claim 1, wherein the data controller (240) is adapted to increase or decrease the bit value of the data by a previously set constant value.

3. The data driving integrated circuit according to claim 1, wherein the latch (210, 220) comprises:

a sampling latch (210) adapted to store the data in sequence in response to the sampling signal; and
a holding latch (220) adapted to store the data stored in the sampling latch (210) and at the same time to supply the stored data to the register (230).

4. The data driving integrated circuit according to claim 1, wherein the data controller (240) comprises j data controllers (2401, 2402, 2403, 2404, 240j) adapted to adjust the bit values of j data (where, j is a natural number).

5. The data driving integrated circuit according to claim 1, further comprising a selector (255) arranged between the register (230) and the current digital-analog converter (260).

6. The data driving integrated circuit according to claim 5, wherein the selector (255) comprises j switching devices (SW1), each switching device (SW1) being adapted to be turned on for a first period of one horizontal period to supply the data from the register (230) to the current digital-analog converter (260), and to be turned off for a second period of one horizontal period except for the first period to prevent the data having the adjusted bit value from the register (230) being supplied to the current digital-analog converter (260).

7. A light emitting display, comprising:

a plurality of scan lines (S1, S2, Sn);
a plurality of data lines (D1, D2, Dm) and feedback lines (F1, F2, Fm) arranged to intersect the scan lines (S1, S2, Sn);
a pixel portion (130) including a plurality of pixels (140) connected to the scan lines (S1, S2, Sn), the data lines (D1, D2, Dm) and the feedback lines (F1, F2, Fm);
a scan driver adapted to supply scan signals to the scan lines (S1, S2, Sn) in sequence; and
a data driver connected to the data lines (D1, D2, Dm) and the feedback lines (F1, F2, Fm) and comprising at least one data driving integrated circuit (129) according to one of the preceding claims.

8. A method of driving a light emitting display compris-

ing a plurality of pixels (140), each pixel (140) comprising a light emitting device for emitting light by electron-hole combination and a transistor for supplying a pixel current corresponding to a data signal to the light emitting device, and a data driving integrated circuit (129) as defined in any of claims 1 to 6, the method comprising:

generating by the shift register (200) sampling signals in sequence,
storing by the latch (210, 220) external data in response to the sampling signal,
temporarily storing by the register (230) the data stored in the latch (210, 220),
generating by the voltage digital-to-analog converter (250) a gradation voltage corresponding to data; and
supplying by the buffer (270) the gradation voltage as the data signal to the transistor of a pixel (140),
characterized in that the method further comprises:

generating a gradation current by the current digital-to-analog converter (260) corresponding to the data stored in the register (230);
receiving by the data controller (240) the pixel current flowing via the light emitting device in the pixel (140) in correspondence to the data signal and fed back from the pixel (140);
comparing by the comparator (241) the pixel current flowing in the pixel (140) with the gradation current; and
adjusting by the data adjuster (242) a bit value of the data on the basis of the result of the comparison to make the pixel current equal to the gradation current.

9. The method according to claim 8, wherein adjusting a bit value of the data on the basis of compared result comprises increasing or decreasing the bit value of the data to equalize the pixel current with the gradation current.

10. The method according to claim 9, wherein adjusting a bit value of the data on the basis of compared result comprises increasing or decreasing the bit value of the data by a previously set constant value.

Patentansprüche

1. Integrierte Datentreiberschaltung (129) für eine lichtemittierende Anzeige, die eine Mehrzahl von Pixeln (140) umfasst, wobei jedes Pixel (140) eine lichtemittierende Vorrichtung zur Emission von Licht durch Elektronen-Loch-Kombination und einen Transistor zum Liefern eines einem Datensignal entsprechenden Pixelstroms an die lichtemittierende Vorrichtung umfasst, wobei die integrierte Datentreiberschaltung (129) umfasst:

ein Schieberegister (200), das so angepasst ist, dass es Abtastsignale in Folge erzeugt;
einen Zwischenspeicher (210, 220), der so angepasst ist, dass er als Reaktion auf das Abtastsignal externe Daten speichert;
ein Register (230), das so angepasst ist, dass es die im Zwischenspeicher (210, 220) gespeicherten Daten temporär speichert;
einen Digital/Analog-Spannungswandler (250), der so angepasst ist, dass er eine den im Register (230) gespeicherten Daten entsprechende Abstufungsspannung erzeugt; und
einen Puffer (270), der so angepasst ist, dass er die Abstufungsspannung als Datensignal an den Transistor eines Pixels (140) liefert,
dadurch gekennzeichnet, dass
die integrierte Datentreiberschaltung (129) ferner umfasst:

einen Digital/Analog-Stromwandler (260), der so angepasst ist, dass er einen den im Register (230) gespeicherten Daten entsprechenden Abstufungsstrom erzeugt; und
einen Datencontroller (240), der so angepasst ist, dass er den in Übereinstimmung mit dem Datensignal über die lichtemittierende Vorrichtung in dem Pixel fließenden und von dem Pixel zurückgeführten Pixelstrom empfängt und dass er einen Bitwert der im Register (230) gespeicherten Daten anpasst,
wobei der Datencontroller (240) umfasst: einen Komparator (241), der so angepasst ist, dass er den Pixelstrom mit dem Abstufungsstrom vergleicht, und eine Datenanpassungseinheit (242), die so angepasst ist, dass sie den Bitwert der im Register (230) gespeicherten Daten auf der Grundlage der Vergleichsergebnisse erhöht oder verringert, um den Pixelstrom an den Abstufungsstrom anzugleichen.

2. Integrierte Datentreiberschaltung nach Anspruch 1, wobei der Datencontroller so angepasst ist, dass er den Bitwert der Daten um einen vorab festgelegten konstanten Wert erhöht oder verringert.

3. Integrierte Datentreiberschaltung nach Anspruch 1, wobei der Zwischenspeicher (210, 220) umfasst:

einen Abtastzwischenspeicher (210), der so an-

gepasst ist, dass er als Reaktion auf das Abtastsignal die Daten in Folge speichert; und
einen Haltezwischenspeicher (220), der so angepasst ist, dass er die im Abtastzwischenspeicher (210) gespeicherten Daten speichert und gleichzeitig die gespeicherten Daten an das Register (230) liefert.

4. Integrierte Datentreiberschaltung nach Anspruch 1, wobei der Datencontroller (240) j Datencontroller (2401, 2402, 2403, 2404, 240j) umfasst, die so angepasst sind, dass sie die Bitwerte von j Daten (wobei j eine natürliche Zahl ist) anpassen.

5. Integrierte Datentreiberschaltung nach Anspruch 1, die ferner einen zwischen dem Register (230) und dem Digital/Analog-Stromwandler (260) angeordneten Selektor (255) umfasst.

6. Integrierte Datentreiberschaltung nach Anspruch 5, wobei der Selektor j Schaltvorrichtungen (SW1) umfasst, wobei jede Schaltvorrichtung (SW1) so angepasst ist, dass sie für einen ersten Zeitraum eines horizontalen Zeitraums angeschaltet ist, um die Daten vom Register (230) an den Digital/Analog-Stromwandler (260) zu liefern, und für einen zweiten Zeitraum eines horizontalen Zeitraums unter Ausnahme des ersten Zeitraums abgeschaltet ist, um zu verhindern, dass die Daten mit dem angepassten Bitwert vom Register (230) an den Digital/Analog-Stromwandler (260) geliefert werden.

7. Lichtemittierende Anzeige, umfassend:

eine Mehrzahl von Abtastzeilen (S1, S2, Sn);
eine Mehrzahl von Datenzeilen (D1, D2, Dm) und Feedbackzeilen (F1, F2, Fm), die so angeordnet sind, dass sie die Abtastzeilen (S1, S2, Sn) schneiden;
einen Pixelabschnitt (130), der eine Mehrzahl von Pixeln (140) einschließt, die mit den Abtastzeilen (S1, S2, Sn), den Datenzeilen (D1, D2, Dm) und den Feedbackzeilen (F1, F2, Fm) verbunden sind;
einen Abtasttreiber (110), der so angepasst ist, dass er Abtastsignale in Folge an die Abtastzeilen (S1, S2, Sn) liefert; und
einen Datentreiber (120), der mit den Datenzeilen (D1, D2, Dm) und den Feedbackzeilen (F1, F2, Fm) verbunden ist und mindestens eine integrierte Datentreiberschaltung nach einem der vorangehenden Ansprüche umfasst.

8. Verfahren zum Treiben einer lichtemittierenden Anzeige, die umfasst: eine Mehrzahl von Pixeln (140), wobei jedes Pixel (140) eine lichtemittierende Vorrichtung zur Emission von Licht durch Elektronen-Loch-Kombination und einen Transistor zum Liefern eines einem Datensignal entsprechenden Pixelstroms an die lichtemittierende Vorrichtung umfasst, und eine integrierte Datentreiberschaltung (129), wie in einem der Ansprüche 1 bis 6 definiert, wobei das Verfahren umfasst:

Erzeugen von Abtastsignalen in Folge durch das Schieberegister (200),
Speichern externer Daten durch den Zwischenspeicher (210, 220) als Reaktion auf das Abtastsignal,
temporäres Speichern der im Zwischenspeicher (210, 220) gespeicherten Daten durch das Register (230),
Erzeugen einer den Daten entsprechenden Abstufungsspannung durch den Digital/Analog-Spannungswandler (250), und
Liefern der Abstufungsspannung als Datensignal an den Transistor eines Pixels (140) durch den Puffer (270),
dadurch gekennzeichnet, dass das Verfahren ferner umfasst:

Erzeugen eines Abstufungsstroms durch den Digital/Analog-Stromwandler (260) entsprechend den im Register (230) gespeicherten Daten;
Empfangen des in Übereinstimmung mit dem Datensignal über die lichtemittierende Vorrichtung in dem Pixel (140) fließenden und von dem Pixel (140) zurückgeführten Pixelstroms durch den Datencontroller (240);
Vergleichen des in dem Pixel (140) fließenden Pixelstroms mit dem Abstufungsstrom durch den Komparator (241); und
Anpassen eines Bitwerts der Daten auf der Grundlage des Vergleichsergebnisses durch die Datenanpassungseinheit (242), um den Pixelstrom an den Abstufungsstrom anzugleichen.

9. Verfahren nach Anspruch 8, wobei das Anpassen eines Bitwerts der Daten auf der Grundlage des Vergleichsergebnisses das Erhöhen oder Verringern des Bitwerts der Daten zum Angleichen des Pixelstroms an den Abstufungsstrom umfasst.

10. Verfahren nach Anspruch 9, wobei das Anpassen eines Bitwerts der Daten auf der Grundlage des Vergleichsergebnisses das Erhöhen oder Verringern des Bitwerts der Daten um einen vorab festgelegten konstanten Wert umfasst.

Revendications

1. Circuit (129) intégré de commande de données pour

un afficheur électroluminescent comprenant une pluralité de pixels (140), chaque pixel (140) comprenant un dispositif électroluminescent pour émettre de la lumière par une combinaison électron-trou et un transistor pour fournir un courant de pixel correspondant à un signal de données au dispositif électroluminescent, le circuit (129) intégré de commande de données comprenant :

un registre (200) à décalage conçu pour générer des signaux d'échantillonnage dans une séquence ;
un circuit (210, 220) à verrouillage conçu pour stocker des données externes en réponse au signal d'échantillonnage ;
un registre (230) conçu pour stocker temporairement les données stockées dans le circuit (210, 220) à verrouillage ;
un convertisseur (250) de tension numérique-analogique conçu pour générer une tension de gradation correspondant aux données stockées dans le registre (230), et
un tampon (270) conçu pour fournir la tension de gradation, en tant que le signal de données, au transistor d'un pixel (140) ;
le circuit (129) intégré de commande de données étant **caractérisé en ce qu'**il comprend en outre :

un convertisseur (260) de courant numérique-analogique conçu pour générer un courant de gradation correspondant aux données stockées dans le registre (230), et
une unité (240) de commande de données conçue pour recevoir le courant de pixel passant via le dispositif électroluminescent dans le pixel en correspondance au signal de données et renvoyé à partir du pixel et pour ajuster une valeur binaire des données stockées dans le registre (230),
dans lequel l'unité (240) de commande de données comprend un comparateur (241) conçu pour comparer le courant de pixel avec le courant de gradation, et un régulateur (242) de données conçu pour augmenter ou diminuer la valeur binaire des données stockées dans le registre (230) sur la base des résultats de la comparaison pour rendre le courant de pixel égal au courant de gradation.

2. Circuit intégré de commande de données selon la revendication 1, dans lequel l'unité de commande de données est conçue pour augmenter ou diminuer la valeur binaire des données par une valeur constante précédemment définie.

3. Circuit intégré de commande de données selon la revendication 1, dans lequel le circuit (210, 220) à verrouillage comprend :

un circuit (210) à verrouillage d'échantillonnage conçu pour stocker les données dans une séquence en réponse au signal d'échantillonnage ; et
un circuit (220) à verrouillage de maintien conçu pour stocker les données stockées dans le circuit (210) à verrouillage d'échantillonnage et, en même temps, pour fournir les données stockées au registre (230).

4. Circuit intégré de commande de données selon la revendication 1, dans lequel l'unité (240) de commande de données comprend j unités de commande de données (2401, 2402, 2403, 2404, 240j) conçues pour ajuster les valeurs binaires de j données (où j est un entier naturel).

5. Circuit intégré de commande de données selon la revendication 1, comprenant en outre un sélecteur (255) agencé entre le registre (230) et le convertisseur (260) de courant numérique-analogique.

6. Circuit intégré de commande de données selon la revendication 5, dans lequel le sélecteur comprend j dispositifs (SW1) de commutation, chaque dispositif (SW1) de commutation étant conçu de manière à être actif pour une première période d'une période horizontale pour fournir les données à partir du registre (230) au convertisseur (260) de courant numérique-analogique, et à être mis hors tension pour une deuxième période d'une période horizontale à l'exception de la première période, pour prévenir les données ayant les valeurs binaires ajustées à partir du registre (230) d'être fournies au convertisseur (260) de courant numérique-analogique.

7. Afficheur électroluminescent, comprenant :

une pluralité de lignes de balayage (S1, S2, Sn) ;
une pluralité de lignes de données (D1, D2, Dm), et de lignes de rétroaction (F1, F2, F3) agencées de manière à croiser les lignes de balayage (S1, S2, Sn) ;
une partie (130) de pixels comportant une pluralité de pixels (140) reliée aux lignes de balayage (S1, S2, Sn), aux lignes de données (D1, D2, Dm) et aux lignes de rétroaction (F1, F2, F3) ;
un dispositif (110) de commande de balayage conçu pour fournir des signaux de balayage aux lignes de balayage (S1, S2, Sn) dans une séquence ; et
un dispositif (120) de commande de données relié aux lignes de données (D1, D2, Dm) et aux lignes de rétroaction (F1, F2, F3) et comprenant au moins un circuit (129) intégré de commande

de données selon l'une des revendications précédentes.

8. Procédé de commande d'un afficheur électroluminescent comprenant une pluralité de pixels (140), chaque pixel (140) comprenant un dispositif électroluminescent pour émettre de la lumière par une combinaison électron-trou, et un transistor pour fournir un courant de pixel correspondant à un signal de données au dispositif électroluminescent, et un circuit (129) intégré de commande de données tel que défini dans l'une quelconque des revendication 1 à 6, le procédé comprenant le fait :

de générer, par le registre (200) à décalage, des signaux d'échantillonnage dans une séquence,
de stocker, par le circuit (210, 220) à verrouillage, les données externes en réponse au signal d'échantillonnage,
de stocker temporairement, par le registre (230), les données stockées dans le circuit à verrouillage (210, 220),
de générer, par le convertisseur (250) de tension numérique-analogique, une tension de gradation correspondant aux données ; et
de fournir, par le tampon (270), la tension de gradation en tant que le signal de données au transistor d'un pixel (140),
le procédé étant **caractérisé en ce qu'**il comprend en outre le fait :

de générer un courant de gradation par le convertisseur (260) de courant numérique-analogique correspondant aux données stockées dans le registre (230) ;
de recevoir, par l'unité (240) de commande de données, le courant de pixel passant via le dispositif électroluminescent dans le pixel (140) en correspondance au signal de données et renvoyé à partir du pixel (140) ;
de comparer, par le comparateur (241), le courant de pixel (140) passant dans le pixel (140) avec le courant de gradation ; et
d'ajuster, par le régulateur (242) de données, une valeur binaire des données sur la base du résultat de la comparaison pour rendre le courant de pixel égal au courant de gradation.

9. Procédé selon la revendication 8, dans lequel le fait d'ajuster une valeur binaire des données sur la base d'un résultat comparé comprend le fait d'augmenter ou de diminuer la valeur binaire des données pour égaliser le courant de pixel avec le courant de gradation.

10. Procédé selon la revendication 9, dans lequel le fait d'ajuster une valeur binaire des données sur la base d'un résultat comparé comprend le fait d'augmenter ou de diminuer la valeur binaire des données d'une valeur constante précédemment définie.

FIG. 1
(PRIOR ART)

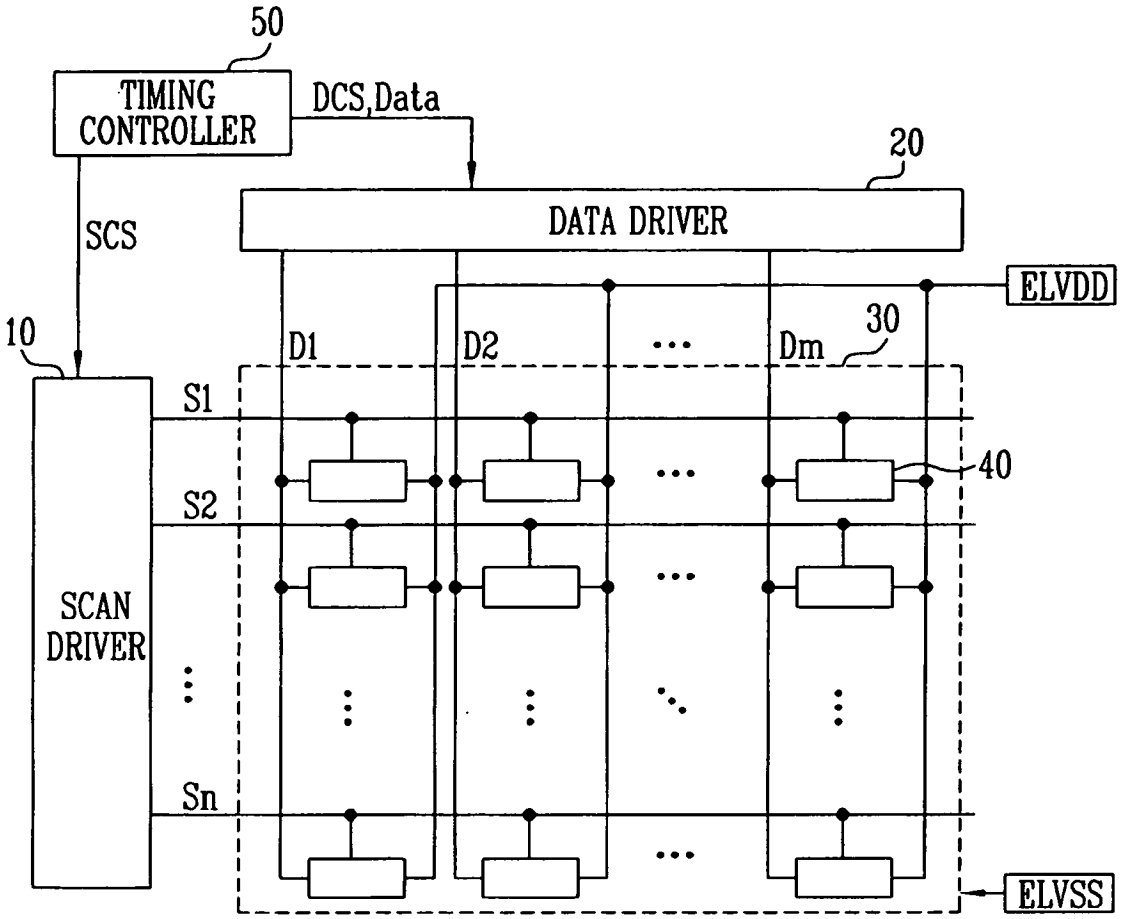


FIG. 2

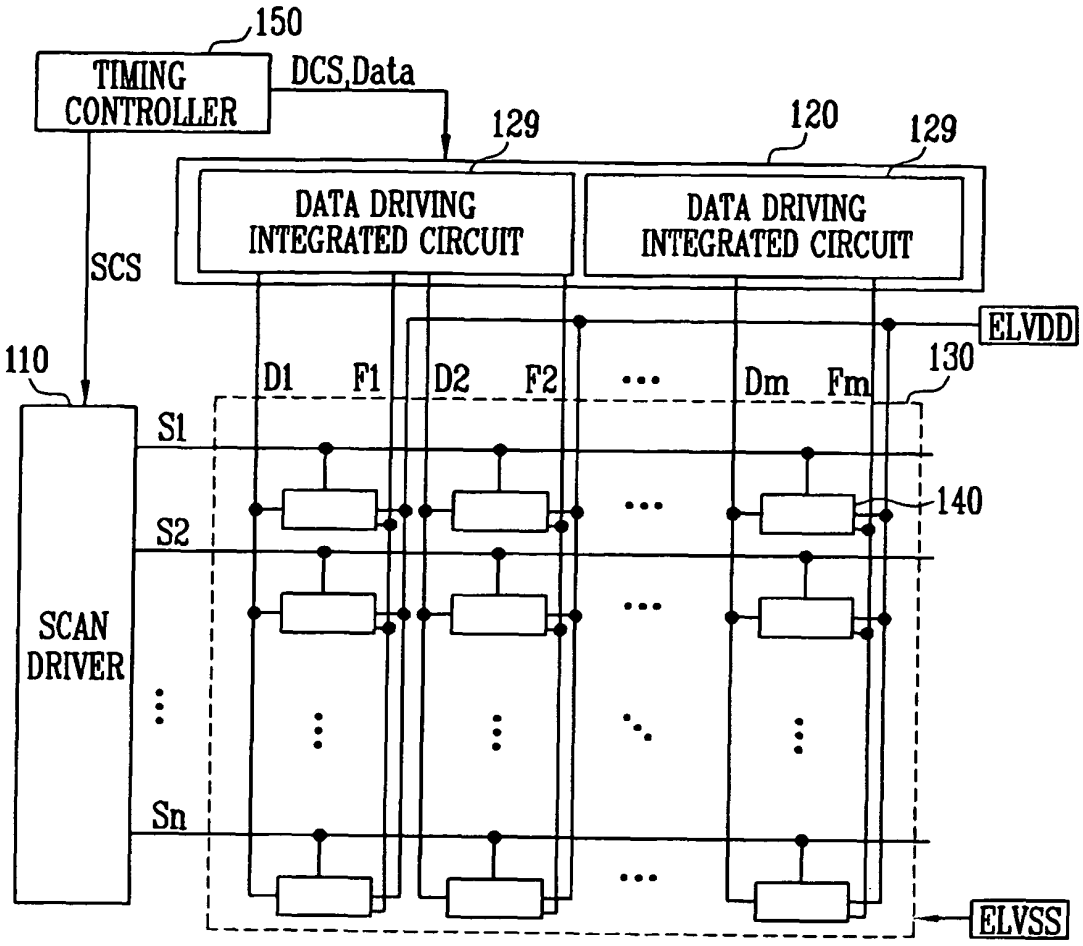

150
TIMING CONTROLLER
DCS,Data
129
120
129
DATA DRIVING INTEGRATED CIRCUIT
DATA DRIVING INTEGRATED CIRCUIT
SCS
ELVDD
110
D1
F1
D2
F2
Dm
Fm
130
S1
S2
140
SCAN DRIVER
Sn
ELVSS

FIG. 3

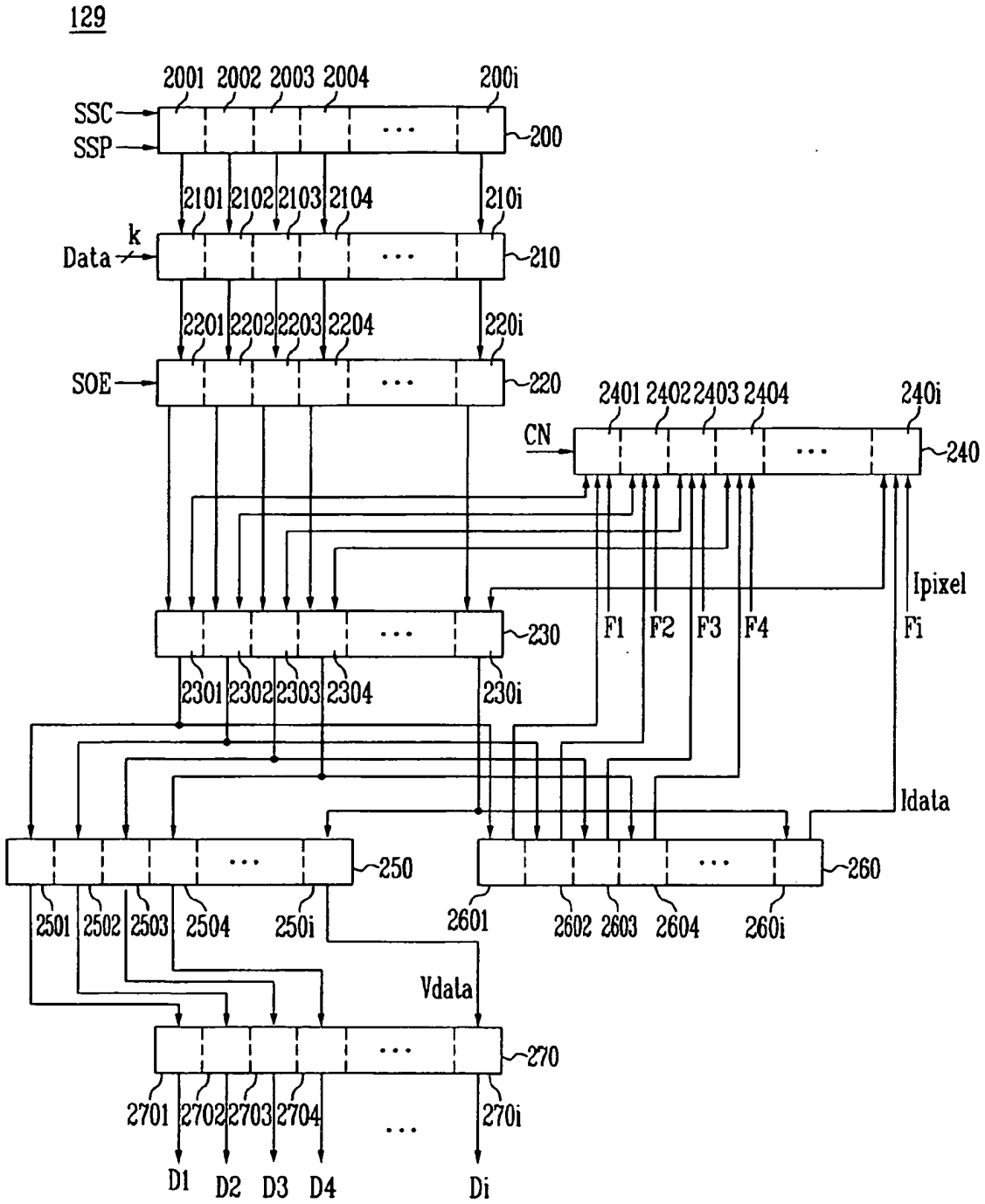

129
2001 2002 2003 2004 200i
SSC
SSP
200
2101 2102 2103 2104 210i
k
Data
210
2201 2202 2203 2204 220i
SOE
220
2401 2402 2403 2404 240i
CN
240
Ipixel
F1 F2 F3 F4 Fi
230
2301 2302 2303 2304 230i
Idata
250
260
2501 2502 2503 2504 250i
2601 2602 2603 2604 260i
Vdata
270
2701 2702 2703 2704 270i
D1 D2 D3 D4 Di

FIG. 4

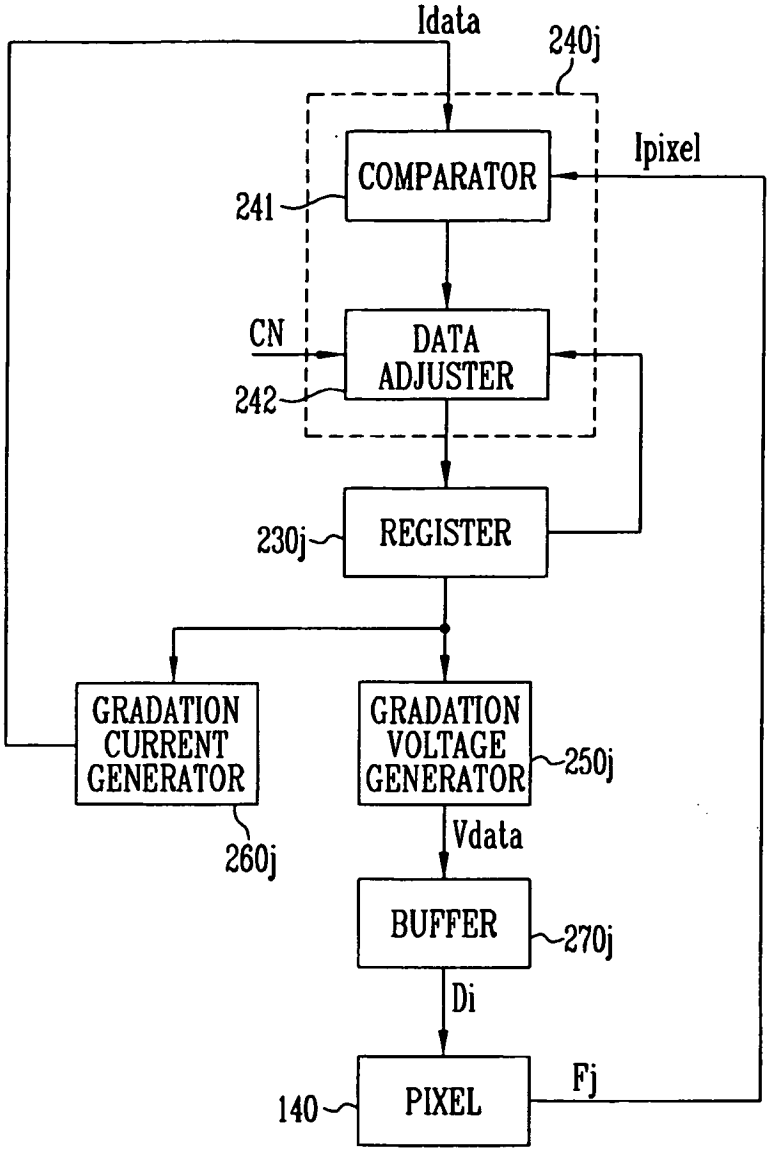

Idata
240j
COMPARATOR
Ipixel
241
CN
DATA ADJUSTER
242
230j
REGISTER
GRADATION CURRENT GENERATOR
260j
GRADATION VOLTAGE GENERATOR
250j
Vdata
BUFFER
270j
Di
140
PIXEL
Fj

FIG. 5

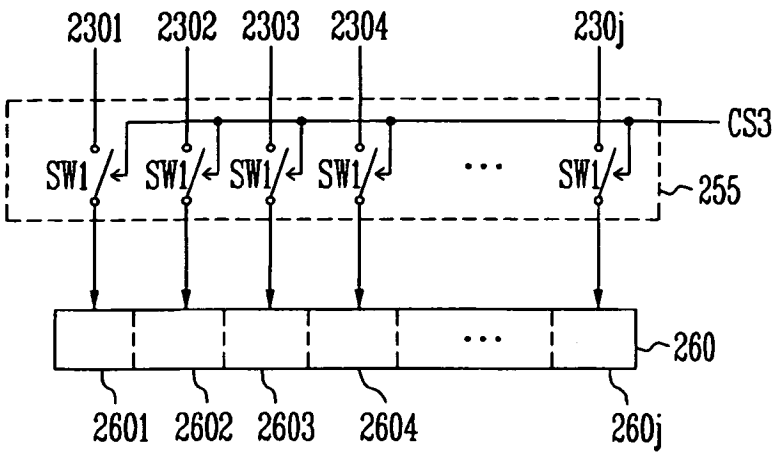

2301
2302
2303
2304
230j
CS3
SW1
SW1
SW1
SW1
SW1
255
260
2601
2602
2603
2604
260j

FIG. 6

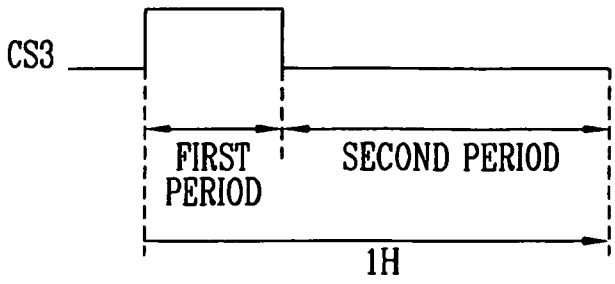
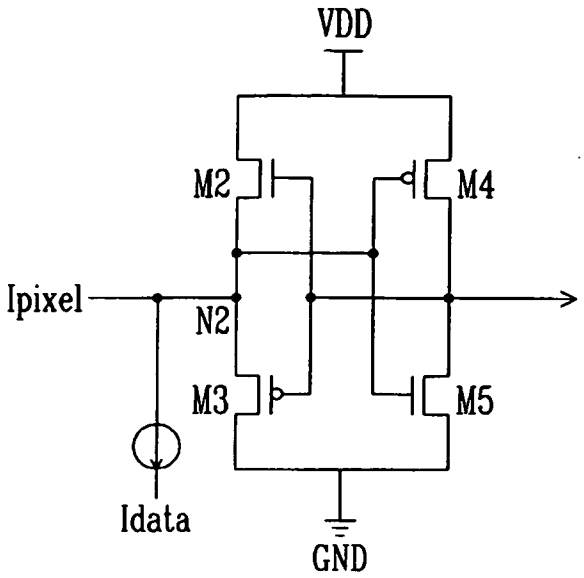


FIG. 7



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2003011314 A1 **[0009]**
- US 2003063081 A1 **[0009]**
- EP 1225557 A1 **[0010]**

专利名称(译)	数据驱动集成电路（IC），使用IC的发光显示器，以及驱动发光显示器的方法		
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申请号	EP2005112589	申请日	2005-12-21
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
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发明人	CHOI, SANG MOO LEGAL & IP TEAM KWON, OH KYONG LEGAL & IP TEAM		
IPC分类号	G09G3/32		
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代理机构(译)	hengelhaupt，Jürgen		
优先权	1020040112530 2004-12-24 KR		
其他公开文献	EP1675096A1		
外部链接	Espacenet		

摘要(译)

一种显示具有所需亮度的图像的数据驱动集成电路（129），包括：移位寄存器（200），用于依次产生采样信号;锁存器（210），适于响应采样信号存储外部数据;寄存器（230），适于临时存储锁存器中存储的数据;电压数模转换器（250），适于产生与存储在寄存器中的数据相对应的灰度电压;电流数模转换器（260），用于产生与存储在寄存器中的数据相对应的灰度电流;缓冲器（270），适于将灰度电压作为数据信号提供给像素;数据控制器（240），适于接收与灰度电压对应的在像素中流动的像素电流，并从像素反馈并调整存储在寄存器中的数据的比特值。