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(54) **Light emitting display and driving device and method thereof**

(57) A driving device for a light emitting display, which includes a plurality of scan lines for transferring a selection signal, comprises: a first driver for shifting a first signal having a first integer multiple of first pulses by a first period, and sequentially outputting the first signal; a second driver for shifting a second signal having a second pulse by a second period, and sequentially

outputting the second signal; and a third driver for sequentially outputting the selection signal having a second integer multiple of third pulses corresponding to at least one of the first integer multiple of first pulses, and a fourth pulse corresponding to the second pulse, in response to the first signal and the second signal.

**Description****BACKGROUND OF THE INVENTION****Technical Field**

[0001] The present invention relates to a light emitting display, a driving device thereof, and a driving method thereof. More specifically, the present invention relates to a light emitting display using an organic light emitting diode (OLED), and a driving method thereof.

**Related Art**

[0002] In general, an OLED display electrically excites a phosphorous organic compound to emit light, and it voltage-drives or current-drives a plurality of organic emitting cells to display images. The organic emitting cell includes an anode, an organic thin film, and a cathode layer. A method for driving the organic emission cells can be classified as a passive matrix method or as an active matrix method using thin film transistors (TFTs). The passive matrix method provides anodes and cathodes that cross (or cross over) each other, in which method a line to drive the organic emission cells is selected. The active matrix method provides TFTs that access respective pixel electrodes, and a pixel is driven according to a voltage maintained by a capacitance of a capacitor accessed by a gate of a TFT. Depending on the formats of the signals applied to capacitors for establishing the voltage, the active matrix method can be categorized as a voltage programming method or a current programming method.

[0003] The pixel circuit of the voltage programming method has a difficulty in obtaining high gray scales because of deviations of the threshold voltage  $V_{TH}$  and carrier mobility, the deviations being caused by non-uniformity in the manufacturing process. For example, in order to represent 8-bit (*i.e.*, 256) gray scales in the case of driving thin film transistors by a voltage of 3V (volts), it is required to apply the voltage to the gate of the thin film transistor with an interval less than a voltage of 12 mV ( $=3V/256$ ). If the deviation of the threshold voltage of the thin film transistor caused by the non-uniformity in the manufacturing process is 100 mV, it is difficult to represent high gray scales.

[0004] However, the pixel circuit of the current programming method achieves uniform display characteristics when the driving transistor in each pixel has non-uniform voltage-current characteristics, provided that a current source for supplying the current to the pixel circuit is uniform throughout the whole panel.

[0005] However, the pixel circuit of the current programming method involves a long data programming time because of a parasitic capacitance component provided on the data line. In particular, the time for programming the data on the current pixel line is influenced by the voltage state of the data line according to the data

of a previous pixel line, and in particular, the data programming time is further lengthened when the data line is charged with a voltage which is very different from the target voltage (the voltage corresponding to the current data). This phenomenon becomes an even greater factor as the gray level becomes lower (near black).

**SUMMARY OF THE INVENTION**

10 [0006] It is an aspect of the present invention to reduce the data programming time in a light emitting display based on the current driving method.

[0007] In an exemplary embodiment of the present invention, a driving device for a light emitting display which includes a plurality of scan lines for transferring a selection signal is provided. The driving device of a light emitting display includes: a first driver for shifting a first signal having a first integer multiple of first pulses by a first period, and sequentially outputting the first signal; a second driver for shifting a second signal having a second pulse by a second period, and sequentially outputting the second signal; and a third driver for sequentially outputting a selection signal having a second integer multiple of third pulses corresponding to at least one of the first integer multiple of first pulses, and for outputting a fourth pulse corresponding to the second pulse in response to the first signal and the second signal.

[0008] The first driver may include: a fourth driver for shifting a third signal having a first integer multiple of first pulses by a third period, and sequentially outputting the third signal; and a fifth driver for selecting a third signal which is sequentially shifted by the first period in response to one of the third signals sequentially outputted from the fourth driver, the first period being a third integer multiple of the third period.

[0009] The first driver may include: a fourth driver for shifting by the first period a third signal having a third integer multiple of fifth pulses, and sequentially outputting the third signal; a fifth driver for shifting by the first period a fourth signal having a sixth pulse, which is a fifth pulse shifted by the third period, and sequentially outputting the fourth signal; and a sixth driver for outputting a first signal having the first pulse in a period in which levels of the first signal and the second signal are different.

[0010] The first driver may include: a fourth driver for shifting a third signal having a fifth pulse by the first period, and sequentially outputting the fifth signal; and a fifth driver for receiving the third signal and a fourth signal having a sixth pulse repeated in a predetermined cycle, and outputting the first signal having the first pulse in a period in which the fifth pulse and the sixth pulse overlap each other.

Preferably the second period is the same as the first period. Preferably a start time point of the second pulse in the second signal is shifted from a start time point of the first pulse in the first signal by a first integer multiple of the first period.

Preferably the first driver comprises a fourth driver for shifting a third signal having the first integer multiple of the first pulses by a third period, and for sequentially outputting the third signal; and a fifth driver for selecting the third signal sequentially shifted by the first period as the first signal in response to one of a plurality of third signals sequentially outputted by the fourth driver, the first period being a third integer multiple of the third period. Preferably the third period has a width the same as a width of the first pulse. Preferably the fourth driver comprises a shift register, and a clock cycle used in the shift register corresponds to twice a width of the first pulse. Preferably the first driver comprises a shift register, and a clock cycle used in the shift register is the same as a width of the first pulse. Preferably the fourth driver comprises a shift register, and the fifth driver selects the first signal according to a third integer interval in the plurality of third signals sequentially outputted by the fourth driver.

In another preferred embodiment of the invention the first driver comprises a fourth driver for shifting a third signal having a third integer multiple of fifth pulses by the first period, and for sequentially outputting the shifted third signal; a fifth driver for shifting by the first period a fourth signal having a sixth pulse which is a fifth pulse shifted by the third period, and for sequentially outputting the fourth signal; and a sixth driver for outputting the first signal having a first pulse in a period, wherein levels of the first signal and the second signal are different. Preferably the third period has a width the same as a width of the first pulse. Preferably a width between two adjacent fifth pulses in a plurality of the fifth pulses is the same as a width of the fifth pulse. Preferably the third period has a width shorter than the width of the fifth pulse. Preferably the third integer corresponds to twice the first integer. Preferably the second driver, the fourth driver and the fifth driver respectively comprise a shift register, and a cycle of a clock used in the second driver corresponds to twice a cycle of a clock used in the fourth driver and the fifth driver. Preferably the second driver, the fourth driver and the fifth driver respectively comprise a shift register, and a cycle of a clock used in the second driver is the same as a cycle of a clock used in the fourth driver and the fifth driver.

In another preferred embodiment of the invention the first driver comprises a fourth driver for shifting a third signal having a fifth pulse by the first period, and for sequentially outputting the fifth signal; and a fifth driver for receiving a fourth signal having a sixth pulse which is repeated in a predetermined cycle, and the third signal, and for outputting the first signal having the first pulse in a period in which the fifth pulse and the sixth pulse overlap each other. Preferably a width of the sixth pulse is the same as a width of the first pulse. Preferably a width of the fifth pulse includes more than a first integer multiple of the sixth pulses. Preferably a cycle of the sixth pulse is the same as a cycle of the first period. Preferably the fourth driver includes a shift register, and a

cycle of a clock used in the fourth driver corresponds to twice a cycle of the sixth pulse. Preferably the fourth driver includes a shift register, and a cycle of a clock used in the fourth driver is the same as a cycle of the sixth pulse.

[0011] In another exemplary embodiment of the present invention, a light emitting display includes a display area and a scan driver. The display area includes a plurality of data lines for transferring a data signal, a plurality of scan lines arranged in a direction crossing the data line, and a plurality of pixels coupled to the data lines and the scan lines, respectively. The scan driver sequentially applies a selection signal having at least one of a first level of a first pulse and the first level of a second pulse to the plurality of scan lines, the second pulse having a narrower width than the first pulse.

Preferably the first pulse is repeated a predetermined number of times before the second pulse is outputted. Preferably a selection signal having the first pulse is applied to at least one of second scan lines, which are different from a first scan line of the plurality of scan lines, in a period in which a selection signal having the second pulse is applied to the first scan line of the plurality of scan lines. Preferably an interval between start time points of two adjacent first pulses is substantially the same as an interval between a start time point of the second pulse and a start time point of the first pulse adjacent to the second pulse. Preferably the scan driver comprises a first driver for shifting a first signal having a predetermined number of third pulses by a first period, and for sequentially outputting the first signal; a second driver for outputting the first signal, shifted in an interval of a second period, as a second signal in response to one first signal of the first signals outputted sequentially, the second period being an integer multiple of the first period; and a third driver for generating the first pulse of the selection signal in response to at least one third pulse of the predetermined number of third pulses in the first signal. Preferably the second period is substantially the same as a cycle of the third pulse.

In another preferred embodiment the scan driver preferably comprises a first driver for shifting a first signal having a predetermined number of third pulses by a first period, and for sequentially outputting the first signal; a second driver for shifting a second signal having fourth pulses by the first period, and for sequentially outputting the second signal, the fourth pulses being the predetermined number of third pulses shifted by a second period; a third driver for outputting a third signal having a fifth pulse in a period such that respective levels of the first signal and the second signal are different; and a fourth driver for generating the first pulse of the selection signal in response to at least one fifth pulse of the third signal. Preferably an interval between adjacent two third pulses in the first signal is the same as a width of the third pulse. Preferably the second period is shorter than the first period.

In another preferred embodiment the scan driver pref-

erably comprises a first driver for receiving a first signal having a third pulse repeated in a predetermined cycle, for shifting a second signal having a predetermined number of third pulses by a first period, and for sequentially outputting the second period; and a second driver for generating the first pulse of the selection signal in response to at least one of third pulses of the second signal. the predetermined cycle is the same as the first period. Preferably the first driver generates a second signal having a fourth pulse which has a width which is a period including the predetermined number of third pulses, and the first driver selects the third pulse with the fourth pulse of the second signal. Preferably the scan driver generates a third signal having a fifth pulse corresponding to the fourth pulse in the second signal, and wherein the pixels stop emitting light in response to the fifth pulse.

Preferably each pixel comprises at least one of a first switch for transferring a data signal from one of the data lines in response to the first level in the selection signal applied to the scan line; a capacitor for charging to a voltage corresponding to the data signal transferred; a transistor for outputting a current according to the voltage charged on the capacitor; and a light emitting element for emitting light according to a magnitude of the current outputted by the transistor.

Preferably the data signal is a current type of signal; the second pulse of the selection signal is applied to a first scan line of a plurality of the scan lines, and the first pulse of the selection signal is applied to at least one of second scan lines which are different from the first scan line in a first period; a first current is applied to the data line in the first period; the second pulse of the selection signal is applied to the first scan line, and a second level of the selection signal of the second level, which is different from the first level, is applied to the second scan line in a second period; and a data signal is applied to the data line in the second period, the data signal corresponding to one of the pixels coupled to the first scan line. Preferably the first current is substantially the same as the current corresponding to the data signal multiplied by a number equal to one more than a number of the second scan lines, the first pulse of the selection signal being applied to the second scan line in the first period. Preferably a current substantially corresponding to a data signal from the first current is transferred in the first period to pixels coupled to the first scan line and the second scan line, respectively.

**[0012]** In another exemplary embodiment of the present invention, a driving method of a light emitting display having a plurality of scan lines for transferring a selection signal is provided. The driving method of the light emitting display includes the steps of: sequentially outputting a first signal having at least one first level of a first pulse while shifting the first signal by a first interval; selecting the first signal shifted by a second interval of the first signals sequentially outputted as a second signal, the second interval being an integer multiple of

the first interval; outputting a third signal having a third pulse corresponding to the first pulse in the second signal; and generating at least one fourth pulse in response to at least one third pulse in the third signal, and outputting the selection signal having at least one fourth pulse.

**[0013]** In another exemplary embodiment of the present invention, a driving method of a light emitting display having a plurality of scan lines for transferring a selection signal is provided. The driving method of the light emitting display includes the steps of: outputting a first signal having at least one first level of a first pulse; outputting a second signal having at least one first level of a second pulse, wherein a start time point is shifted by a predetermined period from a start time point of the first pulse; outputting a third signal having a third level of a third pulse in at least one period in which levels of the first signal and the second signal are different; and generating at least one fourth pulse in response to each of at least one third pulse in the third signal, and outputting the selection signal having the at least one fourth pulse.

**[0014]** In another exemplary embodiment of the present invention, a driving method of a light emitting display having a plurality of scan lines for transferring a selection signal is provided. The driving method of the light emitting display includes the steps of: outputting a first signal having a first level of a first pulse repeated in a predetermined cycle; outputting a second signal having a second level of a second pulse, wherein a width includes at least one first pulse; selecting at least one first pulse with the second pulse of the second signal; and outputting a third signal having a third pulse corresponding to the selected first pulse, generating at least one fourth pulse in response to at least one third pulse in the third signal, and outputting the selection signal having at least one fourth pulse.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

**[0015]** A more complete appreciation of the invention, and many of the attendant advantages thereof, will be readily apparent as the same becomes better understood by reference to the following detailed description when considered in conjunction with the accompanying drawings, in which like reference symbols indicate the same or similar components, wherein:

**[0016]** FIG. 1 is a graph illustrating variations of data programming times versus gray levels to be written in a light emitting display device;

**[0017]** FIG. 2 is a simplified plan view of a light emitting display according to a first exemplary embodiment of the present invention;

**[0018]** FIG. 3 is a simplified circuit diagram of a pixel circuit in a light emitting display according to the first exemplary embodiment of the present invention;

**[0019]** FIG. 4 is a driving timing diagram of a light emitting display according to the first exemplary embodiment of the present invention;

[0020] FIG. 5A shows a current supply state in the precharging stage;

[0021] FIG. 5B shows a current supply state in the data programming stage;

[0022] FIG. 6 shows a scan driver in a light emitting display according to a second exemplary embodiment of the present invention;

[0023] FIG. 7 is a signal timing diagram of a scan driver according to a third exemplary embodiment of the present invention;

[0024] FIG. 8A is a simplified circuit diagram of a first shift register in the scan driver of FIG. 6;

[0025] FIG. 8B is a simplified diagram of a flip-flop used in the shift register in FIG. 8A;

[0026] FIG. 9 is a timing diagram for an output signal of the flip-flop and an output signal of a NOR gate used in the shift register in FIG. 8A;

[0027] FIG. 10 is a simplified circuit diagram of a second shift register in the scan driver of FIG. 6;

[0028] FIG. 11 is a simplified circuit diagram of a first shift register in the scan driver according to the third exemplary embodiment of the present invention;

[0029] FIG. 12 is a signal timing diagram of the scan driver according to the third exemplary embodiment of the present invention;

[0030] FIGS. 13A and 13B show respective simplified diagrams of the flip-flops used in the shift register of FIG. 11;

[0031] FIG. 14 shows a scan driver according to a fourth exemplary embodiment of the present invention;

[0032] FIG. 15 is a signal timing diagram of the scan driver according to the fourth exemplary embodiment of the present invention;

[0033] FIG. 16 is a simplified circuit diagram of a first shift register in the scan driver of FIG. 14;

[0034] FIG. 17 is a simplified circuit diagram of a first shift register in the scan driver according to a fifth exemplary embodiment of the present invention;

[0035] FIG. 18 is a signal timing diagram of the scan driver according to the fifth exemplary embodiment of the present invention;

[0036] FIG. 19 shows a scan driver according to a sixth exemplary embodiment of the present invention;

[0037] FIG. 20 is a signal timing diagram of the scan driver according to the sixth exemplary embodiment of the present invention;

[0038] FIG. 21 is a simplified circuit diagram of a first shift register in the scan driver of FIG. 19;

[0039] FIG. 22 is a signal timing diagram of a scan driver according to a seventh exemplary embodiment of the present invention;

[0040] FIG. 23 is a simplified circuit diagram of a first shift register in a scan driver according to an eighth exemplary embodiment of the present invention;

[0041] FIG. 24 is a signal timing diagram of the scan driver according to the eighth exemplary embodiment of the present invention; and

[0042] FIG. 25 is a signal timing diagram of a scan

driver according to a ninth exemplary embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

[0043] FIG. 1 is a graph illustrating variations of data programming times versus gray levels to be written in a light emitting display device.

[0044] The time  $t_1$  to  $t_7$  in FIG. 1 represents the data programming times, and the gray lines (e.g., gray 00 through gray 63) on the right of the graph indicate gray levels of the data programmed to the pixel circuit coupled to the previous pixel line.

[0045] For example, when the gray level of the data programmed to the pixel circuit coupled to the previous pixel line is "8" and the gray level of the data to be programmed to the pixel circuit coupled to the current pixel line is 8 (i.e., a point where a curve meets the horizontal axis), the time needed for data programming is almost "0" since there is no difference between the voltage state of the data line and the target voltage.

[0046] By contrast, the time needed for data programming increases as the difference between the voltage state of the data line and the target voltage increases because the gray level of the data to be currently programmed becomes further away from the gray level of 8.

[0047] Also, the time needed for data programming is inversely proportional to the magnitude of the data current for driving the data line. As such, when the gray level is to be lowered, the data current for driving the data line is reduced, and hence, the data programming time is increased. That is, as can be derived from FIG. 1, when the gray level is lowered (e.g., to near the black level), the data voltage is changed so that it has a large voltage range with a low driving current, and the data programming time is increased.

[0048] In the following detailed description, only certain exemplary embodiments of the present invention are shown and described, simply by way of illustration. As those skilled in the art will realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

[0049] In the context of the present application, to couple one thing to another refers to directly couple a first thing to a second thing, or to couple a first thing to a second thing with a third thing provided therebetween. In addition, to clarify the present invention as shown in the drawings, certain components which are not described in the specification may be omitted, and like reference numerals indicate like components.

[0050] Hereinafter, a light emitting display and a driving method thereof according to exemplary embodiments of the present invention will be described in detail with reference to drawings. In exemplary embodiments of the present invention, the light emitting display is de-

scribed as an organic light emitting diode (OLED). However, the present invention should not be limited to the OLED display.

**[0051]** First, a light emitting display according to a first exemplary embodiment of the present invention is described in detail with reference to FIG. 2, which is a simplified plan view of a light emitting display according to a first exemplary embodiment of the present invention.

**[0052]** As shown in FIG. 2, the light emitting display according to the first exemplary embodiment includes display panel 100, data driver 200, scan driver 300, emission control driver 400, and precharge unit 500.

**[0053]** Display panel 100 includes a plurality of data lines  $Y_1$  to  $Y_n$  arranged in a column direction, a plurality of selection scan lines  $X_1$  to  $X_m$  and a plurality of emitting scan lines  $Z_1$  to  $Z_m$  arranged in a row direction, and a plurality of pixel circuits 110. The selection scan lines  $X_1$  to  $X_m$  transmit selection signals for selecting pixels, and the emitting scan lines  $Z_1$  to  $Z_m$  transmit emit signals for controlling an emit period of an organic light emitting element (or OLED). Pixel circuits 110 are formed at pixel areas defined by data lines  $Y_1$  to  $Y_n$  and selection scan lines  $X_1$  to  $X_m$ .

**[0054]** Data driver 200 applies a data current  $I_{data}$  to the data lines  $Y_1$  to  $Y_n$ . Furthermore, data driver 200 applies a precharge current  $NI_{data}$  to the data lines  $Y_1$  to  $Y_n$ , the precharge current  $NI_{data}$  being  $N$  times the data current  $I_{data}$ . Thus, data driver 200 includes a first current source for generating the data current  $I_{data}$  and a second current source for generating the precharge current  $NI_{data}$ . The precharge current  $NI_{data}$  can be generated from the data current  $I_{data}$  by a current mirror circuit or the like. The methods for generating the precharge current are well known to a person of ordinary skill in the art, and thus a detailed description of the method for generating the precharge current is not given. However, data driver 200 can alternatively supply the precharge current  $NI_{data}$  and the data current  $I_{data}$  to the data lines according to a control signal applied from an external controller (not shown).

**[0055]** Scan driver 300 sequentially applies the selection signals to the selection scan lines  $X_1$  to  $X_m$  so as to select pixel circuits 110. Emit control driver 400 sequentially applies the emit signals to the emitting scan lines  $Z_1$  to  $Z_m$  so as to control light emission of the pixel circuits 110.

**[0056]** Scan driver 300, emit control driver 400 and/or data driver 200 can be electronically coupled to the display panel 100, or can be installed as a chip by means of a tape carrier package (TCP) attached and electronically coupled to display panel 100. They can also be installed as a chip on a flexible printed circuit (FPC) or as a film attached and electronically coupled to display panel 100. In addition, they can be directly installed on a glass substrate of the display panel, or they can also be replaced by a driving circuit on the same layer as that of signal lines, data lines, and thin film transistors (TFTs).

**[0057]** In the first exemplary embodiment of the present invention, the precharge current  $NI_{data}$  corresponding to  $N$  times the data current  $I_{data}$  is applied to a data line  $Y_j$ , before the data current  $I_{data}$  is applied to a pixel circuit 110 coupled to the data line  $Y_j$  and a selection scan line  $X_i$ . Then, when the precharge current  $NI_{data}$  is applied to the data line  $Y_j$ , a low level selection signal is applied to the pixel circuit 110 coupled to the selection scan line  $X_i$  and to  $N-1$  selection scan lines  $X_{i+1}$  to  $X_{i+N-1}$  of the pixel circuit 110 adjacent to the pixel circuit in the column direction. Then, only the selection signal applied to the selection scan line  $X_i$  is maintained at a low level, and the data current  $I_{data}$  is applied to a data line  $Y_j$ . As such, the data line  $Y_j$  is quickly precharged by the precharge current  $NI_{data}$ , which is larger than the data current  $I_{data}$ , and then the data current  $I_{data}$  is applied to the data line  $Y_j$ . Thus, a voltage corresponding to the data current  $I_{data}$  is quickly supplied to and charges the pixel circuit 110.

**[0058]** Hereinafter, referring to FIGs. 3, 4, 5A, and 5B, the operation of the light emitting display according to the first exemplary embodiment of the present invention will be described in detail. For ease of description,  $N$  is assumed to be 5, that is, the precharge current is assumed to be 5 times that of the data current.

**[0059]** First, pixel circuit 110 of the light emitting display according to the first exemplary embodiment of the present invention is described in detail with reference to FIG. 3.

**[0060]** FIG. 3 is a simplified circuit diagram of a pixel circuit in a light emitting display according to the first exemplary embodiment of the present invention. FIG. 3 shows the pixel circuit coupled to the  $j$ th data line  $Y_j$ , the  $i$ th selection scan line  $X_i$ , and emitting scan line  $Z_i$ .

**[0061]** As shown, pixel circuit 110 according to the first exemplary embodiment of the present invention includes organic light emitting element OLED, transistors T1, T2, T3 and T4, and capacitor C. Transistors T1, T2, T3, and T4 are shown as PMOS transistors in FIG. 3, but transistor types of the present invention are not restricted to PMOS transistors. The transistors can be TFTs which have a gate electrode, a drain electrode, and a source electrode formed on the glass substrate of display panel 100 as a control electrode and two main electrodes, respectively.

**[0062]** In detail, the three electrodes (or terminals) of transistor T1 are respectively coupled to the selection scan line  $X_i$ , data line  $Y_j$ , and the gate of transistor T3. Transistor T1 transmits the data current  $I_{data}$  provided by data line  $Y_j$  to the gate of transistor T3 in response to the selection signal provided by selection scan line  $X_i$ . The source of transistor T3 is coupled to the supply voltage VDD, and capacitor C is coupled between the gate and source of transistor T3. Transistor T2 is coupled between the drain of transistor T3 and data lines  $Y_j$ , and transistors T1 and T2 diode-connect transistor T3 in response to the selection signal provided by selection scan lines  $X_i$ . Transistors T1 and T2 may be di-

rectly connected between the gate and drain of transistor T3.

**[0063]** At this point, data current  $I_{data}$  is applied to data line  $Y_i$ , and selection signal (select[1] in FIG. 4) provided by selection scan line  $X_i$  is converted to low level. Transistors T1 and T2 are turned on, and transistor T3 is diode-connected. Then, data current  $I_{data}$  is applied to and charges capacitor C, the gate voltage potential of transistor T3 is lowered, and current flows from the source to the drain of transistor T3. When the voltage charge on capacitor C is increased, and the drain current of transistor T3 increases so as to be the same as data current  $I_{data}$ , the charge on capacitor C is stopped, and the voltage charge on capacitor C is stabilized. Thus, a voltage corresponding to data current  $I_{data}$  provided by data line  $Y_j$  is charged on capacitor C.

**[0064]** Next, the selection signal (select [1] in FIG. 4) provided by the selection scan line  $X_i$  is converted to a high level, and the emit signal (emit[1] in FIG. 4) provided by the emitting scan line  $Z_i$  is converted to a low level. Then, transistors T1 and T2 are turned off, transistor T4 coupled between transistor T3 and the organic light emitting element OLED is turned on, and the current provided by transistor T3 is transferred to the organic light emitting element OLED. The cathode of the organic light emitting element OLED is coupled to a voltage source VSS which is lower than a supply voltage VDD, and the organic light emitting element OLED emits light in response to the current supplied via transistor T4. The current  $I_{OLED}$  transmitted to the organic light emitting element OLED can be given in Equation 1 according to the voltage charged on capacitor C connected to transistor T3.

Equation 1

$$I_{OLED} = \frac{\beta}{2} (V_{GS} - V_{TH})^2 = I_{data}$$

where  $V_{GS}$  is the voltage between the gate and the source of transistor T3,  $V_{TH}$  is a threshold voltage at transistor T3, and  $\beta$  is a constant.

**[0065]** Next, referring to FIGs. 4, 5A, and 5B, the operation of the light emitting display according to the first exemplary embodiment of the present invention will be further described in detail.

**[0066]** FIG. 4 is a driving timing diagram of a light emitting display according to the first exemplary embodiment of the present invention; FIG. 5A shows a current supply state in the precharging stage; and FIG. 5B shows a current supply state in the data programming stage. In FIGs. 5A and 5B, five pixel circuits coupled to the first selection scan line thru the fifth selection scan line  $X_1$  to  $X_5$  and the five emitting scan lines  $Z_1$  to  $Z_5$  are shown for convenience. In FIG. 4, and in FIGs. 5A and 5B, select[i] indicates a selection signal applied to the selection scan line  $X_i$ , and emit[i] indicates an emit signal applied to the emitting scan line  $Z_i$ . Reference nu-

merals  $X_i$  and  $Z_i$  corresponding to the selection scan lines and the emitting scan lines are omitted.

**[0067]** As shown in FIG. 4, when the data is programmed in the pixel circuit coupled to the first selection scan line  $X_1$ , low level selection signals select[1] to select [5] are supplied to the first thru fifth selection scan lines  $X_1$  to  $X_5$ , respectively. At the same time, data driver 200 applies the precharge current  $5I_{data}$  to the data line  $Y_j$  so as to perform a precharge operation during a precharge period  $T_p$ .

**[0068]** Transistors T1 and T2 of the pixel circuits 110 coupled to the selection scan lines  $X_1$  to  $X_5$  are turned on in response to the low level selection signals select [1] to select[5], and thus transistor T3 assumes a diode-connected state. As such, as shown in FIG. 5A, the precharge current  $5I_{data}$  flows on the data line  $Y_j$ . At this point, when the ratio W/L (hereinafter, transistor size) of the channel width W and channel length L of transistors T3 in the five pixel circuits are the same, 1/5 of the precharge current  $5I_{data}$  provided by the data line  $Y_j$  is respectively supplied to the five pixel circuits. That is, the data current is supplied to each of the five pixel circuits. Then, the voltage  $V_{GS}$  of Equation 1 is charged on capacitor C. That is, the precharge voltage from the gate voltage  $V_G$  to the gate-source voltage  $V_{GS}$  is applied to the data lines  $Y_j$ . However, when the precharge period  $T_p$  is short, the precharge voltage may not achieve a suitable voltage which should be applied to the data lines  $Y_j$  by the data current  $I_{data}$ . However, the precharge voltage  $5I_{data}$  is larger than the data current  $I_{data}$ , and thus a voltage corresponding to the data current  $I_{data}$  can be applied to the data line  $Y_j$  even though the precharge period  $T_p$  is short.

**[0069]** Next, as shown in FIG. 4, the selection signal select[1] applied to the first selection scan line  $X_1$  is maintained at a low level, but the other selection signals select[2] to select[5] are changed to the high level. At the same time, data driver 200 applies the data current, the 1/5 of the precharge current  $5I_{data}$ , to the data line  $Y_j$ . Then, as shown in FIG. 5B, transistors T1 and T2 coupled to the first selection scan line  $X_1$  are turned on, and the data current  $I_{data}$  is transmitted to transistor T3. Thus, a voltage corresponding to the data current  $I_{data}$  is charged on capacitor C of the pixel circuit coupled to the first selection scan line  $X_1$  so as to perform the data programming operation. At this point, the precharge voltage (the voltage corresponding to the data current  $I_{data}$ ) has been applied to the data line  $Y_j$  by the previous precharge operation, and thus a voltage corresponding to the data current  $I_{data}$  can be quickly charged on capacitor C.

**[0070]** Then, when the data programming operation is completed, the selection signal select[1] is turned to a high level, and transistor T4 is turned on by the low level of the emit signal emit[1] applied by the emitting scan line  $Z_1$ . Then, the current  $I_{OLED}$  provided by transistor T3 is supplied to the organic light emitting element OLED through transistor T4, and the organic light emit-

ting element OLED emits light corresponding to the current  $I_{\text{OLED}}$ .

**[0071]** As such, when the emit operation of the pixel circuit coupled to the first selection scan line  $X_1$  is performed, the low levels of selection signals select[2] to select[6] are applied to selection scan lines  $X_2$  to  $X_6$ , respectively. The precharge current  $5I_{\text{data}}$  equal to 5 times the data current  $I_{\text{data}}$ , and corresponding to the pixel circuit coupled to the selection scan line  $X_2$ , is applied to the data line  $Y_j$  so as to perform a precharge operation on the pixel circuit coupled to the second selection scan line  $X_2$ . Then, the selection signals select [3] to select[6] are converted to a high level after the precharge operation, and a data current  $I_{\text{data}}$  corresponding to the pixel circuit coupled to the selection scan line  $X_2$  is applied to the data line  $Y_j$  so as to perform the data programming operation on the pixel circuit coupled to the second selection scan line  $X_2$ .

**[0072]** As such, in the first exemplary embodiment of the present invention, before data is programmed in a pixel circuit coupled to an  $i$ th selection scan line  $X_i$ , a precharge current  $N I_{\text{data}}$  corresponding to 5 times the data current  $I_{\text{data}}$  is applied to the pixel circuit when the selection signal is applied to the  $i$ th to  $(i+1)$ th selection scan lines  $X_i$  to  $X_{i+N-1}$ . Then, if the sizes of transistors T3 in pixel circuits arranged in the column direction are the same, a current corresponding to  $1/N$  of the precharge current  $N I_{\text{data}}$  is supplied to  $N$  pixel circuits coupled to the  $i$ th to  $(i+1)$ th selection scan lines  $X_i$  to  $X_{i+N-1}$  so as to perform a precharge operation. Next, when the selection signal of the  $i$ th selection scan line  $X_i$  is maintained at a low level, the selection signals of the  $(i+1)$ th to  $(i+1)$ th selection scan lines  $X_i$  to  $X_{i+N-1}$  turn to a high level, while the data current  $I_{\text{data}}$  is applied to the data line  $Y_j$  so as to perform the data programming operation.

**[0073]** As such, the first exemplary embodiment of the present invention can program data in the pixel circuit by precharging a data line by means of a precharge current which is larger than the data current before the data is programmed. The data programming can be achieved in a predetermined period of time.

**[0074]** Hereinafter, with respect to the selection signal select[i] of FIG. 4, "precharge pulse" means a pulse that is of a low level only during a precharge period, and "selection pulse" means a pulse that is of a low level during a precharge period and a data programming period. Then, as shown in FIG. 4, a selection signal select[i] applied to the selection scan line  $X_i$  has one selection pulse and at least one precharge pulse per cycle. In the selection signal select[i], the interval of start time points of two adjacent precharge pulses is the same as the interval of starting points of a selection pulse and a precharge pulse adjacent to the selection pulse. Furthermore, the selection signal select[i] has a number of precharge pulses corresponding to the number of pixels used in the precharge, excluding the pixel to which data is programmed. In addition, the precharge period  $T_p$  is the same as the width of the precharge pulse.

**[0075]** Hereinafter, a driver for generating the above driving waveform is described in detail with reference to FIG. 6 thru FIG. 25.

**[0076]** In the exemplary embodiments of the present invention, a selection signal is generated by combining an output signal from a shift register for generating a precharge pulse and an output signal from a shift register for generating a selection pulse. Hereinafter, a particular shift register for generating the precharge pulse is described in detail.

**[0077]** Furthermore, in exemplary embodiments of the present invention, the number of selection scan lines  $X_1$  to  $X_m$  is  $m$ , and a selection signal select[i] with four precharge pulses is described, if not particularly mentioned to the contrary. That is, four neighboring pixel circuits are used in the precharge of a pixel circuit for data programming.

**[0078]** FIG. 6 shows a scan driver in a light emitting display according to a second exemplary embodiment of the present invention, and FIG. 7 is a signal timing diagram of a scan driver according to a third exemplary embodiment of the present invention.

**[0079]** As shown in FIG. 6, scan driver 300 of the second exemplary embodiment of the present invention includes two shift registers 310 and 320, and  $m$  NOR gates NOR11 to NOR1 $m$ .

**[0080]** As shown in FIG. 6 and FIG. 7, shift register 310 receives clock signal VCLK11 and a starting signal VSP11, shifts output signals out11[1] to out11[4 $m$ -3] by half of a cycle of clock signal VCLK11, and sequentially provides the shifted output signals. The output signal out11[i] has four high level pulses in one cycle. The width of the high level pulse is the same as the half clock cycle of clock signal VCLK11, and the cycle of the high level pulse is twice the clock cycle of clock signal VCLK11. At this point, the precharge period  $T_p$  is determined by the width of the high level pulse. In addition, the  $(4i-3)$ th output signal out11[4 $i$ -3] of the output signals out11[1] to out11[4 $m$ -3] becomes an input signal scan11[i] of the  $i$ th NOR gate NOR $_{1i}$ ,  $i$  being an integer from 1 to  $m$ .

**[0081]** Shift register 320 receives clock signal VCLK12 and starting signal VSP12, shifts output signals scan12[1] to scan12[ $m$ ] having one high level pulse by a half of a clock cycle of clock signal VCLK12, and sequentially provides the shifted output signals. The width of the high level pulse of the output signal scan12[i] is the same as the half clock cycle of clock signal VCLK12, and the clock cycle of clock signal VCLK12 is four times the clock cycle of clock signal VCLK11. A start time point of the high level pulse in the output signal scan12[i] is half of a clock cycle of clock signal VCLK12 away from a start time point of the last high level pulse in the output signal scan11[i].

**[0082]** NOR gate NOR $_{1i}$  performs a NOR operation on the output signal scan11[i] of shift register 310 and the output signal scan12[i] of shift register 320, and outputs the selection signal select[i]. The output signal select[i] of NOR gate NOR $_{1i}$  has a low level by virtue of the

NOR operation when at least one of two output signals scan11[i] and scan12[i] has a high level. Thus, the output signal select[i] has four low level pulses (precharge pulse) and then one low level pulse (selection pulse) in one cycle as shown in FIG. 7. Thus, as shown in FIG. 4 and FIG. 7, the selection signal select[i] applied to the selection scan line  $X_i$  can be generated as the output signal of the NOR gate NOR<sub>1j</sub>.

**[0083]** Next, shift registers 310 and 320 for generating the output signals out11[i], scan11[i], and scan 12[i] explained in FIG. 6 and FIG. 7 are described with reference to FIGs. 8A to 13B.

**[0084]** FIG. 8A is a simplified circuit diagram of a first shift register in the scan drive of FIG. 6, FIG. 8B is a simplified diagram of a flip-flop used in the shift register in FIG. 8A, and FIG. 9 is a timing diagram for an output signal of the flip-flop and an output signal of a NOR gate used in the shift register in FIG. 8A. More specifically, FIG. 8A is a simplified circuit diagram of shift register 310 in the scan driver of FIG. 6; FIG. 8B is a simplified diagram of a flip-flop used in the shift register in FIG. 8A; and FIG. 9 is a timing diagram for an output signal of the flip-flop and an output signal of the NOR gate used in the shift register of FIG. 8A. In FIGs. 8A and 8B, VCLK11b indicates an inverted clock signal VCLK11. However, VCLK11b is omitted in the signal timing diagram of FIG. 7 and FIG. 9.

**[0085]** As shown in FIG. 8A, shift register 310 includes (4m-2) flip-flops FF<sub>11</sub> to FF<sub>1(4m-2)</sub> and (4m-3) NOR gates NOR<sub>21</sub> to NOR<sub>2(4m-3)</sub>. The output signals of each NOR gate NOR<sub>2k</sub> become the output signals out11[k] of shift register 310, k being an integer from 1 to (4m-3).

**[0086]** In FIG. 8A, the input signal of the first flip-flop FF<sub>11</sub> is the start signal VSP11 of FIG. 7 and FIG. 9, and the output signal SR<sub>k</sub> of the kth flip-flop FF<sub>1k</sub> is the input signal of the (k+1)th flip-flop FF<sub>1(k+1)</sub>. The kth NOR gate NOR2k performs a NOR operation on the output signal SR<sub>1k</sub> of the kth flip-flop FF<sub>1k</sub> and the output signal SR<sub>1(R+1)</sub> of the (k+1)th flip-flop FF<sub>1(R+1)</sub> so as to generate the input signal out11[k].

**[0087]** The flip-flop FF<sub>1k</sub> outputs input signal in as it is inputted when clock clk is at a high level, but the flip-flop FF<sub>1k</sub> latches the input signal in inputted when the clock clk was at a high level, and outputs the resultant signal. Furthermore, the clock clk is inverted in the two adjacent flip-flops FF<sub>1k</sub> and FF<sub>1(k+1)</sub>, and output signal SR<sub>1(R+1)</sub> of the flip-flop FF<sub>1(k+1)</sub> is the output signal SR<sub>1k</sub> of the flip-flop FF<sub>1k</sub> shifted by half of a clock cycle of clock signal VCLK1. That is, the clock signals VCLK11 and VCLK11b are inputted to the two flip-flops FF<sub>1k</sub> and FF<sub>1(k+1)</sub> in the opposite direction.

**[0088]** In detail, in FIG.8A, the flip-flop FF<sub>1k</sub> which is located at an odd-numbered position in the column direction receives the clocks VCLK11 and VCLK11b as inner clocks clk and clkb, respectively. The flip-flop FF<sub>1k</sub> which is located at an even-numbered position in the column direction receives the clocks VCLK11 and VCLK11b as inner clocks clkb and clk, respectively. The

starting signal VSP11, which is an input signal in of flip-flop FF<sub>11</sub>, has four low level pulses in one cycle. The low level pulse corresponds to a high level of the clock VCLK11 per two clocks VCLK11 of the interval. Then, the flip-flops FF<sub>11</sub> to FF<sub>1(4m-2)</sub> can shift output signals SR<sub>1</sub> to SR<sub>4m-2</sub> having four low level pulses per cycle by half of a clock cycle of clock VCLK11, and sequentially output the output signals.

**[0089]** The kth NOR gate NOR2k performs a NOR operation on output signals SR<sub>k</sub> and SR<sub>k+1</sub> of the flip-flops FF<sub>1k</sub> and FF<sub>1(k+1)</sub>, respectively, and thus the kth NOR gate NOR2k outputs a high level pulse when both output signals SR<sub>k</sub> and SR<sub>k+1</sub> are at a low level. The output signal SR<sub>k+1</sub> is the output signal SR<sub>k</sub> shifted by half of a clock cycle of clock VCLK11. Thus, as shown in FIG. 9, the output signal out11[k] of the NOR gate NOR2k has a high level pulse in half of a cycle of clock VCLK11. The output signal out11[k+1] of NOR gate NOR<sub>2(k+1)</sub> is the output signal out11[k] of NOR gate NOR2k shifted by half of a clock cycle of clock VCLK11. The (4i-3)th output signal out11[4i-3] of output signals out11[1] to out11[4m-3] of NOR gates NOR21 to NOR2(4m-3) is selected as a final output signal scan11 [i] of shift register 310, i being an integer from 1 to m.

**[0090]** Next, referring to FIG. 8B, one example of flip-flop FF<sub>1k</sub> used in shift register 310 of FIG. 8A is described.

**[0091]** As shown in FIG. 8B, the flip-flop FF<sub>1k</sub> includes clock inverter 311a located at the input terminal, inverter 311b forming a latch, and clock inverter 311c. When clock clk is at a high level, clock inverter 311a inverts the input signal in and outputs the resultant signal, while inverter 311b inverts the output signal of clock inverter 311a and outputs the resultant signal. When clock clk is at a low level, the output of clock inverter 311a is cut off, the output of inverter 311b is inputted to clock inverter 311c, and the output of clock inverter 311c is inputted to inverter 311b to form a latch. Then, the output signal of inverter 311b becomes the output signal of the flip-flop FF<sub>1k</sub>. As such, the flip-flop FF<sub>1k</sub> outputs the input signal in, as it is inputted when clock clk is at a high level, and the flip-flop FF<sub>1k</sub> latches the input signal in, inputted when the clock clk was at a high level, and outputs the resultant signal.

**[0092]** Next, the construction and operation of shift register 320 of FIG. 6 is described with reference to FIG. 10, which is a simplified circuit diagram of a second shift register in the scan driver of FIG. 6. FIG. 10 shows a simplified circuit diagram of shift register 320. In FIG.10, VCLK12b indicates an inverted signal of clock VCLK12. However, VCLK11b is omitted in the signal timing diagram of the FIG. 7.

**[0093]** As shown in FIG. 7, shift register 320 shifts a high level pulse by half of a clock cycle of clock VCLK12 and outputs the resultant signal, as does shift register 310. The high level pulse has a width of half of a clock cycle of clock VCLK12. Thus, a shift register having the same function as the shift register 310 can be used.

Hereinafter, the difference between the two shift registers 310 and 320 is described. As shown in FIG. 7, the clock cycle of clock VCLK12 is four times the clock cycle of clock VCLK11.

**[0094]** As shown in FIG. 10, shift register 320 has the same construction as the shift register 310, excluding the number of flip-flops and NOR gates, as well as the start signal and clock used.

**[0095]** In detail, shift register 320 includes  $(m+1)$  flip-flops  $FF_{21}$  to  $FF_{2(m+1)}$ , and  $m$  NOR gates  $NOR_{31}$  to  $NOR_{3m}$ . An output signal of each NOR gate  $NOR_{3i}$  becomes the output signal  $scan12[i]$  of shift register 320,  $i$  being an integer from 1 to  $m$ . An input signal of a first flip-flop  $FF_{21}$  is a starting signal VSP12 of FIG. 7, and an output signal of the  $i$ th flip-flop  $FF_{2i}$  becomes the input signal of the  $(i+1)$ th flip-flop  $FF_{2(i+1)}$ . The  $i$ th NOR gate  $NOR_{3i}$  performs a NOR operation on the output signal of the  $i$ th flip-flop  $FF_{2i}$  and the output signal of  $(i+1)$ th flip-flop  $FF_{2(i+1)}$ , and outputs the resultant signal  $scan12[i]$ .

**[0096]** The flip-flop  $FF_{2i}$  which is located at an odd-numbered position in the column direction in FIG. 10 receives the clocks VCLK12 and VCLK12b as inner clocks  $clk$  and  $clkb$ , respectively. The flip-flop  $FF_{2i}$  which is located at an even-numbered position in the column direction receives the inverted clocks VCLK12 and VCLK12b as inner clocks  $clk$  and  $clkb$ , respectively. The starting signal VSP12 is established so as to have one low-level pulse when the clock VCLK12 is at a high level. Furthermore, a start time point of the high level pulse in the output signal  $scan12[i]$  is established so as to be half of a clock cycle of clock VCLK12 away from a start time point of the last high level pulse in the output signal  $scan11[i]$  of shift register 310. As such, shift register 320 shifts output signals  $scan12[1]$  to  $scan12[m]$  by half of a clock cycle of clock VCLK12 and outputs the resultant signal. The output signals  $scan12[1]$  to  $scan12[m]$  have a high level pulse, the cycle of which is half of a clock cycle of clock VCLK12.

**[0097]** The  $i$ th NOR gate  $NOR_{1i}$  of scan driver 300 performs a NOR operation on the  $i$ th final output signal  $scan11[i]$  and the  $i$ th output signal  $scan12[i]$  of shift register 320, and outputs the resultant signal. Thus, the selection signal  $select[i]$  may include four precharge pulses and a selection pulse.

**[0098]** As such, in FIG. 6 thru FIG. 10, the width of the selection pulse is four times the width of a precharge pulse. However, scan driver 300 of FIG. 6 thru FIG. 10 may generate selection signals having different precharge pulse widths.

**[0099]** As mentioned above, the width of the precharge pulse is determined by the output of the flip-flop  $FF_{1k}$ , and thus a low level pulse of the output signal  $SR_k$  of the flip-flop  $FF_{1k}$  is assumed to have the narrowest width so as to lower the frequency of the clock VCLK11. That is, the width of the low level pulse of the output signal  $SR_k$  of the flip-flop  $FF_{1k}$  is assumed to be the same as the width of one clock cycle VCLK11.

**[0100]** Under the above assumption, a cycle of a low level pulse of the output signal  $SR_k$  of the flip-flop  $FF_{1k}$  is always  $n$  times the width,  $n$  being an integer of more than 2. Then, a cycle of a high level pulse in the output signal  $out11[k]$  of the NOR gate  $NOR_{2k}$  becomes  $2n$  times the width (that is, an even number of times more than 4). Thus, the width of the precharge pulse in the output signal  $scan11[i]$  is always  $1/2n$  times the cycle. When a clock cycle of clock VCLK12 is  $2n$  times a clock cycle of clock VCLK11, the width of selection pulse can be  $2n$  times the width of the precharge pulse, and the interval by which the selection pulse is shifted may be the same as the cycle of the precharge pulse. The output signal  $out11[k]$  of shift register 310 is shifted by half of a clock cycle of clock VCLK11 and is outputted. Thus, the total  $[2n \times i - (2n - 1)]$ th output signal  $out[2n \times i - (2n - 1)]$  is selected as the final output signal  $scan11[i]$  of shift register 310.

**[0101]** Next, an exemplary embodiment wherein the width of a selection pulse may be an even number of times, or less than at most 3 times, the width of a precharge pulse is described in detail with reference to FIG. 11 and FIG. 12.

**[0102]** FIG. 11 is a simplified circuit diagram of a first shift register in the scan driver according to the third exemplary embodiment of the present invention, and FIG. 12 is a signal timing diagram of the scan driver according to the third exemplary embodiment of the present invention. More specifically, FIG. 11 shows a simplified circuit diagram of shift register 310' according to a third exemplary embodiment of the present invention, and FIG. 12 shows a signal timing diagram of a scan driver according to the third exemplary embodiment. In FIG. 11, VCLK11b' indicates an inverted signal of clock VCLK11'. However, VCLK11b' is omitted in the signal timing diagram of FIG. 12. Furthermore, for ease of description, a cycle of the precharge pulse is three times the width in the third exemplary embodiment of the present invention. The construction and operation of shift register 320 and NOR gates  $NOR_{11}$  to  $NOR_{1m}$  may be the same as those in the second exemplary embodiment, and thus the descriptions for those are omitted here.

**[0103]** As shown in FIG. 11, shift register 310' includes  $(3m-2)$  flip-flops  $FF_{31}$  to  $FF_{3(3m-2)}$ . Output signals of each of the flip-flops  $FF_{31}$  to  $FF_{3(3m-2)}$  become the output signals  $out11[1]'$  to  $out11[3m-2]'$  of shift register 310'.

**[0104]** The flip-flop  $FF_{3k}$  receives the clock signals VCLK11' and VCLK11b' as inner clocks  $clk$  and  $clkb$ , respectively. The flip-flop  $FF_{3k}$  receives an input signal when clock  $clk$  is at a low level, while the flip-flop  $FF_{3k}$  outputs an input signal latched in a previous clock  $clk$  cycle. The flip-flop  $FF_{3k}$  latches the signal inputted at a low level, and outputs the resultant signal when clock  $clk$  is at a high level. As a result, the flip-flop  $FF_{3k}$  delays the signal inputted at a low level of clock  $clk$  by half of a clock cycle of clock  $clk$ , and outputs the resultant signal during one clock cycle of clock  $clk$ .

**[0105]** As shown in FIG. 12, the output signal  $out11$

[1]' of the flip-flop FF31 has four high level pulses per cycle. The width of the high level pulse is the same as a clock cycle of clock VCLK11', and the cycle is three times the width. A start signal VSP11', which is an input signal in of the flip-flop FF31, has three high level pulses per cycle. This high level pulse corresponds to a low level of clock VCLK11' per three clocks VCLK11'. Then, the flip-flop FF<sub>3k</sub> shifts the output signal out11[k]' having four high level pulses per cycle by one clock cycle of clock VCLK11', and sequentially outputs the resultant signals. The (3i-2)th output signal out11[3i-2]' of output signals out11[k]' of the flip-flop FF<sub>3k</sub> is selected as the final output signal scan11[i]', i being an integer from 1 to m.

**[0106]** As such, when the width of the high level pulse is established to be one clock cycle of clock VCLK11' in the output signal scan11[i]' of shift register 310', a cycle of the high level pulse can be established to be more than twice the width of the high level pulse (three times in FIG. 12). Since the high level pulse corresponds to a precharge pulse in the output signal scan11[i]', the width T<sub>p</sub> of the precharge pulse is always 1/n times (1/3 times in FIG. 11) the cycle, n being an integer of more than 2. When a clock cycle of clock VCLK12 of the shift register 320 is established to be 2n times (six times in FIG. 11) the clock VCLK11' of shift register 310', the width of the selection pulse may be n times (three times in FIG. 11) the width of the precharge pulse, while the selection pulse may be shifted by an interval of the cycle of the precharge pulse.

**[0107]** When a cycle of the high level pulse is n times the width in output signal out11[k]' of shift register 310', a total of [n×m-(n-1)] output signals out11[k]' are required in shift register 310'. The [n×i-(n-1)]th output signal out1[n×i-(n-1)]' of the latter output signals becomes the final output signal scan11[i]' of shift register 310'.

**[0108]** As such, when the cycle of the precharge pulse is established to be an odd number of times or less than 3 times the width, shift register 310' can be used according to the third exemplary embodiment. Shift register 310', according to the third exemplary embodiment, can be used when the cycle of the precharge pulse is an even number of times of more than four times the width. However, its construction becomes complicated and the frequency of the clock VCLK11' is increased in comparison with shift register 310 as described in the second exemplary embodiment.

**[0109]** Next, one example of a flip-flop used in the shift register of FIG. 11 is described with reference to FIGS. 13A and 13B.

**[0110]** FIGS. 13A and 13B show respective simplified diagrams of the flip-flops used in the shift register of FIG. 11. The flip-flop FF<sub>3k</sub> of FIG. 13A and FIG. 13B is formed as a master/slave type of latch. Clocks VCLK11' and VCLK11b' are inputted to inner clocks clk and clkb, respectively, of the flip-flop FF<sub>3k</sub>.

**[0111]** As shown in FIG. 13A, in master latch 313, PMOS transistor 313a located in the input terminal transfers the input signal in to inverter 313b in response

to a low level of one clock cycle of clock clk, and inverter 313b inverts the output signal of PMOS transistor 313a and outputs the resultant signal as an output signal of master latch 313. Furthermore, inverter 313c inverts the output signal of inverter 313b, and outputs the resultant signal. PMOS transistor 313d transfers the output signal of inverter 313c to inverter 313b in response to a low level of the clock clk, that is, a high level of one clock cycle clkb. In other words, master latch 313 inverts the input signal inputted during a low level of the clock clk, and outputs the resultant signal during one clock cycle of clock clk.

**[0112]** Next, in slave latch 314, PMOS transistor 314a located at the input terminal transfers the output signal of master latch 313 to inverter 314b in response to a low level of an inverted clock clkb, and inverter 314b inverts the output signal of PMOS transistor 314a and outputs the resultant signal as an output signal of slave latch 314. Furthermore, inverter 314c inverts the output signal of inverter 314b and outputs the resultant signal, and PMOS transistor 314d transfers the output signal of inverter 314c to inverter 314b in response to a low level of the clock clk. That is, slave latch 314 inverts the output signal of master latch 313 during a high level of the clock clk, and outputs the resultant signal during one clock cycle of clock VCLK1.

**[0113]** Therefore, the flip-flop FF<sub>3k</sub> of FIG. 13A may delay the input signal inputted during a low level of the clock VCLK11' by half of a clock cycle of clock VCLK11', and outputs the resultant signal during one clock cycle of clock VCLK11'.

**[0114]** In contrast with FIG. 13A, a master and a slave of the flip-flop FF<sub>3k</sub> may be formed with the same construction as the flip-flop of FIG. 8B, as shown in FIG. 13B. At this time, master latch 315 uses the clocks clk and clkb in a method contrasted with the flip-flop in FIG. 8B, and slave latch 316 uses the clocks clk and clkb in the same method as the flip-flop in FIG. 8B.

**[0115]** Master latch 315 outputs the input signal in inputted during a low level of the clock clk during one clock cycle, and slave latch 316 outputs the output signal of master latch 315 during a high level of the clock clk during one clock cycle of clock clk. Thus, the flip-flop FF<sub>3k</sub> of FIG. 13B delays the input signal in during a low level of the clock VCLK11' by half of a clock cycle of clock VCLK11', and outputs the resultant signal during one clock cycle of clock VCLK11'.

**[0116]** As explained above, scan drivers 300 according to the second and third exemplary embodiments shift a first output signal having a high level pulse corresponding to the precharge pulse by an interval corresponding to the width of the high level pulse, and sequentially output the resultant signal. Scan drivers 300 select a signal shifted by a predetermined interval corresponding to the cycle of the high level pulse of the first output signals, and use the signal as the precharge pulse.

**[0117]** FIG. 14 shows a scan driver according to a

fourth exemplary embodiment of the present invention, and FIG. 15 is a signal timing diagram of the scan driver according to the fourth exemplary embodiment of the present invention.

**[0118]** As shown in FIG. 14, scan driver 300' according to the fourth exemplary embodiment includes: three shift registers 330, 340, and 350; a plurality of XOR gates XOR<sub>11</sub> to XOR<sub>1m</sub>; and a plurality of NOR gates NOR<sub>41</sub> to NOR<sub>4m</sub>.

**[0119]** As shown in FIG. 14 and FIG. 15, shift register 330 receives a clock signal VCLK21 and a starting signal VSP21, shifts output signals out21[1] to out21[m] by one clock cycle of clock VCLK21, and sequentially outputs the resultant signal. The output signal out21[i] includes two high level pulses in one cycle. In the high level pulse, its width is the same as a period Tc1 of the clock VCLK21, and its period is twice the period Tc1 of the clock VCLK21, i being an integer from 1 to m.

**[0120]** Shift register 330 receives a clock signal VCLK22 and a starting signal VSP22, and shifts output signals out22[1] to out22[m] by one cycle of clock VCLK22, and sequentially outputs the resultant signal. The clock VCLK22 has the same cycle Tc1 as the clock VCLK21, and is the signal for the clock VCLK21 to be shifted by the precharge period Tp. The output signal out22[i] also has two high level pulses in one cycle. The width of the high level pulse is the same as the clock cycle of clock VCLK22, and the cycle of the high level pulse is twice the clock cycle of clock VCLK22, i being an integer from 1 to m. The output signal out22[i] of shift register 340 is the signal for the output signal out21[i] of shift register 330 to be shifted by the precharge period Tp.

**[0121]** Each XOR gate XOR<sub>1i</sub> performs an XOR operation on the output signal out21[i] of shift register 330 and the output signal out22[i] of shift register 340, and outputs the resultant output signal scan21[i]. The output signal scan21[i] assumes a high level when one of the two output signals out21[i] and out22[i] is at a high level by virtue of the XOR operation. Since the output signal out22[i] is the signal for the output signal out21[i] to be shifted by the precharge period Tp, the output signal scan21[i] has four high level pulses in one cycle when the precharge period Tp is shorter than one clock cycle of clock VCLK21. The output signal scan21[i+1] of the XOR gate XOR<sub>1(i+1)</sub> becomes a signal for the previous output signal scan21[i] to be shifted by one clock cycle of clock VCLK21, and three of four high level pulses of the output signal scan21[i+1] correspond to the high level pulses of the output signal scan21[i].

**[0122]** Shift register 350, like shift register 320 of FIG. 6, receives a clock signal VCLK23 and a starting signal VSP23, shifts the output signals scan22[1] to scan22[m] having the high level pulse by half of a clock cycle of clock VCLK23, and sequentially outputs the resultant signals. The clock cycle of clock VCLK23 is twice the clock cycle of clock VCLK21. The start time point of the high level pulse in the output signal scan22[i] is half of

a clock cycle of clock VCLK21 away from a start time point of the last high level pulse in the output signal scan21[i].

**[0123]** NOR gate NOR<sub>4i</sub> performs a NOR operation on the two output signals scan21[i] and scan22[i], and outputs a selection signal select[i] as does NOR gate NOR<sub>4i</sub> of FIG. 6. The width and cycle of the precharge pulse are the same as the width and cycle, respectively, of the high level pulse of the output signal scan21[i], and the width of the selection pulse is the same as the width of the high level pulse of the selection signal scan2[i]. Thus, as shown in FIG. 4 and FIG. 15, the selection signal select[i] applied to a selection scan line X<sub>i</sub> can be generated from the output signal of NOR gate NOR<sub>4i</sub>.

**[0124]** Next, shift registers 330, 340, and 350 for generating the output signals out21[i], out22[i], and scan22[i], respectively, explained in FIG. 14 and FIG. 15, are described in detail with reference to FIG. 16.

**[0125]** FIG. 16 is a simplified circuit diagram of a first shift register in the scan driver of FIG. 14. More specifically, FIG. 16 is a simplified circuit diagram of the shift register 330 of FIG. 14. VCLK21b indicates an inverted version of clock signal VCLK21 in FIG. 16. Shift registers 330 and 340 have the same types of output signals, and thus they may have the same construction or shift register. Thus, hereinafter, the shift register 330 is mainly described.

**[0126]** As shown in FIG. 16, shift register 330 of FIG. 16 includes m flip-flops FF<sub>41</sub> to FF<sub>4m</sub>, and the output signal of each flip-flop FF<sub>4i</sub> become the output signal out21[i] of shift register 330, i being an integer from 1 to m.

**[0127]** In FIG. 16, an input signal of a first flip-flop FF<sub>41</sub> is the starting signal VSP21 of FIG. 15, and an input signal in of the (i+1)th flip-flop FF<sub>4(i+1)</sub> is the output signal out21[i] of the ith flip-flop FF<sub>4i</sub>. The flip-flop FF<sub>4i</sub> receives the clock signal VCLK21 and VCLK21b as inner clocks clk and clkb, respectively. The flip-flop FF<sub>4i</sub> delays the signals inputted during a low level of the clock clk by half of a clock cycle of clock clk and outputs the resultant signal, as do the flip-flops described in FIGs. 11, 13A, and 13B.

**[0128]** As shown in FIG. 15, the output signal out21[i] of the flip-flop FF<sub>4i</sub> has two high level pulses in one cycle, the width of the high level pulse is the same as the clock cycle VCLK21, and the cycle of the high level pulse is twice the clock cycle of clock VCLK21. The starting signal VSP21 and the input signal in of the flip-flop FF<sub>41</sub> have two high level pulses in one cycle, and the high level pulses correspond to the low level of the clock VCLK21 per two clock intervals of clock VCLK21. The flip-flops FF<sub>41</sub> to FF<sub>4m</sub> shift the output signals out21[1] to out21[m] having two high level pulses by one clock cycle of clock VCLK21, and sequentially output the resultant signal.

**[0129]** Further, shift register 340 has the same construction as shift register 330, the clock signal VCLK22 and the starting signal VSP22 are signals that represent

the clock signal VCLK21 and the starting signal VSP21, respectively, shifted by the precharge period ( $T_p$ ), and they are inputted to shift register 340. Then, as shown in FIG. 15, shift register 340 sequentially outputs the signal out22[i] such that the output signal out21[i] is shifted by the precharge period ( $T_p$ ).

**[0130]** As shown in FIG. 7 and FIG. 14, the output signal scan22[i] of shift register 350 is the same as the output signal scan12[i] of shift register 320 in FIG. 10. Thus, when the clock signal VCLK23 and a starting signal VSP23 of FIG. 14 are inputted to shift register 320 in FIG. 10, the output signal scan22[i] of shift register 350 can be generated.

**[0131]** Furthermore, other numbers of precharge pulses, in addition to four, may be generated by applying scan driver 300' of the fourth exemplary embodiment.

**[0132]** For example, when the precharge pulse is  $2n$ ,  $n$  high level pulses may be generated in the output signals out21[i] and out22[i] of shift registers 330 and 340, and the cycle of the high level pulse may be twice the width. In particular, when the precharge pulses are two, scan driver 300' can be embodied by the shift register 320 of FIG. 10. Hereinafter, such an exemplary embodiment is described with reference to FIG. 17 and FIG. 18.

**[0133]** FIG. 17 is a simplified circuit diagram of a first shift register in the scan driver according to a fifth exemplary embodiment of the present invention, and FIG. 18 is a signal timing diagram of the scan driver according to the fifth exemplary embodiment of the present invention. In FIG. 17 and FIG. 18, out21[i]', VCLK21' and VSP21' indicate an output signal, a clock signal and a starting signal, respectively, of shift register 330', and out22[i]', VCLK22', and VSP22' indicate an output signal, a clock signal and a starting signal, respectively, of shift register 340,  $i$  being an integer from 1 to  $m$ .

**[0134]** As shown in FIG. 17, shift register 330' includes flip-flops  $FF_{51}$  to  $FF_{5(m+1)}$  and  $m$  NOR gates  $NOR_{51}$  to  $NOR_{5m}$ . The flip-flops  $FF_{51}$  to  $FF_{5(m+1)}$  and  $m$  NOR gates  $NOR_{51}$  to  $NOR_{5m}$  are substantially the same as flip-flops  $FF_{31}$  to  $FF_{3(m+1)}$  and  $m$  NOR gates  $NOR_{31}$  to  $NOR_{3m}$  of FIG. 10, and thus descriptions thereof are omitted. Furthermore, shift register 340' has the same construction as shift register 330', and VCLK22' and VSP22' are inputted as clock and starting signals, respectively.

**[0135]** The clocks VCLK21' and VCLK22' inputted to shift registers 330' and 340' have the same cycle as the clock VCLK23 of shift register 350. The starting signals VSP21' and VSP22' of shift registers 330 and 340 have a low level pulse, while the clocks VCLK21' and VCLK22' are at a high level.

**[0136]** As shown in FIG. 18, the output signals out21[i]' and out22[i]' having high level pulses are shifted by half of a clock cycle of clock VCLK23. The width of the high level pulse corresponds to half of a clock cycle of clock VCLK23. The construction and operation of the scan driver can be easily understood from the above descriptions, and thus the detailed description is omitted.

**[0137]** As such, the construction of a scan driver can be simplified by using the shift register of FIG. 10 as shift registers 330', 340' and 350 of the scan driver. Furthermore, the clock cycles of clocks VCLK21' and VCLK22' are longer than the clock cycle of FIG. 15, and thus the frequency can be reduced.

**[0138]** As mentioned above, scan driver 300' according to the fourth and fifth exemplary embodiments of the present invention sequentially outputs a first output signal having high level pulses. The number of the high level pulses is one-half the number of the precharge pulses, or a larger number than one-half the number of the precharge pulses by 1. The cycle of the high level pulse is twice the width. Scan driver 300' sequentially outputs a second output signal for the first output signal to be shifted by the precharge period, and generates a pulse corresponding to the precharge pulse, while the first output signal and the second output signal have different levels from each other.

**[0139]** FIG. 19 shows scan driver according to a sixth exemplary embodiment of the present invention, and FIG. 20 is a signal timing diagram of the scan driver according to the sixth exemplary embodiment of the present invention.

**[0140]** As shown in FIG. 19, scan driver 300" according to the sixth exemplary embodiment of the present invention includes two shift registers 360 and 370, and a plurality of NOR gates  $NOR_{61}$  to  $NOR_{6m}$  and  $NOR_{71}$  to  $NOR_{7m}$ .

**[0141]** As shown in FIG. 18 and FIG. 19, shift register 360 receives a clock signal VCLK31 and a starting signal VSP31, and shifts the output signals out31[1] to out31[m] by half of a clock cycle of clock VCLK31, and sequentially outputs the resultant signal. The output signal out31[i] has one low-level pulse in one cycle, and the width of the low-level pulse is twice the clock cycle of clock VCLK31,  $i$  being an integer from 1 to  $m$ .

**[0142]** NOR gate  $NOR_{5i}$  performs a NOR operation on a precharge control signal PC and the output signal out31[i] of shift register 360, and outputs the output signal scan31[i]. As shown in FIG. 20, the precharge control signal PC has a low-level pulse in a predetermined cycle. The width  $T_p$  of the low-level pulse is the same as the precharge period, and the cycle of the precharge control signal PC corresponds to half of a clock cycle of clock VCLK31. As such, the width of the low-level pulse of the output signal out31[i] becomes four times the cycle of the precharge control signal PC, and the four low-level pulses of the precharge control signal PC correspond to the output signal out31[i].

**[0143]** NOR gate  $NOR_{6i}$  outputs a high-level pulse when both the precharge control signal PC and the output signal out31[i] are at a low level, and thus the output signal scan31[i] of the NOR gate  $NOR_{6i}$  has four high-level pulses in one cycle. The width and cycle of the high-level pulse are the same as the width and cycle, respectively, of the precharge control signal PC, and the precharge pulse may be generated by the high-level

pulse. Furthermore, an output signal  $out31[i+1]$  is the signal for the output signal  $out31[i]$  to be shifted by half of a clock cycle of clock VCLK31, and thus the output signal  $scan31[i+1]$  of NOR gate  $NOR_{6(i+1)}$  is the signal for the output signal  $scan31[i]$  to be shifted by half of a clock cycle of clock VCLK31. That is, the three pulses of four high-level pulses of the output signal  $scan31[i+1]$  correspond to the high-level pulse of the output signal  $scan31[i]$ .

**[0144]** Shift register 370 receives a clock signal VCLK32 and a starting signal VSP32, shifts the output signals  $scan32[1]$  to  $scan32[m]$  by half of a clock cycle of clock VCLK31, and sequentially outputs the resultant signal. The output signals  $scan32[i]$  to  $scan32[m]$  have one high-level pulse in one cycle. The width of the high-level pulse of the output signal  $scan32[i]$  is  $\frac{1}{2}$  times the clock cycle of clock VCLK32, and the cycle of the clock VCLK32 is the same as that of the clock VCLK31. The start time point of the high-level pulse in the output signal  $scan32[i]$  is half of a clock cycle of clock VCLK32 away from a start time point of the last high-level pulse in the output signal  $scan31[i]$ .

**[0145]** NOR gate  $NOR7i$  performs a NOR operation on an output signal  $scan32[i]$  of shift register 360 and an output signal  $scan31[i]$  of NOR gate  $NOR6i$ , and outputs a selection signal  $select[i]$ . The width and cycle of the precharge pulse are the same as the width and cycle, respectively, of the high-level pulse of the output signal  $scan31[i]$ , and the width of the selection pulse is the same as the width of the high-level pulse of the output signal  $scan31[i]$ .

**[0146]** Next, shift registers 360 and 370 for generating the output signals  $out31[i]$  and  $scan32[i]$  described in FIG. 19 and 20 are described in detail with reference to FIG. 21 to FIG. 25.

**[0147]** FIG. 21 is a simplified circuit diagram of a first shift register in the scan drive of FIG. 19. In FIG. 21, VCLK31b indicates an inverted version of a clock signal VCLK31, but VCLK31b is not shown in the signal timing diagram of the FIG. 20.

**[0148]** As shown in FIG. 21, shift register 360 includes  $m$  flip-flops  $FF61$  to  $FF6m$ , and output signals of each flip-flop  $FF6i$  become an output signal  $out31[i]$  of shift register 360,  $i$  being an integer from 1 to  $m$ . In FIG. 20, an input signal of a first flip-flop  $FF61$  is the start signal VSP31 of FIG. 19, and an output signal  $out31[i]$  of the  $i$ th flip-flop  $FF6i$  becomes an input signal of the  $(i+1)$ th flip-flop  $FF6(i+1)$ .

**[0149]** The flip-flop  $FF6i$  outputs an input signal in as it is inputted when a clock  $clk$  is at a high level, but the flip-flop  $FF6i$  latches the input signal in inputted when the clock  $clk$  was at a high level, and outputs the resultant signal as does the flip-flop of FIGs. 8A and 8B. Furthermore, the clock  $clk$  is inverted between two adjacent flip-flops  $FF6i$  and  $FF6(i+1)$ , as does the shift register of FIG. 8A.

**[0150]** In FIG. 20, the flip-flop  $FF6i$  which is located at an odd-numbered position in the column direction re-

ceives clocks VCLK31 and VCLK31b as inner clocks  $clk$  and  $clkb$ , respectively. The flip-flop  $FF6i$  which is located at an even-numbered position in the column direction receives clocks VCLK31 and VCLK31b as inner clocks  $clk$  and  $clkb$ , respectively. The starting signal VSP31, which is the input signal in of flip-flop  $FF61$ , has a low level pulse in two clock cycles when the clock VCLK31 is at a high level. Then, the flip-flops  $FF61$  to  $FF6m$  can shift output signals  $out31[1]$  to  $out31[m]$  having low-level pulses in two clock cycles of clock VCLK31 by half of a clock cycle of clock VCLK31, and sequentially output the resultant signals.

**[0151]** Furthermore, as shown in FIG. 7 and FIG. 20, the output signal  $scan32[i]$  of shift register 370 is the same as the output signal  $scan12[i]$  of shift register 320 of FIG. 10. Thus, when the clock signal VCLK32 and the starting signal VSP32 are inputted to shift register 320 of FIG. 10, the output signal  $scan32[i]$  of shift register 370 can be generated.

**[0152]** As such, scan driver 300" described in FIG. 19 to FIG. 21 can generate the selection signal  $select[i]$  shown in FIG. 4. Although the selection signal has four precharge pulses in FIG. 19 to FIG. 21, scan driver 300" of FIG. 19 to FIG. 21 can generate a selection signal having other numbers of precharge pulses.

**[0153]** For example, for  $2n$  precharge pulses, the width of the high-level pulse is established to be twice the cycle of the precharge control signal PC in the output signal  $out31[i]$  of shift register 360. Then, the output signals  $scan31[i]$  of NOR gate  $NOR5i$  have  $2n$  high-level pulses.

**[0154]** Scan driver 300" of FIG. 19 can be applied to generate odd-numbered precharge pulses in addition to even-numbered precharge pulses. Hereinafter, the case of generating an odd number of precharge pulses is described with reference to FIG. 22, which is a signal timing diagram of a scan driver according to the seventh exemplary embodiment of the present invention, specifically, the scan driver 300" thereof.

**[0155]** The signal timing of FIG. 22 is the same as the signal timing of FIG. 20, excluding the timing of the starting signal VSP32', the signal clock VCLK32', and the output signal  $scan32[i]$ '.

**[0156]** In detail, the start time point of the last high level pulse of the output signal  $scan31[i]$  of NOR gate  $NOR6i$  is established so as to correspond to the start time point of the high-level pulse of the output signal  $scan32[i]$ ' of shift register 370. The last high-level pulse of the output signal  $scan31[i]$  of NOR gate  $NOR6i$  is subjected to a NOR operation with the high-level pulse of the output signal  $scan32[i]$ ' of shift register 370, and thus an odd number of precharge pulses can be generated.

**[0157]** As such, the method described in FIG. 21 can be applied to the second to fifth exemplary embodiments. That is, in the second to fifth exemplary embodiments, the start time points of the last high-level pulse of the output signals  $scan11[i]$ ,  $scan11[i]'$ ,  $scan21[i]$  are established to correspond to the start time points of the

high-level pulse of the output signals scan12[i], scan12[i]', and scan22[i]. Then, the number of precharge pulses can be made less than the number of high-level pulses by 1 in the selection signal select[i].

**[0158]** Shift register 360 having half of a clock cycle shift function is applied in FIG. 19 to FIG. 22. However, shift register 360' having a one clock cycle shift function can also be applied. Hereinafter, such an exemplary embodiment is described in detail with reference to FIG. 23 and FIG. 24.

**[0159]** FIG. 23 is a simplified circuit diagram of a first shift register in a scan driver according to an eighth exemplary embodiment of the present invention, and FIG. 24 is a signal timing diagram of the scan driver according to the eighth exemplary embodiment of the present invention.

**[0160]** As shown in FIG. 23, shift register 360' includes m flip-flops FF<sub>71</sub> to FF<sub>7m</sub>, and the output signal of the flip-flop FF<sub>7i</sub> becomes the output signal out31[i]' of shift register 360', i being an integer from 1 to m.

**[0161]** The flip-flop FF<sub>7i</sub> receives the clock signals VCLK31 and VCLK31b as inner clocks clk and clkb, respectively. The flip-flop FF<sub>7i</sub> delays a signal inputted at a low level of clock clk by half of a clock cycle of clock clk and outputs the resultant signal during one clock cycle of clock clk, as do the flip-flops described in FIGs. 13A and 13B. Thus, the flip-flops FF<sub>71</sub> to FF<sub>7m</sub> can shift the output signals out31[1]' to out31[m]' by one clock cycle of clock VCLK31', and sequentially output the resultant signal as shown in FIG. 24.

**[0162]** However, the flip-flop FF<sub>7i</sub> shifts the output signal by one clock cycle of clock VCLK31', and thus the clock cycle of clock VCLK31' is one-half of the clock cycle of clock VCLK32, while the clock cycle of clock VCLK31' is the same as the cycle of the precharge control signal PC, apart from FIG. 19. Furthermore, the output signal out31[i]' has a low-level pulse, the width of which is four times the cycle of the precharge control signal PC, and thus the width of the low-level pulse of the output signal out31[i]' is the same as four times the clock cycle of clock VCLK31'. The starting signal VSP31', the input signal in of the flip-flop FF<sub>71</sub>, is converted to a high-level signal after the clock VCLK31' has low levels during the four cycles of clock VCLK31'. Then, the flip-flops FF<sub>71</sub> to FF<sub>7m</sub> shift the output signals out31[i] to out31[m]' having the low-level pulse during four clock cycles of clock VCLK31' by one cycle of clock VCLK31', and sequentially output the resultant signal. Thus, the output signal scan31[i]' having four high-level pulses can be outputted, as shown in FIG. 24.

**[0163]** In the scan driver described in FIG. 23 and FIG. 24, when the high-level pulse of the output signal scan32[i] of shift register 370' is established so as to correspond to the last-high level pulse of the output signal scan31[i]' of NOR gate NOR<sub>6i</sub>, an odd number of precharge pulses can be generated. Furthermore, in the scan driver, the number of high-level pulses of the output signal scan31[i]' of NOR gate NOR<sub>6i</sub> can be established

so as to be an odd number. That is, the width of the low-level pulse of the output signal out31[i]' of shift register 360' can be established so as to be an odd number multiple of the cycle of the precharge control signal PC, that is, an odd number multiple of the clock cycle of clock VCLK31'.

**[0164]** Furthermore, an emit signal emit[i] of FIG. 4 can be generated by using scan driver 300 described in FIG. 23 and FIG. 24. Hereinafter, such an exemplary embodiment is described with reference to FIG. 25.

**[0165]** FIG. 25 is a signal timing diagram of a scan driver according to a ninth exemplary embodiment of the present invention.

**[0166]** As shown in FIG. 25, shift register 370 outputs an output signal scan32[i]', such that a start time point of a high-level pulse in the output signal scan32[i]' corresponds to a start time point of the last high-level pulse in the output signal scan31[i]' of NOR gate NOR<sub>6i</sub>. As such, a period in which the output signal scan31[i]' of NOR gate NOR<sub>6i</sub> is a high-level pulse, and a period in which the output signal scan32[i]' of shift register 370 is a high-level pulse, are included in a period in which the output signal out31[i]' of shift register 360' is a low-level pulse. That is, while the selection signal select[i] has the selection pulse and the precharge pulse, the output signal out31[i]' of shift register 360' is at a low level. Thus, an inverted signal of the output signal of shift register 360' can be used as the emit signal emit[i].

**[0167]** As such, scan driver 300' according to the sixth to eighth exemplary embodiments of the present invention uses a precharge control signal in which a first pulse having a width corresponding to the precharge pulse is repeated a predetermined number of cycles. In the precharge control signal, the first pulses corresponding to the number of precharge pulses are selected to generate the precharge pulse. In this respect, scan driver 300' selects the first pulse by using a second pulse, the width of which includes the first pulses corresponding to the number of the precharge pulses.

**[0168]** In the first to eighth exemplary embodiments of the present invention, the selection signal outputted from the scan driver is directly applied to the selection scan line. However, the selection signal outputted from the scan driver may be applied to the selection scan line through a buffer formed between the scan driver and the display area. Furthermore, a level shifter may be formed between the scan driver and the display area so as to modify levels of the selection signal and the emit signal.

**[0169]** According to the present invention, the time for charging the data line can be reduced, and thus quick data programming and a correct gray expression can be achieved.

**[0170]** While this invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications included within the spirit and scope of the appended claims and equivalents

thereof.

### Claims

1. A driving device for a light emitting display which includes a plurality of scan lines for transferring a selection signal, the driving device comprising:

a first driver for sequentially outputting a first signal, the first signal having a first integer multiple of first pulses and being shifted by a first period;

a second driver for sequentially outputting a second signal, the second signal having a second pulse and being shifted by a second period; and

a third driver for sequentially outputting the selection signal in response to the first signal and the second signal, the selection signal having a second integer multiple of third pulses corresponding to at least one of the first integer multiple of first pulses, and having a fourth pulse corresponding to the second pulse.

2. The driving device of claim 1, wherein the first driver comprises:

a fourth driver for shifting a third signal having a third integer multiple of fifth pulses by the first period, and for sequentially outputting the shifted third signal;

a fifth driver for shifting by the first period a fourth signal having a sixth pulse which is a fifth pulse shifted by the third period, and for sequentially outputting the fourth signal; and

a sixth driver for outputting the first signal having a first pulse in a period, wherein levels of the first signal and the second signal are different.

3. The driving device of claim 2, wherein the third period has a width the same as a width of the first pulse.

4. The driving device of claim 3, wherein a width between two adjacent fifth pulses in a plurality of the fifth pulses is the same as a width of the fifth pulse.

5. The driving device of claim 4, wherein the third period has a width shorter than the width of the fifth pulse.

6. The driving device of claim 2, wherein the third integer corresponds to twice the first integer and/or wherein the second driver, the fourth driver and the fifth driver respectively comprise a shift register, and a cycle of a clock used in the second driver corre-

sponds to twice a cycle of a clock used in the fourth driver and the fifth driver and/or wherein the second driver, the fourth driver and the fifth driver respectively comprise a shift register, and a cycle of a clock used in the second driver is the same as a cycle of a clock used in the fourth driver and the fifth driver.

7. The driving device of claim 1, wherein the first driver comprises:

a fourth driver for shifting a third signal having a fifth pulse by the first period, and for sequentially outputting the fifth signal; and

a fifth driver for receiving a fourth signal having a sixth pulse which is repeated in a predetermined cycle, and the third signal, and for outputting the first signal having the first pulse in a period in which the fifth pulse and the sixth pulse overlap each other.

8. The driving device of claim 16, wherein a width of the sixth pulse is the same as a width of the first pulse and/or wherein a width of the fifth pulse includes more than a first integer multiple of the sixth pulses and/or wherein a cycle of the sixth pulse is the same as a cycle of the first period and/or wherein the fourth driver includes a shift register, and a cycle of a clock used in the fourth driver corresponds to twice a cycle of the sixth pulse.

9. A light emitting display, comprising:

a display area comprising a plurality of data lines for transferring a data signal, a plurality of scan lines arranged in a direction which crosses a direction of the data lines, and a plurality of pixels respectively coupled to the data lines and the scan lines; and

a scan driver for sequentially applying a selection signal having at least one of a first level of a first pulse and a first level of a second pulse to the plurality of scan lines, the second pulse having a width which is narrower than a width of the first pulse.

10. The light emitting display of claim 9, wherein the scan driver comprises:

a first driver for shifting a first signal having a predetermined number of third pulses by a first period, and for sequentially outputting the first signal;

a second driver for outputting the first signal, shifted in an interval of a second period, as a second signal in response to one first signal of the first signals outputted sequentially, the second period being an integer multiple of the first period; and

a third driver for generating the first pulse of the selection signal in response to at least one third pulse of the predetermined number of third pulses in the first signal.

11. The light emitting display of claim 10, wherein the second period is substantially the same as a cycle of the third pulse.

12. The light emitting display of claim 9, wherein the scan driver comprises:

a first driver for shifting a first signal having a predetermined number of third pulses by a first period, and for sequentially outputting the first signal;

a second driver for shifting a second signal having fourth pulses by the first period, and for sequentially outputting the second signal, the fourth pulses being the predetermined number of third pulses shifted by a second period;

a third driver for outputting a third signal having a fifth pulse in a period such that respective levels of the first signal and the second signal are different; and

a fourth driver for generating the first pulse of the selection signal in response to at least one fifth pulse of the third signal.

13. The light emitting display of claim 12, wherein an interval between adjacent two third pulses in the first signal is the same as a width of the third pulse and/or wherein the second period is shorter than the first period.

14. The light emitting display of claim 9, wherein the scan driver comprises:

a first driver for receiving a first signal having a third pulse repeated in a predetermined cycle, for shifting a second signal having a predetermined number of third pulses by a first period, and for sequentially outputting the second period; and

a second driver for generating the first pulse of the selection signal in response to at least one of third pulses of the second signal.

15. The light emitting display of claim 9, wherein each pixel comprises:

at least one of a first switch for transferring a data signal from one of the data lines in response to the first level in the selection signal applied to the scan line;

a capacitor for charging to a voltage corresponding to the data signal transferred;

a transistor for outputting a current according

to the voltage charged on the capacitor; and a light emitting element for emitting light according to a magnitude of the current outputted by the transistor.

16. A method for driving a light emitting display having a plurality of scan lines for transferring a selection signal, the driving method comprising the steps of:

sequentially outputting a first signal having at least one first level of a first pulse while shifting the first signal by a first interval;

selecting the first signal shifted sequentially by a second interval of the first signal and sequentially outputting the selected first signal as a second signal, the second interval being an integer multiple of the first interval;

outputting a third signal having a third pulse corresponding to the first pulse; and

generating at least one fourth pulse in response to at least one third pulse in the third signal, and outputting the selection signal including said at least one fourth pulse.

17. The driving method of claim 16, wherein the selection signal further includes a fifth pulse having a width longer than a width of the fourth pulse and following said at least one fourth pulse.

18. The driving method of claim 16, wherein a cycle of the first pulse is substantially the same as the second interval.

19. The driving method of claim 16, wherein a width of the first pulse is substantially the same as the first interval.

20. A method for driving a light emitting display having a plurality of scan lines for transferring a selection signal, the driving method comprising the steps of:

outputting a first signal having at least one first level of a first pulse;

outputting a second signal having at least one first level of a second pulse, said second pulse having a start time point which is shifted from a start time point of the first pulse by a predetermined period;

outputting a third signal having a third level of a third pulse in at least one period in which levels of the first signal and the second signal are different; and

generating at least one fourth pulse in response to each said third pulse in the third signal, and outputting the selection signal including said at least one fourth pulse.

21. The driving method of claim 20, wherein the selec-

tion signal further includes a fifth pulse having a width longer than a width of the fourth pulse, said fifth pulse following the fourth pulse, and wherein an interval between a start time point of the fifth pulse and a start time point of the fourth pulse adjacent to the fifth pulse is the same as an interval between start time points of two adjacent fourth pulses.

22. The driving method of claim 20, wherein a width of the first pulse is the same as a width of the second pulse, and the predetermined period is shorter than the width of the first pulse.

23. The driving method of claim 20, wherein at least two first pulses are present in the first signal, a fourth level period between two adjacent first pulses being the same as a width of the first pulse, and wherein at least two second pulses are present in the second signal, a fourth level period between two adjacent second pulses being the same as a width of the second pulse.

24. A method for driving a light emitting display having a plurality of scan lines for transferring a selection signal, the driving method comprising the steps of:

outputting a first signal having a first level of a first pulse which is repeated in a predetermined cycle;  
 outputting a second signal having a second level of a second pulse, said second pulse having a width which includes at least one first pulse;  
 selecting said at least one first pulse with the second pulse, and outputting a third signal having a third pulse corresponding to the selected said at least one first pulse; and  
 generating at least one fourth pulse in response to at least one third pulse, and outputting the selection signal including said at least one fourth pulse.

25. The driving method of claim 24, wherein the selection signal further includes a fifth pulse having a width longer than a width of said at least one fourth pulse, said fifth pulse following said at least one fourth pulse.

26. The driving method of claim 24, wherein an interval between a start time point of a fifth pulse and a start time point of a fourth pulse adjacent to the fifth pulse is the same as the predetermined cycle.

55

FIG.1

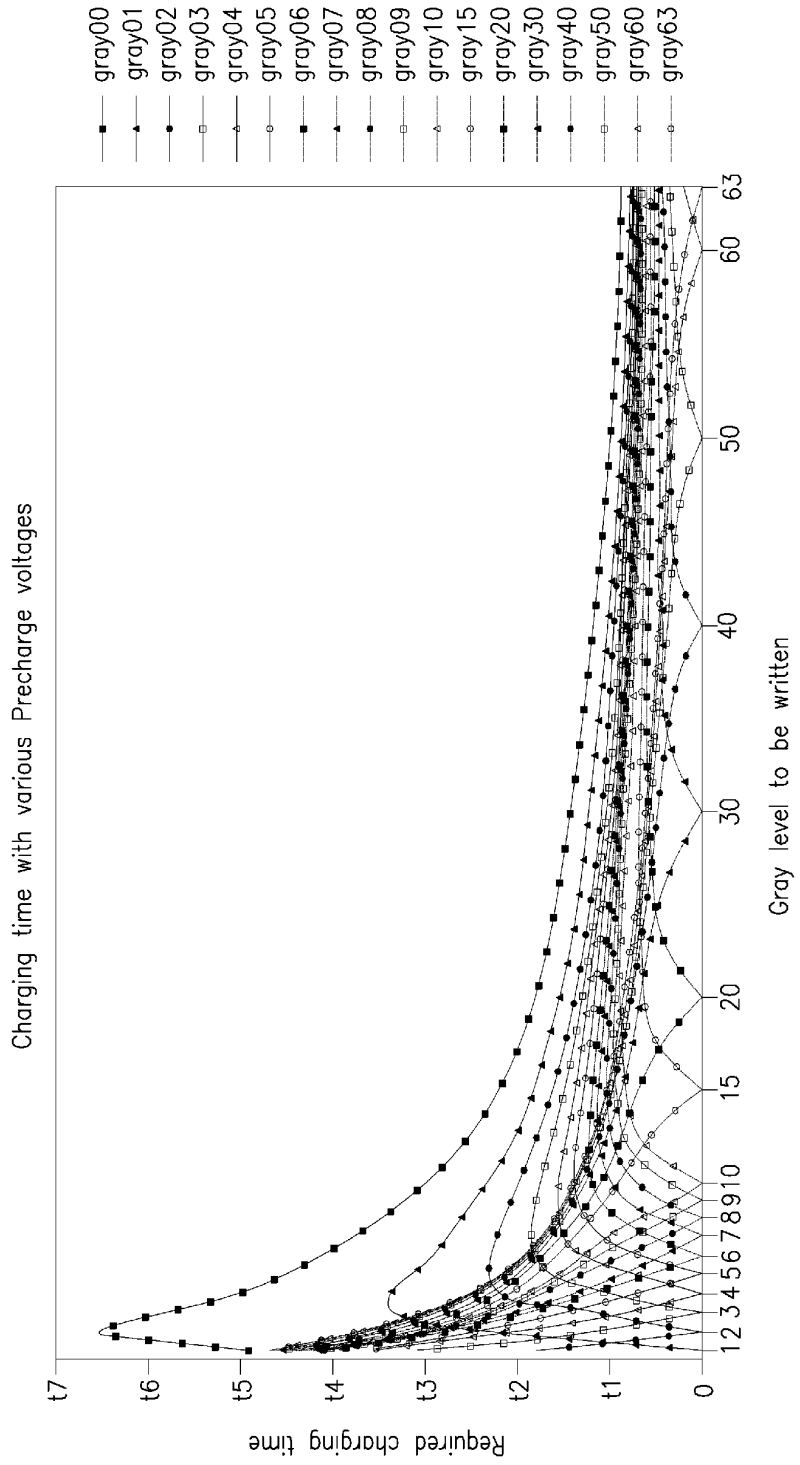


FIG.2

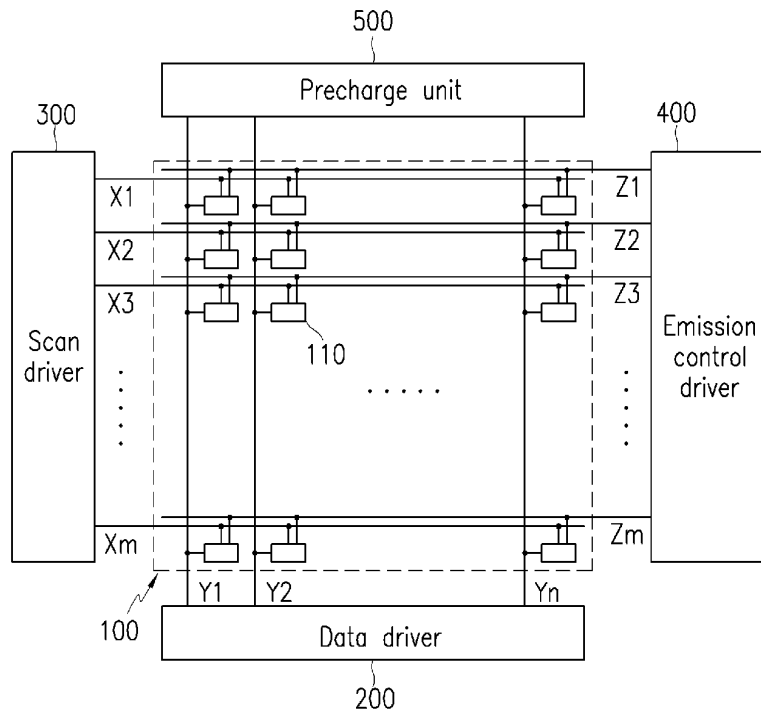


FIG.3

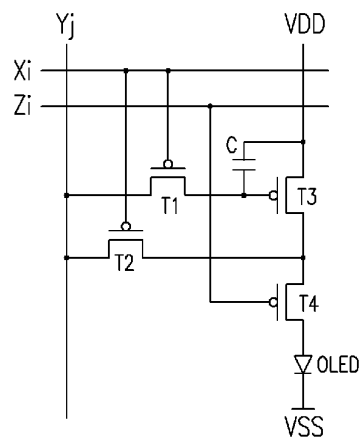


FIG.4

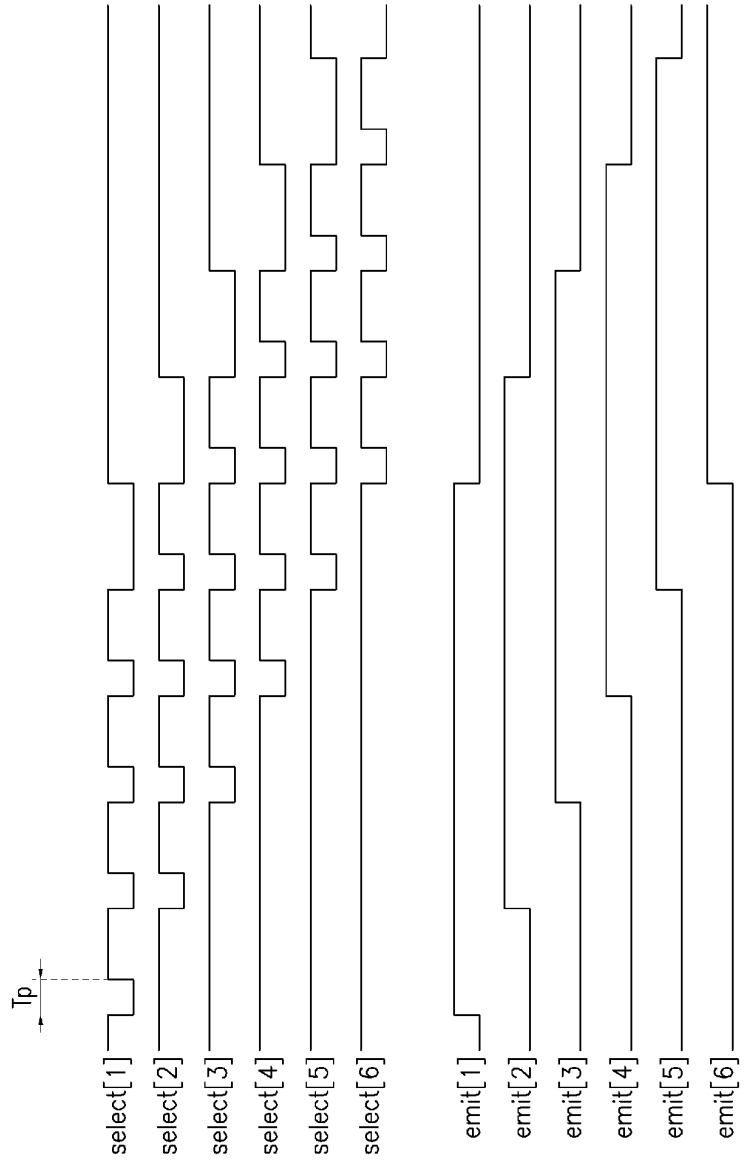


FIG.5A

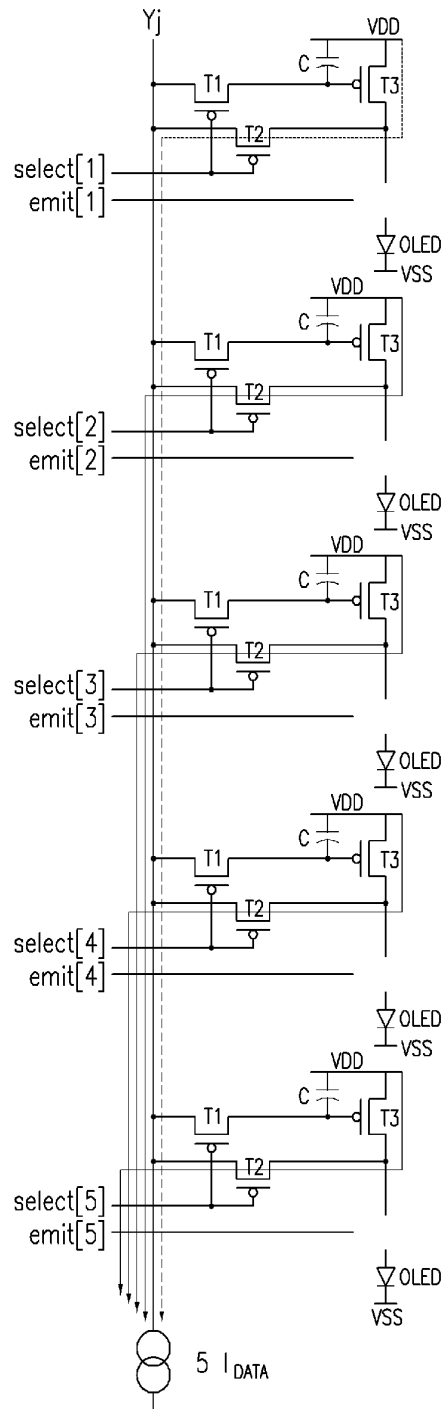


FIG.5B

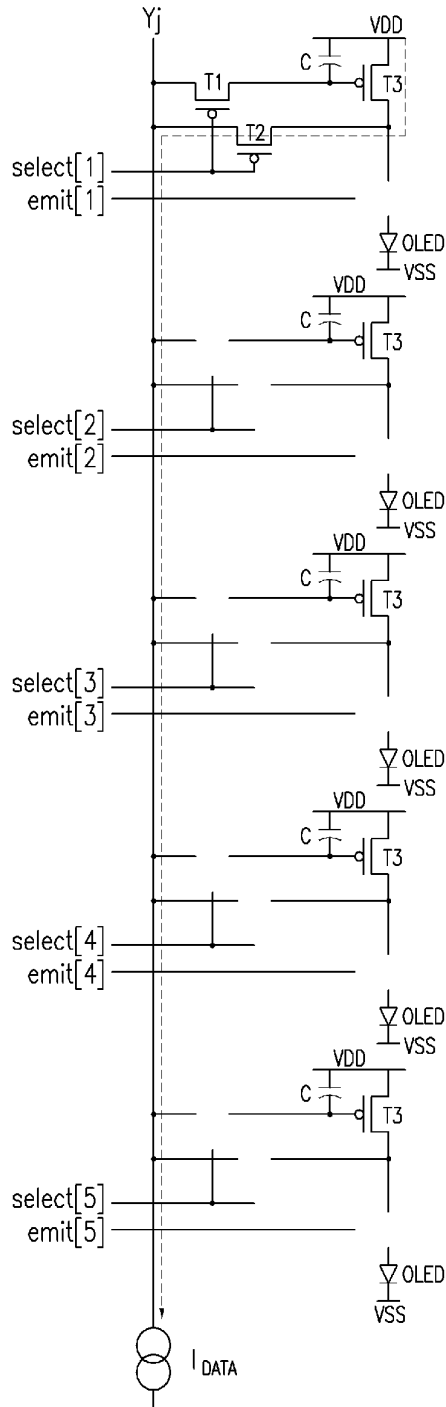


FIG.6

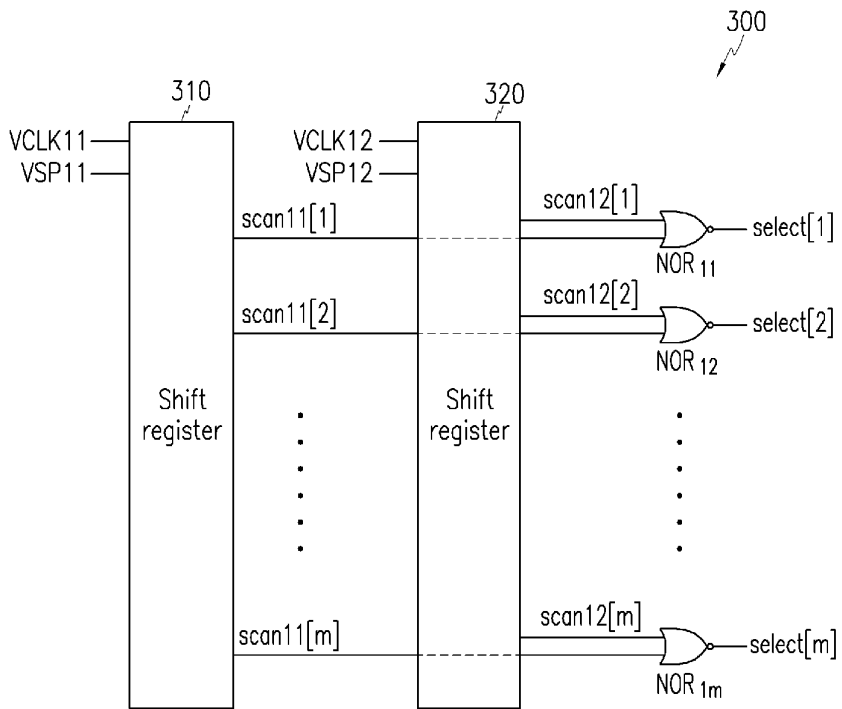


FIG.7

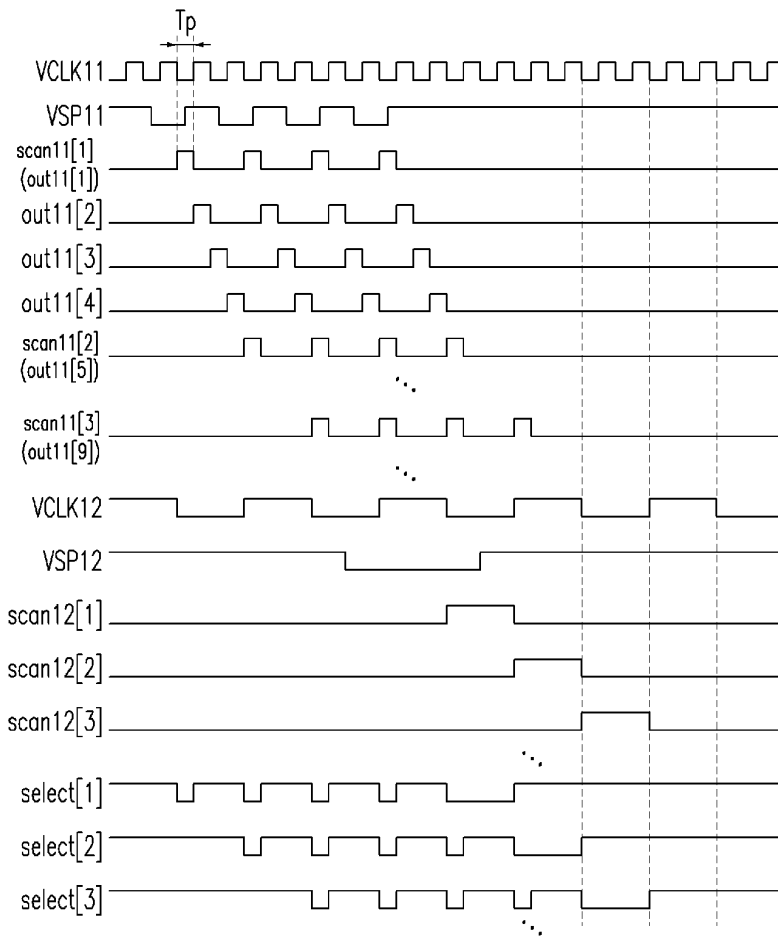


FIG.8A

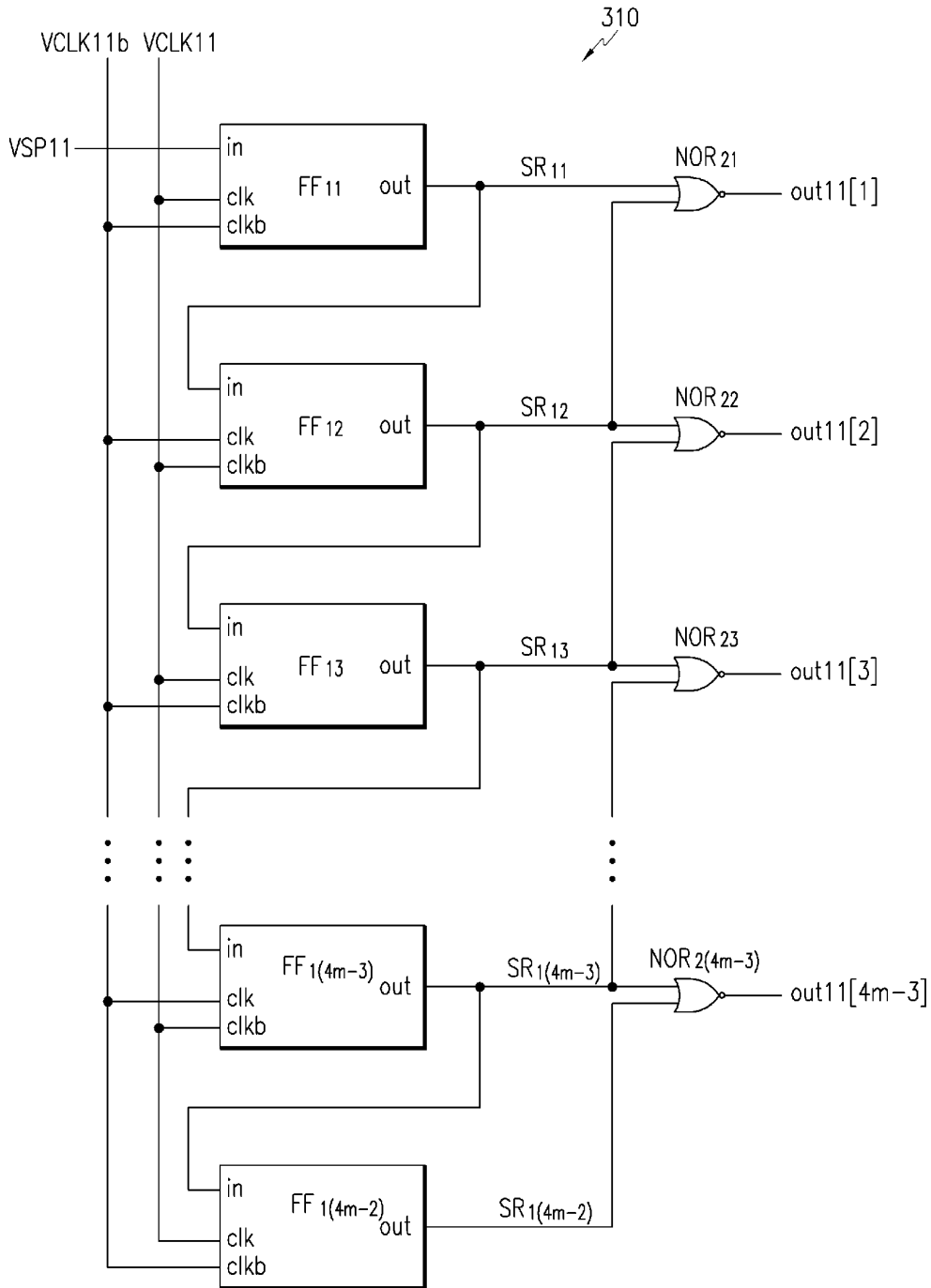


FIG.8B

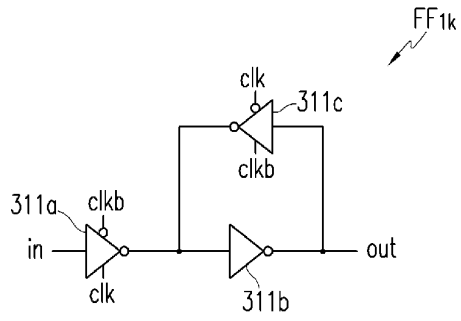


FIG.9

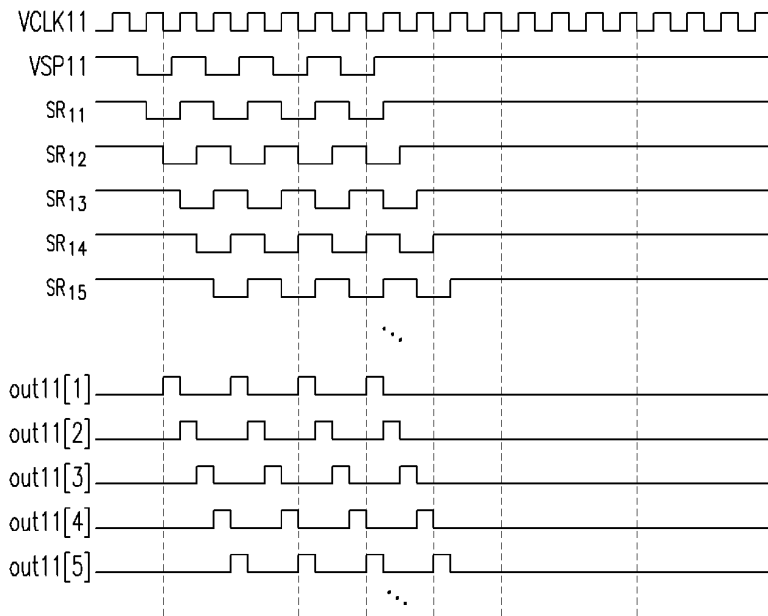


FIG.10

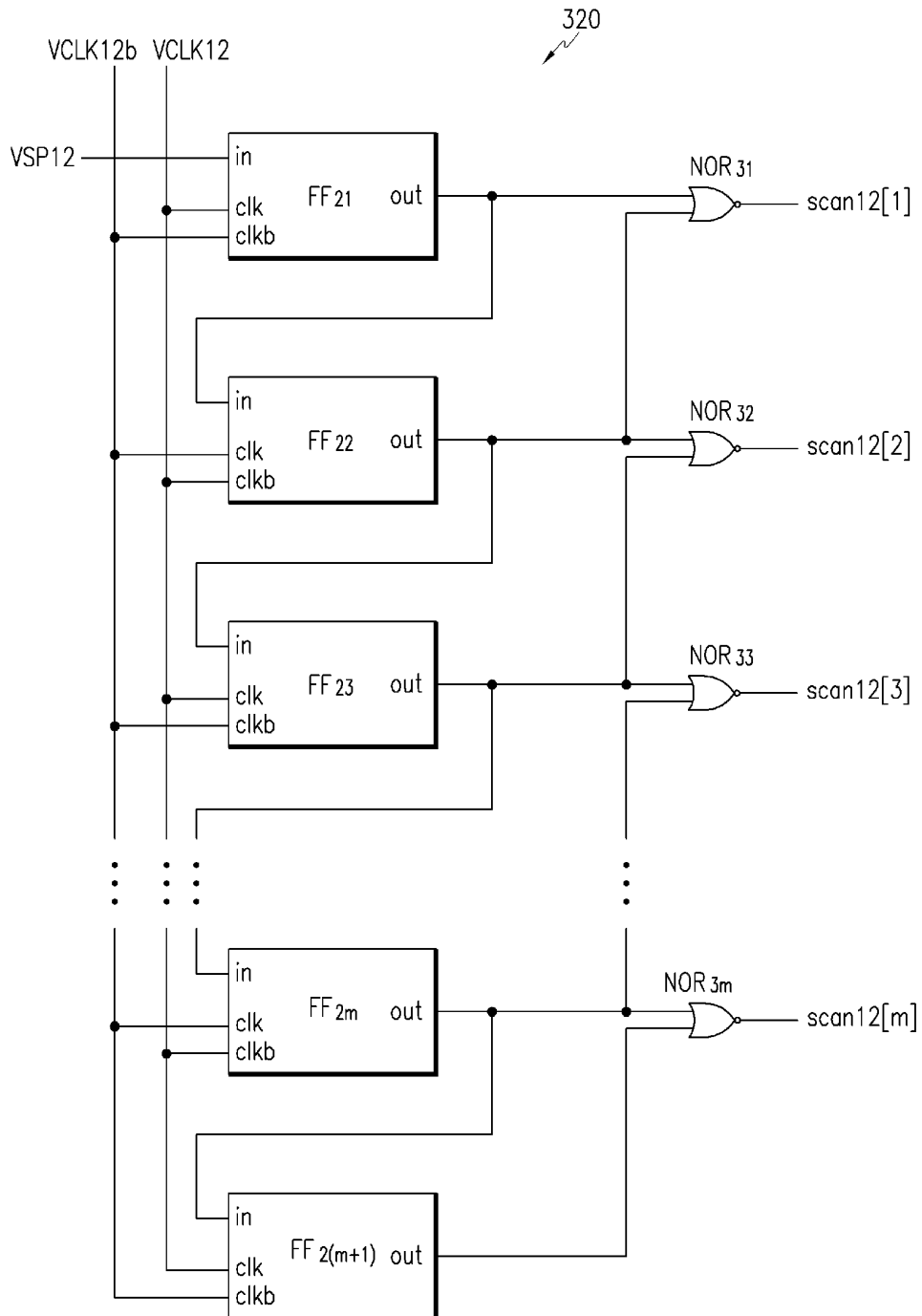


FIG.11

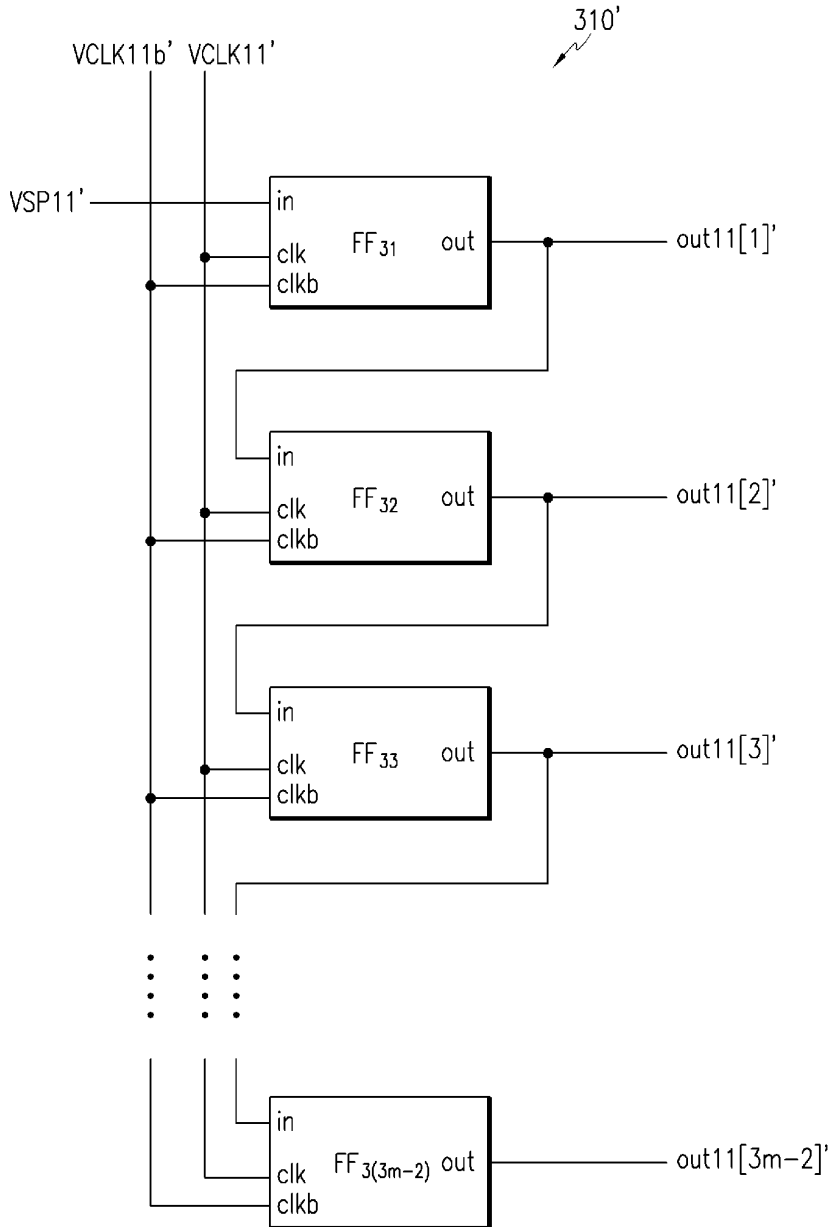


FIG.12

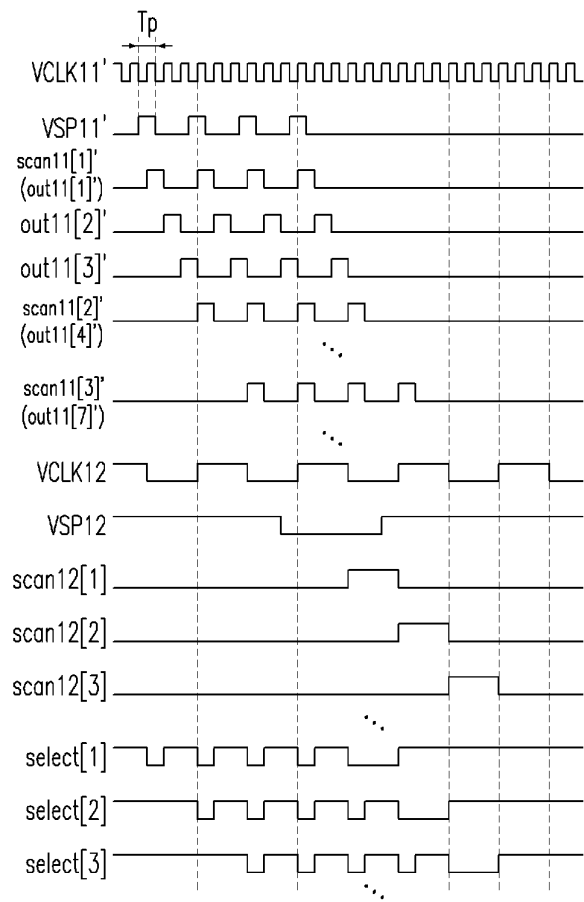


FIG.13A

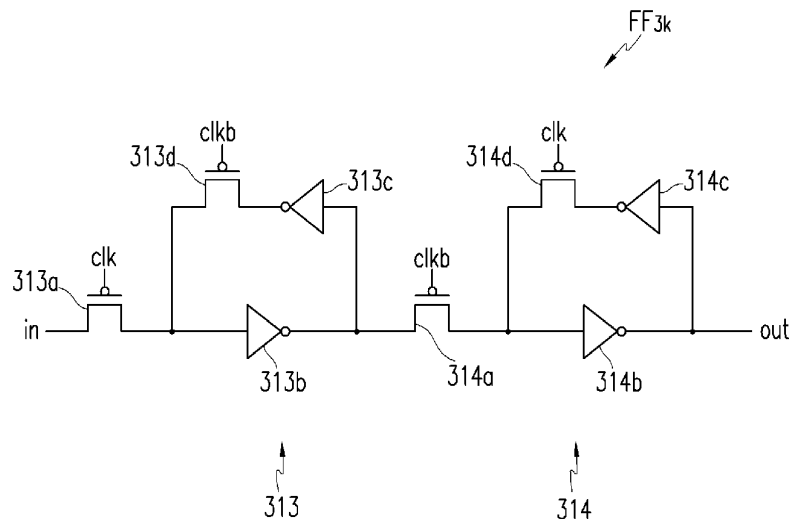


FIG.13B

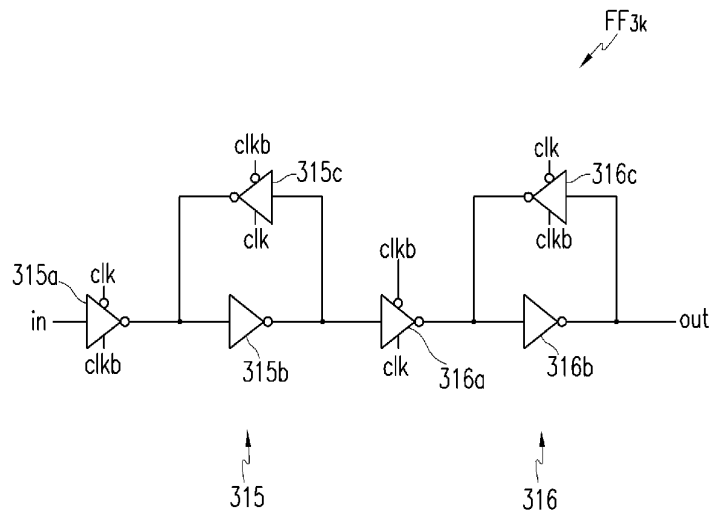


FIG.14

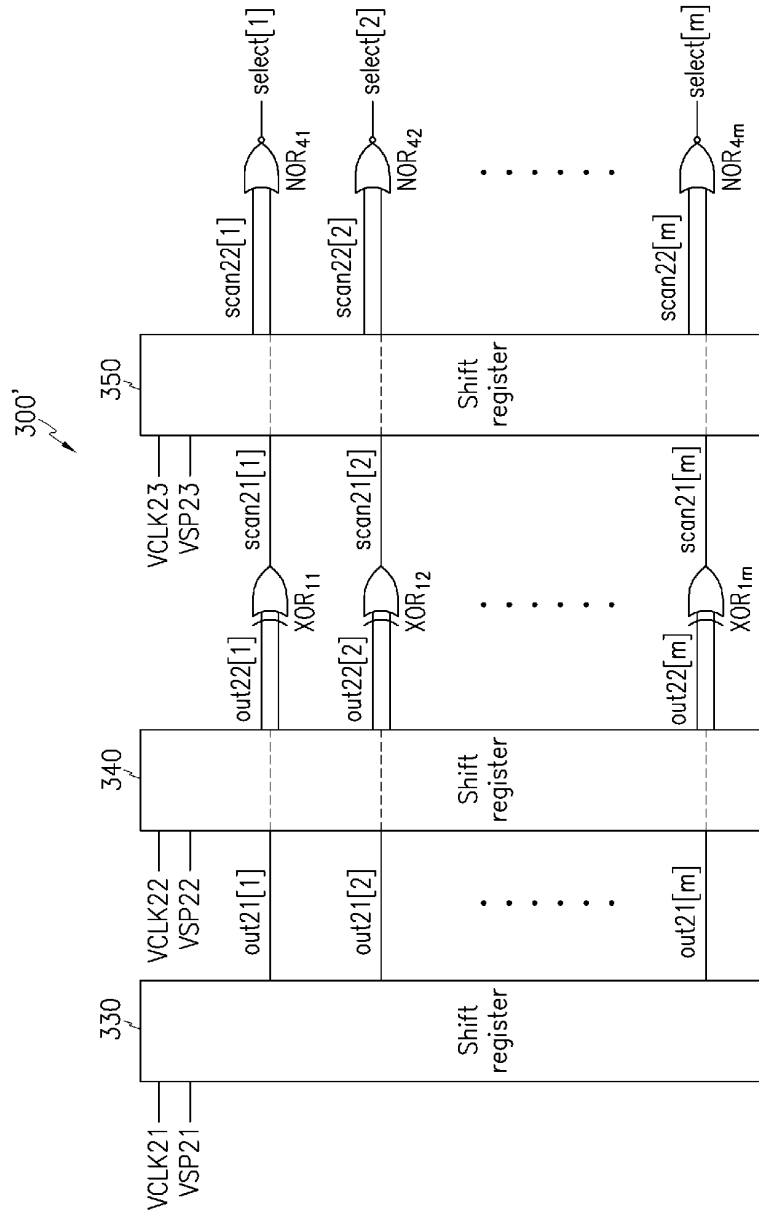


FIG.15

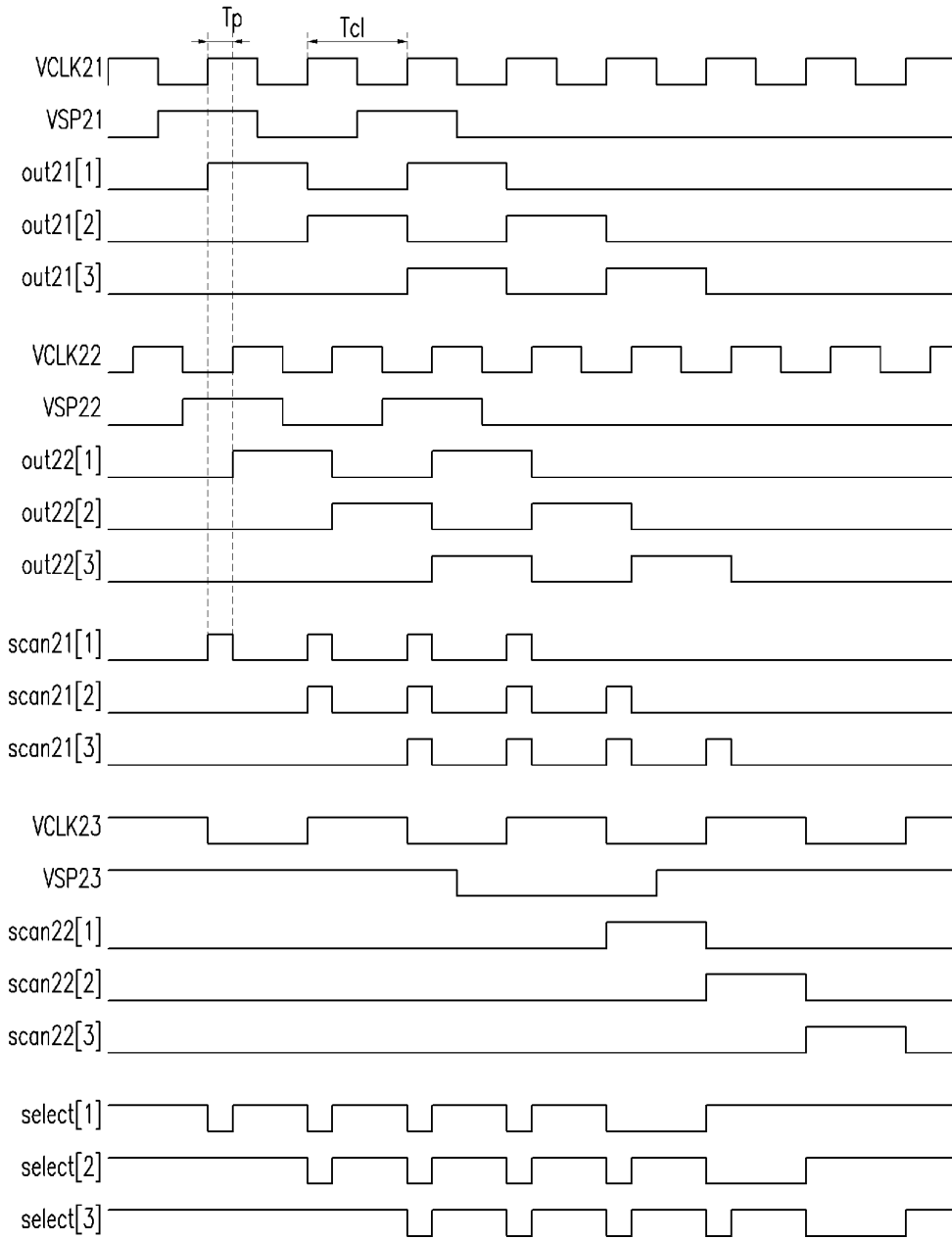


FIG.16

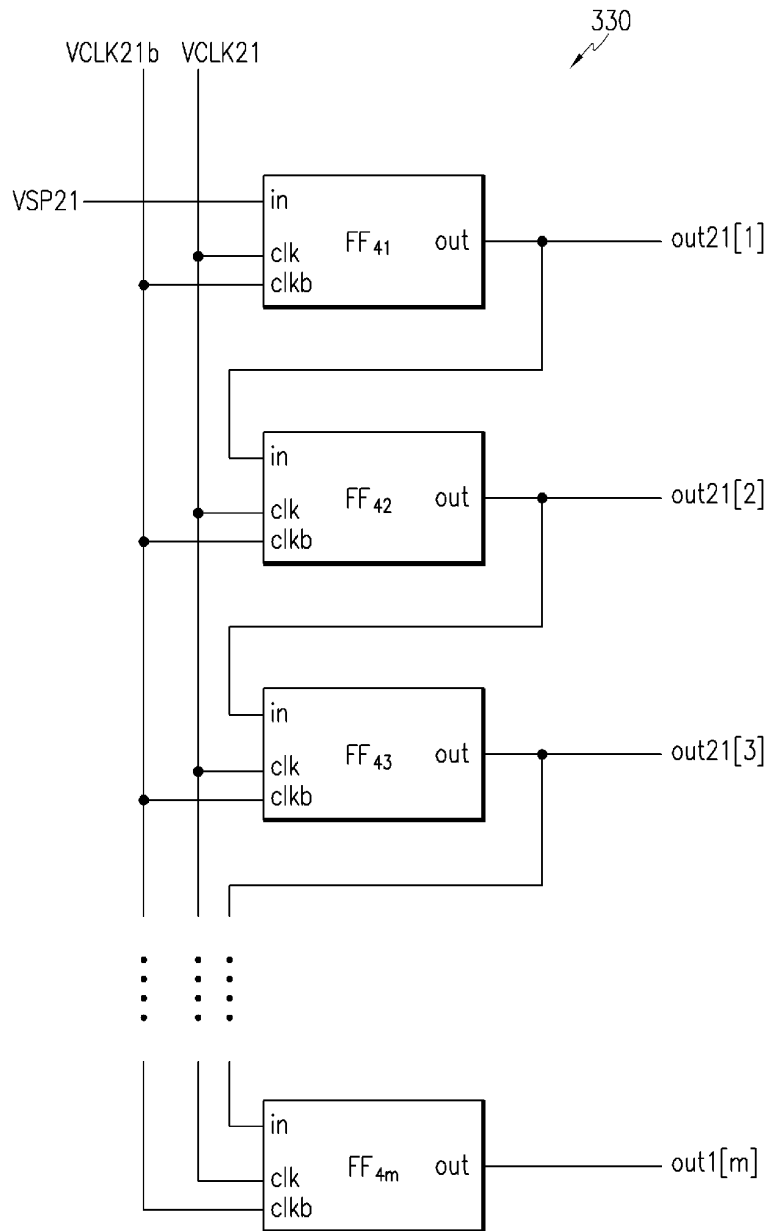


FIG.17

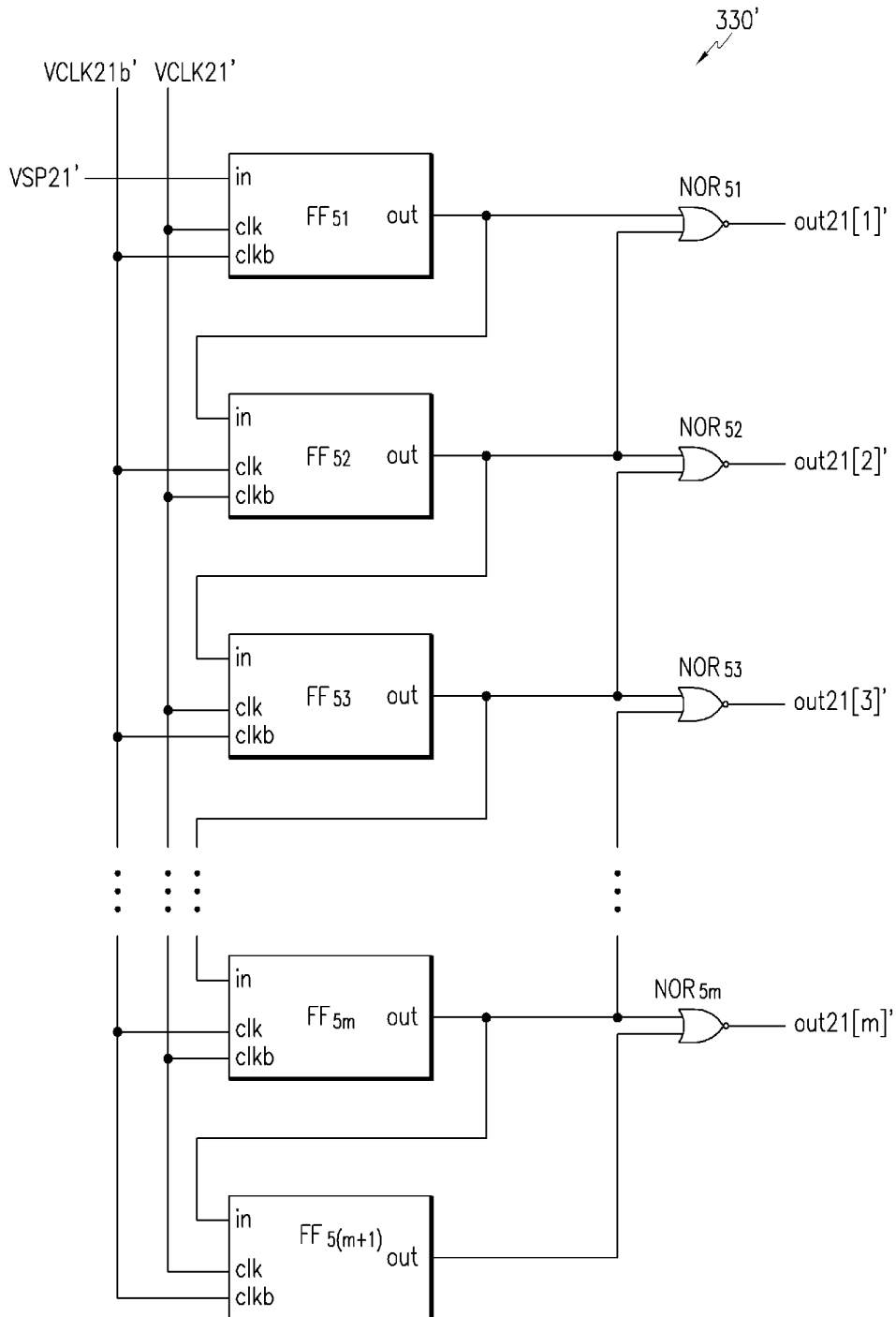


FIG.18

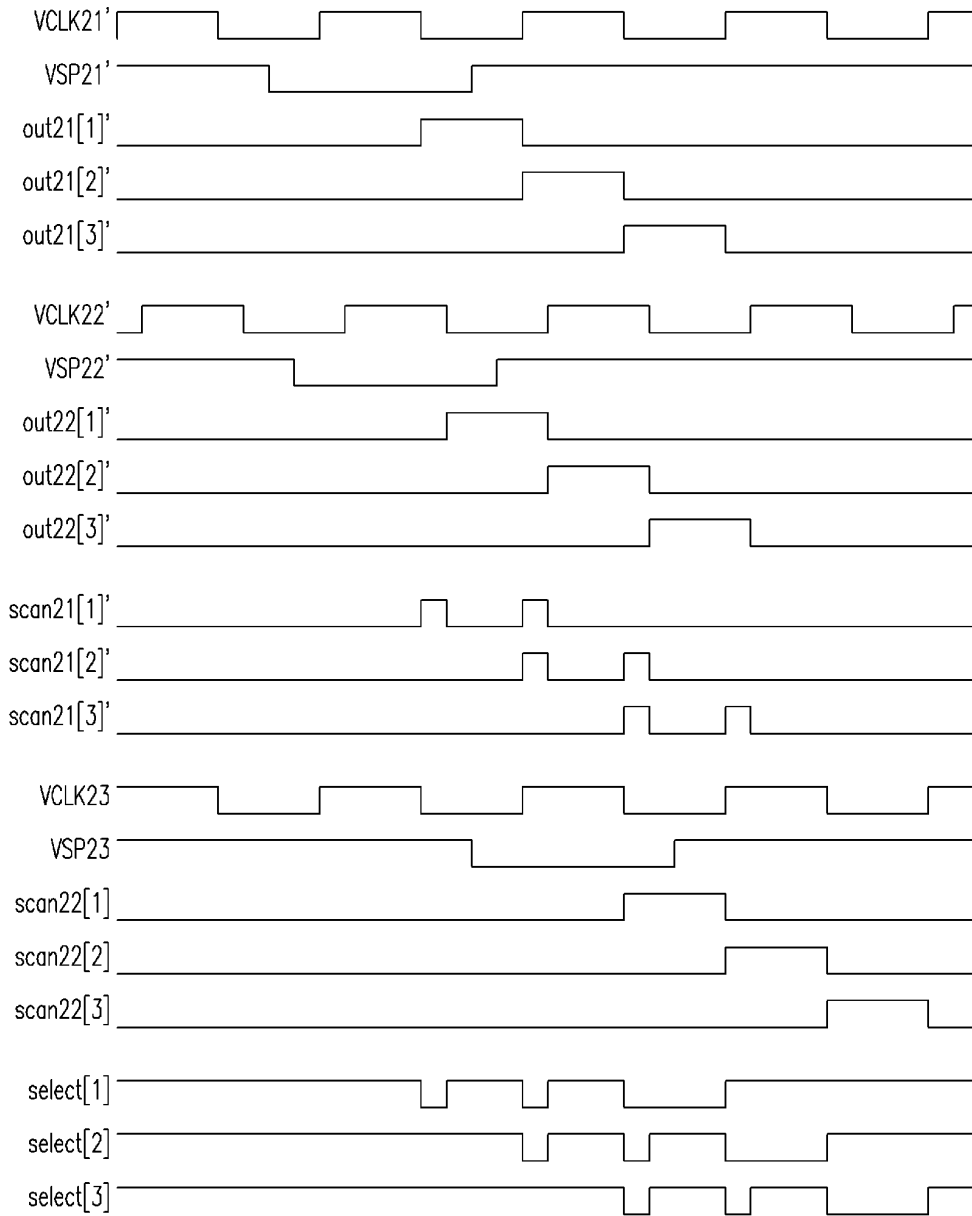


FIG.19

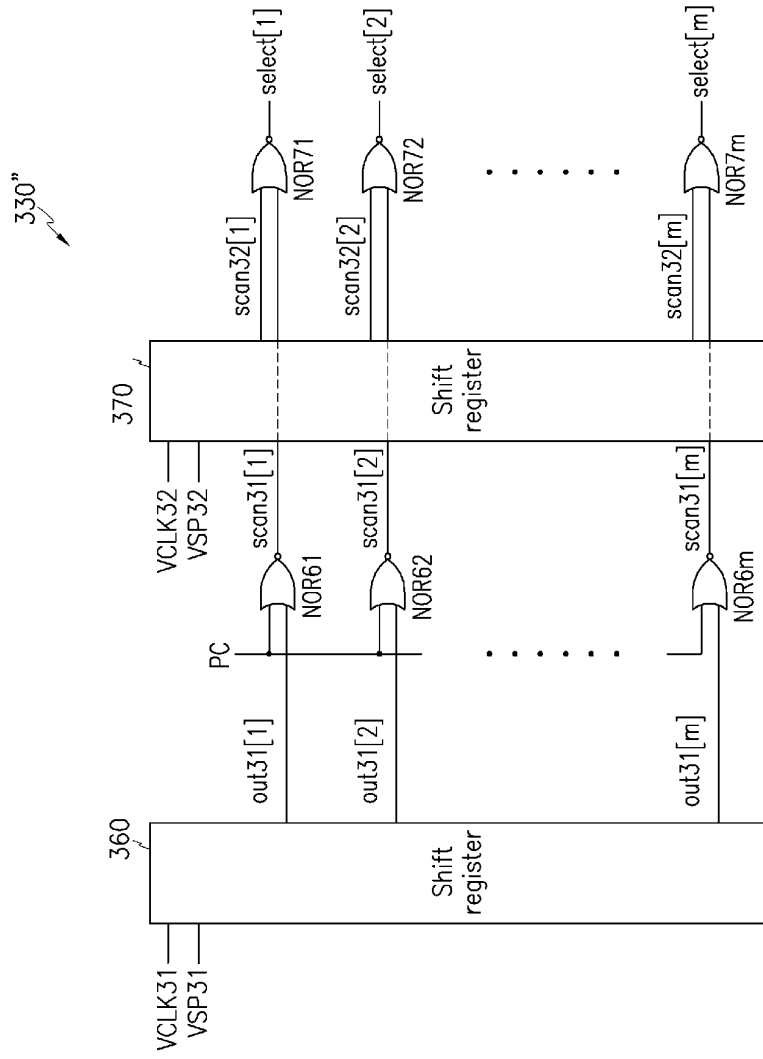


FIG.20

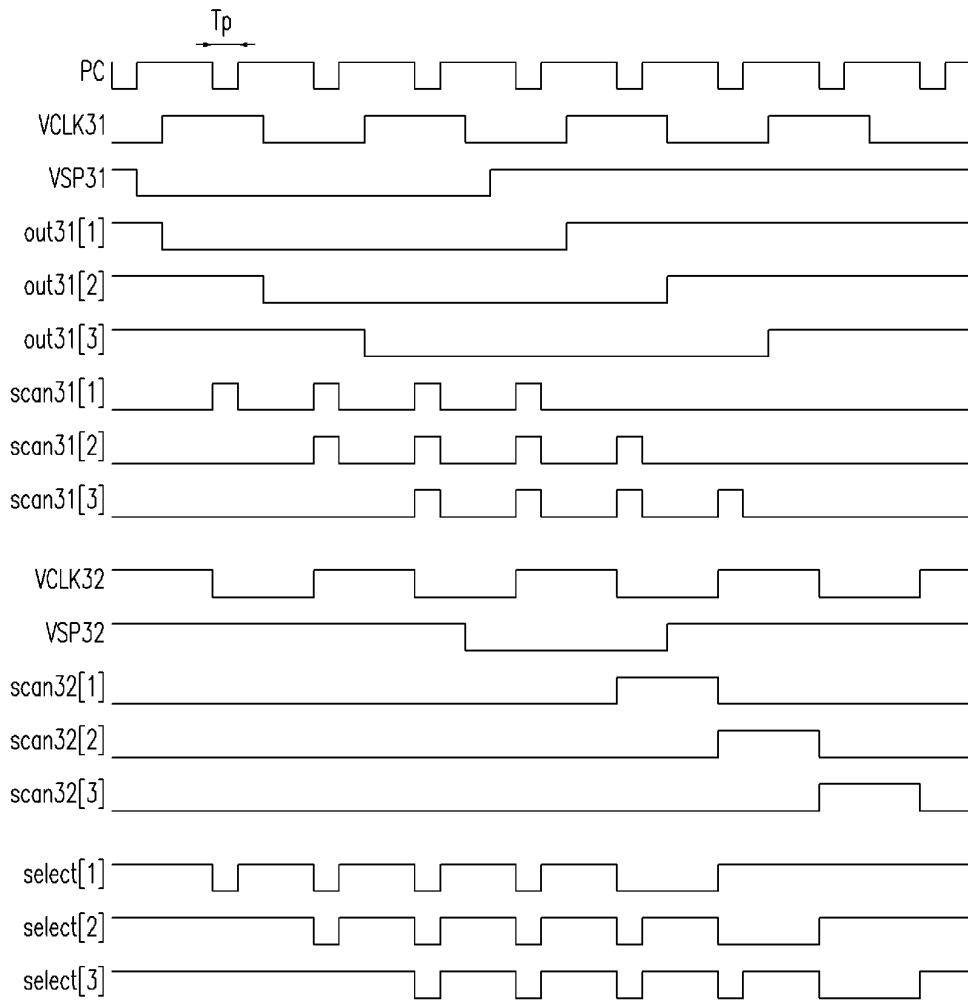


FIG.21

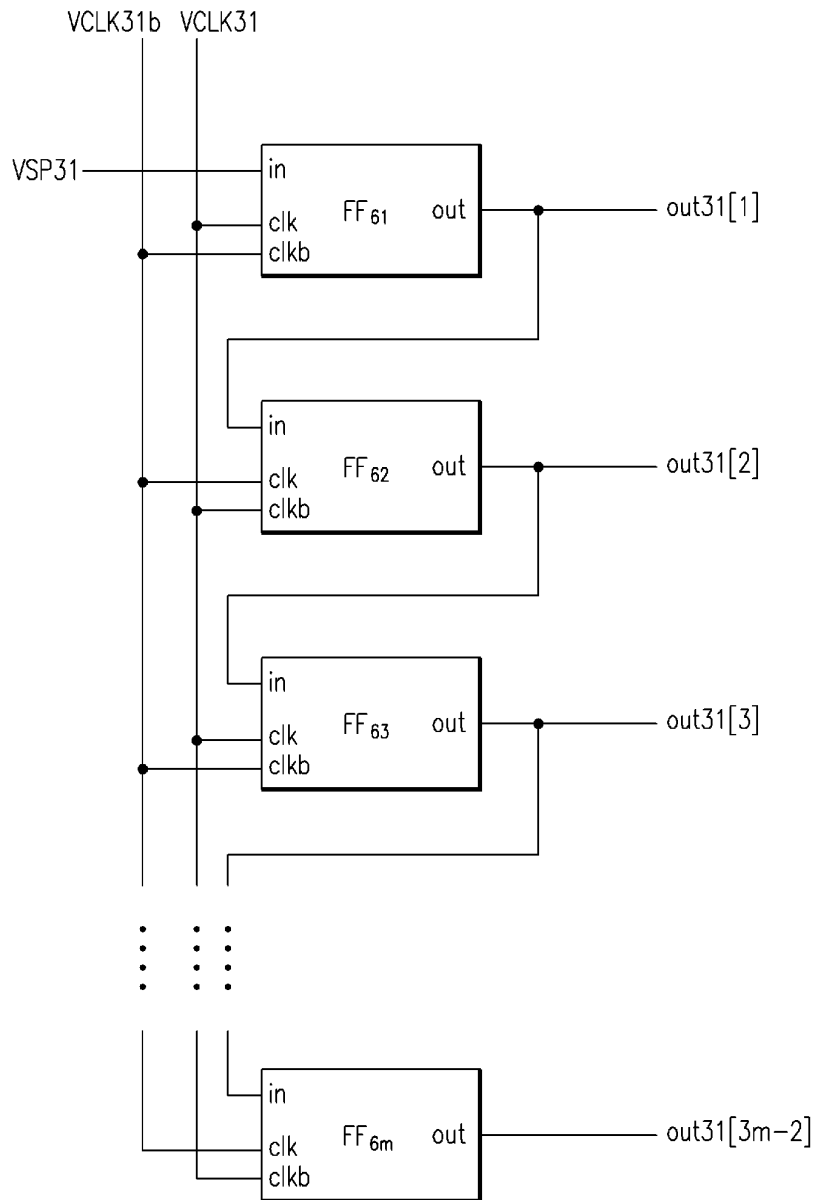


FIG.22

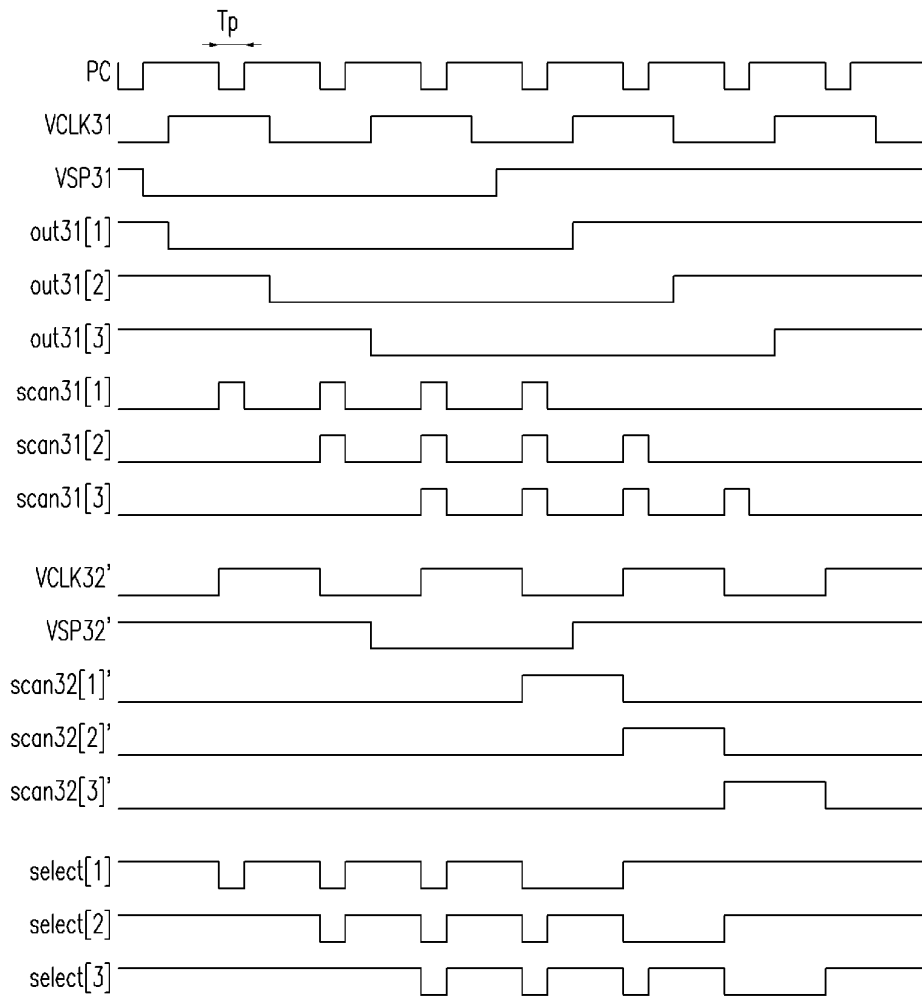


FIG.23

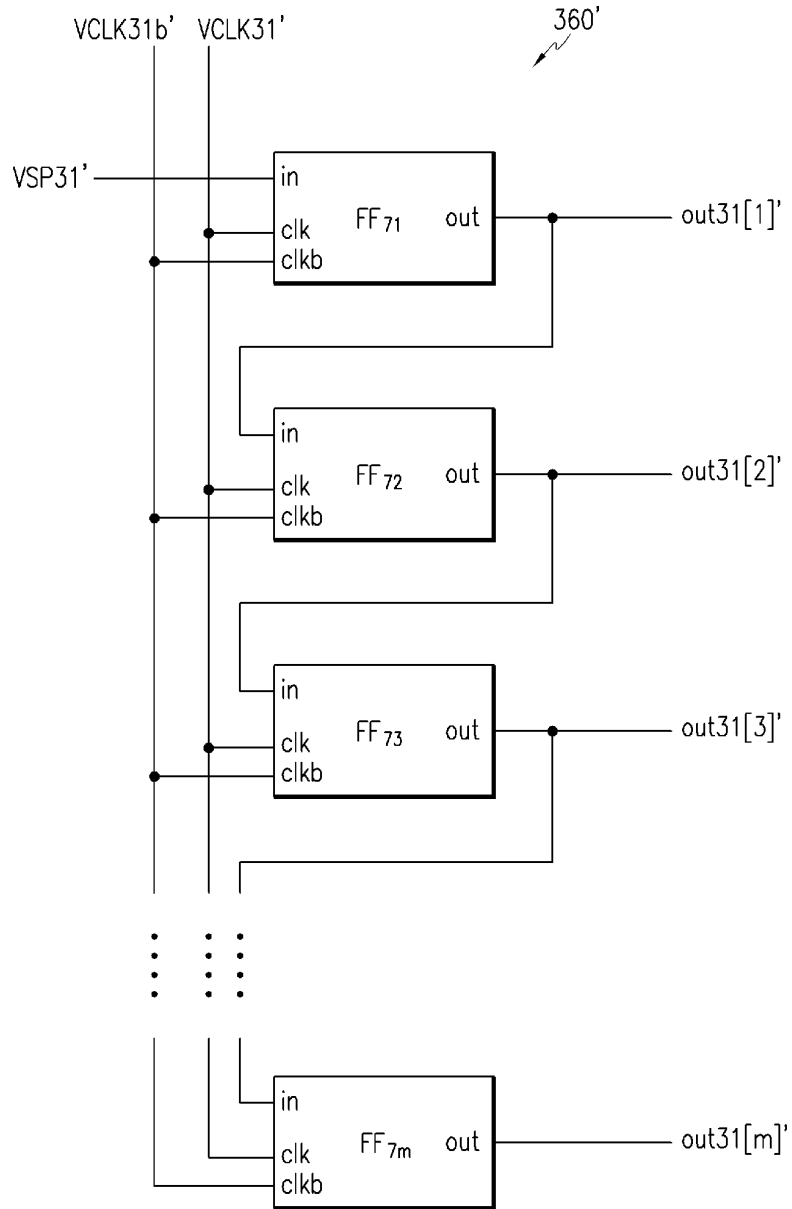


FIG.24

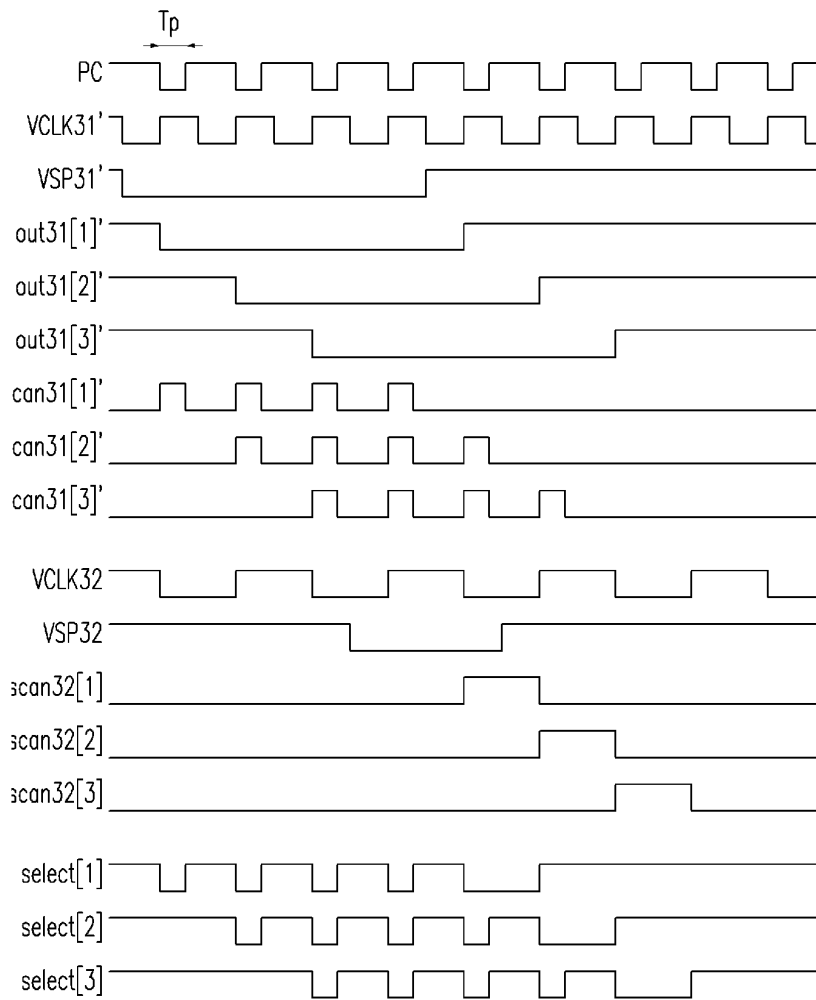
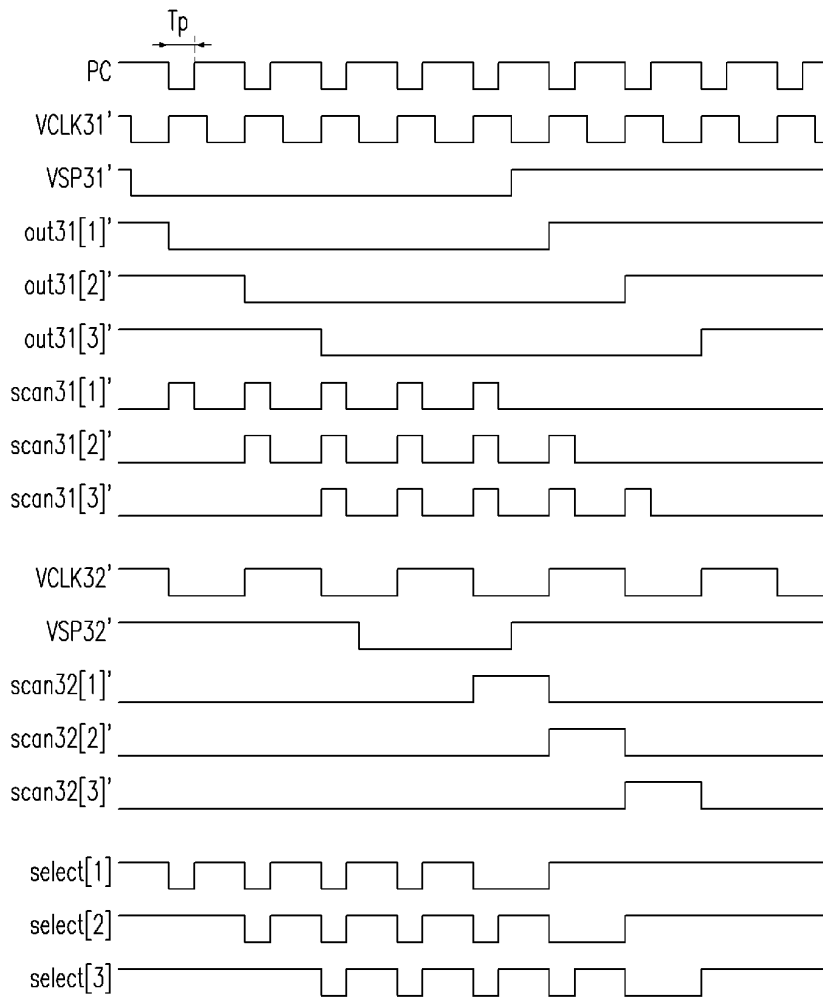


FIG.25



专利名称(译)	发光显示器及其驱动装置和方法		
公开(公告)号	<a href="#">EP1610293A2</a>	公开(公告)日	2005-12-28
申请号	EP2005105436	申请日	2005-06-21
[标]申请(专利权)人(译)	三星斯笛爱股份有限公司		
申请(专利权)人(译)	三星SDI CO. , LTD.		
当前申请(专利权)人(译)	三星SDI CO. , LTD.		
发明人	SHIN, DONG-YONG, LEGAL & IP TEAM, SAMSUNG SDI LTD		
IPC分类号	G09G3/20 G09G3/30 G09G3/32 G11C19/00		
CPC分类号	G09G3/325 G09G3/3266 G09G2300/0842 G09G2300/0861 G09G2310/0251 G11C19/00 G11C19/28		
代理机构(译)	hengelhaupt , Jürgen		
优先权	1020040048154 2004-06-25 KR 1020040048152 2004-06-25 KR 1020040048153 2004-06-25 KR		
其他公开文献	EP1610293B1 EP1610293A3		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

一种用于发光显示器的驱动装置，包括用于传输选择信号的多条扫描线，包括：第一驱动器，用于将具有第一整数倍的第一脉冲的第一信号移位第一周期，并依次输出第一驱动器信号；第二驱动器，用于将具有第二脉冲的第二信号移位第二周期，并顺序输出第二信号；第三驱动器，用于响应于第一信号和顺序输出具有与第一脉冲的第一整数倍中的至少一个相对应的第三整数倍的第二整数倍的选择信号，以及与第二脉冲相对应的第四脉冲。第二个信号。

Equation 
$$I_{OLED} = \frac{\beta}{2} (V_{GS} - V_{TH})^2 = I_{data}$$