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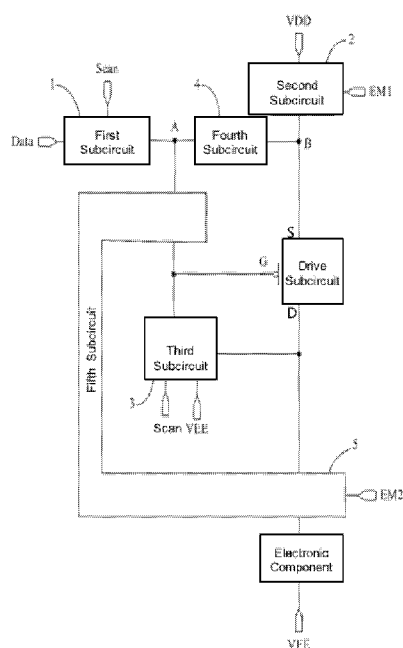


FIG. 1A

(57) Abstract: An electronic circuit for driving an electronic component is disclosed. The electronic circuit includes a drive subcircuit, a first subcircuit, a second subcircuit, a third subcircuit, a fourth subcircuit, and a fifth subcircuit. Under control of a data signal terminal, a scan signal terminal, a first control signal terminal, a second control signal terminal, a first power supply terminal, and a second power supply terminal, the drive subcircuit is configured to have a diode connection or a source-follower connection so as to maintain a substantially stable working current running through the electronic component. The electronic circuit can be a pixel circuit, and the electronic component can be a light-emitting component comprising an organic light-emitting diode (OLED). A display panel and a display apparatus containing the electronic circuit, as well as a method for driving the electronic circuit are also disclosed.

**ELECTRONIC CIRCUIT AND DRIVING METHOD,
DISPLAY PANEL, AND DISPLAY APPARATUS**

CROSS-REFERENCES TO RELATED APPLICATION

[001] The present application claims priority to Chinese Patent Application No. 201610543844.X filed on July 11, 2016, the disclosure of which is hereby incorporated by reference in its entirety.

TECHNICAL FIELD

[002] The present disclosure relates generally to the field of display technologies, and more specifically to an electronic circuit and its driving method, a display panel, and a display apparatus.

BACKGROUND

[003] Organic light-emitting diode (OLED) is a hot area in the current development of flat panel display devices. Compared with liquid crystal display (LCD) devices, OLED display devices typically have advantages such as low power consumption, low manufacturing cost, self-luminescence, wide viewing angle, and fast response speed. At present time, OLED display devices are starting to replace traditional LCD display devices, such as in cell phones, tablet computers, digital cameras, large-screen TVs, etc.

[004] Unlike an LCD, which employs a stable voltage to control its brightness, an OLED is driven by an electric current, and a stable current is needed for the control of light emission. For reasons related to manufacturing processes and component aging, the threshold voltage (V_{th}) of driver transistors of the pixel circuit is not constant, causing changes in the current flowing through each OLED, which in turn results in

5 non-uniform brightness of display, negatively influencing the whole image display effect.

[005] In addition, the current flowing through each OLED is related to the voltage of the source electrode of the associated driver transistor, i.e., the voltage of the power supply. A voltage drop across the circuits resulting from the product of the electrical
10 current (I) and the resistance (R), referred to as the IR Drop, can also result in differences in currents in different areas of the screen, in turn causing non-uniform brightness in OLEDs in different areas.

SUMMARY

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[006] In order to address the issues associated with current OLED display technologies, the present disclosure provides an electronic circuit and a driving method thereof, a display panel, and a display apparatus.

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[007] In a first aspect, an electronic circuit is disclosed, which is configured to maintain a substantially stable working current running through an electronic component.

[008] The electronic circuit includes a drive subcircuit, a first subcircuit, a second subcircuit, a third subcircuit, a fourth subcircuit, and a fifth subcircuit.

25

[009] The drive subcircuit includes a first terminal, a second terminal, and a third terminal. The first terminal is coupled to a second node. A current from a first terminal to a second terminal is controlled by a signal from a third terminal. The drive subcircuit is configured to drive the electronic component via the second terminal.

[010] The first subcircuit is coupled to a data signal terminal, a scan signal terminal and a first node, and the first subcircuit is configured to provide a signal from the data signal terminal to the first node under control of the scan signal terminal.

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[011] The second subcircuit is coupled to a first power supply terminal, a first control signal terminal and a second node, and the second subcircuit is configured to provide a signal from the first power supply terminal to the second node under control of the first control signal terminal.

- 5 **[012]** The third subcircuit is coupled to the scan signal terminal and a second power supply terminal, and is further coupled to the second terminal and the third terminal of the drive subcircuit. The third subcircuit is configured to control the drive subcircuit to have a diode connection or a source-follow connection via the scan signal terminal and the second power supply terminal.
- 10 **[013]** The fourth subcircuit is coupled to the first node and the second node, and the fourth subcircuit is configured to charge or discharge under control of a signal from the first node and a signal from the second node, and is further configured to maintain a stable voltage difference between the first node and the second node if the first node is in a floating state.
- 15 **[014]** The fifth subcircuit is coupled to a second control signal terminal, the first node, the second terminal, and the third terminal, of the drive subcircuit, and a first terminal of the electronic component. The fifth subcircuit is configured to electrically couple the first node with the third terminal of the drive subcircuit, and to electrically couple the second terminal of the drive subcircuit with the electronic component under control of the second control signal terminal, so as to control the drive subcircuit to drive the electronic component.
- 20 **[015]** Herein the drive subcircuit can be a driver transistor, and the electronic circuit can be a pixel circuit employed in light-emitting component such as an organic light-emitting diode (OLED), and can also be a circuit employed in other types of electronic components.
- 25 **[016]** According to some embodiments of the electronic circuit, the drive subcircuit includes a driver transistor. As such the first terminal, the second terminal, and the third terminal of the electronic circuit are respectively a source electrode, a drain electrode, and a gate electrode of the driver transistor.
- 30 **[017]** In the electronic circuit as described above, the third subcircuit can include a first sub-portion and a second sub-portion.
- [018]** A first terminal of the first sub-portion is coupled to the scan signal terminal; a second terminal of the first sub-portion is coupled to a signal terminal; and a third terminal of the first sub-portion is coupled to the gate electrode of the driver transistor.

5 **[019]** A first terminal of the second sub-portion is coupled to the scan signal terminal; a second terminal of the second sub-portion is coupled to the second power supply terminal; and a third terminal of the second sub-portion is coupled to the drain electrode of the driver transistor.

10 **[020]** Herein the first sub-portion is configured to provide a signal from the signal terminal to the gate electrode of the driver transistor under control of the scan signal terminal, wherein the signal has a voltage lower than or equal to a voltage of the second power supply terminal.

15 **[021]** Herein the second sub-portion is configured to provide a signal from the second power supply terminal to the drain electrode of the driver transistor under control of the scan signal terminal.

20 **[022]** In the embodiments of the electronic circuit as mentioned above, the first sub-portion includes a first switch transistor. A gate electrode of the first switch transistor is coupled to the scan signal terminal; a source electrode of the first switch transistor is coupled to the signal terminal; and a drain electrode of the first switch transistor is coupled to the gate electrode of the driver transistor.

25 **[023]** In the embodiments of the electronic circuit as mentioned above, the second sub-portion comprises a second switch transistor. A gate electrode of the second switch transistor is coupled to the scan signal terminal; a source electrode of the second switch transistor is coupled to the second power supply terminal; and a drain electrode of the second switch transistor is coupled to the drain electrode of the driver transistor.

[024] According to some embodiments of the electronic circuit, the signal terminal is the second power supply terminal.

30 **[025]** According to some other embodiments of the electronic circuit, the signal terminal is an initial signal terminal, which is configured to provide a signal having a voltage lower than the voltage of the second power supply terminal.

[026] In the electronic circuit, at least one of the first subcircuit, the second subcircuit, or the fifth subcircuit can include a switch transistor.

- 5 **[027]** In embodiments of electronic circuit where the first subcircuit includes a third switch transistor, a gate electrode of the third switch transistor can be coupled to the scan signal terminal; a source electrode of the third switch transistor can be coupled to the data signal terminal; and a drain electrode of the third switch transistor can be coupled to the first node.
- 10 **[028]** In embodiments of electronic circuit where the second subcircuit includes a fourth switch transistor, a gate electrode of the fourth switch transistor is coupled to the first control signal terminal; a source electrode of the fourth switch transistor is coupled to the first power supply terminal; and a drain electrode of the fourth switch transistor is coupled to the second node.
- 15 **[029]** In embodiments of electronic circuit where the fifth subcircuit comprises a fifth switch transistor and a sixth switch transistor, a gate electrode of the fifth switch transistor is coupled to the second control signal terminal; a source electrode of the fifth switch transistor is coupled to the first node; and a drain electrode of the fifth switch transistor is coupled to the gate electrode of the driver transistor; a gate electrode of the sixth switch transistor is coupled to the second control signal terminal; a source electrode of the sixth switch transistor is coupled to the drain electrode of the driver transistor; and a drain electrode of the sixth switch transistor is coupled to the first terminal of the electronic component.
- 20 **[030]** In the electronic circuit, the fourth subcircuit can include a capacitor. A first terminal of the capacitor is coupled to the first node; and a second terminal of the capacitor is coupled to the second node.
- 25 **[031]** In any of the embodiments of the electronic circuit as described above, the driver transistor can be a P-type transistor, and the electronic component can include a light-emitting component.
- 30 **[032]** Herein the light-emitting component can include an organic light-emitting diode (OLED), and the electronic circuit is accordingly configured to maintain the substantially stable working current through the driver transistor independent of a threshold voltage of the driver transistor or a power supply voltage of the first power supply terminal.

5 **[033]** In a second aspect, the present disclosure further provides a display panel. The display panel includes an electronic circuit according to any of the embodiments as mentioned above.

10 **[034]** In a third aspect, the present disclosure further provides a display apparatus. The display apparatus includes a display panel according to any of the embodiments as mentioned above.

[035] In a fourth aspect, the present disclosure further provides a method of driving the electronic circuit. The method comprises a first stage, a second stage, a third stage, and a fourth stage.

15 **[036]** During the first stage, the first subcircuit provides a signal from the data signal terminal to the first node under control of the scan signal terminal; the second subcircuit provides a signal from the first power supply terminal to the second node under control of the first control terminal; the fourth subcircuit charges under control of the signal from the first node and the signal from the second node; and the third subcircuit controls the driver transistor to have a diode connection or a source-follow connection via the signal terminal and the second power supply terminal.

20 **[037]** During the second stage, the first subcircuit provides a signal from the data signal terminal to the first node under control of the scan signal terminal; the third subcircuit controls the driver transistor to have a diode connection or a source-follow connection via the signal terminal and the second power supply terminal; and the fourth subcircuit discharges under control of the signal from the first node and the signal from the second node.

25 **[038]** During the third stage, the second subcircuit provides a signal from the first power supply terminal to the second node under control of the first control signal terminal; and the fourth subcircuit maintains a stable voltage difference between the first node and the second node when the first node is in a floating state.

30 **[039]** During the fourth stage, the second subcircuit provides a signal from the first power supply terminal to the second node under control of the first control signal terminal; and the fifth subcircuit conducts the first node with the gate electrode of the driver transistor and conducts the drain electrode of the driver transistor with the

5 electronic component under control of the second control signal terminal, to thereby control the driver transistor to drive the electronic component.

[040] In the method as described above, during a saturation mode of the driver transistor, the working current flowing through the driver transistor can be independent of a threshold voltage of the driver transistor or a power supply voltage of the first power supply terminal.

[041] According to some embodiments of the method, the signal terminal is an initial signal terminal configured to provide a signal having a voltage lower than the voltage of the second power supply terminal, and the third subcircuit controls the driver transistor to have a source-follow connection via the signal terminal and the second power supply terminal.

[042] Herein, the working current flowing through the driver transistor satisfies the following formula:

$$[043] \quad I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{DD} - V_{Int} + V_{th} - V_{DD}) - V_{th}]^2 = K(V_{Data} - V_{Int})^2$$

[044] where I_L represents the working current flowing through the driver transistor; V_{GS} represents the gate-source voltage of the driver transistor; K is a structure parameter; V_{Int} represents the voltage of the initial signal terminal Int; V_{Data} represents the voltage of the data signal terminal Data; V_{th} represents the threshold voltage of the driver transistor; and V_{dd} represents the voltage of the first power supply terminal.

[045] According to some other embodiments of the method, the signal terminal is the second power supply terminal, and the third subcircuit controls the driver transistor to have a diode connection.

[046] Herein, the working current flowing through the driver transistor satisfies the following formula:

$$[047] \quad I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{DD} - V_{EE} + V_{th} - V_{DD}) - V_{th}]^2 = K(V_{Data} - V_{EE})^2$$

[048] where I_L represents the working current flowing through the driver transistor; V_{GS} represents the gate-source voltage of the driver transistor; K is a structure

parameter; V_{EE} represents the voltage of the second power supply terminal; V_{Data} represents the voltage of the data signal terminal Data; V_{th} represents the threshold voltage of the driver transistor; and V_{dd} represents the voltage of the first power supply terminal.

[049] In any of the aforementioned embodiments of the method, the electronic component includes a light-emitting component, which can comprise an organic light-emitting diode (OLED).

[050] Other embodiments may become apparent in view of the following descriptions and the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[051] To more clearly illustrate some of the embodiments disclosed herein, the following is a brief description of the drawings. The drawings in the following descriptions are only illustrative of some embodiments. For those of ordinary skill in the art, other drawings of other embodiments can become apparent based on these drawings.

[052] FIG. 1A is a schematic diagram of an electronic circuit according to some other embodiments of the present disclosure;

[053] FIG. 1B is a schematic diagram of a pixel circuit according to some embodiments of the present disclosure;

[054] FIG. 1C is a schematic diagram of a pixel circuit according to some other embodiments of the present disclosure;

[055] FIG. 2A is a circuit diagram of a pixel circuit according to a first embodiment of the present disclosure;

[056] FIG. 2B is a circuit diagram of a pixel circuit according to a second embodiment of the present disclosure;

[057] FIG. 2C is a circuit diagram of a pixel circuit according to a third embodiment

5 of the present disclosure;

[058] FIG. 2D is a circuit diagram of a pixel circuit according to a fourth embodiment of the present disclosure;

[059] FIG. 2E is a circuit diagram of a pixel circuit according to a fifth embodiment of the present disclosure;

10 [060] FIG. 2F is a circuit diagram of a pixel circuit according to a sixth embodiment of the present disclosure;

[061] FIG. 3A is a time sequence diagram of the pixel circuit as shown in FIG. 2A;

[062] FIG. 3B is a time sequence diagram of the pixel circuit as shown in FIG. 2B;

15 [063] FIG. 4 is a flowchart illustrating a driving method of a pixel circuit according to some embodiments.

DETAILED DESCRIPTION

[064] In the following, with reference to the drawings of various embodiments disclosed herein, the technical solutions of the embodiments of the disclosure will be described in a clear and fully understandable way.

[065] It is obvious that the described embodiments are merely a portion but not all the embodiments of the disclosure. Based on the described embodiments of the disclosure, those ordinarily skilled in the art can obtain other embodiment(s), which come(s) within the scope sought for protection by the disclosure.

25 [066] In a first aspect, the present disclosure provides an electronic circuit, which is configured to maintain a substantially stable working current running through an electronic component.

[067] As illustrated in FIG. 1A, the electronic circuit comprises a drive subcircuit, a first subcircuit, a second subcircuit, a third subcircuit, a fourth subcircuit, and a fifth subcircuit.

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- 5 **[068]** The drive subcircuit comprises a first terminal, a second terminal, and a third terminal, wherein the first terminal is coupled to a second node; a current from a first terminal to a second terminal is controlled by a signal from a third terminal, and the drive subcircuit is configured to drive the electronic component via the second terminal;
- 10 **[069]** The first subcircuit is coupled to a data signal terminal, a scan signal terminal and a first node, and is configured to provide a signal from the data signal terminal to the first node under control of the scan signal terminal;
- 15 **[070]** The second subcircuit is coupled to a first power supply terminal, a first control signal terminal and a second node, and is configured to provide a signal from the first power supply terminal to the second node under control of the first control signal terminal;
- 20 **[071]** The third subcircuit is coupled to the scan signal terminal and a second power supply terminal and to the second terminal and the third terminal of the drive subcircuit, and the third subcircuit is configured to control the drive subcircuit to have a diode connection or a source-follow connection via the scan signal terminal and the second power supply terminal;
- 25 **[072]** The fourth subcircuit is coupled to the first node and the second node, and is configured to charge or discharge under control of a signal from the first node and a signal from the second node, and to maintain a stable voltage difference between the first node and the second node if the first node is in a floating state;
- 30 **[073]** The fifth subcircuit is coupled to a second control signal terminal, the first node, the second terminal, and the third terminal, of the drive subcircuit, and a first terminal of the electronic component, and is configured to electrically couple the first node with the third terminal of the drive subcircuit, and to electrically couple the second terminal of the drive subcircuit with the electronic component under control of the second control signal terminal, so as to control the drive subcircuit to drive the electronic component.
- [074]** Herein the drive subcircuit can be a driver transistor, and the electronic circuit can be a pixel circuit employed in light-emitting component such as an organic

5 light-emitting diode (OLED), and can also be a circuit employed in other types of electronic components. There are no limitations.

[075] In the following, detailed description over the electronic circuit as mentioned above will be provided with pixel circuit as an illustrating example.

10 [076] Accordingly, in the pixel circuit disclosed herein, the drive subcircuit, the first subcircuit, the second subcircuit, the third subcircuit, and the fourth subcircuit, and the fifth subcircuit as mentioned above in the electronic circuit are respectively a drive subcircuit, a data writing subcircuit, a power supply voltage control subcircuit, a conduction control subcircuit, a storage subcircuit, and a light-emitting control subcircuit.

15 [077] The scan signal terminal, the data signal terminal, the first control signal terminal, the second control signal terminal, the first power supply terminal, the second power supply terminal, and the signal terminal as mentioned above in the electronic circuit are a scan signal terminal (Scan), a data signal terminal (Data), a first light-emitting control signal terminal (EM1), a second light-emitting control signal terminal (EM2), a first power supply terminal (VDD), a second power supply terminal (VEE), and an signal terminal (Int) in the pixel circuit, respectively.

25 [078] FIG. 1B illustrates a pixel circuit according to some embodiments of the present disclosure. As shown in FIG. 1B, the pixel circuit comprises a data writing subcircuit 1, a power supply voltage control subcircuit 2, a conduction control subcircuit 3, a storage subcircuit 4, a light-emitting control subcircuit 5, a driver transistor M0, and a light-emitting component L. Herein, a subcircuit can be a modular design, and can be referred also as a module. A subcircuit can also be a portion of a circuit, include one or more components, or an electronic device itself.

30 [079] A first terminal of the data writing subcircuit 1 is electrically coupled to a scan signal terminal Scan; a second terminal of the data writing subcircuit 1 is electrically coupled to a data signal terminal Data; and a third terminal of the data writing subcircuit 1 is electrically coupled to a first node A. The data writing subcircuit 1 is configured to provide a signal from the data signal terminal Data to the first node A under control of the scan signal terminal Scan. The electrical coupling can be

5 realized with a direct electrical connection, such as through a wire, or can be realized through intermediate electronic components such as transistors, capacitors, etc.

[080] A first terminal of the power supply voltage control subcircuit 2 is electrically coupled to a first light-emitting control signal terminal EM1; the second terminal of the power supply voltage control subcircuit 2 is electrically coupled to a first power supply terminal VDD; and a third terminal of the power supply voltage control subcircuit 2 is respectively electrically coupled to a second node B and a source electrode S of the driver transistor M0. The power supply voltage control subcircuit 2 is configured to provide a signal from the first power supply terminal VDD to the second node B under control of the first light-emitting control signal terminal EM1.

[081] A first terminal of the conduction control subcircuit 3 is electrically coupled to an initial signal terminal Int; a second terminal of the conduction control subcircuit 3 is electrically coupled to a second power supply terminal VEE; a third terminal of the conduction control subcircuit 3 is electrically coupled to a gate electrode G of the driver transistor M0; and a fourth terminal of the conduction control subcircuit 3 is electrically coupled to a drain electrode D of the driver transistor M0. The conduction control subcircuit 3 is configured to control the driver transistor M0 to be in a diode state through the initial signal terminal Int and the second power supply terminal VEE.

[082] A first terminal of the storage subcircuit 4 is electrically coupled to the first node A; and a second terminal of the storage subcircuit 4 is electrically coupled to the second node B. The storage subcircuit 4 is configured to charge or discharge under control of both a signal from the first node A and a signal from the second node B, and to maintain a stable voltage difference between the first node A and the second node B when the first node A is in a floating state.

[083] A first terminal of the light-emitting control subcircuit 5 is electrically coupled to a second light-emitting control signal terminal EM2; a second terminal of the light-emitting control subcircuit 5 is electrically coupled to the first node A; a third terminal of the light-emitting control subcircuit 5 is electrically coupled to the gate electrode G of the driver transistor M0; a fourth terminal of the light-emitting control

subcircuit 5 is electrically coupled to the drain electrode D of the driver transistor M0; a fifth terminal of the light-emitting control subcircuit 5 is electrically coupled to a first terminal of the light-emitting component L, whereas a second terminal of the light-emitting component L is electrically coupled to the second power supply terminal VEE.

[084] The light-emitting control subcircuit 5 is configured to electrically couple the first node A with the gate electrode G of the driver transistor M0, and to electrically couple the drain electrode D of the driver transistor M0 with the light-emitting component L under the control of the second light-emitting control signal terminal EM2, so as to control the driver transistor M0 to drive the light-emitting component L to emit light.

[085] In the embodiment of the pixel circuit as described above, the pixel circuit comprises a data writing subcircuit, a power supply voltage control subcircuit, a conduction control subcircuit, a storage subcircuit, a light-emitting control subcircuit, the driver transistor, and a light-emitting component.

[086] The data writing subcircuit is configured to provide a signal from the data signal terminal to the first node under control of the scan signal terminal. The power supply voltage control subcircuit is configured to provide a signal from the first power supply terminal to the second node under control of the first light-emitting control signal terminal. The conduction control subcircuit is configured to control the driver transistor to be in a diode state through the initial signal terminal and the second power supply terminal. The storage subcircuit is configured to charge and discharge under the common control of a signal from the first node and a signal from the second node and to maintain a stable voltage difference between the first node and the second node when the first node is in floating state. The light-emitting control subcircuit is configured to electrically couple the first node with the gate electrode of the driver transistor, and to electrically couple the drain electrode of the driver transistor with the light-emitting component to control the driver transistor to drive the light-emitting component to thereby emit light.

[087] In the pixel circuit as described above, through a coordination of the

5 aforementioned five subcircuits and the driver transistor, the working current of the driver transistor in the pixel circuit that drives the light-emitting component to emit light can be allowed to be related only to the voltage of the data signal terminal and the voltage of the initial signal terminal, but not related to the threshold voltage of the driver transistor and the voltage of the first power supply terminal. As such, the influence of the threshold voltage of the driver transistor and the influence of IR Drop to the working current flowing through the light-emitting component can be avoided, thereby the working current that drives the light-emitting component can be maintained to be stable. Therefore, an improved uniformity of the brightness of the images in the display area of the display apparatus can be achieved.

15 **[088]** In some embodiments of the pixel circuit as described above, as shown in FIG. 1B, the driver transistor M0 can be a P-type transistor. Because the shreshold voltage of a P-type transistor V_{th} is generally a negative value, in order to ensure the driver transistor M0 to work normally, the voltage VDD at the first power supply terminal is generally set as a positive value, and the voltage VEE at the second power supply terminal is generally set as ground (zero), or a negative value.

25 **[089]** In some embodiments of the pixel circuit, the voltage of the first power supply terminal VDD is larger than the voltage of the second power supply terminal VEE, and the voltage of the initial signal terminal V_{int} . In addition, the voltage (V_{dd}) of the first power supply terminal VDD and the voltage of the initial signal terminal V_{int} can satisfy: $V_{dd} > V_{int} - V_{th}$.

[090] In the pixel circuit as described above, the light-emitting component can be an OLED, which emits light upon application of an eletric current when the driver transistor is in a saturatation mode.

30 **[091]** In some other embodiments of the pixel circuit, as shown in FIG. 1C, the conduction control subcircuit 3 can comprise: a first conduction control sub-portion 31, and a second conduction control sub-portion 32.

[092] A first terminal of the first conduction control sub-portion 31 is electrically coupled to the scan signal terminal Scan; a second terminal of the first conduction control sub-portion 31 is electrically coupled to the initial signal terminal Int; and a

third terminal of the first conduction control sub-portion 31 is electrically coupled to the gate electrode G of the driver transistor M0. The first conduction control sub-portion 31 is configured to provide a signal from the initial signal terminal Int to the gate electrode G of the driver transistor M0 under control of the scan signal terminal Scan.

[093] A first terminal of the second conduction control sub-portion 32 is electrically coupled to the scan signal terminal Scan; a second terminal of the second conduction control sub-portion 32 is electrically coupled to the second power supply terminal VEE; and a third terminal of the second conduction control sub-portion 32 is electrically coupled to the drain electrode D of the driver transistor M0. The second conduction control sub-portion 32 is configured to provide a signal from the second power supply terminal VEE to the drain electrode D of the driver transistor M0 under control of the scan signal terminal Scan.

[094] The pixel circuit according to some embodiments disclosed herein will be described in more detail below. It is noted that these specific embodiments or implementations are only for illustrative purposes, and do not impose limitations on the scope of the present disclosure.

[095] For example, in the various embodiments of the pixel circuit as illustrated in FIGS. 2A–2D, the first conduction control sub-portion 31 can comprise a first switch transistor M1.

[096] A gate electrode of the first switch transistor M1 is electrically coupled to the scan signal terminal Scan; a source electrode of the first switch transistor M1 is electrically coupled to the initial signal terminal Int; and a drain electrode of the first switch transistor M1 is electrically coupled to the gate electrode G of the driver transistor M0.

[097] According to some specific implementations of the pixel circuit as shown in FIG. 2A and FIG. 2C, the first switch transistor M1 can be a P-type switch transistor. Alternatively, according to some other specific implementations of the pixel circuit as shown in FIG. 2B and FIG. 2D, the first switch transistor M1 can be an N-type transistor. There are no limitations herein.

5 **[0098]** In specific implementations, in the pixel circuit according to the
aforementioned embodiments of the present disclosure, the first switch transistor M1
can be configured to provide a signal from the initial signal terminal Int to the gate
electrode G of the driver transistor M0, when it is in a conductive state under the
control of the scan signal terminal SCAN.

10 **[0099]** It is noted that the above specific embodiments are only examples for
illustrating the specific structures of the first conduction control sub-portion in the
pixel circuit according to some embodiments of the present disclosure. In practical
implementation, the specific structures of the first conduction control sub-portion are
not limited to the structures as described above, and can also adopt other structures
15 that can be understood by those skilled in the art. There are no limitations herein.

[0100] Specifically, in the various embodiments of the pixel circuit as illustrated in
FIGS. 2A-2D, the second conduction control sub-portion 32 can comprise a second
switch transistor M2.

20 **[0101]** A gate electrode of the second switch transistor M2 is electrically coupled to
the scan signal terminal Scan; a source electrode of the second switch transistor M2
is electrically coupled to the second power supply terminal VEE; and a drain
electrode of the second switch transistor M2 is electrically coupled to the drain
electrode D of the driver transistor M0.

25 **[0102]** According to some specific implementations of the pixel circuit as shown in
FIG. 2A and FIG. 2C, the second switch transistor M2 can be a P-type switch
transistor. Alternatively, according to some other specific implementations of the
pixel circuit as shown in FIG. 2B and FIG. 2D, the second switch transistor M2 can
be an N-type transistor. There are no limitations herein.

30 **[0103]** In some specific implementations, in the pixel circuit according to some
embodiments of the present disclosure, the second switch transistor M2 is
configured to provide a signal from the second power supply terminal VEE to the
drain electrode D of the driver transistor M0, when it is in a conductive state under
control of the scan signal terminal SCAN.

[0104] In the embodiments of the pixel circuit as shown in any one of FIGS. 2A-2D,

5 where the first conduction control sub-portion 31 comprises the first switch transistor M1, and the second conduction control sub-portion 32 comprises the second switch transistor M2, if a signal from the scan signal terminal SCAN turns on the first switch transistor M1 and the second switch transistor M2, the gate electrode G of the driver transistor M0 is conductive with the initial signal terminal Int, and
10 the drain electrode D of the driver transistor M0 is conductive with the second power supply terminal VEE, thereby realizing a source-follow connection for the driver transistor M0. It is noted that in order to ensure the source-follow connection for the driver transistor M0, it is required that $V_{Int} < V_{EE}$.

[0105] Herein by such a configuraton, it substantially realizes a source-follow
15 connection for the driver transistor M0 under control of the scan signal terminal SCAN, the initial signal terminal Int, and the the second power supply terminal VEE, which causes the threshold voltage (V_{th}) of the driver transistor M0 to be compensated to thereby allow the working current flowing through the driver transistor M0 to be unaffected by the threshold voltage (V_{th}) of driver transistor M0
20 and thus become substantially stable.

[0106] It is noted that besides the above embodiments of the pixel circuit as shown in FIGS. 2A-2D, other embodiments are also possible.

[0107] In one embodiment, as shown in FIG. 2E, the circuit diagram for the second switch transistor M2 is substantially identical to the emboidments shown in FIGS.
25 2A-2D (i.e., a gate electrode of the second switch transistor M2 is electrically coupled to the scan signal terminal Scan; a source electrode of the second switch transistor M2 is electrically coupled to the second power supply terminal VEE; and a drain electrode of the second switch transistor M2 is electrically coupled to the drain electrode D of the driver transistor M0). Yet the circuit diagram for the first switch transistor M1 differs from the emboidments shown in FIGS. 2A-2D by having a source electrode of the first switch transistor M1 electrically coupled to the second power supply terminal VEE, while other connections are substantially same (i.e. gate electrode of the first switch transistor M1 is electrically coupled to the scan signal terminal Scan; a drain electrode of the first switch transistor M1 is electrically
30 coupled to the gate electrode G of the driver transistor M0).
35

5 **[0108]** In another embodiment as shown in FIG. 2F, the circuit diagram for the second switch transistor M2 is substantially identical to the embodiments shown in FIGS. 2A-2D (i.e., a gate electrode of the second switch transistor M2 is electrically coupled to the scan signal terminal Scan; a source electrode of the second switch transistor M2 is electrically coupled to the second power supply terminal VEE; and a drain electrode of the second switch transistor M2 is electrically coupled to the drain electrode D of the driver transistor M0). Yet the circuit diagram for the first switch transistor M1 differs from the embodiments shown in FIGS. 2A-2D by having a source electrode of the first switch transistor M1 electrically coupled to the source electrode of the second switch transistor M2, while other connections are substantially same (i.e. gate electrode of the first switch transistor M1 is electrically coupled to the scan signal terminal Scan; a drain electrode of the first switch transistor M1 is electrically coupled to the gate electrode G of the driver transistor M0).

20 **[0109]** In both the embodiments as mentioned above and as illustrated in FIG. 2E and FIG. 2F, the source electrode of the first switch transistor M1 is electrically coupled to the second power supply terminal VEE. As such, when the scan signal terminal SCAN turns on the first switch transistor M1 and the second switch transistor M2, the gate electrode G of the driver transistor M0 is electrically coupled to the second power supply terminal VEE via the first switch transistor M1, and the drain electrode D of the driver transistor M0 is also electrically coupled to the second power supply terminal VEE via the second switch transistor M2, thereby equaling to a connection between the gate electrode G and the drain electrode D of the driver transistor M0.

30 **[0110]** Herein by such a configuration, it substantially realizes a diode connection for the driver transistor M0 under control of the scan signal terminal SCAN and the second power supply terminal VEE, which causes the threshold voltage (V_{th}) of the driver transistor M0 to be compensated to thereby allow the working current flowing through the driver transistor M0 to be unaffected by the threshold voltage (V_{th}) of driver transistor M0 and thus become substantially stable.

35 **[0111]** It is noted that the above specific embodiments are only examples for

5 illustrating the specific structures of the second conduction control sub-portion in the pixel circuit according to some embodiments of the present disclosure. In practical implementations, the specific structures of the second conduction control sub-portion are not limited to the structures as described above, and can also adopt other structures that can be understood by those skilled in the art. There are no
10 limitations herein.

[0112] In the various embodiments of the pixel circuit as illustrated in FIGS. 2A-2F, the data writing subcircuit 1 can comprise a third switch transistor M3 according to some implementations.

[0113] A gate electrode of the third switch transistor M3 is electrically coupled to the scan signal terminal Scan; a source electrode of the third switch transistor M3 is
15 electrically coupled to the data signal terminal Data; and a drain electrode of the third switch transistor M3 is electrically coupled to the first node A.

[0114] According to some specific implementations of the pixel circuit as shown in FIG. 2A and FIG. 2C, the third switch transistor M3 can be a P-type switch transistor. Alternatively, according to some other specific embodiments of the pixel circuit as
20 shown in FIG. 2B and FIG. 2D, the third switch transistor M3 can also be an N-type switch transistor. There are no limitations herein.

[0115] In some specific implementations, in the pixel circuit according to some embodiments of the present disclosure, the third switch transistor can be configured to provide a signal from the data signal terminal to the first node when it is in a
25 conductive state under control of the scan signal terminal.

[0116] It is noted that the above specific embodiments are only examples for illustrating the specific structures of the data writing subcircuit in the pixel circuit according to some embodiments of the present disclosure. In practical
30 implementations, the specific structures of the data writing subcircuit are not limited to the structures as described above, and can also adopt other structures that can be understood by those skilled in the art. There are no limitations herein.

[0117] In some specific implementations, in the pixel circuit as illustrated in FIGS. 2A-2F, the power supply voltage control subcircuit 2 can comprise a fourth switch

5 transistor M4.

[0118] A gate electrode of the fourth switch transistor M4 is electrically coupled to the first light-emitting control signal terminal EM1; a source electrode of the fourth switch transistor M4 is electrically coupled to the first power supply terminal VDD; and a drain electrode of the fourth switch transistor M4 is electrically coupled to the second node B.

[0119] According to some specific implementations of the pixel circuit as shown in FIG. 2A and FIG. 2D, the fourth switch transistor M4 can be a P-type switch transistor. Alternatively, according to some other specific embodiments of the pixel circuit as shown in as shown in FIG. 2B and FIG. 2C, the fourth switch transistor M4 can also be an N-type switch transistor. There are no limitations herein.

[0120] In some specific implementations of the pixel circuit, the fourth switch transistor can be configured to provide a signal from the first power supply terminal to the second node, when it is in a conductive state under control of the first light-emitting control signal terminal.

[0121] It is noted that the above specific embodiments are only examples for illustrating the specific structures of the power supply voltage control subcircuit in the pixel circuit according to some embodiments of the present disclosure. In practical implementation, the specific structures of the power supply voltage control subcircuit are not limited to the structures as described above, and can also adopt other structures that can be understood by those skilled in the art. There are no limitations herein.

[0122] For example, in the various embodiments of the pixel circuit as illustrated in FIGS. 2A–2D, the light-emitting control subcircuit 5 can specifically comprise a fifth switch transistor M5, and a sixth switch transistor M6.

[0123] A gate electrode of the fifth switch transistor M5 is electrically coupled to the second light-emitting control signal terminal EM2; a source electrode of the fifth switch transistor M5 is electrically coupled to the first node A; and a drain electrode of the fifth switch transistor M5 is electrically coupled to the gate electrode G of the driver transistor M0.

5 **[0124]** A gate electrode of the sixth switch transistor M6 is electrically coupled to the second light-emitting control signal terminal EM2; a source electrode of the sixth switch transistor M6 is electrically coupled to the drain electrode D of the driver transistor M0; and a drain electrode of the sixth switch transistor M6 is electrically coupled to the first terminal of the light-emitting component L.

10 **[0125]** According to some specific implementations of the pixel circuit as shown in FIG. 2A and FIG. 2D, the fifth switch transistor M5 and the sixth switch transistor M6 can be P-type transistors. Alternatively, according to some other specific implementations of the pixel circuit as shown in FIG. 2B and FIG. 2C, the fifth switch transistor M5 and the sixth switch transistor M6 can also be N-type
15 transistors. There are no limitations herein.

[0126] In some specific implementations, the fifth switch transistor can be configured, when the fifth switch transistor is in a conductive state under the control of the second light-emitting control signal terminal, to electrically couple the first node with the second node to thereby provide a signal from the first node to the second
20 node, and to thereby at least provide the threshold voltage of the driver transistor and the voltage of the first power supply terminal to the gate electrode of the driver transistor.

[0127] The sixth switch transistor can be configured, when the sixth switch transistor is in a conductive state under control of the second light-emitting control signal terminal, to electrically couple the drain electrode of the driver transistor with the
25 light-emitting component to thereby control the driver transistor to drive the light-emitting component to emit light.

[0128] It is noted that the above specific embodiments are only examples for illustrating the specific structures of the light-emitting control subcircuit in the pixel circuit according to some embodiments of the present disclosure. In practical
30 implementations, the specific structures of the light-emitting control subcircuit are not limited to the structures as described above, and can also adopt other structures that can be understood by those skilled in the art. There are no limitations herein.

[0129] In some implementations of the pixel circuit as illustrated in FIGS. 2A–2F, the

5 storage subcircuit 4 can comprise a capacitor C.

[0130] A first terminal of the capacitor C is electrically coupled to the first node A; and a second terminal of the capacitor C is electrically coupled to the second node B.

10 [0131] In specific implementations of the pixel circuit, the capacitor is configured to charge under the common control of a signal from the first node and a signal from the second node; to discharge under the common control of a signal from the first node and a signal from the second node; and, when the first node is in a floating state, to maintain a stable voltage difference between the first node and the second node such that the threshold voltage of the driver transistor V_{th} and the voltage of the first power supply terminal V_{dd} can be stored at the first node.

15 [0132] It is noted that the abovementioned embodiments are only examples for illustrating some specific structures of the storage subcircuit in the pixel circuit. In practical implementations, the specific structures of the storage subcircuit are not limited to the structures as described above, and can also adopt other structures that can be understood by those skilled in the art. There are no limitations herein.

20 [0133] In some embodiments of the pixel circuit as described above, such as that shown in FIG. 2A, all switch transistors can be P-type transistors. In some other embodiments, such as that shown in FIG. 2B, all switch transistors can be N-type transistors. There are no limitations herein.

25 [0134] For example, as the driver transistor M0 is selected to be a P-type transistor, as shown in FIG. 2A, all switch transistors can be selected to be P-type transistors. As such, the manufacturing process of the pixel circuit can be simplified.

30 [0135] The P-type switch transistors are OFF upon application of a high electric potential (i.e., under a high voltage), and are ON upon application of a low electric potential (i.e., under a low voltage). Conversely, the N-type switch transistors are ON upon application of a high electric potential (i.e., under a high voltage), and are OFF upon application of a low electric potential (i.e., under a low voltage). As such, for the different selections of the P-type transistors or N-type transistors, the control voltages can be selected accordingly.

5 **[0136]** The driver transistor and the switch transistors can be thin-film transistors (TFTs), or can be metal oxide semiconductors (MOS), and there are no limitations herein.

10 **[0137]** In some implementations, the functions of the source electrodes and the drain electrodes of these switch transistors can be interchangeable, depending on the types of the switch transistor and the signals of the signal terminal, and thus they will not be specifically distinguished herein. In the following illustrative examples, both the driver transistor and the switch transistor are thin-film transistors.

15 **[0138]** In the following, using the pixel circuit shown in FIG. 2A and FIG. 2B as examples and with reference to time sequence diagrams, the working process of the pixel circuit according to some embodiments will be described in detail.

20 **[0139]** It should be noted that in the following descriptions, 1 represents a high electric potential, and 0 represents a low electric potential. It should be further noted that 1 and 0 represent logic electric potentials, and are configured to better explain the specific working process of some of the embodiments of the present disclosure. Therefore, the numerals “1” and “0” are not necessarily the actual electric potentials applied to the gate electrodes of each of the switch transistors.

[0140] Embodiment 1

25 **[0141]** As shown in FIG. 2A, the driver transistor M0 is a P-type transistor, and all of the switch transistors are P-type transistors. As such, each of the switch transistors is OFF upon application of a high electric potential, and ON upon application of a low electric potential. A corresponding input time sequence diagram is illustrated in FIG. 3A.

[0142] Specifically, four stages T1, T2, T3 and T4 as shown in the input time sequence diagram of FIG. 3A are used as examples for the following description.

30 **[0143]** During T1 stage, Scan=0, EM1=0, EM2=1.

[0144] Because Scan=0, the first switch transistor M1, the second switch transistor M2, and the third switch transistor M3 are all ON; because EM1=0, the fourth

5 switch transistor M4 is ON; because EM2=1, the fifth switch transistor M5 and the sixth switch transistor M6 are both OFF.

[0145] The third switch transistor M3 that is ON provides the voltage of the data signal terminal Data V_{Data} to the first node A, that is, the first terminal of the capacitor C, and as such, the voltage of the first terminal of the capacitor C is V_{Data} .

10 [0146] The fourth switch transistor M4 that is ON provides the voltage of the first power supply terminal VDD V_{dd} to the second node B, that is, the source electrode S of the driver transistor M0 and the second terminal of the capacitor C, and as such, the voltage of the second terminal of the capacitor C is V_{dd} .

15 [0147] The first switch transistor M1 that is ON provides the voltage of the initial signal terminal Int V_{Int} to the gate electrode G of the driver transistor M0.

[0148] The second switch transistor M2 that is ON provides the voltage V_{ee} of the second power supply terminal VEE to the drain electrode D of the driver transistor M0 to control the driver transistor M0 to be in a diode state to thereby ensure that the current flowing from the source electrode to the drain electrode of the driver transistor M0 is stable.

20

[0149] However, because the sixth switch transistor M6 is OFF, the light-emitting component L does not emit light.

[0150] During T2 stage, Scan=0, EM1=1, EM2=1.

25 [0151] Because Scan=0, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all ON; because EM2=1, the fifth switch transistor M5, the sixth switch transistor M6 are both OFF; and because EM1=1, the fourth switch transistor M4 is OFF.

[0152] The third switch transistor M3 that is ON provides the voltage V_{Data} of the data signal terminal Data to the first node A, that is, the first terminal of the capacitor C, therefore the voltage of the first terminal of the capacitance C is V_{Data} .

30

[0153] The fourth switch transistor M4 that is OFF disconnects the first power supply terminal VDD with the second node B, therefore the second node B is in a floating

5 state.

[0154] The first switch transistor M1 that is ON provides the voltage of the initial signal terminal Int to the gate electrode G of the driver transistor M0.

[0155] The second switch transistor M2 that is ON provides the voltage V_{ee} of the second power supply terminal VEE to the drain electrode D of the driver transistor M0 to thereby control the driver transistor M0 to be in a diode state.

[0156] Because the gate-source voltage of the driver transistor M0 is larger than its threshold voltage V_{th} , the driver transistor M0 is turned ON. Because the driver transistor M0 is in the diode state, the capacitor C discharges through the driver transistor M0, until the voltage of the second node B, i.e., the voltage of the second terminal of the capacitor C becomes: $V_{Int} - V_{th}$, when the driver transistor M0 is OFF, and the capacitor C stops discharging. Therefore the voltage difference between the two terminals of the capacitor C is : $V_{Data} - V_{Int} + V_{th}$.

[0157] During T3 stage, during the first half of the time period, Scan=1, EM1=1, EM2=1.

[0158] Because Scan=1, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all OFF; because EM=1, the fourth switch transistor is OFF; because EM2=1, the fifth switch transistor and the sixth switch transistor are both OFF.

[0159] During T3 stage, during the second half of the time period, Scan=1, EM1=0, EM2=1.

[0160] Because Scan=1, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all OFF; because EM2=1, the fifth switch transistor M5 and the sixth switch transistor M6 are both OFF; because EM1=0, the fourth switch transistor M4 is ON.

[0161] The fourth switch transistor M4 that is ON provides the voltage V_{dd} of the first power supply terminal VDD to the second node B, therefore the voltage of the second node B, that is, the voltage of the second terminal of the capacitor, is V_{dd} .

5 [0162] The third switch transistor M3 that is OFF disconnects the data signal terminal Data with the first node A, therefore the first node A is in a floating state.

[0163] Because the first node A is in the floating state, according to the capacitor coupling principle, in order to maintain the voltage difference between the two terminals of the capacitor as: $V_{Data} - V_{Int} + V_{th}$, the voltage of the first terminal of the capacitor C has a sudden change from V_{Data} to $V_{Data} + V_{dd} - V_{Int} + V_{th}$.

10

[0164] During T4 stage, Scan=1, EM1=0, EM2=0.

[0165] Because Scan=1, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all OFF; because EM2=0, the fifth switch transistor M5 and the sixth switch transistor M6 are both ON; because EM1=0, the fourth switch transistor M4 is ON.

15

[0166] The fifth switch transistor that is ON provides the voltage of the first node A, that is, the voltage $V_{Data} + V_{dd} - V_{Int} + V_{th}$ of the first terminal of the capacitor, to the second node B, therefore the voltage of the gate electrode G of the driver transistor M0 is $V_{Data} + V_{dd} - V_{Int} + V_{th}$.

20 [0167] The fourth switch transistor M4 that is ON provides the voltage of the first power supply terminal VDD V_{dd} to the second node B, therefore the voltage of the source electrode D of the driver transistor M0 is V_{dd} .

[0168] Because the driver transistor M0 is in a saturated state, it can be known that based on the characteristics of currents in a saturated state, the working current I_L flowing through the driver transistor M0 satisfies:

25

$$[0169] \quad I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{dd} - V_{Int} + V_{th} - V_{dd}) - V_{th}]^2 = K(V_{Data} - V_{Int})^2$$

[0170] wherein V_{GS} represents the gate-source voltage of the driver transistor M0; K the structure parameter. Because the value of K is relatively stable in same structures, it can be treated as a constant value.

30 [0171] It can be known from the above formula that, when the driver transistor M0 is in a saturated state, the current is only related to the voltage V_{Int} of the initial signal

5 terminal Int and the voltage V_{Data} of the data signal terminal Data, but not related to the threshold voltage V_{th} of the driver transistor M0 and the voltage V_{dd} of the first power supply terminal VDD.

[0172] As such, the problem associated with drifting of the threshold voltage V_{th} that is caused by the manufacturing process and/or the long-time operation of the driver transistor M0, as well as the influence of IR Drop on the current flowing through the
10 light-emitting component, can be effectively solved. Thereby the working current of the light-emitting component L can be kept stable, in turn ensuring the normal functioning of the light-emitting component L.

[0173] Embodiment 2

15 [0174] As shown in FIG. 2B, the driver transistor M0 can be a P-type transistor, and all switch transistors can be N-type switch transistors. Each of the switch transistors is ON upon application of a high electric potential, and is OFF upon application of a low electric potential. A corresponding input time sequence diagram is shown in FIG. 3B.

20 [0175] Specifically, the four stages T1, T2, T3, T4 in the input time sequence diagram as shown in FIG. 3B are selected for detailed description.

[0176] During T1 stage, Scan=1, EM1=1, EM2=0.

[0177] Because Scan=1, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all ON; because EM1=1, the fourth switch
25 transistor M4 is ON; because EM2=0, the fifth switch transistor M5 and the sixth switch transistor M6 are both OFF.

[0178] The third switch transistor M3 that is ON provides the voltage V_{Data} of the data signal terminal Data to the first node A, that is, the first terminal of the capacitor C, therefore the voltage of the first terminal of the capacitor C is V_{Data} .

30 [0179] The fourth switch transistor M4 that is ON provides the voltage V_{dd} of the first power supply terminal VDD to the second node B, that is, the source electrode S of the driver transistor M0 and the second terminal of the capacitor C, therefore the

5 voltage of the second terminal of the capacitor C is V_{dd} .

[0180] The first switch transistor M1 that is ON provides the voltage V_{Int} of the initial signal terminal Int to the gate electrode G of the driver transistor M0.

10 [0181] The second switch transistor M2 that is ON provides the voltage V_{ee} of the second power supply terminal VEE to the drain electrode D of the driver transistor M0 to thereby control the driver transistor M0 to be in a diode state to have a stable current flowing from its source electrode to its drain electrode.

[0182] However, because the sixth switch transistor M6 is OFF, the light-emitting component L does not emit light.

[0183] During T2 stage, Scan=1, EM1=0, EM2=0.

15 [0184] Because Scan=1, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all ON; because EM2=0, the fifth switch transistor M5 and the sixth switch transistor M6 are both OFF; because EM1=0, the fourth switch transistor M4 is OFF.

20 [0185] The third switch transistor M3 that is ON provides the voltage V_{Data} of the data signal terminal Data to the first node A, that is, the first terminal of the capacitor C, therefore the voltage of the first terminal of the capacitor C is V_{Data} .

[0186] The fourth switch transistor M4 that is OFF disconnects the first power supply terminal VDD from the second node B, therefore the second node B is in a floating state.

25 [0187] The first switch transistor M1 that is ON provides the voltage V_{Int} of the initial signal terminal Int to the gate electrode G of the driver transistor M0.

[0188] The second switch transistor M2 that is ON provides the voltage V_{ee} of the second power supply terminal VEE to the drain electrode D of the driver transistor M0 to thereby control the driver transistor M0 to be in a diode state.

30 [0189] Because the gate-source voltage of the driver transistor M0 is larger than its threshold voltage V_{th} , the driver transistor M0 is turned ON. Because the driver

- 5 transistor M0 is in a diode state, the capacitor C discharges through the driver transistor M0, until the voltage of the second node B, that is, the voltage of the second terminal of the capacitor becomes $V_{\text{Int}} - V_{\text{th}}$, when the driver transistor M0 is OFF, and the capacitor C stops discharging. As such, the voltage difference between the two terminals of the capacitor is: $V_{\text{Data}} - V_{\text{Int}} + V_{\text{th}}$.
- 10 **[0190]** During T3 stage, and during the first half of the time period, Scan=0, EM1=0, EM2=0.
- [0191]** Because Scan=0, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all OFF; because EM1=0, the fourth switch transistor M4 is OFF; because EM2=0, the fifth switch transistor M5 and the
- 15 sixth switch transistor M6 are both OFF.
- [0192]** During T3 stage, and during the second half of the time period, Scan=0, EM1=1, EM2=0.
- [0193]** Because Scan=0, the first switch transistor M1, the second switch transistor M2 and the third switch transistor M3 are all OFF; because EM2=0, the fifth switch
- 20 transistor M5 and the sixth switch transistor M6 are both OFF; because EM1=1, the fourth switch transistor M4 is ON.
- [0194]** The fourth switch transistor M4 that is ON provides the voltage of the first power supply terminal VDD, V_{dd} , to the second node B, therefore the voltage of the second node B, that is, the voltage of the second terminal of the capacitor is V_{dd} .
- 25 **[0195]** The third switch transistor M3 that is OFF disconnects the data signal terminal Data with the first node A, therefore the first node A is in a floating state.
- [0196]** Because the first node A is in a floating state, according to the capacitor coupling principle, in order to maintain the voltage difference between the two terminals of the capacitor as: $V_{\text{Data}} - V_{\text{Int}} + V_{\text{th}}$, the voltage of the first terminal of the
- 30 capacitor C has a sudden change from V_{Data} to $V_{\text{Data}} + V_{\text{dd}} - V_{\text{Int}} + V_{\text{th}}$.
- [0197]** During T4 stage, Scan=0, EM1=1, EM2=1.
- [0198]** Because Scan=0, the first switch transistor M1, the second switch transistor

5 M2 and the third switch transistor M3 are all OFF; because EM2=1, the fifth switch transistor M5 and the sixth switch transistor M6 are both ON; because EM1=1, the fourth switch transistor M4 is ON.

[0199] The fifth switch transistor that is ON provides the voltage of the first node A, that is, the voltage $V_{Data}+V_{dd}-V_{Int}+V_{th}$ of the first terminal of the capacitor to the second node B, therefore the voltage of the gate electrode G of the driver transistor M0 is $V_{Data}+V_{dd}-V_{Int}+V_{th}$.

[0200] The fourth switch transistor M4 that is ON provides the voltage of the first power supply terminal VDD, V_{dd} , to the second node B, therefore the voltage of the source electrode S of the driver transistor M0 is V_{dd} .

15 [0201] Because the driver transistor M0 is in a saturated state, it can be known based on the characteristic of currents in a saturated state, the working current I_L flowing through the driver transistor satisfies:

$$[0202] \quad I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{dd} - V_{Int} + V_{th} - V_{dd}) - V_{th}]^2 = K(V_{Data} - V_{Int})^2$$

[0203] Wherein, V_{GS} is the gate-source voltage of the driver transistor M0; K is structure parameter. Because the value of K is relatively stable in same structures, it can be treated as a constant.

[0204] It can be known from the aforementioned formula that, when the driver transistor M0 is in a saturated state, the current is only related to the voltage of the initial signal terminal Int, V_{Int} , and the voltage of the data signal terminal Data, V_{Data} , but not related to the threshold voltage V_{th} of the driver transistor M0 and the voltage of the first power supply terminal VDD, V_{dd} .

[0205] As such, the problem associated with drifting of the threshold voltage V_{th} that is caused by the manufacturing process and/or long-time operation of the driver transistor M0, as well as the influence of IR Drop on the current flowing through the light-emitting component, can be effectively solved. Therefore, the working current of the light-emitting component L can be kept stable, ensuring the normal functioning of the light-emitting component L.

5 **[0206]** In both Embodiment 1 and Embodiment 2 as described above, because there is a stable current flowing through the driver transistor at T1 stage, the hysteresis effect can be effectively avoided, which in turn can improve the response time of the driver transistor and can reduce the dark-state luminance.

10 **[0207]** Based on similar inventive concepts, in another aspect of the present disclosure, a method for driving any embodiment of the aforementioned pixel circuits as described above, is further provided.

[0208] As shown in FIG. 4, the method comprises a first stage, a second stage, a third stage, and a fourth stage.

15 **[0209]** S401: During the first stage, the data writing subcircuit provides a signal from the data signal terminal to the first node under control of the scan signal terminal; the power supply voltage control subcircuit provides a signal from the first power supply terminal to the second node under control of the first light-emitting control terminal; the storage subcircuit charges under control of the signal from the first node and the signal from the second node; and the conduction control subcircuit
20 controls the driver transistor to have a diode connection or a source-follow connection via the signal terminal and the second power supply terminal;

[0210] S402: During the second stage, the data writing subcircuit provides a signal from the data signal terminal to the first node under control of the scan signal terminal; the conduction control subcircuit controls the driver transistor to have a
25 diode connection or a source-follow connection via the signal terminal and the second power supply terminal; and the storage subcircuit discharges under control of the signal from the first node and the signal from the second node;

[0211] S403: During the third stage, the power supply voltage control subcircuit provides a signal from the first power supply terminal to the second node under
30 control of the first light-emitting control signal terminal; and the storage subcircuit maintains a stable voltage difference between the first node and the second node when the first node is in a floating state;

[0212] S404: During the fourth stage, the power supply voltage control subcircuit provides a signal from the first power supply terminal to the second node under

control of the first light-emitting control signal terminal; and the light-emitting control subcircuit conducts the first node with the gate electrode of the driver transistor and conducts the drain electrode of the driver transistor with the light-emitting component under control of the second light-emitting control signal terminal, to thereby control the driver transistor to drive the light-emitting component to emit light.

[0213] According to some embodiments, the signal terminal is an initial signal terminal configured to provide a signal having a voltage lower than the voltage of the second power supply terminal.

[0214] As such, the third subcircuit controls the driver transistor to have a source-follow connection via the signal terminal and the second power supply terminal, and a working current flowing through the driver transistor satisfies:

$$I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{dd} - V_{Int} + V_{th} - V_{dd}) - V_{th}]^2 = K(V_{Data} - V_{Int})^2$$

where I_L represents the working current flowing through the driver transistor; V_{GS} represents the gate-source voltage of the driver transistor; K is a structure parameter; V_{Int} represents the voltage of the initial signal terminal Int; V_{Data} represents the voltage of the data signal terminal Data; V_{th} represents the threshold voltage of the driver transistor; and V_{dd} represents the voltage of the first power supply terminal.

[0215] According to some other embodiments, the signal terminal is the second power supply terminal.

[0216] As such, the third subcircuit controls the driver transistor to have a diode connection, and a working current flowing through the driver transistor satisfies:

$$I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{DD} - V_{EE} + V_{th} - V_{DD}) - V_{th}]^2 = K(V_{Data} - V_{EE})^2$$

where I_L represents the working current flowing through the driver transistor; V_{GS} represents the gate-source voltage of the driver transistor; K is a structure parameter; V_{EE} represents the voltage of the second power supply terminal; V_{Data} represents the voltage of the data signal terminal Data; V_{th} represents the threshold voltage of the driver transistor; and V_{dd} represents the voltage of the first power supply terminal.

5 **[0217]** The aforementioned driving method according to some embodiments of the present disclosure can ensure that the working current of the driver transistor in the pixel circuit that drives the light-emitting component to emit light is only related to the voltage of the data signal terminal and the voltage of the initial signal terminal, but not related to the threshold voltage of the driver transistor and the voltage of the first power supply terminal.

10 **[0218]** As such, the influence of the threshold voltage of the driver transistor and IR Drop on the working current flowing through the light-emitting component can be effectively avoided. Therefore, the working current that drives the light-emitting component to emit light can be maintained stable, in turn improving the uniformity of the brightness of the images in the display area in the display apparatus.

15 **[0219]** Based on similar inventive concepts, the present disclosure further provides an organic electroluminescent display panel, which comprises a pixel circuit according to any one of the embodiments as described above. The manners in which the organic electroluminescent display panel addresses the problems are similar to that of the aforementioned pixel circuit, and the implementations of the organic electroluminescent display panel can reference to the implementations of the aforementioned pixel circuits. It will not be repeated herein.

20 **[0220]** Based on similar inventive concepts, the present disclosure further provides a display apparatus, which comprises the organic electroluminescent display panel according to any of the embodiments as described above.

25 **[0221]** Herein the display apparatus can be any products or components that have display functions such as cell phones, tablets, television, monitors, notebooks, digital photo frames and navigators. Other essential components for the display apparatus can be understood by those skilled in the art, and thus they will not be repeated herein and they shall not be construed as limitations to the scope of the present disclosure. The implementations of the display apparatus can reference to the embodiments of the pixel circuit, and they will not be repeated herein.

30 **[0222]** All references cited in the present disclosure are incorporated by reference in their entirety. Although specific embodiments have been described above in detail,

5 the description is merely for purposes of illustration. It should be appreciated, therefore, that many aspects described above are not intended as required or essential elements unless explicitly stated otherwise.

10 **[0223]** Various modifications of, and equivalent acts corresponding to, the disclosed aspects of the exemplary embodiments, in addition to those described above, can be made by a person of ordinary skill in the art, having the benefit of the present disclosure, without departing from the spirit and scope of the disclosure defined in the following claims, the scope of which is to be accorded the broadest interpretation so as to encompass such modifications and equivalent structures.

5

CLAIMS

1. An electronic circuit configured to maintain a substantially stable working current running through an electronic component, comprising:

10 a drive subcircuit, comprising a first terminal, a second terminal, and a third terminal, wherein the first terminal is coupled to a second node; a current from a first terminal to a second terminal is controlled by a signal from a third terminal, and the drive subcircuit is configured to drive the electronic component via the second terminal;

15 a first subcircuit, coupled to a data signal terminal, a scan signal terminal and a first node, and configured to provide a signal from the data signal terminal to the first node under control of the scan signal terminal;

a second subcircuit, coupled to a first power supply terminal, a first control signal terminal and a second node, and configured to provide a signal from the first power supply terminal to the second node under control of the first control signal terminal;

20 a third subcircuit, coupled to the scan signal terminal and a second power supply terminal and to the second terminal and the third terminal of the drive subcircuit, and configured to control the drive subcircuit to have a diode connection or a source-follow connection via the scan signal terminal and the second power supply terminal;

25 a fourth subcircuit, coupled to the first node and the second node, and configured to charge or discharge under control of a signal from the first node and a signal from the second node, and to maintain a stable voltage difference between the first node and the second node if the first node is in a floating state; and

30 a fifth subcircuit, coupled to a second control signal terminal, the first node, the second terminal, and the third terminal, of the drive subcircuit, and a first terminal of the electronic component, and configured to electrically couple the first node with the third terminal of the drive subcircuit, and to electrically couple the second terminal of the drive subcircuit with the electronic component under control of the second control signal terminal, so as to control the drive subcircuit to drive the electronic component.

35 2. The electronic circuit of Claim 1, wherein the drive subcircuit comprises a driver transistor, wherein the first terminal, the second terminal, and the third terminal thereof are respectively a source electrode, a drain electrode, and a gate electrode of the driver transistor.

5

3. The electronic circuit of Claim 2, wherein the third subcircuit comprises:

a first sub-portion, wherein:

a first terminal of the first sub-portion is coupled to the scan signal terminal;

a second terminal of the first sub-portion is coupled to a signal terminal;

10

a third terminal of the first sub-portion is coupled to the gate electrode of the driver transistor; and

the first sub-portion is configured to provide a signal from the signal terminal to the gate electrode of the driver transistor under control of the scan signal terminal, wherein the signal has a voltage lower than or equal to a voltage of the second power supply terminal;

15

and

a second sub-portion, wherein:

a first terminal of the second sub-portion is coupled to the scan signal terminal;

20

a second terminal of the second sub-portion is coupled to the second power supply terminal;

a third terminal of the second sub-portion is coupled to the drain electrode of the driver transistor; and

25

the second sub-portion is configured to provide a signal from the second power supply terminal to the drain electrode of the driver transistor under control of the scan signal terminal.

4. The electronic circuit of Claim 3, wherein the first sub-portion comprises a first switch transistor, wherein:

30

a gate electrode of the first switch transistor is coupled to the scan signal terminal;

a source electrode of the first switch transistor is coupled to the signal terminal; and

a drain electrode of the first switch transistor is coupled to the gate electrode of the driver transistor.

35

5. The electronic circuit of Claim 4, wherein the second sub-portion comprises a second switch transistor, wherein:

a gate electrode of the second switch transistor is coupled to the scan signal

5 terminal;

a source electrode of the second switch transistor is coupled to the second power supply terminal; and

a drain electrode of the second switch transistor is coupled to the drain electrode of the driver transistor.

10 6. The electronic circuit of Claim 4, wherein the signal terminal is the second power supply terminal.

7. The electronic circuit of Claim 4, wherein the signal terminal is an initial signal terminal, configured to provide a signal having a voltage lower than the voltage of the
15 second power supply terminal.

8. The electronic circuit of Claim 1, wherein at least one of the first subcircuit, the second subcircuit, or the fifth subcircuit comprises a switch transistor.

20 9. The electronic circuit of Claim 8, wherein the first subcircuit comprises a third switch transistor, wherein:

a gate electrode of the third switch transistor is coupled to the scan signal terminal;

a source electrode of the third switch transistor is coupled to the data signal terminal;

25 and

a drain electrode of the third switch transistor is coupled to the first node.

10. The electronic circuit of Claim 8, wherein the second subcircuit comprises a fourth switch transistor, wherein:

30 a gate electrode of the fourth switch transistor is coupled to the first control signal terminal;

a source electrode of the fourth switch transistor is coupled to the first power supply terminal; and

a drain electrode of the fourth switch transistor is coupled to the second node.

35 11. The electronic circuit of Claim 8, wherein the fifth subcircuit comprises:

a fifth switch transistor, wherein:

- 5 a gate electrode of the fifth switch transistor is coupled to the second control signal terminal;
 a source electrode of the fifth switch transistor is coupled to the first node;
 a drain electrode of the fifth switch transistor is coupled to the gate electrode of the driver transistor;
- 10 and
 a sixth switch transistor, wherein:
 a gate electrode of the sixth switch transistor is coupled to the second control signal terminal;
 a source electrode of the sixth switch transistor is coupled to the drain
15 electrode of the driver transistor; and
 a drain electrode of the sixth switch transistor is coupled to the first terminal of the electronic component.
12. The electronic circuit of Claim 1, wherein the fourth subcircuit comprises a
20 capacitor, wherein:
 a first terminal of the capacitor is coupled to the first node; and
 a second terminal of the capacitor is coupled to the second node.
13. The electronic circuit of Claim 2, wherein the driver transistor is a P-type transistor.
- 25 14. The electronic circuit of any one of Claims 1-13, wherein the electronic component comprises a light-emitting component.
15. The electronic circuit of Claim 14, wherein the light-emitting component comprises
30 an organic light-emitting diode (OLED), and the electronic circuit is configured to maintain the substantially stable working current through the driver transistor independent of a threshold voltage of the driver transistor or a power supply voltage of the first power supply terminal.
- 35 16. A display panel, comprising an electronic circuit according to any one of Claims 1-15.

- 5 17. A display apparatus, comprising the display panel according to Claim 16.
18. A method of driving the electronic circuit according to Claim 2, comprising:
a first stage, wherein:
the first subcircuit provides a signal from the data signal terminal to the
10 first node under control of the scan signal terminal;
the second subcircuit provides a signal from the first power supply
terminal to the second node under control of the first control terminal;
the fourth subcircuit charges under control of the signal from the first node
and the signal from the second node; and
15 the third subcircuit controls the driver transistor to have a diode
connection or a source-follow connection via the signal terminal and the
second power supply terminal;
a second stage, wherein:
the first subcircuit provides a signal from the data signal terminal to the
20 first node under control of the scan signal terminal;
the third subcircuit controls the driver transistor to have a diode
connection or a source-follow connection via the signal terminal and the
second power supply terminal; and
the fourth subcircuit discharges under control of the signal from the first
25 node and the signal from the second node;
a third stage, wherein:
the second subcircuit provides a signal from the first power supply
terminal to the second node under control of the first control signal terminal;
and
30 the fourth subcircuit maintains a stable voltage difference between the first
node and the second node when the first node is in a floating state;
and
a fourth stage, wherein:
the second subcircuit provides a signal from the first power supply
35 terminal to the second node under control of the first control signal terminal;
and
the fifth subcircuit conducts the first node with the gate electrode of the

5 driver transistor and conducts the drain electrode of the driver transistor with
the electronic component under control of the second control signal terminal,
to thereby control the driver transistor to drive the electronic component.

10 19. The method of Claim 18, wherein during a saturation mode of the driver transistor,
the working current flowing through the driver transistor is independent of a threshold
voltage of the driver transistor or a power supply voltage of the first power supply
terminal.

15 20. The method of Claim 19, wherein the signal terminal is an initial signal terminal
configured to provide a signal having a voltage lower than the voltage of the second
power supply terminal, and the third subcircuit controls the driver transistor to have a
source-follow connection via the signal terminal and the second power supply terminal,
wherein:

the working current flowing through the driver transistor satisfies:

$$20 \quad I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{DD} - V_{Int} + V_{th} - V_{DD}) - V_{th}]^2 = K(V_{Data} - V_{Int})^2$$

wherein I_L represents the working current flowing through the driver transistor;
 V_{GS} represents the gate-source voltage of the driver transistor; K is a structure
parameter; V_{Int} represents the voltage of the initial signal terminal Int; V_{Data}
represents the voltage of the data signal terminal Data; V_{th} represents the
25 threshold voltage of the driver transistor; and V_{dd} represents the voltage of the
first power supply terminal.

21. The method of Claim 19, wherein the signal terminal is the second power supply
terminal, and the third subcircuit controls the driver transistor to have a diode connection,
wherein:

30 the working current flowing through the driver transistor satisfies:

$$I_L = K(V_{GS} - V_{th})^2 = K[(V_{Data} + V_{DD} - V_{EE} + V_{th} - V_{DD}) - V_{th}]^2 = K(V_{Data} - V_{EE})^2$$

wherein I_L represents the working current flowing through the driver transistor;
 V_{GS} represents the gate-source voltage of the driver transistor; K is a structure
parameter; V_{EE} represents the voltage of the second power supply terminal;

5 V_{Data} represents the voltage of the data signal terminal Data; V_{th} represents the threshold voltage of the driver transistor; and V_{dd} represents the voltage of the first power supply terminal.

22. The method of Claim 18, wherein the electronic component comprises a light-emitting component.

10

23. The method of Claim 22, wherein the light-emitting component comprises an organic light-emitting diode (OLED).

15

20

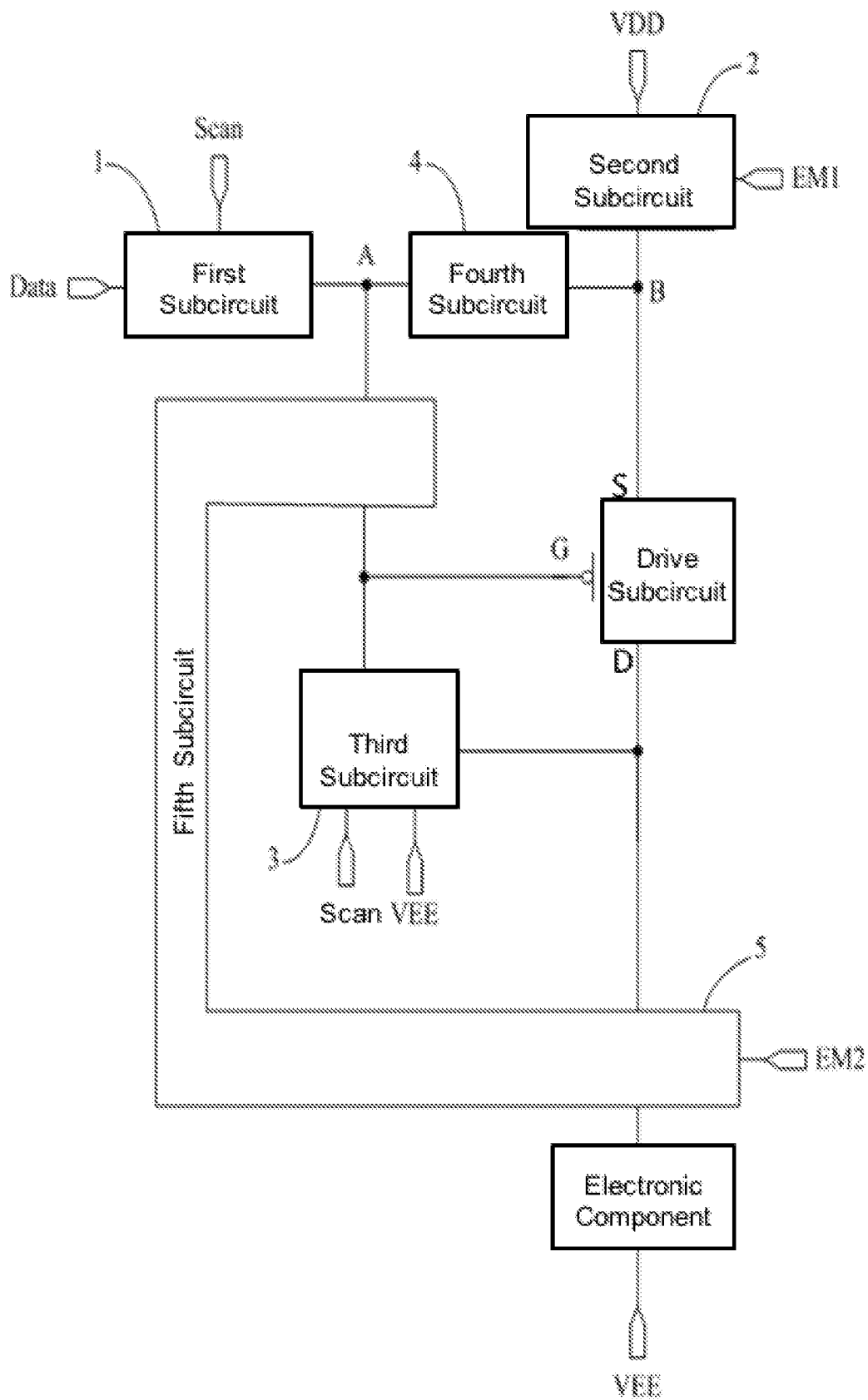


FIG. 1A

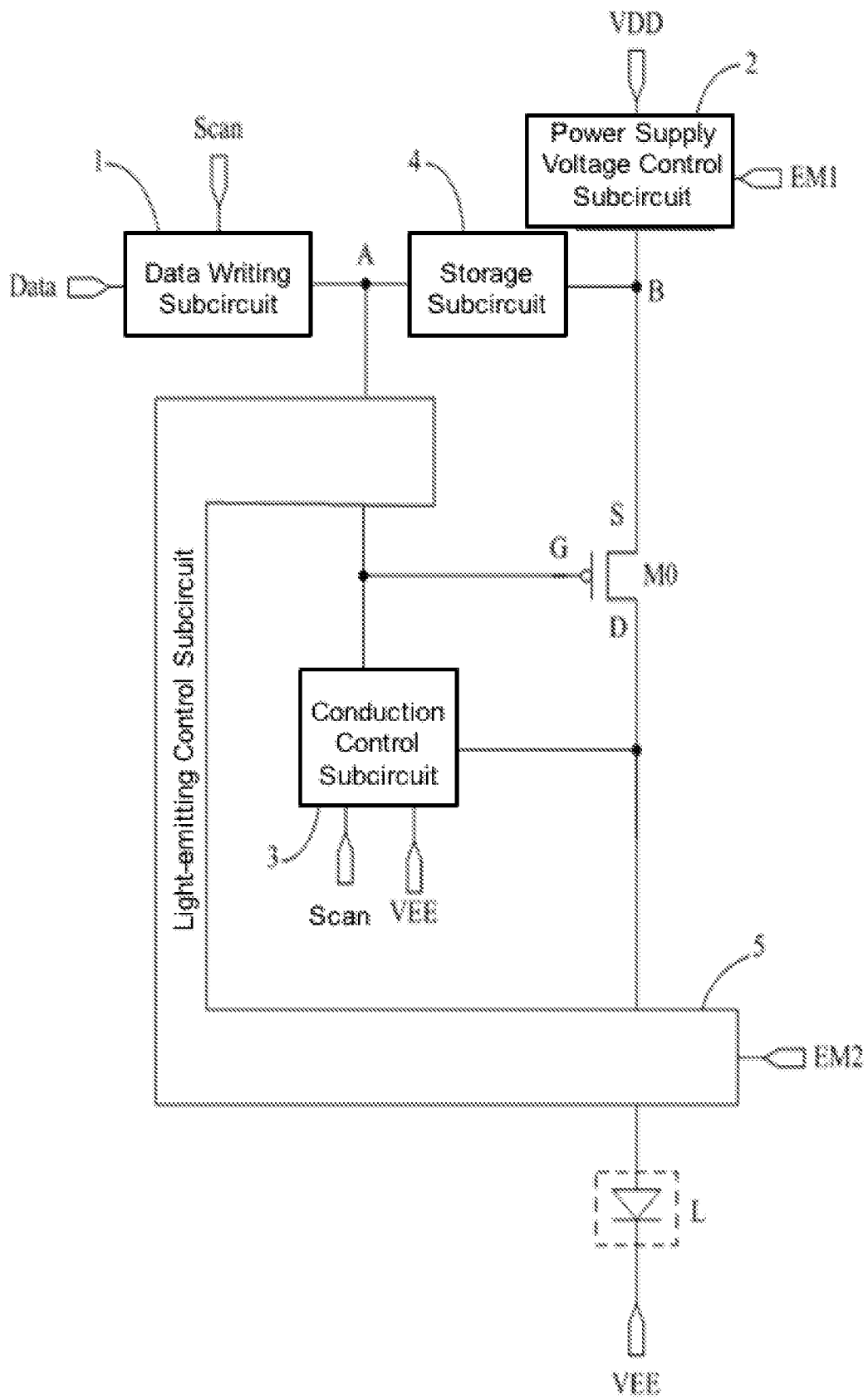


FIG. 1B

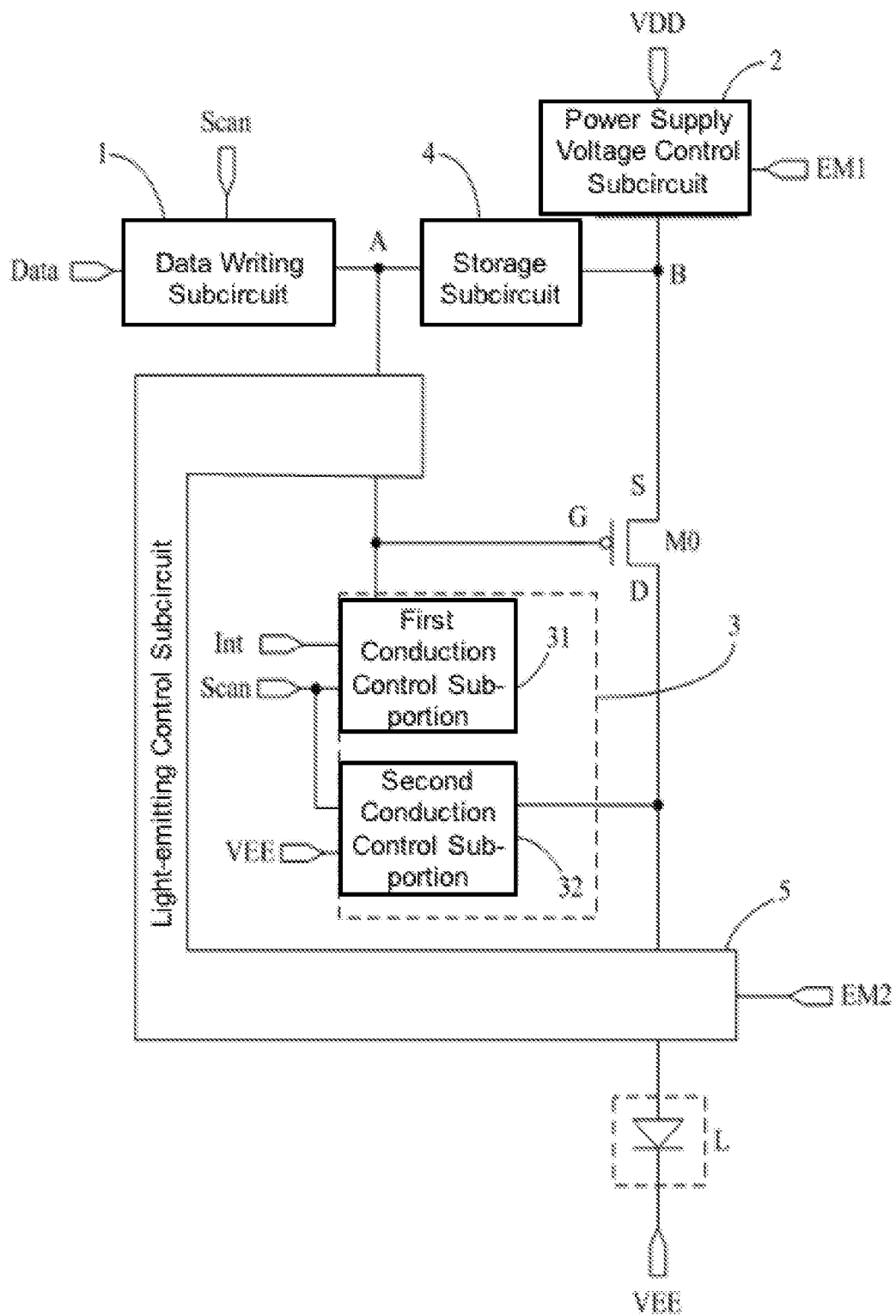


FIG. 1C

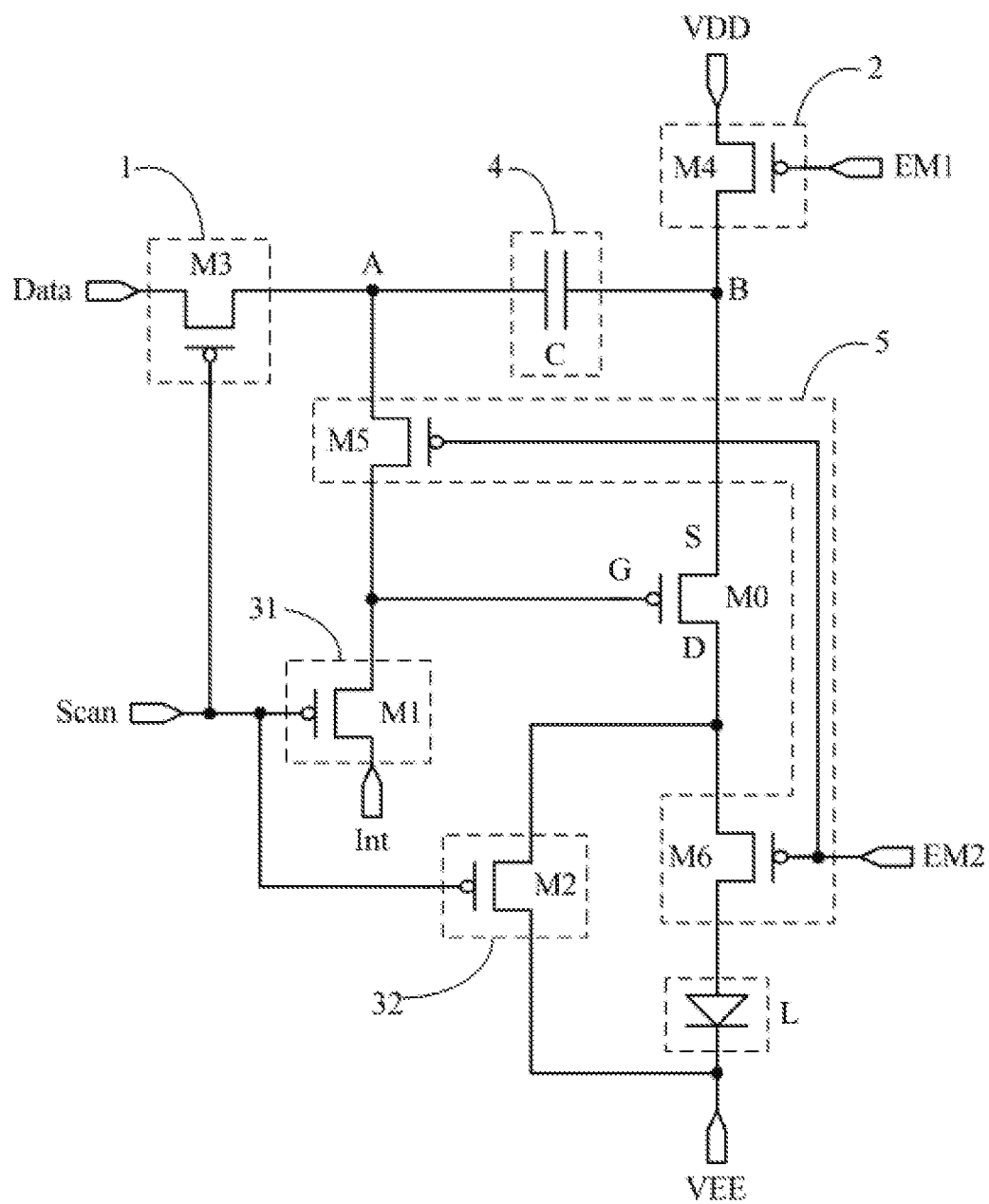


FIG. 2A

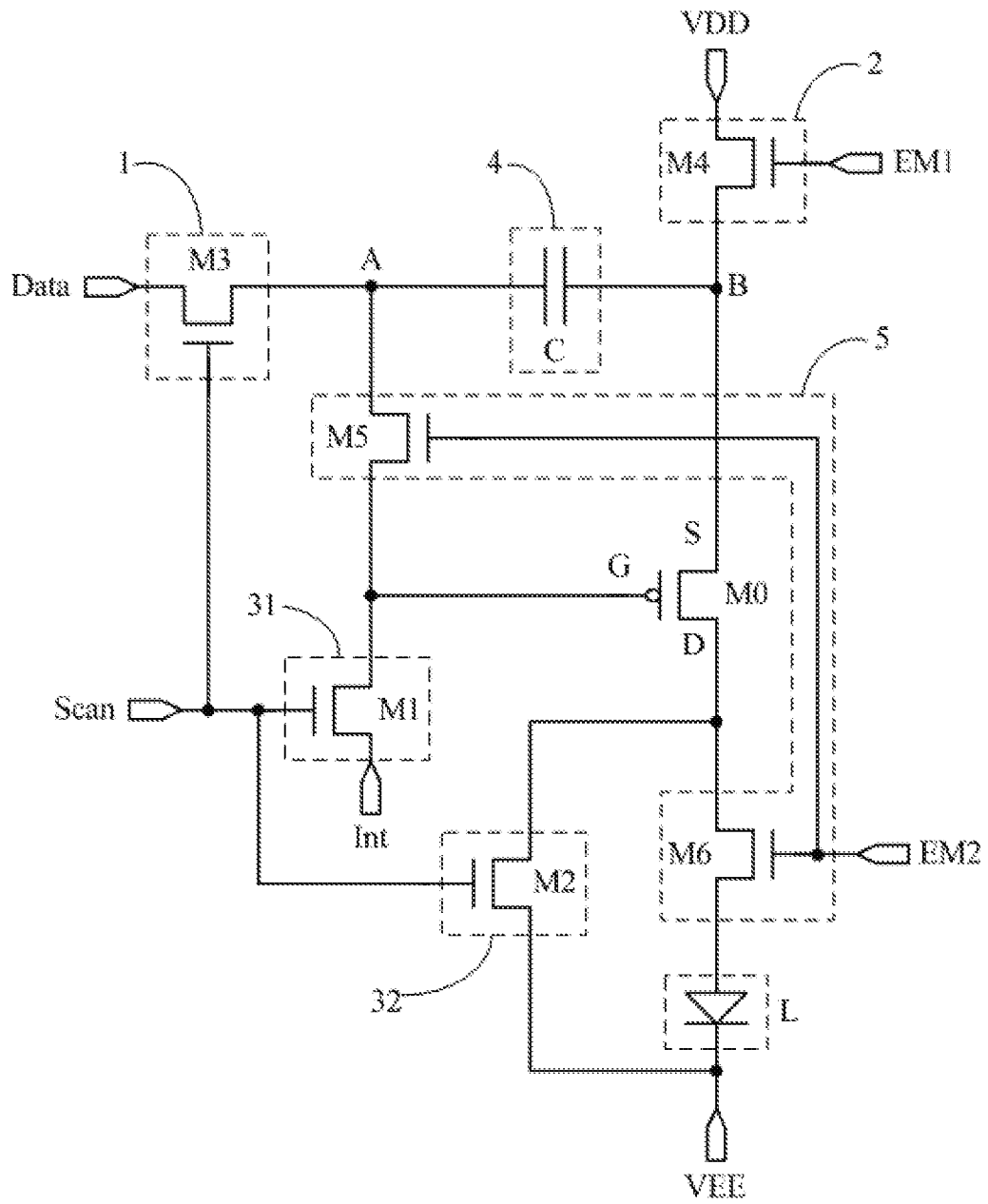


FIG. 2B

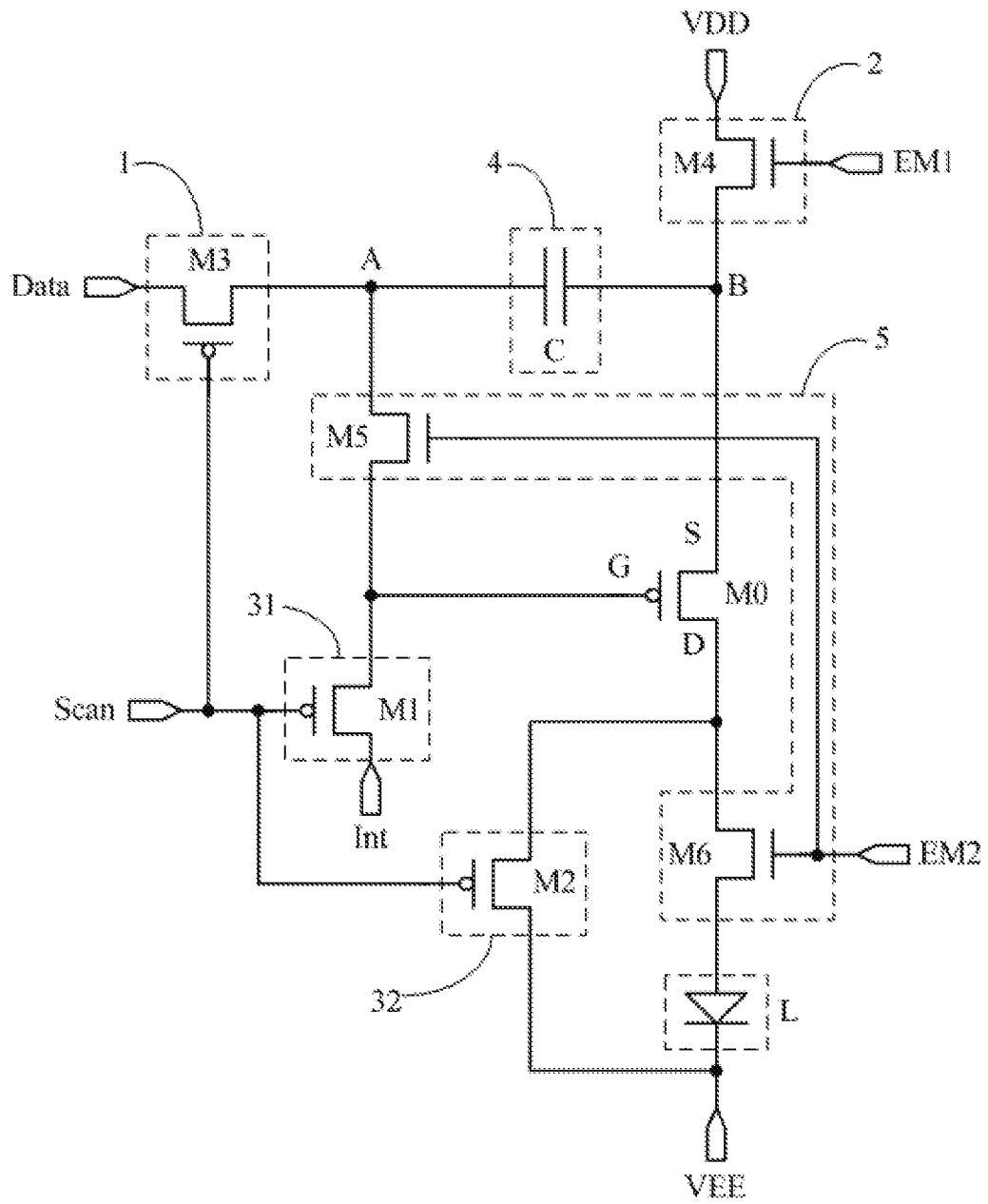


FIG. 2C

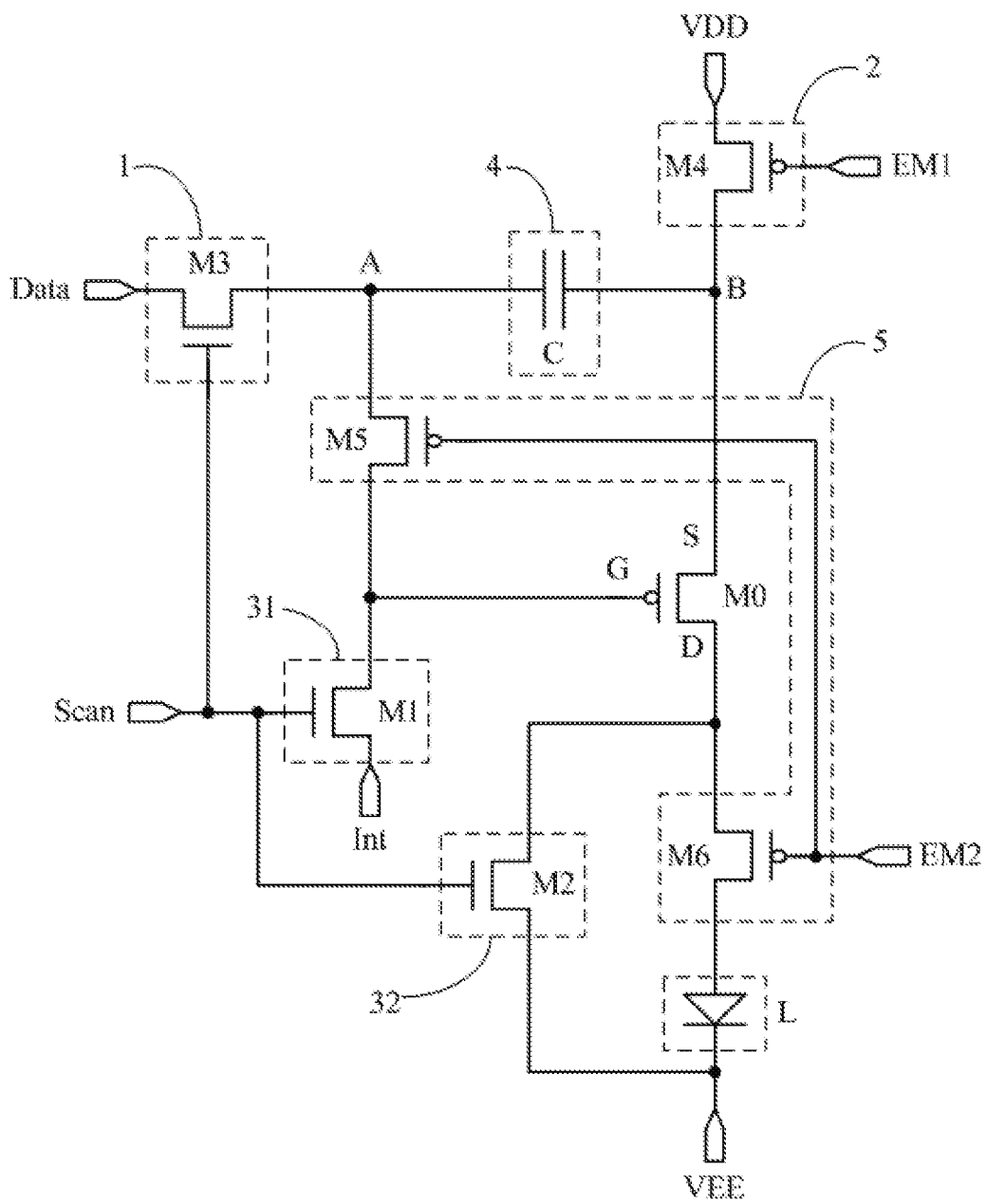


FIG. 2D

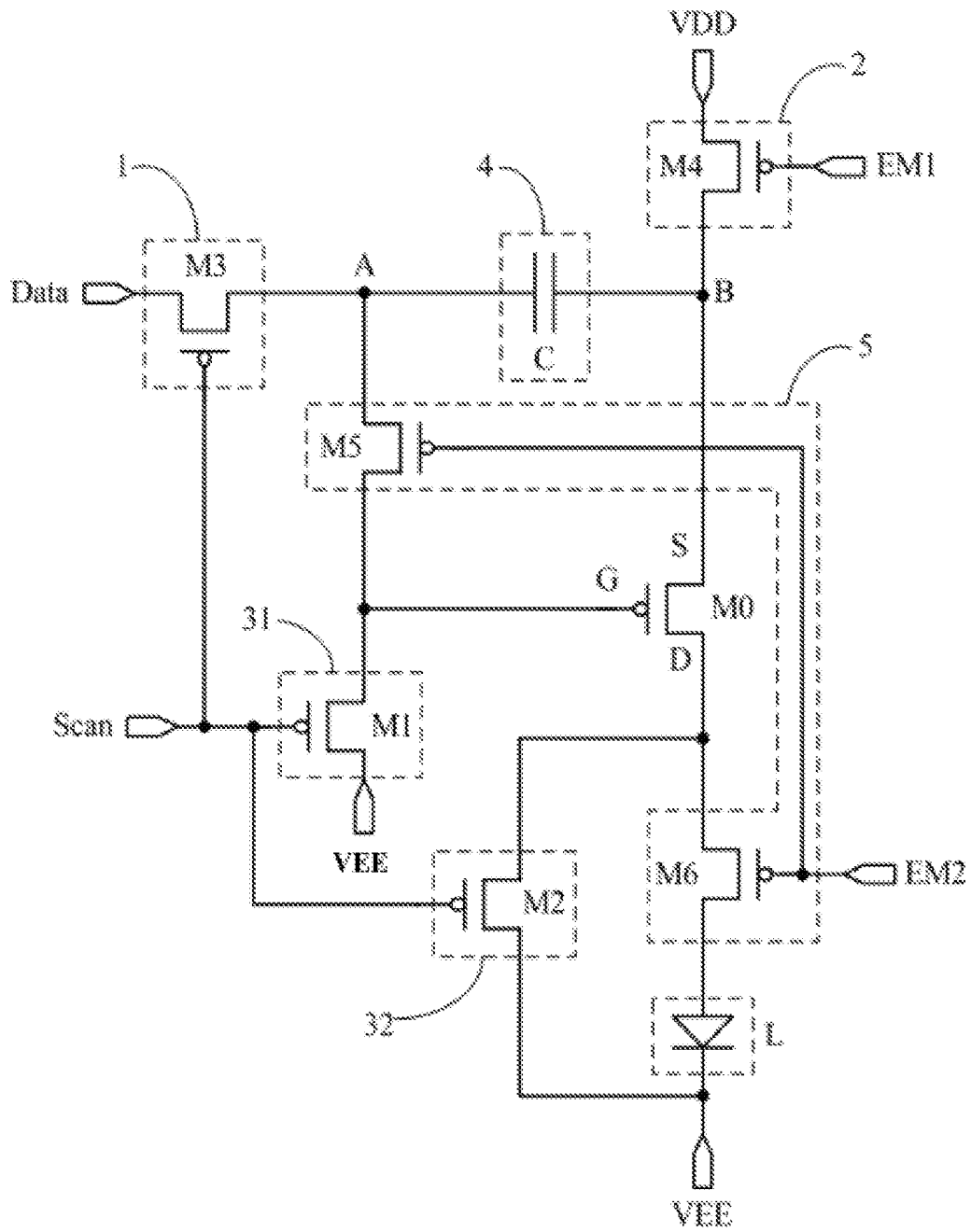


FIG. 2E

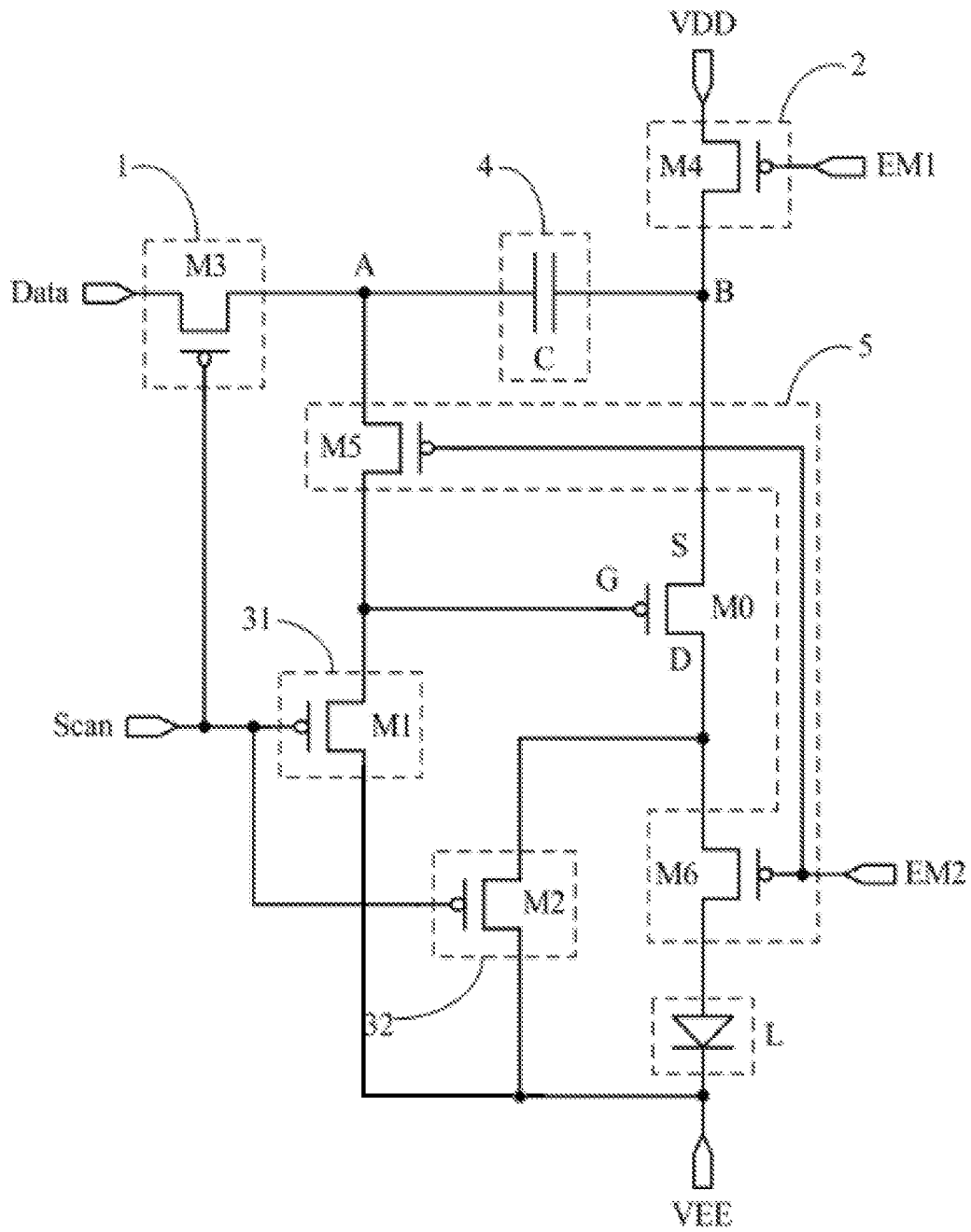


FIG. 2F

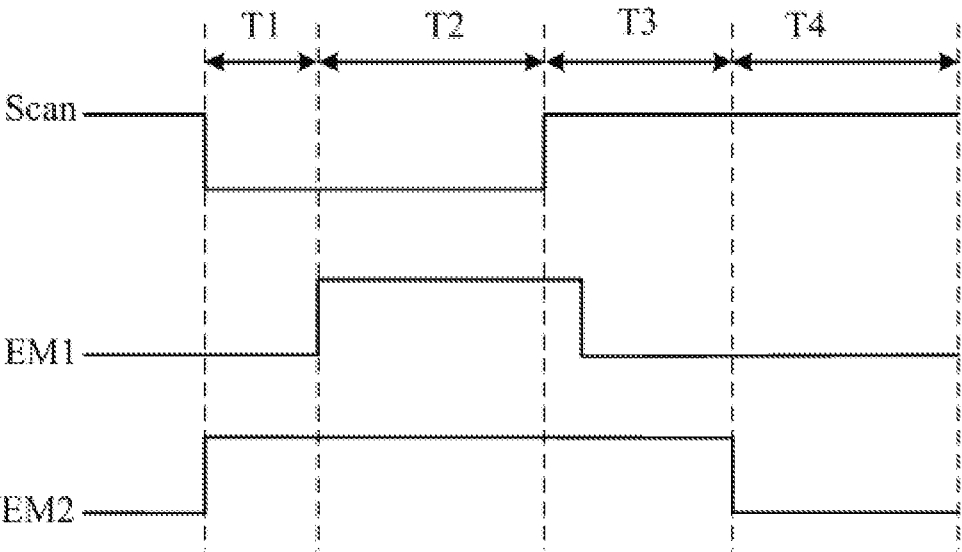


FIG. 3A

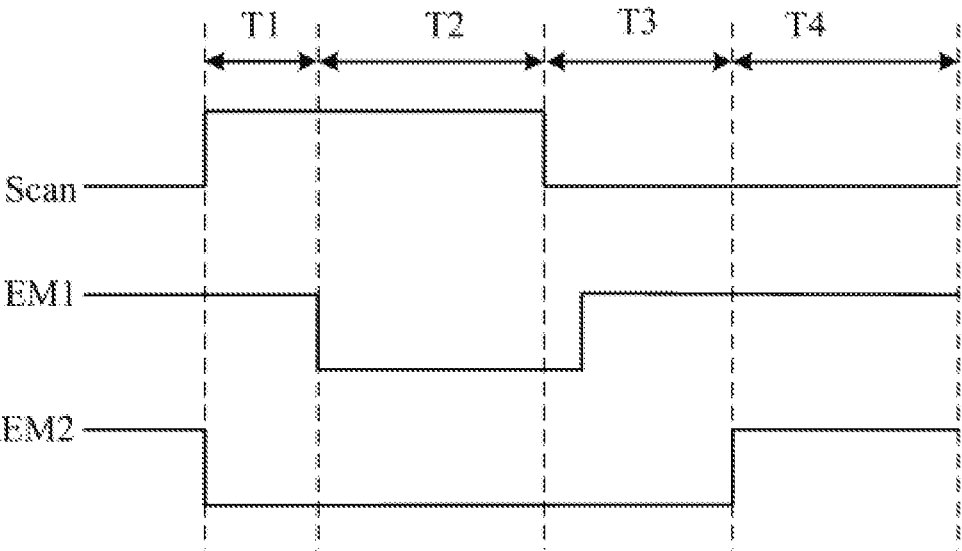


FIG. 3B

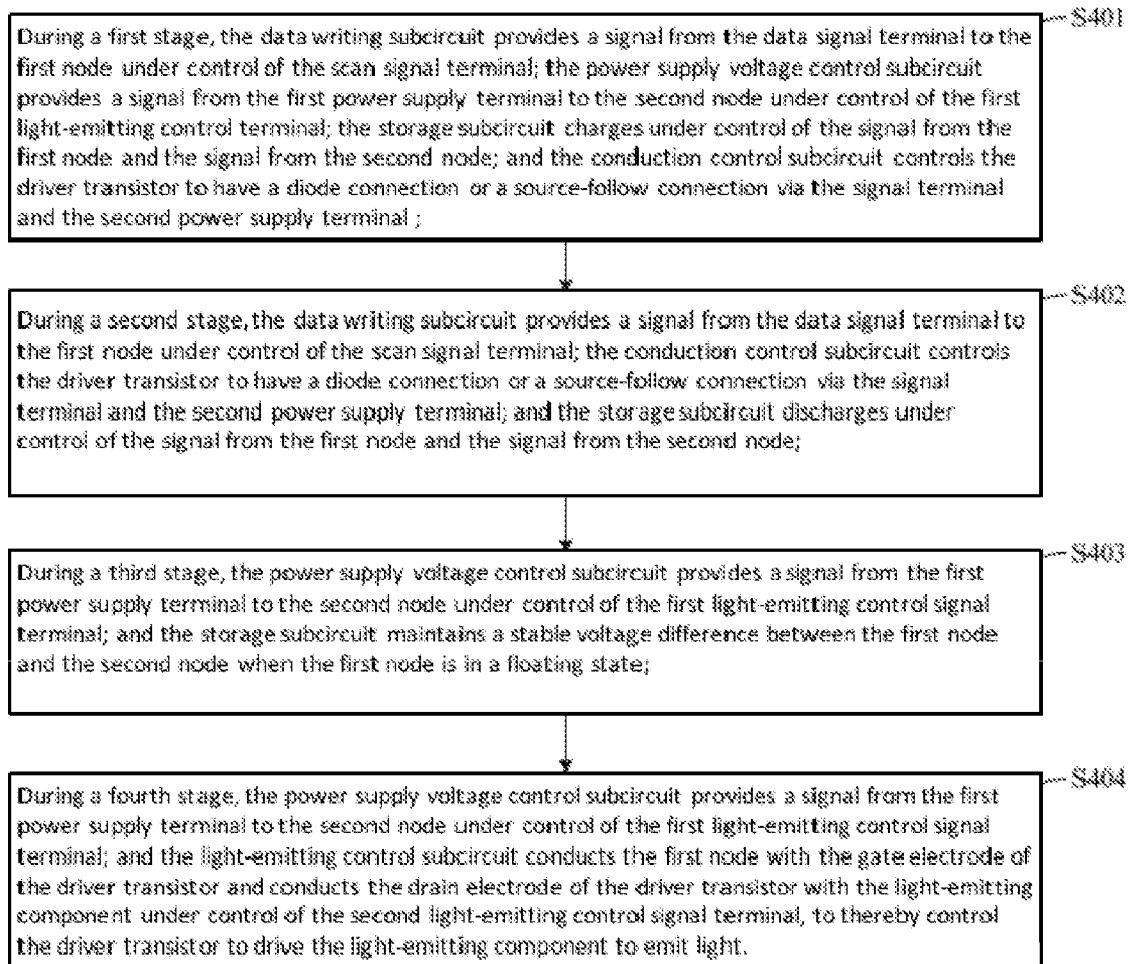


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2017/087883

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/3225(2016.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT, WPI, EPODOC, CNKI: pixel?, circuit, display, drive, subcircuit, terminal, node, signal, data, scan+, power w supply, writing, control, storage, conduction, LED,OLED

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 106205491 A (京东方科技集团股份有限公司) 07 December 2016 (2016-12-07) description [0047]-[0082], Figs.1-4	1-23
PX	CN 205810345 U (京东方科技集团股份有限公司) 14 December 2016 (2016-12-14) description [0047]-[0082], Figs.1-4	1-23
A	CN 103700346 A (合肥京东方光电科技有限公司 等) 02 April 2014 (2014-04-02) description [0043]-[0074], Figs.1-5	1-23
A	CN 104409043 A (京东方科技集团股份有限公司 等) 11 March 2015 (2015-03-11) the whole document	1-23
A	CN 104809989 A (京东方科技集团股份有限公司) 29 July 2015 (2015-07-29) the whole document	1-23
A	US 2010109717 A1 (LIN CHIN-LUNG ET AL.) 06 May 2010 (2010-05-06) the whole document	1-23
A	US 2014022150 A1 (INNOLUX CORP.) 23 January 2014 (2014-01-23) the whole document	1-23

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

10 August 2017

Date of mailing of the international search report

05 September 2017

Name and mailing address of the ISA/CN

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INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2017/087883

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
CN	106205491	A	07 December 2016	None			
CN	205810345	U	14 December 2016	None			
CN	103700346	A	02 April 2014	CN	103700346	B	31 August 2016
				EP	3089148	A1	02 November 2016
				WO	2015096390	A1	02 July 2015
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CN	104409043	A	11 March 2015	US	9691328	B2	27 June 2017
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US	2014022150	A1	23 January 2014	US	9001113	B2	07 April 2015
				TW	I471843	B	01 February 2015
				TW	201405515	A	01 February 2014

专利名称(译)	电子电路及其控制方法，显示面板和显示装置		
公开(公告)号	EP3482389A4	公开(公告)日	2020-01-22
申请号	EP2017800352	申请日	2017-06-12
[标]申请(专利权)人(译)	京东方科技集团股份有限公司		
申请(专利权)人(译)	京东方科技集团股份有限公司.		
当前申请(专利权)人(译)	京东方科技集团股份有限公司.		
[标]发明人	WANG ZHILIANG MA ZHANJIE		
发明人	WANG, ZHILIANG MA, ZHANJIE		
IPC分类号	G09G3/3225		
CPC分类号	G09G3/3225 G09G3/3233 G09G3/3266 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0251 G09G2310/0262 G09G2320/045 G09G3/3275 G09G2320/0233		
优先权	201610543844.X 2016-07-11 CN		
其他公开文献	EP3482389A1		
外部链接	Espacenet		

摘要(译)

公开了一种用于驱动电子部件的电子电路。该电子电路包括驱动子电路，第一子电路，第二子电路，第三子电路，第四子电路和第五子电路。在数据信号端子，扫描信号端子，第一控制信号端子，第二控制信号端子，第一电源端子和第二电源端子的控制下，驱动子电路被配置为具有二极管连接或二极管连接。源极跟随连接，以维持流经电子元件的基本稳定的工作电流。电子电路可以是像素电路，并且电子组件可以是包括有机发光二极管 (OLED) 的发光组件。还公开了一种包含电子电路的显示面板和显示设备，以及用于驱动该电子电路的方法。