

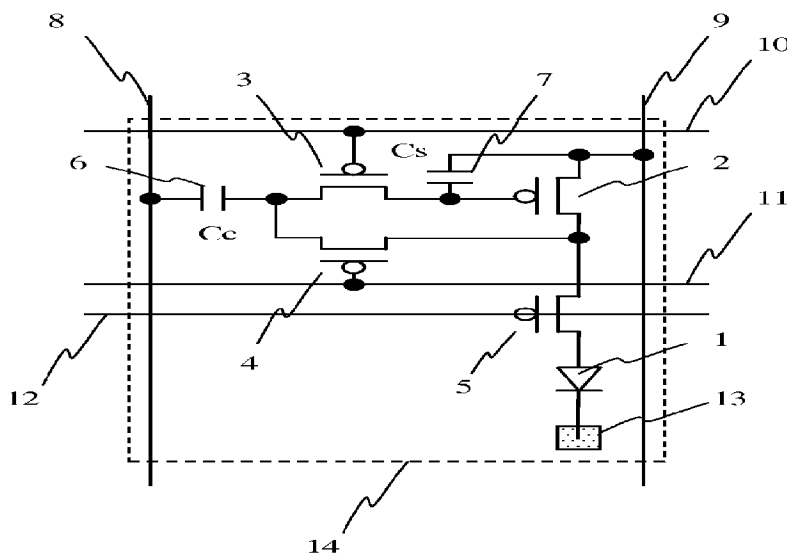


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(54) **Title:** DISPLAY DEVICE USING CAPACITOR COUPLED LIGHT EMISSION CONTROL TRANSISTORS



**FIG. 1**

(57) **Abstract:** In order to efficiently execute threshold value compensation for a driving transistor, a coupling capacitor (6) has one end connected to a data line (8). Another end of the coupling capacitor (6) is connected to a selection transistor (3) and one end of a reset transistor (4). A control terminal of a driving transistor (2) is connected to the other end of the selection transistor (3), and an organic EL element (1) is connected to this driving transistor (2) via a light emission control transistor (5). A data voltage, corresponding to a gradation signal supplied to the data line (8), is written to a storage capacitor (7) via the coupling capacitor (6), and with the selection transistor (3) and the light emission control transistor (5) in an off state and the reset transistor (4) turned on, a compensation voltage corresponding to a degree of mobility of the driving transistor (2) is written to the coupling capacitor (6).

WO 2010/120733 A1

## DISPLAY DEVICE

## BACKGROUND OF THE INVENTION

## 1. Field Of The Invention

5 [0001]

The present invention relates to a display panel with pixels, including current driven type light emitting elements, arranged in a matrix shape.

## 2. Description of the related Art

[0002]

10 Because an organic EL display that uses organic EL elements, being current driven light emitting elements, is of the self-emissive type, it has high contrast and fast response, making it suitable for moving picture applications such as a television for displaying natural images. Generally, an organic EL element is driven with a fixed current using a control element such as a transistor, but the transistor in that case is used in the saturation region. Therefore, even if the  
15 same gradation voltage is supplied, a different current is generated in each pixel due to variations in characteristics such as  $V_{th}$  (threshold voltage) and mobility of the transistors, making it difficult to maintain uniformity of emission brightness. In order to solve this problem, means having a circuit for compensating for  $V_{th}$  provided inside a pixel is disclosed in patent document  
1.

20 [0003]

Patent document 1: JP2002-514320T

[0004]

If the  $V_{th}$  correction circuit shown in FIG., 3 of patent publication 1 is used, a gradation signal voltage is normally applied to the gate terminal of a drive transistor for supplying current  
25 to an organic EL element to offset that  $V_{th}$ .  $V_{th}$  of the drive transistor is therefore automatically corrected. However, it is also difficult to correct mobility of carriers such as electrons in the transistor with the  $V_{th}$  correction circuit of the related art disclosed in patent document 1, and it is difficult to ensure high brightness uniformity over a wide gradation range when there are variations in mobility between pixels.

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## SUMMARY OF THE INVENTION

[0005]

The present invention is a display device, having pixels that are arranged in a matrix, and  
5 a driver for controlling potential of each line, wherein  
each pixel comprises

a coupling capacitor having one end connected to a data line;

a selection transistor, having one end connected to the coupling capacitor, and which is  
switched ON and OFF by a selection line connected to a control terminal;

10 a driving transistor, having a control terminal connected to the other end of the selection  
transistor, and one end connected to a power supply;

an emission control transistor, having one end connected to another end of the driving  
transistor, and being turned ON and OFF by an emission control line;

15 a current driven type light emitting element connected to another end of the emission  
control transistor;

a storage capacitor which connects the control terminal of the driving transistor and the  
one end of the driving transistor that is connected to the power supply side; and

20 a reset transistor that connects the emission control transistor side other end of the driving  
transistor and a selection transistor side other end of the coupling capacitor, and that is turned ON  
and OFF by a reset line,

and wherein

25 the driver writes a data voltage, corresponding to a gradation signal supplied to the data  
line, to the storage capacitor via the coupling capacitor, and with the selection transistor and the  
emission control transistor in an off state and the reset transistor turned on, writes a  
compensation voltage corresponding to mobility of the driving transistor to the coupling  
capacitor.

[0006]

It is also possible for the current driven light-emitting element to be an organic EL  
element.

30 [0007]

It is also possible for the driver to be capable of varying the time that the reset transistor is turned on with the selection transistor and the emission control transistors in an off state.

[0008]

It is also possible for the driver to turn the emission control transistor on in a state where  
5 the selection transistor and the reset transistor are turned off, and after that turn the reset transistor on with the selection transistor and the emission control transistor turned off.

[0009]

It is also possible for the driver to write a compensation voltage to the coupling capacitor in a state where the same gradation signal is supplied to all pixels, then turn off the selection  
10 transistor, turn on the emission control transistor and the reset transistor, and write a voltage corresponding to voltage lowering of the driving transistor to the coupling capacitor, and after that perform equalization processing for the current characteristics of the driving transistor by causing current to flow in the drive transistor based on a voltage at the coupling capacitor.

Effect of the invention

15 [0010]

Since it is possible to carry out correction based on mobility of the driving transistor, high brightness uniformity can be ensured even in the event that there are variations in mobility between driving transistors of each pixel.

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#### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a drawing showing the structure of one example of a pixel circuit of the embodiments.

FIG. 2 is a timing chart showing an example of states of each line.

FIG. 3 is a drawing showing variation in I-V curve accompanying differences in mobility of a  
25 driving transistor.

FIG. 4 is a timing chart showing another example of states of each line.

FIG. 5 is a timing chart showing a further example of states of each line.

FIG. 6 is a drawing showing another example structure for a pixel circuit.

FIG. 7 is a drawing showing yet another example structure for a pixel circuit.

30 FIG. 8 is a drawing showing the overall structure of a display device.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

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[0011]

Embodiments of the present invention will be described in the following based on the drawings.

[0012]

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The circuit structure for a pixel of this embodiment is shown in FIG. 1. In a pixel 14, an organic EL element 1 has a cathode connected to a cathode electrode 13 common to all pixels (for supplying a specified low voltage VSS), and an anode connected to a drain terminal of a light emission control transistor 5 having a gate terminal connected to a light emission control line 12. A source terminal of the light emission control transistor 5 is connected to a drain terminal of a driving transistor 2 having a source connected to a power supply line 9 common to all pixels (for supplying a specified high voltage VDD). A source terminal of a reset transistor 4 having a gate terminal connected to a reset line 11 is connected to a point of connection between a light emission control transistor 5 and a driving transistor 2. Also, a drain terminal of the reset transistor 4 is connected to one end of a coupling capacitor 6 having its other end connected to a data line 8, and to a drain terminal of a selection transistor 3 having its gate terminal connected to a selection line 10. The source terminal of the selection transistor 3 is connected to a gate terminal of the driving transistor 2 and to one end of a storage capacitor 7 that has its other end connected to a power supply line 9.

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[0013]

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Here, the coupling capacitor 6 has a capacitance value  $C_c$ , and the storage capacitor 7 has a capacitance value  $C_s$ . It is preferable, in preventing reduction in dynamic range of a gradation signal voltage  $V_{sig}$  supplied to the data line 8, to make the capacitance value  $C_c$  of the coupling capacitor large compared to the capacitance value  $C_s$  of the storage capacitor. With this embodiment, by forming the coupling capacitor 6 crossing the data line 8 its capacitance  $C_c$  is sufficiently ensured.

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[0014]

A control method for compensating  $V_{th}$  and mobility of the driving transistor 2 using the pixel 14 of FIG. 1 is shown in FIG. 2. As shown in FIG. 2, one horizontal period is divided into a reset period (1), a first data write period (2), a current supply period (3), a mobility compensation period (4), and a second data write period (5).

[0015]

In a horizontal period for selecting a line of pixels 14, the select line 10 is made Low to select the line of pixels. Here, in the reset period (1) in the first half of this horizontal period, the reset line 11 is made Low, the selection transistor 3 and the reset transistor 4 are turned on, and the drive transistor 2 is diode connected to enable current to temporarily flow in the organic EL element 1. After that, because the light emission control line 12 is made High and the light emission control transistor 5 is turned off, the current that was flowing in the organic EL element 1 is made to flow via the reset transistor 4 to the coupling capacitor 6 and storage capacitor 7. While this is happening the same power supply potential VDD as on the power supply line 9 is supplied to the data line 8, and so by the time a certain length of time has elapsed and current no longer flows,  $V_{th}$  is held at the coupling capacitor 6 and the storage capacitor 7. The reset transistor 4 is turned off by setting the reset line 11 High at this time, and the potential held at the coupling capacitor 6 and the storage capacitor 7 is settled, and the reset period (1) is completed.

[0016]

After that, a transition is made to the first write period (2), and if the gradation signal potential  $V_{sig}$  is supplied to the data line 8, the gate source potential  $V_{gs}$  of the driving transistor 2 is controlled to  $V_{gs} = \{C_c/(C_c+C_s)\} * V_{sig} + V_{th}$  with coupling by the coupling capacitor, and the gradation signal potential  $V_{sig}$  with  $V_{th}$  of the driving transistor 2 corrected is written. Next, by making the select line 10 High, that potential is written to the storage capacitor 7 (above described  $V_{gs}$  is retained), and the first data write period (2) is completed. However, the previously described reset period does not have to continue until there is substantially no current flow in the driving transistor 2, and can be a length of time such as a few  $\mu s$  to a few tens of  $\mu s$ .

[0017]

The capacitance  $C_c$  of the coupling capacitor 6 is sufficiently larger than the capacitance  $C_s$  of the storage capacitor 7, which means that  $C_c/(C_c+C_s)$  is substantially equal to 1, and the dynamic range of the gradation signal potential  $V_{sig}$  is maintained.

[0018]

5 If the reset period (1) and the first data write period (2) are complete, specifically, if  $V_{th}$  is compensated and the gradation signal potential  $V_{sig}$  has been written, there is a transition to the current supply period (3), where the light emission control line 12 is made Low and the light emission control transistor 5 is turned on. Therefore, drive current corresponding to the written gradation signal potential  $V_{sig}$  flows via the light emission control transistor 5 into the organic  
10 EL element 1. With the lapse of a comparatively short current supply period (3) the light emission control line 12 is made High, current flow is interrupted, and the current supply period (3) is completed.

[0019]

15 Next, there is a transition to the mobility compensation period (4), where the reset line is made Low, and current that was flowing in the organic EL element 1 (mobility compensation current) flows via the reset transistor 4 to the coupling capacitor 6. At this time, a gradation signal potential being supplied to the data line 8 stays at  $V_{sig}$ .

[0020]

20 At this time, if mobility of the driving transistor 2 is high, mobility compensation current is large, that is, the drain potential of the driving transistor 2 is increased, which means that a higher potential is written to the coupling transistor 6, while in the case of low mobility the mobility compensation current is small and the drain potential of the driving transistor 2 is lowered, which means that a lower potential is written.

[0021]

25 If the reset line 11 is made High, the mobility compensation period (4) is completed, and a potential that has been compensated according to mobility difference is settled at the coupling capacitor 6.

[0022]

30 After that, there is a transition to the second data write period (5), and if the select line 10 is made Low and the second write period commences, the correction signal potential written to

the coupling capacitor 6 is reflected at the gate terminal of the driving transistor 2, and by making the select line 10 High a mobility corrected potential is written to the storage capacitor 7. The select line 10 is then made High and the light emission control line 12 made Low, to complete the second data write period (5).

5 [0023]

In this manner, in a single horizontal period where a line of pixels 14 are selected, data write to each pixel of that line is completed. Light emission is then carried out according to the compensated potential written to the storage capacitor 7 at this time, until writing is carried out in the next frame. Accordingly, display is carried out using a signal with  $V_{th}$  and mobility

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compensated.

[0024]

If control is carried out in this way, the mobility compensation potential  $V_u$  is represented as  $V_u = I_{ds} \cdot \Delta t / C_c$ , using a rather short mobility compensation period  $\Delta t$ , and is proportional to drive current  $I_{ds}$  and compensation period  $\Delta t$ . Also, using mobility  $u$ , gate capacitance per unit area  $C_{ox}$ , and transistor size  $W$ ,  $L$ , drive current  $I_{ds}$  is expressed as  $I_{ds} = 0.5 \cdot u \cdot C_{ox} \cdot (W/L) \cdot V_{sig}^2$  (provided  $V_{th}$  is compensated and  $C_c$  is sufficiently larger than  $C_s$ ), and since it is proportional to mobility  $u$ , the mobility compensation potential  $V_u$  is dependent on mobility  $u$ , compensation period  $\Delta t$  and  $V_{sig}$ . Accordingly, after completion of the second write period the signal potential becomes  $V_{gs} = \{C_c / (C_c + C_s)\} \cdot V_{sig} + V_{th} - I_{ds} \cdot \Delta t / C_c$ ,

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and an offset potential  $V_u$  corresponding to mobility and the gradation signal potential is subtracted from a potential with  $V_{th}$  compensated.

[0025]

The effect of this type of mobility compensation will be described using FIG. 3. FIG. 3 shows I-V curves for a driving transistor a and a driving transistor b with  $V_{th}$  compensated. If

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mobility differs, a difference in the inclination of the I-V curve arises between the transistors, and current flowing in the organic EL element 1 is different even if the same signal potential  $V_{sig}$  is applied. For example, even if  $V_{sig1}$  is written to a pixel after  $V_{th}$  compensation, the transistor a and the transistor b with different mobility output respectively different drive currents of  $I_a(V_{sig1})$  and  $I_b(V_{sig1})$  to the organic EL element 1.

30 [0026]

If the mobility compensation of this embodiment is adopted, a mobility compensated potential  $V_u$  corresponding to drive current  $I_{ds}$  is subtracted from a potential across a gate and source with  $V_{th}$  compensated, which means that it is possible to make the drive current uniform. For example, if  $V_{sig1}$  is written after compensation of  $V_{th}$ , with the transistor a current  $I_a(V_{sig1})$  flows in the mobility compensation period, and with the transistor b current  $I_b(V_{sig1})$  flows in the mobility compensation period, and these currents flow into the respective coupling capacitors 6 via the reset transistor 4. As shown in FIG. 3, driving transistor b with a more upright I-V curve has greater current mobility compensation current than transistor a, and mobility compensation potential  $V_u$  is larger. Specifically, since  $V_u(I_b(V_{sig1})) > V_u(I_a(V_{sig1}))$ , driving transistor b has a smaller gate source potential, and output current is constrained. As a result, after completion of mobility compensation, if a signal is again written to the storage capacitor 7 in the second write period the drive current output to the organic EL elements is substantially  $I(V_{sig1})$ , and differences in output current due to mobility of the driving transistors a and b are made uniform.

15 [0027]

Even in the case of writing  $V_{sig2}$  that generates a smaller driving current, mobility compensation is carried out on the same principle and made uniform. In the case of writing  $V_{sig1}$ , since the current  $I(V_{sig1})$  that has been made uniform flows in the driving transistors a and b, a potential difference of  $\Delta V_{u1} = V_u(I_b(V_{sig1})) - (V_u(I_a(V_{sig1})))$  is necessary, but in the case of  $V_{sig2}$ , this potential difference  $\Delta V_{u2} = V_u(I_b(V_{sig2})) - (V_u(I_a(V_{sig2})))$  is required to be smaller than  $\Delta V_{u1}$ . It is therefore necessary to adjust the potential difference  $\Delta V_u$  after compensation depending on the gradation signal potential  $V_{sig}$ , but with mobility compensation of the present invention, since mobility compensation potential  $V_u$  is automatically adjusted according to drive current  $I_{ds}$ , namely  $V_{sig}$ , appropriate mobility compensation is carried out at all gradations.

25 [0028]

Also, with the mobility compensation of this embodiment it is possible to vary the mobility compensation period  $\Delta t$  by either changing a pulse width input to the reset line 11 or inputting pulses a plurality of times etc., and it is possible to easily adjust the mobility compensation potential  $V_u$ . For example, by setting the mobility compensation period  $\Delta t$  long in the case of a panel with large variation in mobility, and setting the mobility compensation

period  $\Delta t$  short with a panel having only slight variation in mobility, it is possible to avoid the drawbacks of insufficient or excessive compensation. Specifically, it is possible to realize an effective compensation amount for each panel by adjusting the mobility compensation period  $\Delta t$ . For example, it is possible to provide a register for setting  $\Delta t$  in a data driver and select driver, that will be described later, to write an externally supplied setting value for  $\Delta t$  in this register, and to carry out control in accordance with a value for  $\Delta t$  written to the register by the select driver at the time of mobility compensation.

[0029]

Another mobility compensation method using the pixels 14 of FIG. 1 is shown in FIG. 4. The power supply period (3) is omitted from FIG. 4. Specifically, once the gradation signal potential  $V_{sig}$  is written after  $V_{th}$  compensation, by making the reset line 11 Low with the light emission control line 12 still High, the mobility compensation current  $I_{ds}$  is charged from the driving transistor 2 to the coupling capacitor 6.

[0030]

The reason this type of control becomes possible is that immediately after making the reset line 11 Low, one terminal of the coupling capacitor 6 and the drain terminal of the driving transistor 2 are connected via the reset transistor 4, but the drain terminal of the driving transistor 2 is at substantially the same potential as the gate terminal, which means that the driving transistor is operated in the saturation region, and a mobility compensation current according to a difference in mobility flows. Accordingly, the mobility compensation potential  $V_u$  is represented as  $V_u = I_{ds} \cdot \Delta t / C_c$ , and mobility compensation according to gradation is realized. As the current supply period (3) can be omitted in this way, control is simplified and it is possible to efficiently utilize the horizontal period. For example, the second write period can be sufficiently ensured, and the horizontal period can be shortened, and image signal writing can be simplified even if there are a lot of lines.

[0031]

Further, by using control such as that in FIG. 5 using the pixels 14, it becomes possible to make variations in brightness accompanying degradation of the organic EL elements 1 uniform.

In FIG. 5, a drive voltage readout period (6) and a third write period (7) have been added to the horizontal period of FIG. 4.

[0032]

5 First,  $V_{th}$  is compensated in the reset period, and after writing the gradation signal  $V_{sig}$  in the first write period mobility is compensated, and the description up to this point is the same as previously. At the time of this processing to make deterioration of the organic EL elements uniform, the same gradation pixel is supplied to all pixels.

[0033]

10 In FIG. 5, after the second write period (5) there is a transition to the drive voltage readout period (6). The light emission control line 12 is made Low, and the organic EL element 1 temporarily emits light. At this time, current flowing in the organic EL element 1 is constant for each pixel, due to compensation of  $V_{th}$  and mobility of the driving transistor 2.

[0034]

15 If the reset line 11 is set Low after waiting for the lapse of a specified time, the anode potential of the organic EL element 1 is written to one end of the coupling capacitor 6. While this is taking place, the other end of the coupling capacitor 6 is fixed at  $V_{sig}$  or another arbitrary potential. In this way, it is possible to read out an anode potential of the organic EL element at the time a fixed current flows, to the coupling capacitor 6.

[0035]

20 The drive potential rises with elapse of time if the flow of current continues in the organic EL element. Specifically, if the same current flows in a deteriorated organic EL element, the drive voltage increases. The potential read out to the coupling capacitor 6 in the drive voltage readout period reflects the extent of deterioration of the organic EL element, and a higher voltage is read out for organic EL elements that suffer greater deterioration.

25 [0036]

After that, if the reset line 11 is set High and the drive voltage readout period is completed, the select line 10 is set low to commence the third write period (7), and the read out drive potential is reflected on the gate terminal of the drive transistor 2. At this time,  $V_{test}$  is applied to the data line 8 in order to adjust the equalizing processing current, and an equalizing

potential written to the storage capacitor 7 is adjusted using this adjustment potential  $V_{test}$  to control current for the equalization processing.

[0037]

If the select line 10 is set High and the equalizing potential is written to the storage  
5 capacitor 7, a current corresponding to the equalizing potential flows in the organic EL element 1.

[0038]

In pixels that have significant deterioration of the organic EL element, since a high drive  
potential is read out the potential  $V_{gs}$  across the gate and source of the driving transistor 2  
becomes smaller, and equalizing current becomes smaller, but in pixels with only slight  
10 deterioration a low drive voltage is read out, and so the potential  $V_{gs}$  across the gate and source  
becomes larger and the equalizing current is increased. During equalization processing, a smaller  
current flows in those pixels with greater deterioration, while a larger current flows in those  
pixels with slight deterioration. Specifically, since pixels with only slight deterioration  
deteriorate rapidly, if the equalization process continues deterioration will become uniform across  
15 pixels. This equalization process can be carried out during non-use periods of the display. It is  
also possible for this equalization process to be carried out with a refresh rate of 60 Hz, the same  
as normal display, or to be carried out at a refresh rate that is different from that of normal display,  
such as a lower frequency of 30 Hz, for example. In this way a single horizontal period becomes  
longer, and it is made possible to sufficiently ensure the  $V_{th}$  compensation time and the  
20 deterioration potential readout time.

[0039]

A pixel 14 of this embodiment uses P-type transistors for all transistors, but it is also  
possible to use N-type transistors in some sections, or to use all N-type transistors.

[0040]

25 FIG. 6 is one example of a pixel 14 constructed with N-type transistors, and is controlled  
on the basis of FIG. 2 and FIG. 4. First, in the reset period an arbitrary potential, for example, a  
cathode potential  $V_{SS}$ , is supplied to the data line 8, the select line 10 is made high and the reset  
line 11 is made high, and the selection transistor 3 and the reset transistor 4 are turned on, and by  
diode connecting the driving transistor 2 current temporarily flows in the organic EL element 1.  
30 Then, the light emission control line 12 that was High is made Low, and the light emission

control transistor 5 is turned off to write  $V_{th}$  of the driving transistor 2 to the coupling capacitor 6 and the storage capacitor 7. In the case of the pixel 14 of FIG. 6, the potential written to the coupling capacitor 6 and the storage capacitor 7 is not strictly speaking  $V_{th}$  of the driving transistor 2, but can be considered to reflect substantially  $V_{th}$ . Next, if the reset line 11 is set Low to turn the reset transistor 4 off and there is a transition to the first write period, a signal potential  $V_{sig}$  is supplied to the data line 8, and a signal potential  $V_{sig}$  with  $V_{th}$  compensated is written to the storage capacitor 7. After that, the select line 10 is set Low, and if the reset line 11 is set High and the reset transistor 4 is turned on in order to carry out mobility compensation a current corresponding to the gradation signal  $V_{sig}$  flows from the driving transistor 2 operated in the saturation region through the reset transistor 4 to discharge the coupling capacitor 6. The discharge amount is dependent on the mobility of the driving transistor 2, and so a potential having the mobility compensated is generated at the coupling capacitor. If the reset line 11 is set Low, the reset transistor turned off and the select line 10 again set High, the select transistor 3 is turned on and the gradation potential with mobility compensated is written to the storage capacitor 7 and that potential is held by setting the select line to Low. Following that, by setting the light emission control line 5 High, a current with  $V_{th}$  and mobility compensated flows in the organic EL element 1, and the organic EL element emits light. That is, the mobility compensation of the present invention also acts efficiently if N-type transistors are used.

[0041]

However, since it is difficult to read out the drive potential of the organic EL element 1 with the pixel 14 of FIG. 6, in the case of using N-type transistors it is desirable to have the pixel structure of FIG. 7.

[0042]

FIG. 7 shows a pixel 14 with the anode of the organic EL element 1 made common. Therefore, VDD is supplied to the anode 13 while VSS is supplied to the power supply line 9. Control of the pixel 14 can use the same method as in FIG. 2 and FIG. 4, but the polarities of pulses input to the select line 10, reset line 11 and emission control line 12 are reversed. In the reset period, while VSS is being supplied to the data line 8, the select line 10 and reset line 11 are made High, and the selection transistor 3 and the reset transistor 4 are turned on to diode connect the driving transistor 2. At this time current temporarily flows in the organic EL element 1, but

by making the light emission control line 12 Low and turning the light emission control transistor 5 off,  $V_{th}$  of the driving transistor 2 is written to the coupling capacitor 6 and the storage capacitor 7. Continuing on, in the first write period the select line is made High to keep the select transistor 3 turned on, the reset line 11 is made Low to turn the reset transistor 4 off, and the gradation signal  $V_{sig}$  supplied to the data line 8 is written to the storage capacitor 7, before a transition to the mobility compensation period. In the mobility compensation period the reset line 11 is made High to turn the reset transistor 4 on, and mobility compensation current  $I_{ds}$  flows from the driving transistor 2, that is operated in the saturation region, to the coupling capacitor 6, and a potential corresponding to mobility and the gradation signal potential  $V_{sig}$  is generated. By turning the reset transistor 4 off, this compensation potential is held at the coupling capacitor 6, and in the second write period if the select line 10 is again set High to turn the selection transistor 3 on then the compensation potential held at the coupling capacitor 6 is written to the storage capacitor 7. If the select transistor 3 is turned off and the light emission control transistor 5 is turned on, current flows in the organic EL element 1.

15 [0043]

In the case of making deterioration in the organic EL elements uniform, with the control method shown in FIG. 5 the previously described  $V_{th}$  and mobility compensation are carried out, and it is possible to write a drive voltage of the organic EL element 1 with flow of equalized current in the organic EL element 1, into the coupling capacitor 6. Specifically, by making the reset line 11 High and turning the reset transistor 4 on, the drive potential is written to the coupling capacitor 6. Since the drive voltage is large for a severely deteriorated organic EL element, the cathode potential is low, while for a slightly deteriorated organic EL element the drive voltage is low and so the cathode potential is high. If the reset line 11 is set Low and the reset transistor 4 is turned off, this drive potential is temporarily held at the coupling capacitor 6, and if the select line 10 is again made High to turn the selection transistor 3 on, this read out drive potential is then reflected at the gate terminal of the driving transistor 2. That is, in the case of a lot of deterioration, the potential  $V_{gs}$  across the gate and source of the driving transistor 2 is small, and equalizing current becomes small, while in the case of only slight deterioration the potential  $V_{gs}$  across the gate and source of the driving transistor is large and equalizing current

becomes large. If the select line 10 is made Low and the selection transistor 3 is turned off, equalizing current flows in the organic EL element 1 until the next selection of the select line 10.

[0044]

During equalization processing, a smaller current is supplied to those pixels with greater deterioration, while a larger current is supplied to those pixels with slight deterioration, thus facilitating equalization. Similarly to FIG. 5, the equalization current can be adjusted using  $V_{test}$  supplied to the data line 8. When it is desired to perform equalization more rapidly, it is preferable to increase equalization current by adjusting  $V_{test}$ , and in the case where it is desirable for display of equalization processing to not be noticeable it is preferable to perform equalization processing with a low current.

[0045]

In this manner, even in the case where the pixels 14 are constructed using N-type transistors, it is possible for the  $V_{th}$  and mobility compensation of FIG. 2 and FIG. 4, and the equalization processing for deterioration of the organic EL element, to be carried out in the same way as for the case where the pixels 14 are constructed of P-type transistors. Also, with the above described example, for P-type or N-type, fixed potentials of VDD and VSS are supplied to the data line 8 in the reset period, and then  $V_{th}$  is compensated with  $V_{sig}$  supplied in the first write period, but it is also possible to reverse this. That is, it is possible to supply  $V_{sig}$  onto the data line 8 in the reset period, and supply a fixed potential constituting  $V_{ref}$  in the first write period. If this is done, control is carried out so as to write a difference between  $V_{sig}$  and  $V_{th}$  to the coupling capacitor 6 in the reset period, and commence flow of current to the driving transistor 2 when the potential of the data line 8 becomes  $V_{sig}$ . Accordingly, if  $V_{ref}$  is written in the first write period, a difference between  $V_{ref}$  and  $V_{sig}$  is reflected at the gate of the driving transistor 2, and added to  $V_{th}$ , and so  $V_{th}$  is compensated. Next, in the mobility compensation period, the selection transistor 3 and the light emission control transistor 5 are kept off, and the reset transistor 4 is turned on, to write a difference in mobility to the coupling capacitor 6 as a potential difference. In the second write period, this potential is written to the storage capacitor 7 to carry out mobility compensation. In this way, mobility compensation of this embodiment is utilized efficiently, even if the  $V_{th}$  compensation method is different.

[0046]

FIG. 8 shows the overall structure of an organic EL display 100 formed from an array of the pixels 14 of the present invention. The organic EL display 100 comprises a pixel array 15 having pixels 14 arranged in an array on a glass substrate or plastic substrate etc., a data driver 16 for driving data lines 8, and a selection driver 17 for driving select lines 10, reset line 11, and emission control lines 12. However, power supply lines 8 and cathode terminals 13 that are common to all pixels are omitted from the drawing. In the pixel array 15, an example of full-color pixels is shown formed from R (red) G (green) and B (blue) sub-pixels, but it is also possible to have a structure where W (white) is added to give full-color pixels of RGBW.

[0047]

The data driver 16 converts image data that has been transferred in dot units from an external section to line unit data using a shift register or the like, and outputs an analog signal potential in line units to the data line 8 by means of digital to analog conversion. In a reset period, in order to write  $V_{th}$ , VDD and VSS signal potentials are output, but in the write period a gradation signal potential  $V_{sig}$  is supplied. As a result of this  $V_{th}$  and mobility compensation are carried out in units of one line. The select driver 17 has three outputs per one line, specifically output to drive the select lines 10, output to drive the reset lines 11, and output to drive the light emission control lines 12, but the respective lines are selectively driven to be made High or Low at the timing of FIG. 4 and FIG. 5. The data driver 16 and the select driver 17 can be formed from elements such as low temperature polysilicon on the same substrate as the pixels 14, or can be provided as driver ICs with the outputs of these ICs connected to each of the lines. From the structure of FIG. 8,  $V_{th}$  compensation and mobility compensation, and also equalization of deterioration of the organic EL elements, is carried out efficiently in the pixels 14.

[0048]

The structure of this embodiment can be used not only with organic EL elements, but with any other display device that uses current driven type light emitting elements.

What is Claimed is:

1. A display device comprising  
pixels arranged in a matrix form, each pixel comprising  
5 a coupling capacitor having one end connected to a data line;  
a selection transistor, having one end connected to the coupling capacitor,  
and which is switched ON and OFF by a selection line connected to a control terminal;  
a driving transistor, having a control terminal connected to the other end of  
the switching transistor, and one end connected to a power supply;  
10 a light emission control transistor, having one end connected to another  
end of the driving transistor, and being turned ON and OFF by a light emission control line;  
a current driven type light emitting element connected to another end of  
the light emission control transistor;  
a storage capacitor which connects a control terminal of the driving  
15 transistor and the one end of the driving transistor that is connected to the power supply side; and  
a reset transistor that connects the light emission control transistor side  
other end of the driving transistor and a selection transistor side of the coupling capacitor, and  
that is turned ON and OFF by a reset line; and  
a driver for controlling potential of each line; wherein  
20 this driver writes a data voltage, corresponding to a gradation signal supplied to the data  
line, to the storage capacitor via the coupling capacitor, and with the selection transistor and the  
light emission control transistor in an off state and the reset transistor turned on, writes a  
compensation voltage according to mobility of the driving transistor to the coupling capacitor.
- 25 2. The display device of claim 1, wherein  
The current driven type light emitting elements are organic EL elements.
3. The display device of claim 1 or claim 2, wherein  
the driver is capable of varying the time that the reset transistor is turned on with the  
30 selection transistor and the light emission control transistors in an off state.

4. The display device of any one of claim 1 to claim 3, wherein  
the driver turns the light emission control transistor on in a state where the selection  
transistor and the reset transistor are turned off, and after that turns the reset transistor on with the  
5 selection transistor and the light emission control transistor turned off.
5. The display device of any one of claim 1 to claim 4, wherein  
the driver writes a correction voltage to the coupling capacitor in a state where the same  
gradation signal is supplied to all pixels, then turns off the selection transistor, turns on the light  
10 emission control transistor and the reset transistor, and writes a voltage corresponding to voltage  
lowering of the driving transistor to the coupling capacitor, and after that performs equalization  
processing of the current characteristics of the driving transistor by causing current to flow in the  
drive transistor based on a voltage at the coupling capacitor.



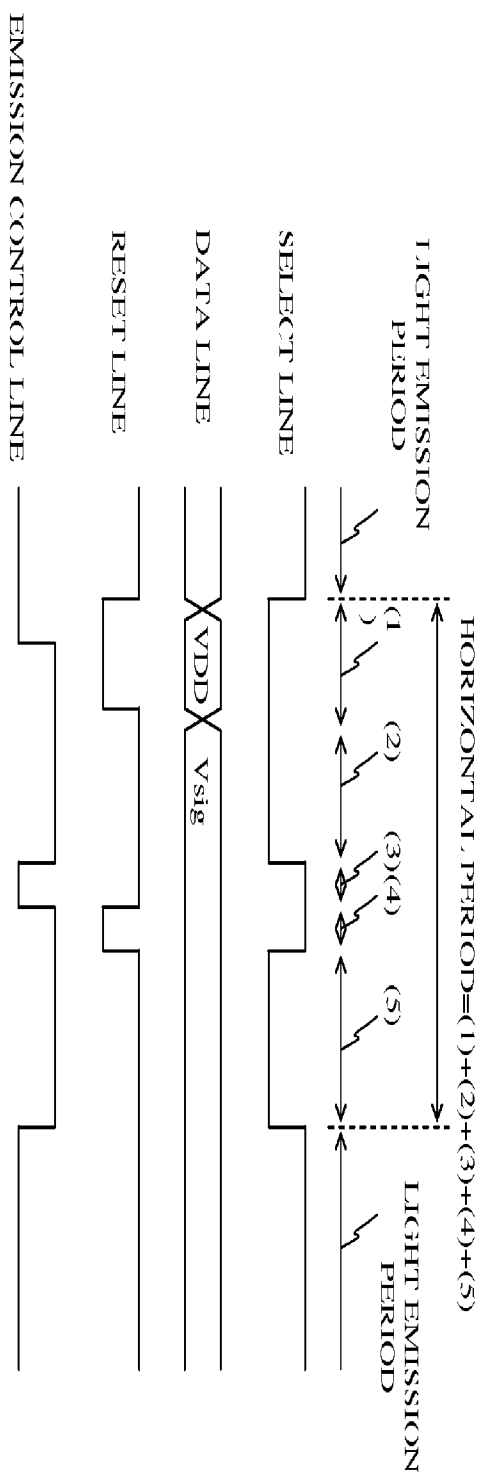


FIG. 2

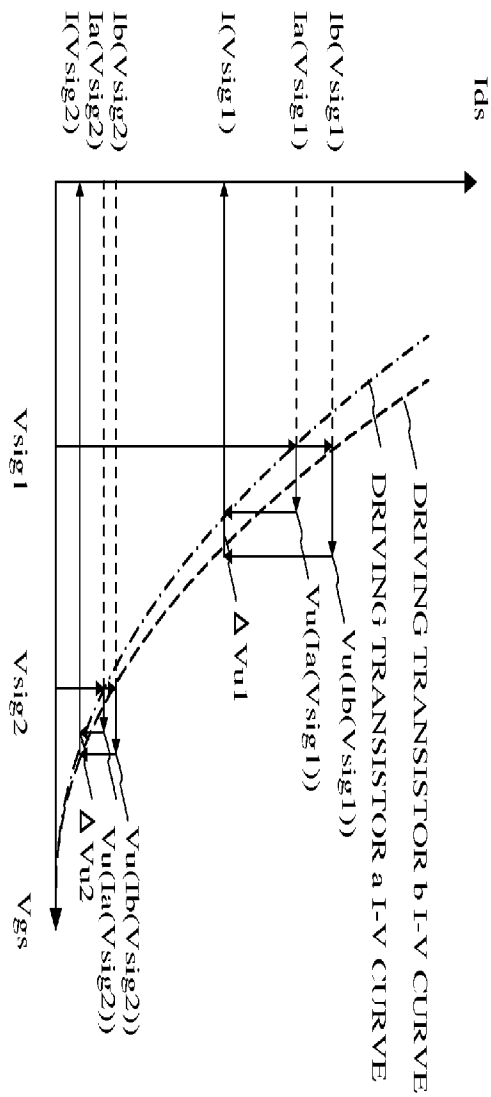


FIG. 3

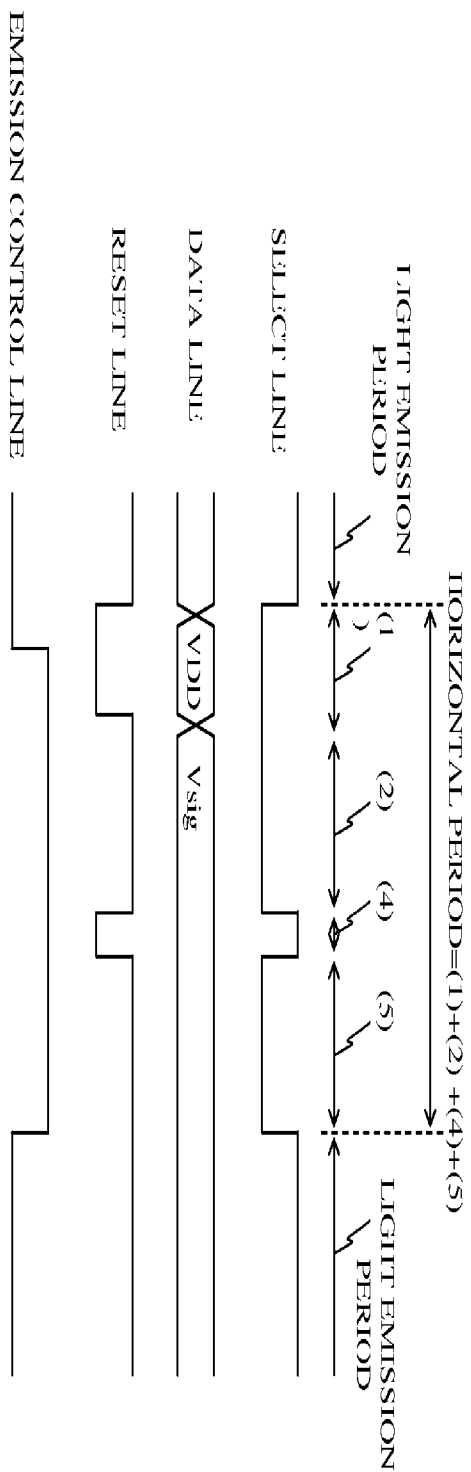


FIG. 4

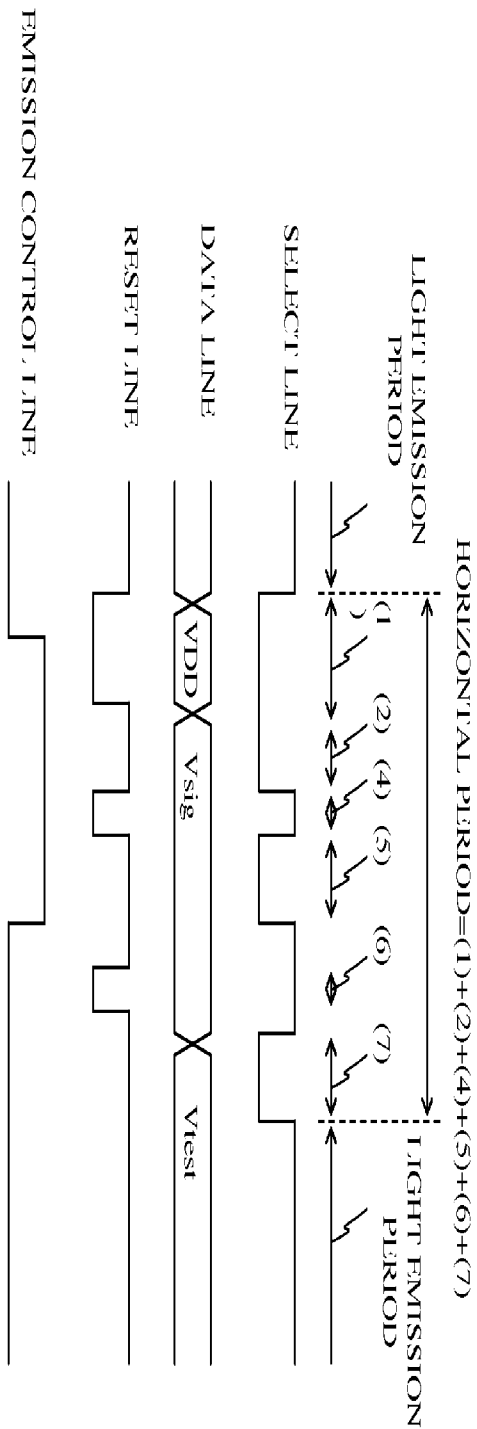


FIG. 5

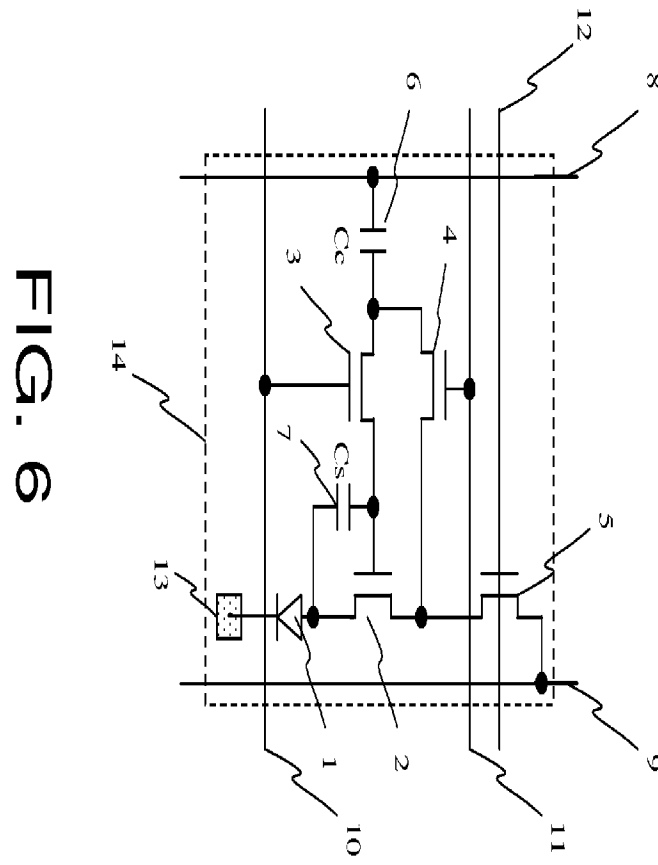


FIG. 6



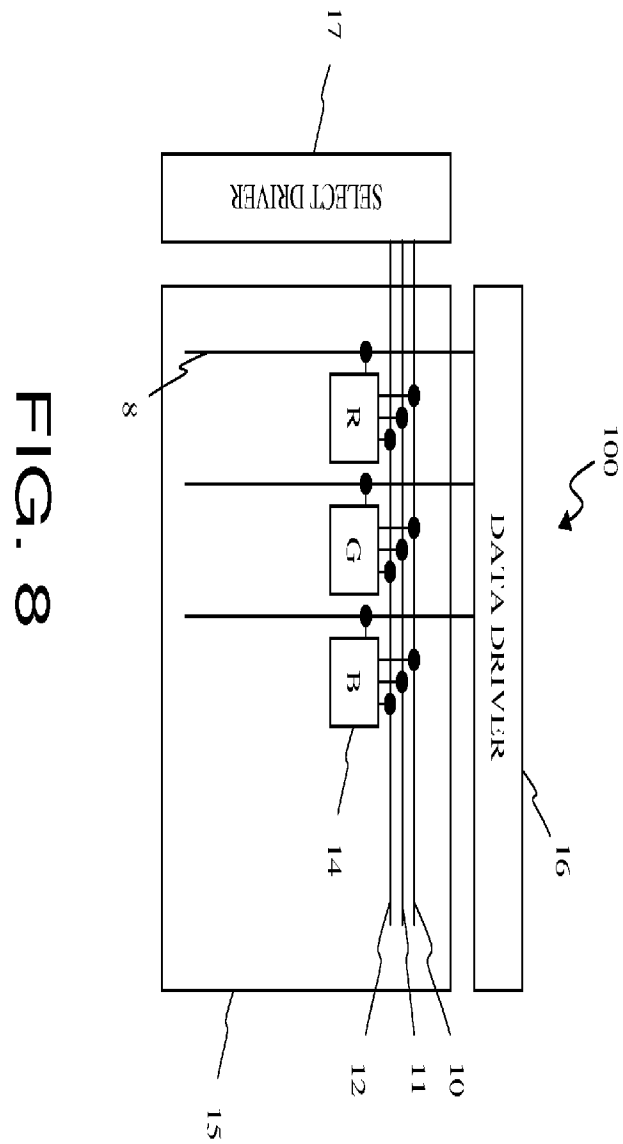


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US 10/30833

A. CLASSIFICATION OF SUBJECT MATTER  
IPC(8) - G09G 3/36 (2010.01)  
USPC - 345/98  
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED  
Minimum documentation searched (classification system followed by classification symbols)  
USPC 345/98

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched  
USPC 345/76, 77, 80, 98, 214, 690; 348/705, 800 (text search--see below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)  
PubWest (PGPB,USPT,EPAB,JPAB); Google Scholar (Patents,Articles)  
Search terms: mobility, compensation, organic, LED, capacitor, coupling, storage, equalization, correction, threshold, saturation

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2006/0139253 A1 (CHOI et al.) 29 June 2006 (29.06.2006) FIGs. 2-4 and 16, and para [0042]-[0053], [0087]-[0090]	1-3
Y	US 2001/0024186 A1 (KANE et al.) 27 September 2001 (27.09.2001) FIG. 3 and para [0039]-[0041]	1-3
Y	US 6,348,906 B1 (DAWSON et al.) 19 February 2002 (19.02.2002) FIG. 2 and col. 9, ln 36-56	3

Further documents are listed in the continuation of Box C.

\* Special categories of cited documents:  
 "A" document defining the general state of the art which is not considered to be of particular relevance  
 "E" earlier application or patent but published on or after the international filing date  
 "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)  
 "O" document referring to an oral disclosure, use, exhibition or other means  
 "P" document published prior to the international filing date but later than the priority date claimed  
 "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention  
 "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone  
 "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art  
 "&" document member of the same patent family

Date of the actual completion of the international search 23 May 2010 (23.05.2010)	Date of mailing of the international search report <b>04 JUN 2010</b>
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Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774
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## INTERNATIONAL SEARCH REPORT

International application No. .

PCT/US 10/30833

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
  
3.  Claims Nos.: 4-5  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2.  As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

专利名称(译)	使用电容器耦合发光控制晶体管的显示装置		
公开(公告)号	<a href="#">EP2419895A1</a>	公开(公告)日	2012-02-22
申请号	EP2010764991	申请日	2010-04-13
[标]申请(专利权)人(译)	全球OLED TECH		
申请(专利权)人(译)	全球OLED科技有限责任公司		
当前申请(专利权)人(译)	全球OLED科技有限责任公司		
[标]发明人	KAWABE KAZUYOSHI		
发明人	KAWABE, KAZUYOSHI		
IPC分类号	G09G3/36 G09G3/32		
CPC分类号	G09G3/3233 G09G3/006 G09G3/3291 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2320/0233 G09G2320/043		
优先权	2009097396 2009-04-13 JP		
其他公开文献	EP2419895A4		
外部链接	<a href="#">Espacenet</a>		

#### 摘要(译)

为了有效地执行驱动晶体管的阈值补偿，耦合电容器（6）的一端连接到数据线（8）。耦合电容器（6）的另一端连接到选择晶体管（3）和复位晶体管（4）的一端。驱动晶体管（2）的控制端子连接到选择晶体管（3）的另一端，并且有机EL元件（1）经由发光控制晶体管（5）连接到该驱动晶体管。对应于提供给数据线（8）的灰度信号的数据电压经由耦合电容器（6）和选择晶体管（3）和发光控制晶体管（存储电容器（7））写入存储电容器（7）。5）在截止状态并且复位晶体管（4）导通时，对应于驱动晶体管（2）的迁移率的补偿电压被写入耦合电容器（6）。