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(54) **ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE**

(57) An organic light emitting diode display apparatus includes a display panel, a discharge circuit configured to discharge a voltage if the display panel is driven for more than a predetermined time and the supply of power to the display panel is interrupted, and a processor configured to, if the power is supplied, determine whether a cooling time required for afterimage compensation of the display panel is satisfied, and if the cooling time is satisfied, perform the afterimage compensation of the display panel.

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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority under 35 U.S.C. 119 and 365 to Korean Patent Application No. 10-2017-0142738, filed on October 30, 2017 in the Korean Intellectual Property Office, the disclosure of which is incorporated herein by reference.

BACKGROUND

[0002] The present disclosure relates to an organic light emitting diode (OLED) display apparatus, and more particularly, to an OLED display apparatus capable of measuring an off time of a display panel even if the supply of power is interrupted.

[0003] Recently, various types of display apparatuses have appeared. Among them, an organic light emitting diode (OLED) display apparatus is widely used. Since the OLED display apparatus is a self-luminous apparatus, the OLED display apparatus has lower power consumption and can be made thinner than a liquid crystal display (LCD) requiring a backlight. In addition, the OLED display apparatus has a wide viewing angle and a fast response time.

[0004] A general OLED display apparatus includes red (R), green (G), and blue (B) sub-pixels as one unit pixel and display one image having various colors through the three sub-pixels.

[0005] In the case of the OLED display apparatus, if a fixed image (for example, an advertisement image of a store) is displayed for a long time, the corresponding light emitting devices also emit light continuously. If a current continuously flows through a specific light emitting device for a long time, the corresponding light emitting device may be overloaded and thus the lifespan of the corresponding light emitting device may be shortened.

[0006] As a result, the color representation capability of the corresponding light emitting device is degraded. Thus, if an image on a screen is changed, there occurs a burn-in phenomenon in which a screen is not displayed clearly as if an afterimage of a previous image remains or a screen is stained.

[0007] An afterimage compensation method is used for solving the problem that an afterimage of a previous image remains on a screen.

[0008] The afterimage compensation method compensates for brightness reduced by deterioration of pixels, and requires a cooling time which is a time for turning off a display panel for a predetermined time. If a cooling time is not ensured for a sufficient time, the temperature of the display panel increases, and thus a voltage is excessively sensed. Thus, the accuracy of afterimage compensation may be reduced.

[0009] If AC power is off, the processor of the OLED display apparatus cannot measure the cooling time. Thus, if AC power is turned on after the AC power is turned off, the screen may be turned off so as to secure the cooling time of the display panel.

[0010] In this case, a user cannot use the display panel for a predetermined time because the screen is turned off. In particular, in a case where the display panel must be immediately used for promotion, just like TVs displayed in stores, store users may suffer great inconvenience because the screen is turned off so as to secure the cooling time.

[0011] Meanwhile, a battery and a real time check (RTC) circuit have been used for measuring the cooling time. However, the configuration of the battery and the RTC circuit is expensive, and the use of the battery is not permanent.

SUMMARY

[0012] Embodiments provide an organic light emitting diode (OLED) display apparatus capable of measuring a cooling time of a display panel even if the supply of power is interrupted.

[0013] Embodiments provides an OLED display apparatus capable of measuring a cooling time of a display panel by using a switch element and a capacitor, even if the supply of power is interrupted, without expensive battery or RTC circuit.

[0014] In one embodiment, an OLED display apparatus includes: a display panel; a discharge circuit configured to discharge a voltage if the display panel is driven for more than a predetermined time and the supply of power to the display panel is interrupted; and a processor configured to, if the power is supplied, determine whether a cooling time required for afterimage compensation of the display panel is satisfied, and if the cooling time is satisfied, perform the afterimage compensation of the display panel.

[0015] According to various embodiments of the present disclosure, if the supply of power is interrupted, the cooling time of the display panel can be measured. Thus, it is unnecessary to turn off the screen so as to secure the cooling time in a state in which the power is on. Therefore, the afterimage compensation can be quickly performed.

[0016] According to various embodiments of the present disclosure, if the supply of power is interrupted, the cooling time of the display panel can be measured by using an inexpensive discharge circuit, thereby achieving cost reduction.

[0017] The details of one or more embodiments are set forth in the accompanying drawings and the description below. Other features will be apparent from the description and drawings, and from the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

Fig. 1 is a block diagram illustrating a configuration

of an OLED display apparatus according to an embodiment of the present disclosure.

Fig. 2 is a block diagram for describing a configuration of a discharge circuit according to an embodiment of the present disclosure.

Fig. 3 is a circuit diagram for describing an actual circuit configuration of the discharge circuit according to an embodiment of the present disclosure.

Fig. 4 is a graph showing a change in an output voltage of a second switch according to a voltage discharge of a capacitor, according to an embodiment of the present disclosure.

Fig. 5 is a flowchart of a method of operating an OLED display apparatus, according to an embodiment of the present disclosure.

Figs. 6 and 7 are circuit diagrams for describing a configuration of a discharge circuit according to another embodiment of the present disclosure.

Fig. 8 is a diagram for describing a waveform of an output voltage of a discharge circuit according to a discharge of a capacitor, according to an embodiment of the present disclosure.

Fig. 9 is a flowchart of a method of operating an OLED display apparatus, according to another embodiment of the present disclosure.

FIG. 10 is a graph for describing a process of performing afterimage compensation of a display panel, according to an embodiment of the present disclosure.

Figs. 11A to 12 show test results for describing problems that may occur if afterimage compensation is performed if a cooling time of a display panel is not satisfied.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0019] Examples of various embodiments are illustrated in the accompanying drawings and described further below. The suffixes "module" and "unit" for components used in the description below are assigned or mixed in consideration of easiness in writing the specification and do not have distinctive meanings or roles by themselves.

[0020] A display apparatus according to an embodiment of the present disclosure is, for example, an intelligent display apparatus in which a computer support function is added to a broadcast reception function. An Internet function or the like is added to the display apparatus that fundamentally has the broadcast reception function. Accordingly, the display apparatus may include an easy-to-use interface, such as a writing input device, a touch screen, or a spatial remote control device. With the support of a wired or wireless Internet function, the display apparatus device may connect to the Internet and computers and perform functions such as e-mail, web browsing, banking, or games. In order to perform such various functions, standardized general-purpose OS may be used.

[0021] Accordingly, since various applications are freely added or deleted on a general purpose OS kernel, a display apparatus described herein may perform various user-friendly functions.

[0022] Fig. 1 is a block diagram illustrating a configuration of an organic light emitting diode (OLED) display apparatus according to an embodiment of the present disclosure.

[0023] Referring to Fig. 1, the OLED display apparatus 100 according to an embodiment of the present disclosure may include a power supply unit 110, a discharge circuit 130, a display panel 150, a memory 170, and a processor 190.

[0024] The power supply unit 110 may supply DC power or AC power to the OLED display apparatus 100.

[0025] If AC power is supplied to the OLED display apparatus 100 and DC power is not supplied thereto, the display panel 150 is in a standby state. From the viewpoint of the practical use, this may be a case where a user turns off the power of the display panel 150 through a remote controller and does not unplug an outlet.

[0026] If AC power is not supplied to the OLED display apparatus 100, the display panel 150 is in an off state. From the viewpoint of the practical use, this may be a case where a user unplugs an outlet.

[0027] The discharge circuit 130 may measure a cooling time necessary for afterimage compensation of the display panel 150.

[0028] If the supply of power is interrupted, the discharge circuit 130 may measure a discharge voltage amount of a capacitor.

[0029] The processor 190 may determine whether the cooling time during which the display panel 150 can be sufficiently cooled is secured by using the measured discharge voltage amount.

[0030] The display panel 150 may display an image.

[0031] The display panel 150 may be an OLED panel.

[0032] The display panel 150 may include a plurality of sub-pixels (SP). The plurality of sub-pixels may be formed in pixel regions defined by a plurality of gate lines and a plurality of data lines intersecting with one another.

[0033] A plurality of driving power lines are formed on the display panel 150. The plurality of driving power lines are formed in parallel to the plurality of data lines and supply driving power.

[0034] Each of the plurality of sub-pixels may be one of a red sub-pixel, a green sub-pixel, a blue sub-pixel, and a white sub-pixel.

[0035] One unit pixel which displays one image may include a red sub-pixel, a green sub-pixel, a blue sub-pixel, and a white sub-pixel adjacent to one another, or may include a red sub-pixel, a green sub-pixel, and a blue sub-pixel.

[0036] Each of the plurality of sub-pixels may include an OLED and a pixel circuit.

[0037] The OLED is connected between the pixel circuit and a second driving power line and emits predetermined color light by emitting light in proportion to a data current amount supplied from the pixel circuit.

[0038] To this end, the OLED includes an anode electrode (or a pixel electrode) connected to the pixel circuit, a cathode electrode (or a reflection electrode) connected to the second driving power line, and a light emitting cell formed between the anode electrode and the cathode electrode to emit light of one of red, green, blue, and white colors.

[0039] The light emitting cell may be formed to have a structure of hole transport layer/organic emission layer/electron transport layer or a structure of hole injection layer/hole transport layer/organic emission layer/electron transport layer/electron injection layer. In addition, the light-emitting cell may further include a functional layer for improving the luminescent efficiency and/or lifespan of the organic emission layer.

[0040] The pixel circuit supplies the OLED with a data current corresponding to a data voltage supplied from a data driver to a data line in response to a gate signal of a gate-on voltage level supplied from a gate driver to a gate line.

[0041] At this time, the data voltage has a voltage value in which deterioration characteristics of the OLED are compensated. To this end, the pixel circuit includes a switching transistor, a driving transistor, and at least one capacitor, which are formed on a substrate by a thin film transistor forming process. The switching transistor and the driving transistor may be a-Si TFT, poly-Si TFT, oxide TFT, organic TFT, or the like.

[0042] The switching transistor may supply a gate electrode of the driving transistor with the data voltage supplied to the data line according to the gate signal of the gate-on voltage level supplied to the gate line.

[0043] Since the driving transistor is turned on according to a gate-source voltage including the data voltage supplied from the switching transistor, it is possible to control a current amount flowing from a driving voltage line (PL1) to the OLED.

[0044] The memory 170 may store the cooling time of the display panel 150. Although described below, the cooling time may be the time during which the display panel 150 must be turned off for afterimage compensation of the display panel 150.

[0045] The processor 190 may control an overall operation of the OLED display apparatus 100.

[0046] The processor 190 may include a timing controller. However, this is merely an example, and the timing controller may be present as a separate element from the processor.

[0047] The timing controller may control driving timings of the gate driver and the data driver based on a timing synchronization signal input from an external system main body (not shown) or a graphic card (not shown).

[0048] The timing controller may generate a gate control signal and a data control signal based on a timing synchronization signal such as a vertical synchronization signal, a horizontal synchronization signal, a data enable signal, a dot clock, or the like.

[0049] The timing controller may control the driving timing of the gate driver through the gate control signal, and may control the driving timing of the data driver through the data control signal so as to be synchronized therewith.

[0050] The processor 190 may measure the use time of the display panel 150. If the measured use time exceeds a predetermined time, the processor 190 may automatically perform an afterimage compensation algorithm for preventing pixel deterioration of the display panel 150.

[0051] In one embodiment, the predetermined time may be 2,000 hours for household use, and 600 hours for a store, but this is merely an example.

[0052] The processor 190 performs an operation for compensating for an afterimage generated in the display panel 150 at regular periods, so as to prevent deterioration of pixels constituting the display panel 150.

[0053] In order for accurate afterimage compensation, the display panel 150 needs to be sufficiently cooled.

[0054] That is, before the afterimage compensation, the display panel 150 needs to secure the cooling time during which the operation must be turned off.

[0055] If the supply of AC power to the OLED display apparatus 100 is maintained and the supply of DC power is interrupted, the processor 190 is in an enabled state, and thus, it is possible to measure the cooling time during which the display panel 150 is turned off.

[0056] In one embodiment, the processor 190 may use a timer to measure the time during which the display panel 150 has been turned off and determine whether the measured time satisfies the cooling time.

[0057] In another embodiment, if the supply of AC power is maintained and the supply of DC power is interrupted, the processor 190 may measure the cooling time of the display panel 150 by using the discharge circuit 130, which will be described below.

[0058] Meanwhile, even if the supply of AC power is interrupted, the processor 190 may check the cooling time of the display panel 150 by using the discharge circuit 130.

[0059] The processor 190 may measure the cooling time of the display panel 150 by checking the discharge amount of the capacitor which is measured by the discharge circuit 130.

[0060] The specific operation of the processor 190 will be described below in more detail.

[0061] Fig. 2 is a block diagram for describing the configuration of the discharge circuit according to an embodiment of the present disclosure, and Fig. 3 is a circuit diagram for describing the actual circuit configuration of the discharge circuit according to an embodiment of the present disclosure.

[0062] The discharge circuit 130 has been described as being present as a separate element from the processor 190, but is not limited thereto. The discharge circuit 130 may be included in the configuration of the processor 190.

[0063] The discharge circuit 130 may be included in

the processor 190 in the form of System On Chip (SOC), or may be configured separately from the processor 190, which is in the SOC form, and connected to the processor 190.

[0064] Referring to Figs. 2 and 3, the discharge circuit 130 may include a DC power supply unit 131, a discharge control terminal 132, a first switch 133, a capacitor 134, a second switch 135, and a discharge check terminal 136.

[0065] In Figs. 2 and 3, the discharge control terminal 132 and the discharge check terminal 136 are described as being included in the discharge circuit 130, but this is merely an example. The discharge control terminal 132 and the discharge check terminal 136 may be included in the processor 190.

[0066] Hereinafter, it is assumed that the case where the supply of power to the display panel 150 is interrupted includes both the case where the supply of AC power to the display panel 150 is interrupted and the case where the supply of DC power to the display panel 150 is interrupted.

[0067] The processor 190 may determine whether the cooling time necessary for cooling the display panel 150 is secured, during a period of time during which the supply of power to the display panel 150 through the discharge circuit 130 is turned off (interrupted).

[0068] If the power is supplied to the processor 190, the processor 190 may determine whether the display panel 150 has satisfied the cooling time during a period of time during which the supply of power to the display panel 150 is interrupted, based on the signal output from the discharge circuit 130.

[0069] The processor 190 determines the cooling time if the power is supplied to the processor 190, because the processor 190 is not enabled if the power is not supplied to the processor 190, and thus, the processor 190 cannot determine whether the display panel 150 has satisfied the cooling time.

[0070] The DC power supply unit 131 may supply DC power to the discharge circuit 130. In particular, the DC power supply unit 131 may supply DC power to the first switch 133 or the second switch 135.

[0071] The DC power supply unit 131 may include the discharge circuit 130 as shown in Fig. 2, but this is merely an example. The DC power supply unit 131 may be present as a separate element from the discharge circuit 130.

[0072] The discharge control terminal 132 may apply, to the first switch 133, a signal capable of determining whether the capacitor 134 is charged or discharged under the control of the processor 190.

[0073] The discharge control terminal 132 may be a general port input/output (GPIO) output terminal.

[0074] The discharge control terminal 132 may determine whether to apply a high signal for turning on the first switch 133 according to whether the power is supplied to the display panel 150.

[0075] If the power is supplied to the display panel 150, the discharge control terminal 132 may apply the high signal for turning on the first switch 133 to the first switch 133.

[0076] If the power is not supplied to the display panel 150, the discharge control terminal 132 may not apply the high signal to the first switch 133. That is, if the power is not supplied to the display panel 150, a voltage for driving the first switch 133 is not applied, and thus the first switch 133 may be turned off.

[0077] This seems as if a low signal for turning off the first switch 133 is applied to the first switch 133.

[0078] The first switch 133 may be a bipolar junction transistor (BJT). The reason why the BJT is used as the first switch 133 is that the use of a field effect transistor (FET) may cause an unintended discharge operation because of parasitic diode components between a source terminal and a drain terminal.

[0079] The first switch 133 may be turned on according to the high signal received from the discharge control terminal 132. As the first switch 133 is turned on, a DC voltage transferred from the DC power supply unit 131 may be applied to the capacitor 134.

[0080] Accordingly, the capacitor 134 may be charged with voltage.

[0081] If the supply of power to the display panel 150 is interrupted, the first switch 133 may be turned off. As the first switch 133 is turned off, the voltage charged in the capacitor 134 may be discharged.

[0082] The capacitor 134 may be charged or discharged according to the on or off operation of the first switch 133.

[0083] If the supply of power is interrupted, the capacitor 134 may have a capacity to measure the time that is the same as the predetermined cooling time of the display panel 150 or exceeds the cooling time thereof.

[0084] In Figs. 2 and 3, it has been assumed that one capacitor 134 is used, but embodiments of the present disclosure are not limited thereto. The capacitor 134 may be configured by a plurality of capacitors.

[0085] The second switch 135 may be turned on according to the discharge of the capacitor 134. That is, the voltage discharged from the capacitor 134 is applied to a gate terminal of the second switch 135, and thus the second switch 135 may be turned on.

[0086] While the voltage is charged to the capacitor 134, no voltage is applied to the gate terminal of the second switch 135, and thus the second switch 135 may be turned off.

[0087] The second switch 135 may be turned off if the voltage charged in the capacitor 134 is completely discharged.

[0088] The discharge check terminal 136 may output a discharge uncompleted signal or a discharge completed signal based on a voltage at a reference point K1 connected to the second switch 135 and the power supply unit 131. The reference point K1 is a reference point for determining whether the voltage of the capacitor 134 has been completely discharged.

[0089] Referring to Fig. 3, the reference point K1 may

be a point at which one end of the discharge check terminal 136, the drain terminal of the second switch (FET) 135, and one end of a third resistor R3 are met.

[0090] The discharge check terminal 136 may detect the on/off state of the second switch 135 based on the measured voltage.

[0091] If the voltage measured at the reference point K1 is a first voltage or lower, the discharge check terminal 136 may determine that the second switch 135 is in a turned-on state, and output a discharge-uncompleted signal indicating that the voltage of the capacitor 134 has not been completely discharged. It will be understood throughout that in alternate embodiments, the discharge check terminal may only output a discharge-completed signal when the voltage of the capacitor has been completely discharged, and no discharge-uncompleted signal is output.

[0092] The first voltage may be a maximum voltage satisfying an output condition of the discharge-uncompleted signal.

[0093] The first voltage may be 0.67 V, but is merely an example.

[0094] If the voltage measured at the reference point K1 is a second voltage or higher, the discharge check terminal 136 may determine that the second switch 135 is in a turned-off state, and output a discharge-completed signal indicating that the voltage of the capacitor 134 has been completely discharged.

[0095] The second voltage may be a minimum voltage satisfying an output condition of the discharge-completed signal.

[0096] The second voltage may be 2.7 V, but is merely an example.

[0097] If the second switch 135 is turned on, the discharge check terminal 136 may recognize that the voltage of the capacitor 134 has not been completely discharged, and output a discharge-uncompleted signal. In alternate embodiments, the discharge check terminal may only output a discharge-completed signal when the voltage of the capacitor has been completely discharged, and no discharge-uncompleted signal is output.

[0098] In addition, if the second switch 135 is turned off, the discharge check terminal 136 may recognize that the voltage of the capacitor 134 has been completely discharged, and output a discharge-completed signal.

[0099] If the discharge-completed signal is output through the discharge check terminal 136, the processor 190 may determine that the cooling time of the display panel 150 is satisfied.

[0100] If the cooling time is satisfied, the processor 190 may perform an afterimage compensation algorithm. To this end, the processor 190 may include an afterimage compensation circuit.

[0101] The afterimage compensation circuit may be a circuit for compensating for the deterioration of the pixels of the display panel 150.

[0102] The afterimage compensation circuit may include a current sensor for measuring a current flowing through the OLED constituting the pixel.

[0103] The afterimage compensation circuit may detect the deterioration degree of the pixel by using a difference between an existing current value and a changed current value with respect to the same voltage.

[0104] The afterimage compensation circuit may acquire a current amount, of which a current value is reduced with respect to an existing current value. The afterimage compensation circuit may compensate for the deterioration of the pixel by applying the reduced current amount to the OLED.

[0105] The cooling time necessary for the afterimage compensation of the display panel 150 may be 55 minutes, but this is merely an example. The cooling time may be changed according to the size of the display panel 150 and the model of the display panel 150.

[0106] The reason why the cooling time of a predetermined time is secured before the afterimage compensation is that, if the afterimage compensation is performed in a state in which the display panel 150 is not sufficiently cooled, the temperature of the display panel 150 is high and an excessive voltage is sensed, and thus the afterimage compensation is not accurately performed.

[0107] If the discharge-uncompleted signal is output through the discharge check terminal 136, or if the discharge-completed signal has not yet been output, the processor 190 may determine that the cooling time of the display panel 150 is not satisfied. In this case, if AC power is supplied, the processor 190 may output a notification indicating that the cooling time is not satisfied through the display panel 150.

[0108] Then, the processor 190 may perform an operation for securing the cooling time of the display panel 150. The operation for securing the cooling time of the display panel 150 may be an operation of turning off a screen of the display panel 150.

[0109] If the cooling time of the display panel 150 is secured, the processor 190 may perform the afterimage compensation algorithm.

[0110] Next, the actual circuit configuration of the discharge circuit 130 according to an embodiment of the present disclosure will be described with reference to Fig. 3.

[0111] One end of the discharge control terminal 132 is connected to one end of a first resistor R1. The other end of the discharge control terminal 132 is connected to the processor 190.

[0112] The other end of the first resistor R1 is connected to a base terminal B of a first switch (BJT) 133.

[0113] A collector terminal C of the first switch 133 is connected to one end of a second resistor R2.

[0114] An emitter terminal E of the first switch 133 is connected to one end of a capacitor 134.

[0115] One end of the capacitor 134 is connected to a gate terminal of the second switch (FET) 135.

[0116] The other end of the capacitor 134 is grounded.

[0117] A source terminal S of the second switch 135 is grounded, and a drain terminal D of the second switch

135 is connected to one end of the discharge check terminal 136 and one end of a third resistor R3.

[0118] The other end of the discharge check terminal 136 is connected to the processor 190.

[0119] The other end of the third resistor R3 is connected to the other end of the second resistor R2 and the DC power supply unit 131

[0120] The reference point K1 may be a point at which one end of the discharge check terminal 136, the drain terminal of the second switch (FET) 135, and one end of the third resistor R3 are met.

[0121] Fig. 4 is a graph showing a change in the output voltage of the second switch according to the voltage discharge of the capacitor, according to an embodiment of the present disclosure.

[0122] Hereinafter, the description of Fig. 4 is given based on the description provided with reference to Figs. 2 and 3.

[0123] In the graph of Fig. 4, a horizontal axis represents a time and a vertical axis represents a voltage value.

[0124] A first waveform 410 is a waveform showing a change in a voltage discharged from the capacitor 134. That is, the first waveform 410 is a waveform showing a change in a voltage across the capacitor 134.

[0125] A second waveform 430 is a waveform showing a change in a voltage output from the reference point K1 of Fig. 3.

[0126] As can be seen from the first waveform 410, as the voltage charged in the capacitor 134 is discharged, the voltage across the capacitor 134 is reduced.

[0127] Accordingly, the discharged voltage is applied to the gate terminal G of the second switch 135, and thus the voltage measured at the reference point K1 may increase (see the second waveform).

[0128] As a result, the voltage measured at the reference point K1 may be a voltage that increases as the capacitor 134 is discharged.

[0129] If the voltage measured at the reference point K1 is a second voltage A, the processor 190 may determine that the cooling time of the display panel 150 is satisfied.

[0130] That is, if the voltage measured at the reference point K1 is the second voltage A, the discharge check terminal 136 may determine that the second switch 135 is turned off, and output the discharge-completed signal.

[0131] More specifically, if the voltage measured at the reference point K1 is the second voltage A or higher, the discharge check terminal 136 may determine that the second switch 135 is turned off, and output the discharge-completed signal.

[0132] The processor 190 may determine that the cooling time of the display panel 150 is satisfied through the discharge-completed signal.

[0133] The processor 190 may drive the afterimage compensation algorithm according to the discharge-completed signal output from the discharge check terminal 136.

[0134] In one embodiment, if the voltage measured at the reference point K1 is the first voltage B or lower, the discharge check terminal 136 may determine that the second switch 135 is turned on, and output the discharge-uncompleted signal. In alternate embodiments, the discharge check terminal may only output a discharge-completed signal when the voltage of the capacitor has been completely discharged, and no discharge-uncompleted signal is output.

[0135] If the discharge-uncompleted signal is detected, or if no discharge-completed signal has been detected, the processor 190 may determine that the cooling time of the display panel 150 is not satisfied, and turn off the screen so as to satisfy the cooling time of the display panel 150.

[0136] Then, if the cooling time of the display panel 150 is secured, the processor 190 may drive the afterimage compensation circuit.

[0137] Next, the process of performing the afterimage compensation algorithm according to whether the cooling time of the display panel 150 is satisfied will be described with reference to the flowchart.

[0138] Fig. 5 is a flowchart of a method of operating the OLED display apparatus, according to an embodiment of the present disclosure.

[0139] Hereinafter, the method of operating the OLED display apparatus will be described with reference to Figs. 1 to 4.

[0140] First, if AC power is supplied to the display panel 150, the processor 190 turns on the first switch 133 (S501), and the voltage transferred from the DC power supply unit 131 is charged to the capacitor 134 as the first switch 133 is turned on (S503).

[0141] Then, if the supply of AC power is interrupted, the first switch 133 is also turned off (S505).

[0142] Accordingly, the voltage charged in the capacitor 134 is discharged (S507).

[0143] The discharge voltage of the capacitor 134 is applied to the second switch 135 (S509). If the supply of AC power is supplied, the processor 190 detects a signal output from the discharge check terminal 136 (S511).

[0144] The processor 190 may determine whether the signal output from the discharge check terminal 136 is a discharge-completed signal (S513).

[0145] If the discharge check terminal 136 outputs the discharge-completed signal, the processor 190 may perform the afterimage compensation algorithm (S515). That is, the discharge-completed signal may be a trigger signal for driving the afterimage compensation algorithm to the display panel 150.

[0146] If the discharge check terminal 136 outputs the discharge-uncompleted signal, or in other embodiment if the discharge completed signal has not yet been output, the processor 190 turns off the screen of the display panel 150 so as to secure the cooling time of the display panel 150 (S517).

[0147] That is, the discharge-uncompleted signal, or in other embodiments the lack of discharge-completed

signal, may be a signal for securing the cooling time of the display panel 150.

[0148] In one embodiment, the processor 190 may output a notification indicating that the operation for securing the cooling time of the display panel 150 is being performed.

[0149] If the cooling time of the display panel 150 is secured (S519), the processor 190 may perform the afterimage compensation algorithm (S515).

[0150] Next, a configuration of a discharge circuit according to another embodiment of the present disclosure will be described.

[0151] Figs. 6 and 7 are circuit diagrams for describing a configuration of a discharge circuit according to another embodiment of the present disclosure.

[0152] In particular, Fig. 6 is a circuit diagram of a discharge circuit 600 for reducing an unknown period of the voltage measured at the reference point K1 described with reference to Fig. 4, and Fig. 7 is a circuit diagram of a discharge circuit 700 for removing an unknown period of the voltage measured at the reference point K1.

[0153] Referring to Fig. 6, the discharge circuit 600 may include a DC power supply unit 131, a discharge control terminal 132, a first switch 133, a capacitor 134, a second switch 135, a third switch 137, and a discharge check terminal 136.

[0154] The DC power supply unit 131, the discharge control terminal 132, the first switch 133, the capacitor 134, and the second switch 135 are substantially the same as those of Figs. 2 and 3.

[0155] The discharge circuit 600 of Fig. 6 may further include the third switch 137, in addition to the discharge circuit 130 of Figs. 2 and 3.

[0156] The third switch 137 may be a FET.

[0157] A gate terminal G of the third switch 137 is connected to a drain terminal of the second switch 135 and one end of the third resistor R3.

[0158] A source terminal S of the third switch 137 is grounded

[0159] A drain terminal D of the third switch 137 is connected to one of the discharge check terminal 136 and one end of a fourth resistor R4. The other end of the fourth resistor R4 is connected to one end of a third resistor R3.

[0160] A reference point K2 may be a point at which one end of the fourth resistor R4, one end of the discharge check terminal 136, and the drain terminal of the third switch 137 are met.

[0161] The third switch 137 may be a switch used for reducing an unknown period.

[0162] This will be described below with reference to Fig. 4.

[0163] Referring to Fig. 4, if the voltage measured at the reference point K1 is a second voltage A or higher, the processor 190 may read the discharge-completed (or high) signal of the discharge check terminal 136 and check that the cooling time of the display panel 150 is satisfied.

[0164] In addition, if the voltage measured at the reference point K1 is the first voltage B or lower, the processor 190 may read the discharge-uncompleted (or low) signal of the discharge check terminal 136.

[0165] That is, the processor 190 may recognize only a case where the voltage measured at the reference point K1 is the first voltage B or lower and a case where the voltage measured at the reference point K1 is the second voltage A or higher. In other words, the processor 190 cannot check the voltage of the reference point K1 which exceeds the first voltage B and is lower than the second voltage A.

[0166] Since the discharge check terminal 136 cannot check the voltage that is lower than the second voltage A and exceeds the first voltage B, the period between the first voltage B and the second voltage A may be referred to as an unknown period t1.

[0167] If the unknown period t1 is long, the time for determining the cooling time of the display panel 150 may not be accurately grasped. Due to this, the afterimage compensation operation of the display panel 150 may not be smoothly performed.

[0168] If the unknown period t1 can be reduced, whether the cooling time is satisfied may be more accurately grasped.

[0169] The discharge circuit 600 of Fig. 6 is capable of reducing the unknown period through the third switch 137.

[0170] The third switch 137 may invert the voltage at the reference point K1 and output the inverted voltage.

[0171] The waveform of the voltage at the reference point K2 will be described with reference to Fig. 8.

[0172] Fig. 8 is a diagram for describing a waveform of an output voltage of a discharge circuit according to a discharge of a capacitor, according to an embodiment of the present disclosure.

[0173] Referring to Fig. 8, a first waveform 410 is a waveform showing a change in a voltage discharged from the capacitor 134. That is, the first waveform 410 is a waveform showing a change in a voltage across the capacitor 134.

[0174] A third waveform 810 is a waveform showing a change in the voltage measured at the reference point K2 of Fig. 6.

[0175] Referring to Fig. 8, the voltage measured at the reference point K2 is inverted while passing through the third switch 137.

[0176] In this case, if the voltage measured at the reference point K2 is the first voltage B or lower, the discharge check terminal 136 may detect the discharge-completed signal.

[0177] If the voltage measured at the reference point K2 exceeds the second voltage A, the discharge check terminal 136 may detect the discharge-uncompleted signal.

[0178] In addition, if a FET is used as the third switch 137, the time to reach the first voltage B from the second voltage A may be reduced through a high speed switching

operation.

[0179] The unknown period in which the voltage measured at the reference point K2 reaches the first voltage B from the second voltage A is remarkably reduced by t2, as compared with the unknown period t1.

[0180] Next, Fig. 7 is described.

[0181] In particular, a circuit of Fig. 7 may be a discharge circuit 700 for removing an unknown period.

[0182] Referring to Fig. 7, the discharge circuit 700 may include a DC power supply unit 131, a discharge control terminal 132, a first switch 133, a capacitor 134, a second switch 135, a diode pair 138, a first capacitor 139, a reset IC circuit 140, a second capacitor 141, and a discharge check terminal 136.

[0183] The DC power supply unit 131, the discharge control terminal 132, the first switch 133, the capacitor 134, and the second switch 135 are substantially the same as those of Figs. 2 and 3.

[0184] The diode pair 138 may include a first diode 138a and a second diode 138b.

[0185] One end of the first diode 138a is connected to one end of a third resistor R3 and a drain terminal of the second switch 135. One end of the first diode 138a is connected to one end of the first capacitor 139 and one end of the reset IC circuit 140.

[0186] One end of the second diode 138b is connected to one end of a fifth resistor R5 and one end of a sixth resistor R6. The other end of the second diode 138b is connected to one end of the first capacitor 139 and one end of the reset IC circuit 140.

[0187] The other end of the fifth resistor R5 is connected to the other end of the third resistor R3, and the other end of the sixth resistor R6 is grounded.

[0188] The other end of the first capacitor 139 is grounded.

[0189] The other end of the reset IC circuit 140 is connected to one end of the discharge check terminal 136, one end of the second capacitor 141, and one end of a seventh resistor R7. The other end of the second capacitor 141 is grounded.

[0190] The other end of the seventh resistor R7 is connected to the DC power supply unit 131.

[0191] The diode pair 138 serves to satisfy a minimum voltage for driving the reset IC circuit 140.

[0192] The first capacitor 139 may remove a noise from a voltage output by the diode pair 138.

[0193] The second capacitor 141 may remove a noise from a voltage output from the reset IC circuit 140.

[0194] If the voltage measured at the reference point K3 exceeds a predetermined voltage, the reset IC circuit 140 may output the discharge-completed signal to the discharge check terminal 136.

[0195] The reference point K3 may be a point at which the other end of the reset IC circuit 140, one end of the discharge check terminal 136, one end of the second capacitor 141, and one end of the seventh resistor R7 are met.

[0196] If the voltage measured at the reference point K3 is lower than the predetermined voltage, the reset IC circuit 140 may output the discharge-uncompleted signal to the discharge check terminal 136. In alternate embodiments, the reset IC circuit may only output a discharge-completed signal when the voltage of the capacitor has been completely discharged, and no discharge-uncompleted signal is output.

[0197] That is, the reset IC circuit 140 may output the discharge-completed signal if the voltage measured at the reference point K3 exceeds the predetermined voltage, and in some embodiments may output the discharge-uncompleted signal if the voltage measured at the reference point K3 is lower than the predetermined voltage.

[0198] If the voltage measured at the reference point K3 is equal to the predetermined voltage, the reset IC circuit 140 may output the discharge-completed signal or in some embodiments the discharge-uncompleted signal.

[0199] That is, even if the voltage measured at the reference point K3 is equal to the predetermined voltage, the reset IC circuit 140 may output the discharge-completed signal or in some embodiments the discharge-uncompleted signal so as to prevent the occurrence of the unknown period.

[0200] Referring to Fig. 8, a fourth waveform 830 shows a waveform of the voltage measured at the reference point K3 if the reset IC circuit 140 is included in the discharge circuit 700.

[0201] It can be seen from the fourth waveform 830 that no unknown period is present in the process of changing the first voltage B to the second voltage A. This is because, due to the presence of the reset IC circuit 140, it is designed to output only the discharge-completed signal or in some embodiments the discharge-uncompleted signal.

[0202] In the case of using the reset IC circuit 140, the unknown period is not present, and thus the cooling time of the display panel 140 may be more accurately measured. Therefore, the afterimage compensation of the display panel 140 may be stably performed.

[0203] Next, a method of operating an OLED display apparatus, according to another embodiment of the present disclosure, will be described with reference to Fig. 9.

[0204] In particular, Fig. 9 is a flowchart of a method of preventing the afterimage compensation algorithm from being driven, even though the cooling time of the display panel 150 is not satisfied, in a case where the FET or the capacitor is burnt or cracked.

[0205] The embodiment of Fig. 9 is described on the assumption of the discharge circuit 700 described with reference to Fig. 7, but is a scenario that is applicable to both of Fig. 3 and 6.

[0206] The power supply unit 110 supplies AC power to the display panel 150 (S901).

[0207] The processor 190 determines whether the discharge completed signal has been received (S903).

[0208] In one embodiment, if the discharge-completed signal is output through the discharge check terminal 136, the processor 190 may determine that the voltage discharge of the capacitor 134 has been completed.

[0209] In one embodiment, if the discharge-uncompleted signal is output through the discharge check terminal 136, or in some embodiments if the discharge completed signal has not yet been output, the processor 190 may determine that the voltage discharge of the capacitor 134 has not been completed.

[0210] If it is determined that the voltage discharge of the capacitor 134 has been completed, the processor 190 recharges the voltage of the capacitor (S905), and determines whether the discharge completed signal has been received (S907).

[0211] If it is determined that the discharge completed signal has been received, the processor 190 determines that the discharge circuit 700 malfunctions, and performs step 903 again, without performing the afterimage compensation algorithm (S907).

[0212] That is, if the voltage of the capacitor 134 is recharged, the discharge check terminal 136 must not output the discharge-completed signal.

[0213] If the discharge-completed signal is detected through the discharge check terminal 136, the processor 190 may determine that the discharge circuit 700 malfunctions and do not perform the afterimage compensation of the display panel 150.

[0214] If it is determined that the voltage discharge of the capacitor has not been completed, the processor 190 performs the afterimage compensation algorithm (S909).

[0215] The processor 190 may perform operations S905 to S909 more than a predetermined number of times. This is done for securing the reliability of the operation of the discharge circuit.

[0216] The processor 190 turns off the screen of the display panel 150 during the execution of the afterimage compensation algorithm (S911).

[0217] After the afterimage compensation algorithm has been completed, the processor 190 may turn on the screen of the display panel 150.

[0218] FIG. 10 is a graph for describing the process of performing the afterimage compensation of the display panel, according to an embodiment of the present disclosure.

[0219] The sequence for compensating for the afterimage of the display panel 150 is shown in Fig. 10.

[0220] It is assumed in Fig. 10 that the use time necessary for the afterimage compensation of the display panel 150 is satisfied.

[0221] The graph of Fig. 10 is divided into a plurality of periods. The plurality of periods may include a pre-compensation activation period H1, an Off-RS compensation period H2, a cooling time period H3, an afterimage compensation period H4, and a post-compensation activation period H5.

[0222] The pre-compensation activation period H1 and the post-compensation activation period H5 may be periods in which AC power is supplied to the display panel 150 and thus the image is driven on the display panel 150.

[0223] The Off-RS compensation period H2 may be a period in which the compensation for the voltage of the display panel 150 is performed without regard to the temperature of the display panel 150 (that is, the cooling time is not needed).

[0224] The Off-RS compensation period H2 may be a period of a standby state in which AC power is supplied, but DC power is not supplied.

[0225] The cooling time period H3 may be a period that turns off the screen of the display panel 150 before the afterimage compensation.

[0226] The afterimage compensation period H4 is a period that compensates for the deterioration of pixels constituting the display panel 150 after the cooling time period H3.

[0227] If the afterimage compensation is performed in a state in which the cooling time of the display panel 150 is not satisfied, a pixel deterioration compensation rate may be reduced.

[0228] This will be described with reference to the accompanying drawings.

[0229] Figs. 11a to 12 show test results for describing problems that may occur if the afterimage compensation is performed if the cooling time of the display panel is not satisfied.

[0230] In particular, Figs. 11a to 12 show a change in a gain value of afterimage compensation according to a change in the cooling time of the display panel 150, after the image driving is finished, if an ambient temperature of the display panel 150 is 25• C.

[0231] In order to properly perform the afterimage compensation of the display panel 150, the gain value must maintain a predetermined value or more.

[0232] Figs. 11a to 11f show a change in an afterimage gain value according to a pixel with respect to each of a plurality of image scanning lines.

[0233] Each test was performed in a case where the afterimage compensation was performed immediately after the display panel 150 finished the image driving, in a case where the afterimage compensation was performed after 2 minutes, in a case where the afterimage compensation was performed after 6 minutes, in a case where the afterimage compensation was performed after 20 minutes, and in a case where the afterimage compensation was performed after 60 minutes. It is assumed that the cooling time of the display panel 150 necessary for the afterimage compensation is 60 minutes.

[0234] In this case, it is assumed that the waveform on which the afterimage compensation is performed satisfies the cooling time after 60 minutes from the finish of the image driving.

[0235] Fig. 11a is a waveform diagram showing a change in an afterimage compensation value according to a pixel, which was measured at a 2100th image scanning line.

[0236] Fig. 11b is a waveform diagram showing a

change in an afterimage compensation value according to a pixel, which was measured at a 1950th image scanning line.

[0237] Fig. 11c is a waveform diagram showing a change in an afterimage compensation value according to a pixel, which was measured at a 1580th image scanning line.

[0238] Fig. 11d is a waveform diagram showing a change in an afterimage compensation value according to a pixel, which was measured at a 1220th image scanning line.

[0239] Fig. 11e is a waveform diagram showing a change in an afterimage compensation value according to a pixel, which was measured at a 1000th image scanning line.

[0240] Fig. 11f is a waveform diagram showing a change in an afterimage compensation value according to a pixel, which was measured at a 500th image scanning line.

[0241] Referring to Figs. 11a to 11f, it is confirmed that the gain value of the afterimage compensation is rapidly reduced so that the afterimage compensation is rapidly performed immediately after the image driving is finished. That is, if the cooling time is short as compared with the cooling time of the display panel 150, the afterimage compensation gain value becomes small, thus causing the problem that reduces the compensation rate of the pixel.

[0242] Referring to Figs. 11a and 11c, immediately after the image driving (it is assumed to be 1 second), it can be seen from the waveform of performing the afterimage compensation that the afterimage compensation gain value is erroneously measured. This is caused by local heat generation. If the afterimage compensation gain value is erroneously measured, it is highly likely that the afterimage compensation is inaccurately performed.

[0243] Fig. 12 is an enlarged view of a portion 1150 of the graph of Fig. 11e.

[0244] Referring to Fig. 12, first to fifth gain waveforms 1201 to 1209 are shown on the 1000th image scanning line.

[0245] The first gain waveform 1201 is a waveform showing a change in the afterimage compensation gain value according to a pixel, if the afterimage compensation is performed, immediately after the image driving (after 1 second) on the display panel 150.

[0246] The second gain waveform 1203 is a waveform showing a change in the afterimage compensation gain value according to a pixel, if the afterimage compensation is performed, after 2 minutes from the finish of the image driving on the display panel 150.

[0247] The third gain waveform 1205 is a waveform showing a change in the afterimage compensation gain value according to a pixel, if the afterimage compensation is performed, after 6 minutes from the finish of the image driving on the display panel 150.

[0248] The fourth gain waveform 1207 is a waveform showing a change in the afterimage compensation gain value according to a pixel, if the afterimage compensation is performed, after 20 minutes from the finish of the image driving on the display panel 150.

[0249] The fifth gain waveform 1209 is a waveform showing a change in the afterimage compensation gain value according to a pixel, if the afterimage compensation is performed, after 60 minutes from the finish of the image driving on the display panel 150.

[0250] In the first to fifth gain waveforms 1201 to 1209, the afterimage compensation gain values corresponding to the 1790th pixel are compared.

[0251] The afterimage compensation gain value is 0.42 in the case of the fifth gain waveform 1209, 0.39 in the case of the fourth gain waveform 1207, 0.31 the case of the third gain waveform 1205, 0.26 the case of the second gain waveform 1203, and 0.18 the case of the first gain waveform 1201.

[0252] As the cooling time is shorter as compared with the cooling time of 60 minutes, the afterimage compensation gain value is reduced.

[0253] As the afterimage compensation gain value is reduced, it is highly likely that the timing controller will inaccurately recognize the deterioration of the pixel, thus causing the problem that reduces the compensation rate.

[0254] According to an embodiment, the above-described method may also be embodied as processor-readable codes on a program-recorded medium. Examples of the processor-readable medium may include a ROM, a RAM, a CD-ROM, a magnetic tape, a floppy disk, and an optical data storage device.

[0255] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the spirit and scope of the principles of this disclosure. More particularly, various variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the disclosure, the drawings and the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

Claims

1. An organic light emitting diode display apparatus comprising:

   a display panel;
   a discharge circuit configured to discharge a voltage if the display panel is driven for more than a predetermined time and the supply of power to the display panel is interrupted; and
   a processor configured to:

      if the power is supplied, determine whether a cooling time required for afterimage com-

pensation of the display panel is satisfied, based on the discharged voltage, and
if the cooling time is satisfied, perform the afterimage compensation of the display panel.

2. The organic light emitting diode display apparatus according to claim 1, wherein the discharge circuit comprises:

a capacitor;
a first switch configured to be turned on or off according to whether the power is supplied to the display panel; and
a second switch configured to be turned on or off according to whether the capacitor is charged or discharged, and
the processor determines whether the cooling time is satisfied according to a turned-on or turned-off state of the second switch.

3. The organic light emitting diode display apparatus according to claim 2, wherein the discharge circuit further comprises:

a discharge control terminal configured to determine whether to apply a high signal for turning on the first switch according to whether the power is supplied to the display panel; and
a discharge check terminal configured to output a discharge-completed signal or a discharge-uncompleted signal according to the turned-on or turned-off state of the second switch.

4. The organic light emitting diode display apparatus according to claim 3, wherein the discharge check terminal measures a voltage at a first reference point that meets one end of the second switch, determines that the second switch is turned on if the voltage measured at the first reference point is a first voltage or lower, and outputs the discharge-uncompleted signal, and
the discharge check terminal determines that the second switch is turned off if the voltage measured at the first reference point is a second voltage or higher, and outputs the discharge-completed signal.

5. The organic light emitting diode display apparatus according to claim 4, wherein the processor performs the afterimage compensation if the discharge-completed signal is detected through the discharge check terminal, and
the processor does not perform the afterimage compensation if the discharge-uncompleted signal is detected.

6. The organic light emitting diode display apparatus according to claim 5, wherein, if the discharge-uncompleted signal is detected, the processor outputs a notification indicating that the cooling time of the display panel is not secured.

7. The organic light emitting diode display apparatus according to claim 6, wherein the processor performs the afterimage compensation if the cooling time is satisfied.

8. The organic light emitting diode display apparatus according to claim 2, wherein the first switch is a bipolar junction transistor, and the second switch is a field effect transistor.

9. The organic light emitting diode display apparatus according to claim 4, further comprising a third switch configured to reduce an unknown period of the voltage measured at the first reference point,
wherein the unknown period is a period taken for the first voltage to reach the second voltage.

10. The organic light emitting diode display apparatus according to claim 9, wherein the third switch is a field effect transistor.

11. The organic light emitting diode display apparatus according to claim 4, wherein the discharge circuit further comprises a reset IC circuit disposed between the second switch and the discharge check terminal and configured to remove an unknown period taken for the first voltage to reach the second voltage, and
the reset IC circuit outputs the discharge-completed signal if a predetermined voltage or more is input, and outputs the discharge-uncompleted signal if a voltage less than the predetermined voltage is input.

12. The organic light emitting diode display apparatus according to claim 3, wherein the process recharges a voltage of the capacitor if the discharge-completed signal is detected, and determines that the discharge circuit malfunctions if the discharge-completed signal indicating that the discharge of the voltage of the capacitor has been completed is redetected, and does not perform the afterimage compensation.

13. The organic light emitting diode display apparatus according to claim 12, wherein the processor recharges the voltage of the capacitor, and performs the afterimage compensation if the discharge-uncompleted signal indicating that the discharge of the voltage of the capacitor has not been completed is detected.

14. The organic light emitting diode display apparatus according to claim 3, wherein the discharge control terminal is a general port input/output (GPIO) output terminal, and the discharge check terminal is a GPIO

input terminal.

15. The organic light emitting diode display apparatus according to claim 1, further comprising an afterimage compensation circuit configured to perform the afterimage compensation,
wherein the afterimage compensation circuit measures a reduced amount of a current flowing through a pixel constituting the display panel, and compensates for the reduced amount of the current for the pixel.

100

FIG. 1

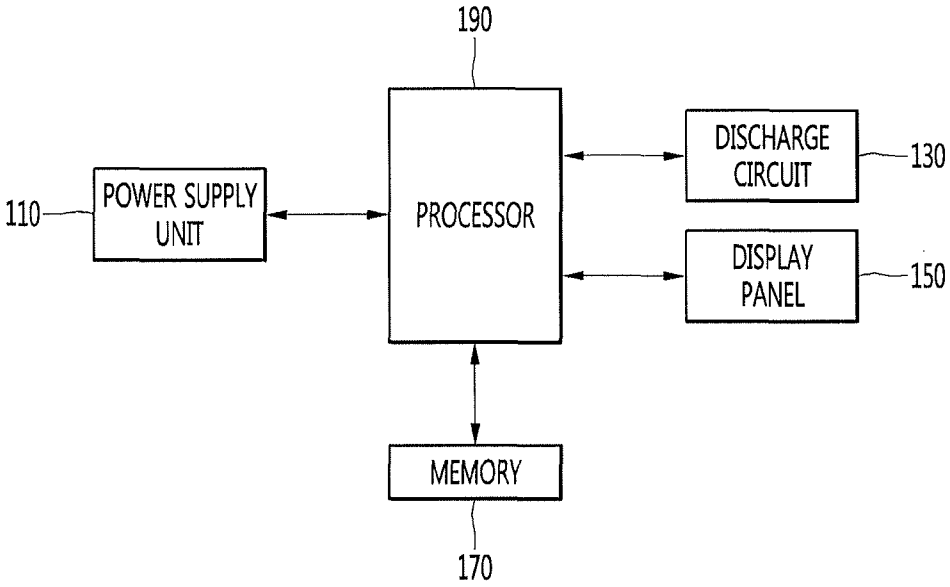


FIG. 2

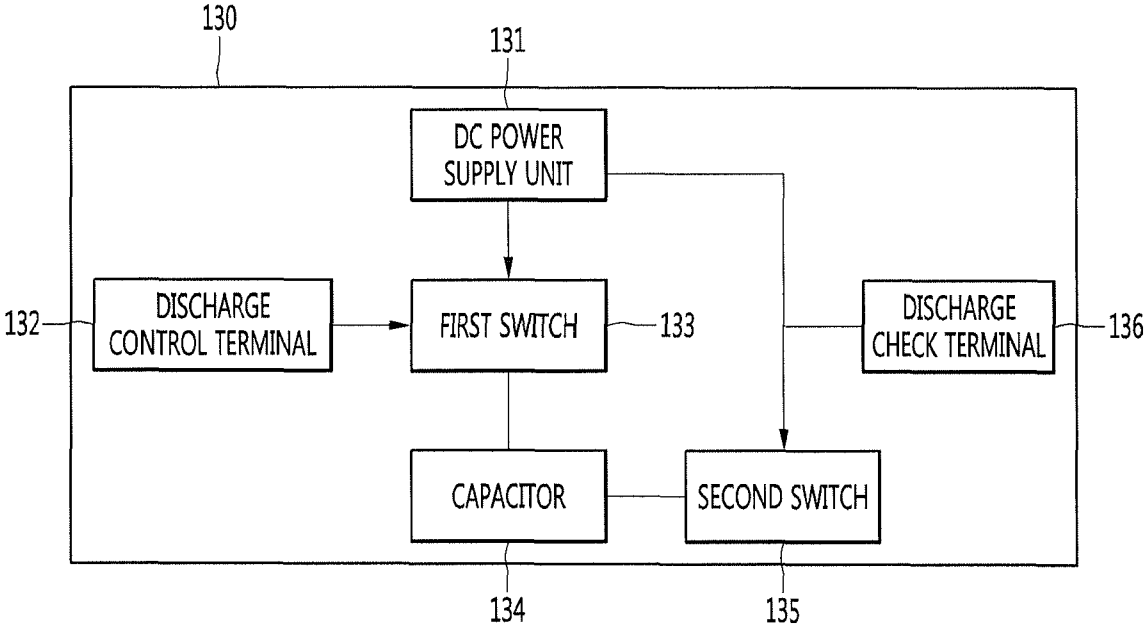


FIG. 3

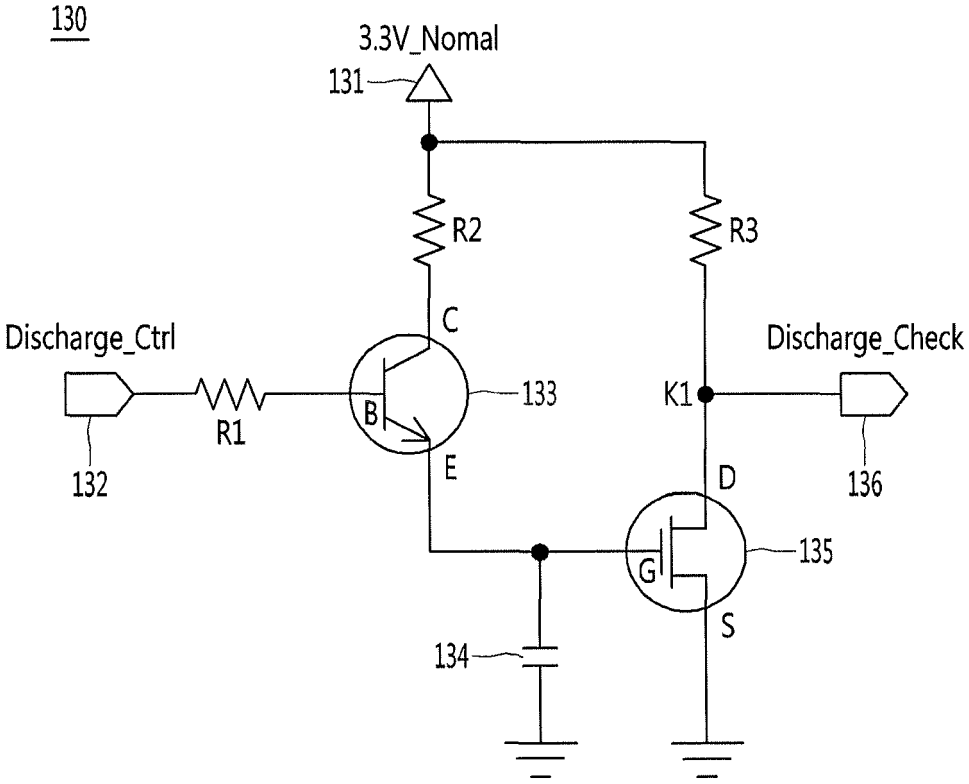

130
3.3V_Nomal
131
R2
R3
C
Discharge_Ctrl
Discharge_Check
133
K1
B
R1
132
E
D
136
135
G
S
134

FIG. 4

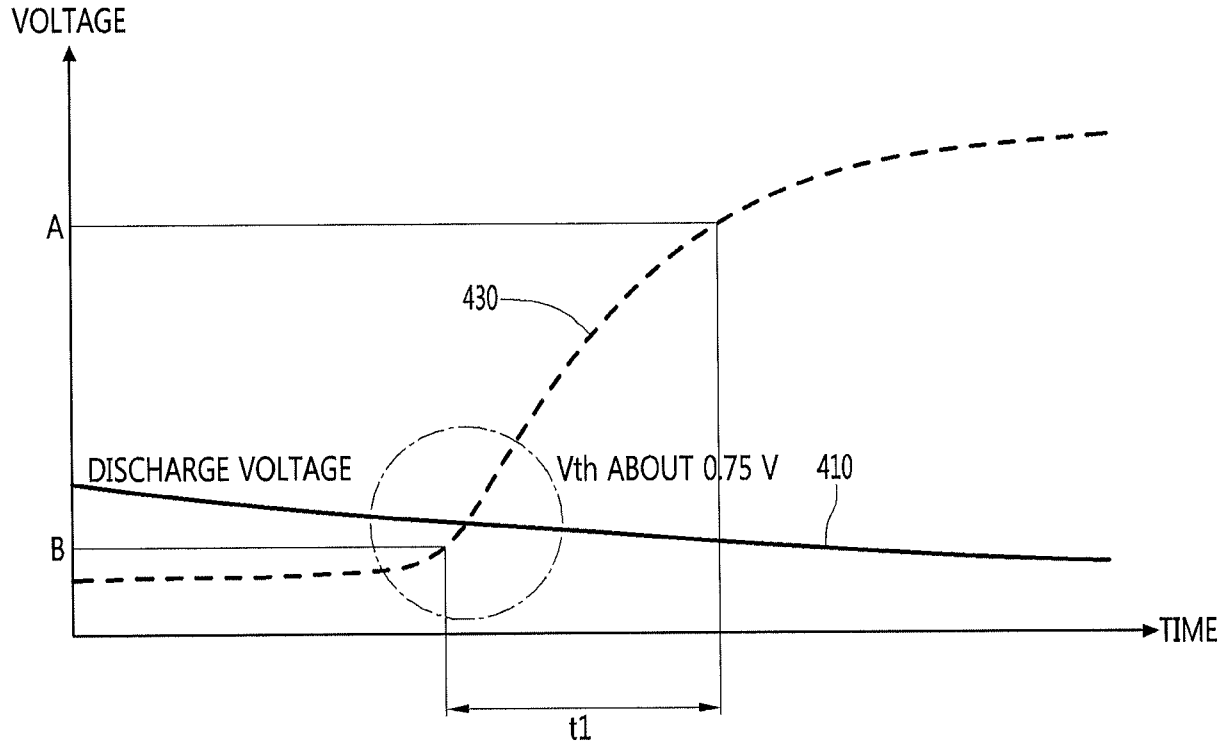


FIG. 5

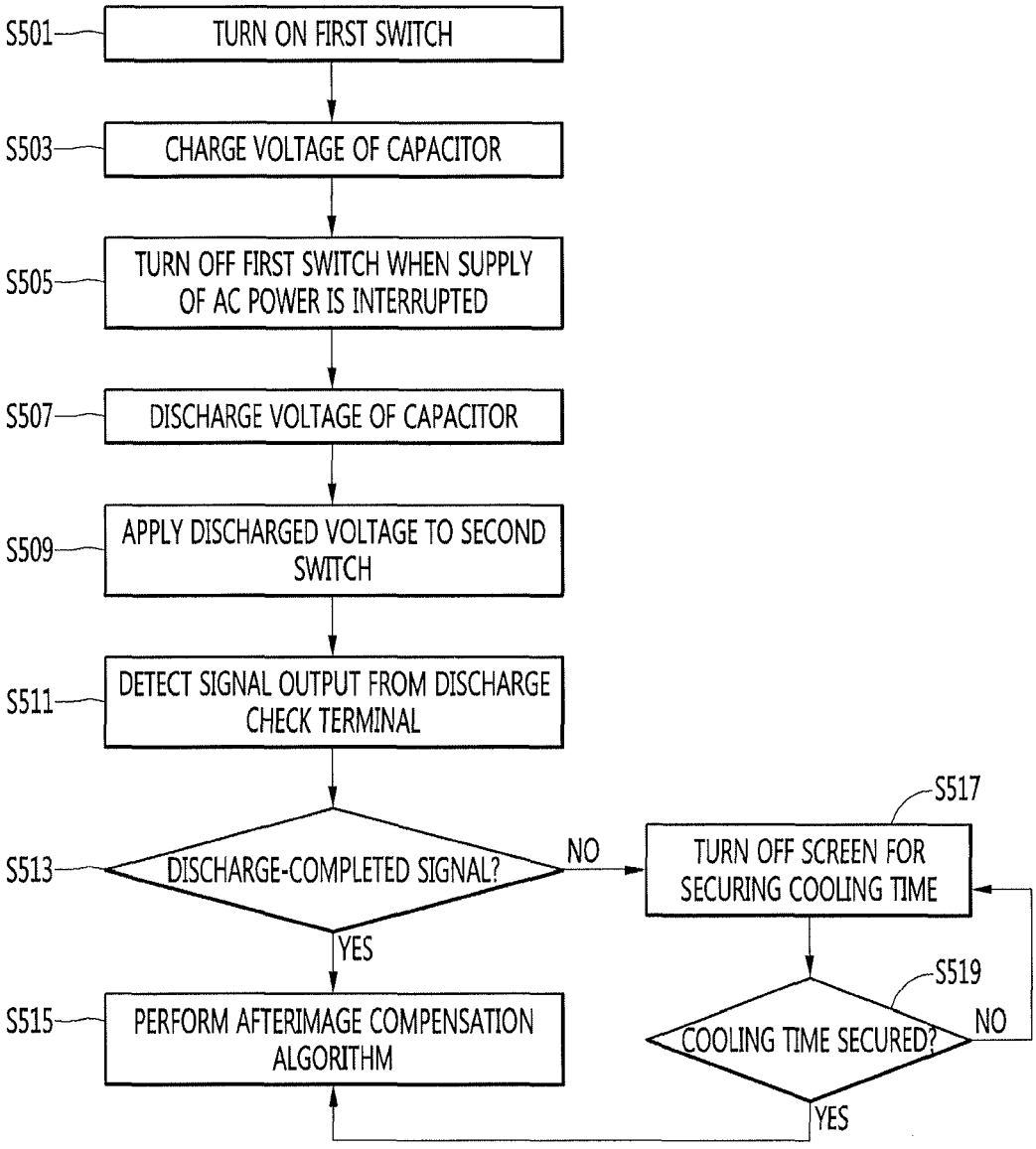

S501
TURN ON FIRST SWITCH
S503
CHARGE VOLTAGE OF CAPACITOR
S505
TURN OFF FIRST SWITCH WHEN SUPPLY OF AC POWER IS INTERRUPTED
S507
DISCHARGE VOLTAGE OF CAPACITOR
S509
APPLY DISCHARGED VOLTAGE TO SECOND SWITCH
S511
DETECT SIGNAL OUTPUT FROM DISCHARGE CHECK TERMINAL
S513
DISCHARGE-COMPLETED SIGNAL?
NO
YES
S515
PERFORM AFTERIMAGE COMPENSATION ALGORITHM
S517
TURN OFF SCREEN FOR SECURING COOLING TIME
S519
COOLING TIME SECURED?
NO
YES

FIG. 6

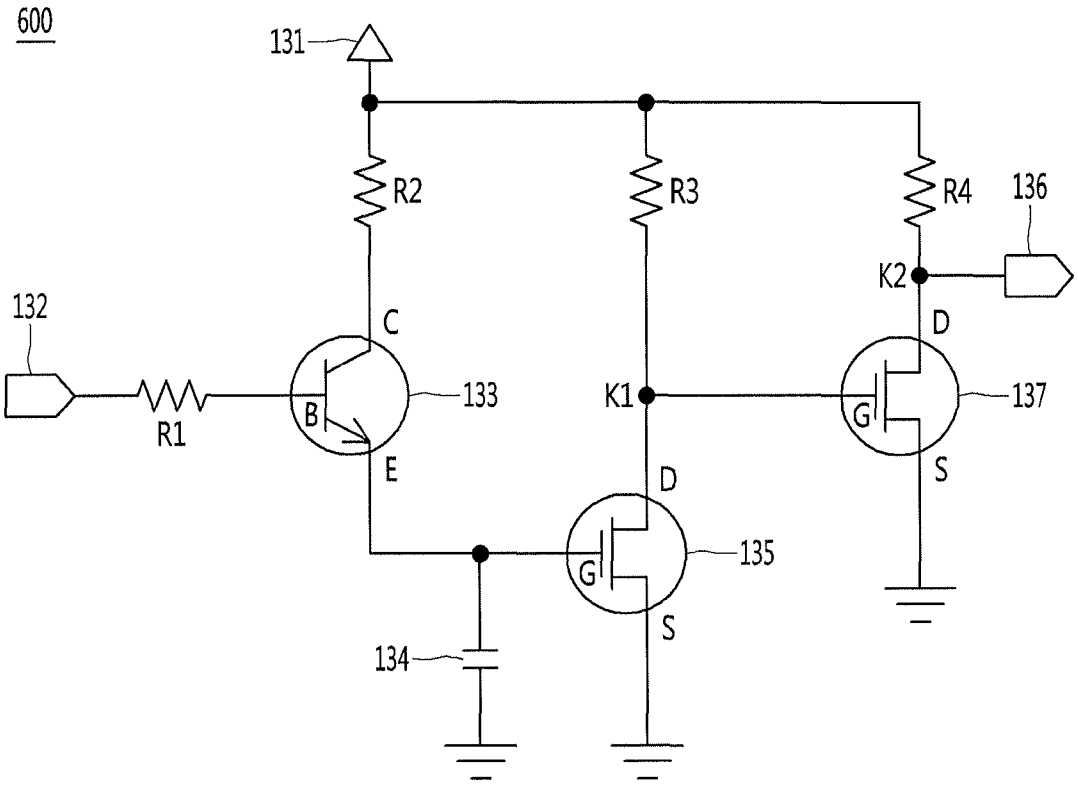


FIG. 7

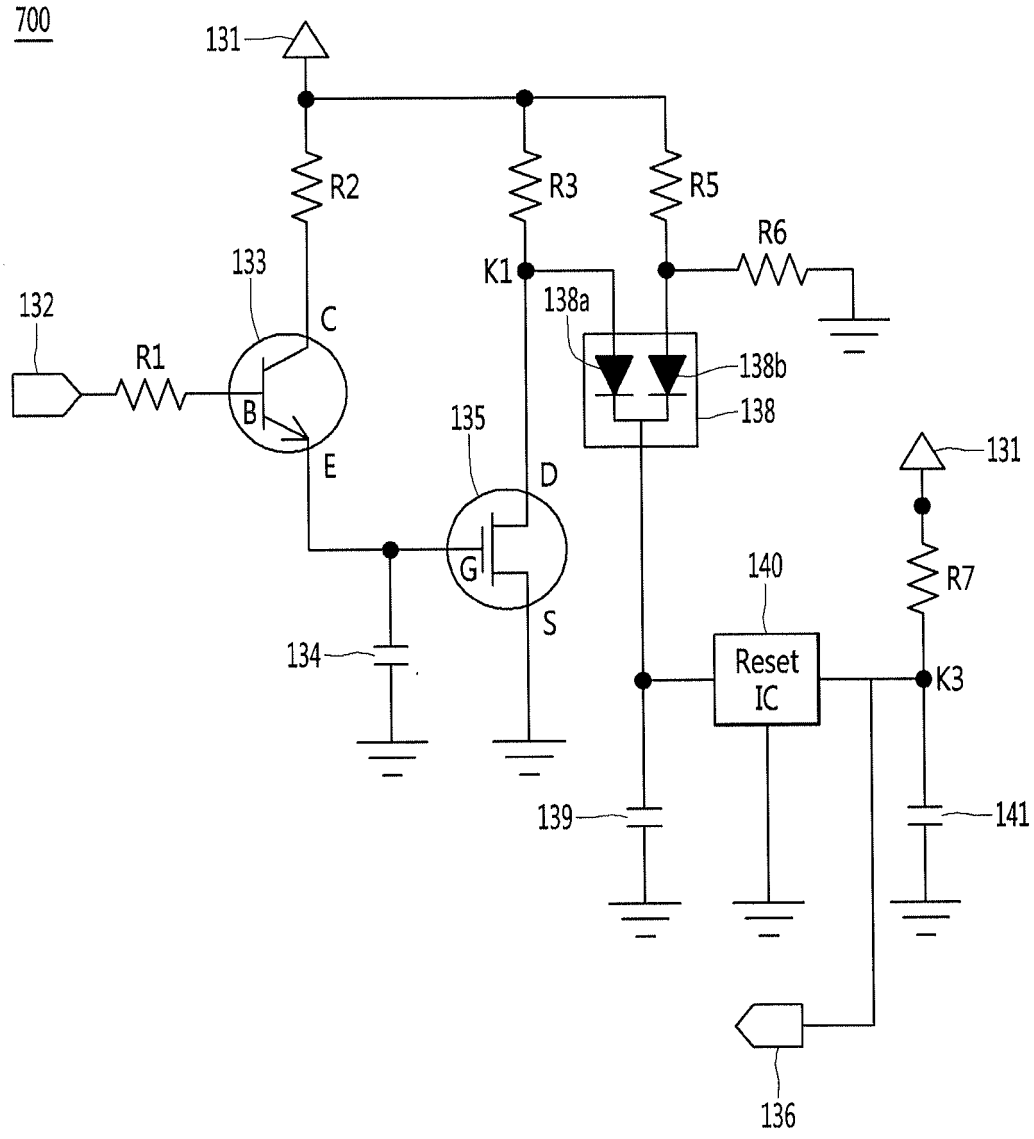

700
131
R2
R3
R5
R6
133
K1
132
C
138a
R1
138b
B
138
135
131
E
D
G
140
R7
S
134
Reset IC
K3
139
141
136

FIG. 8

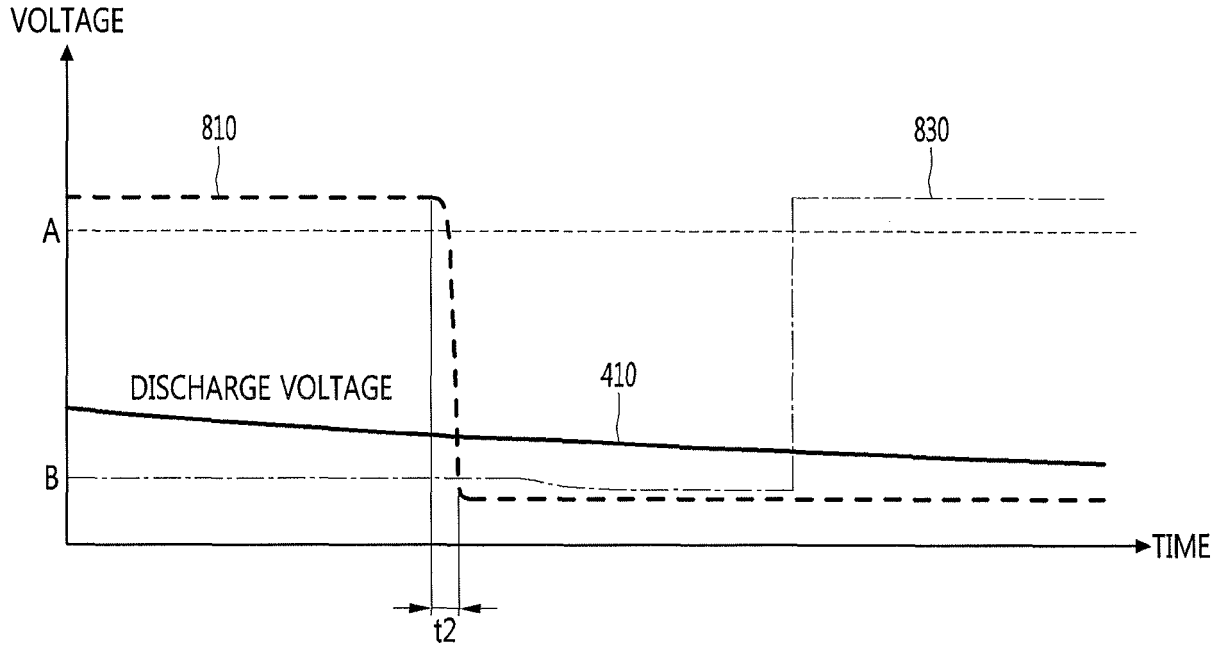


FIG. 9

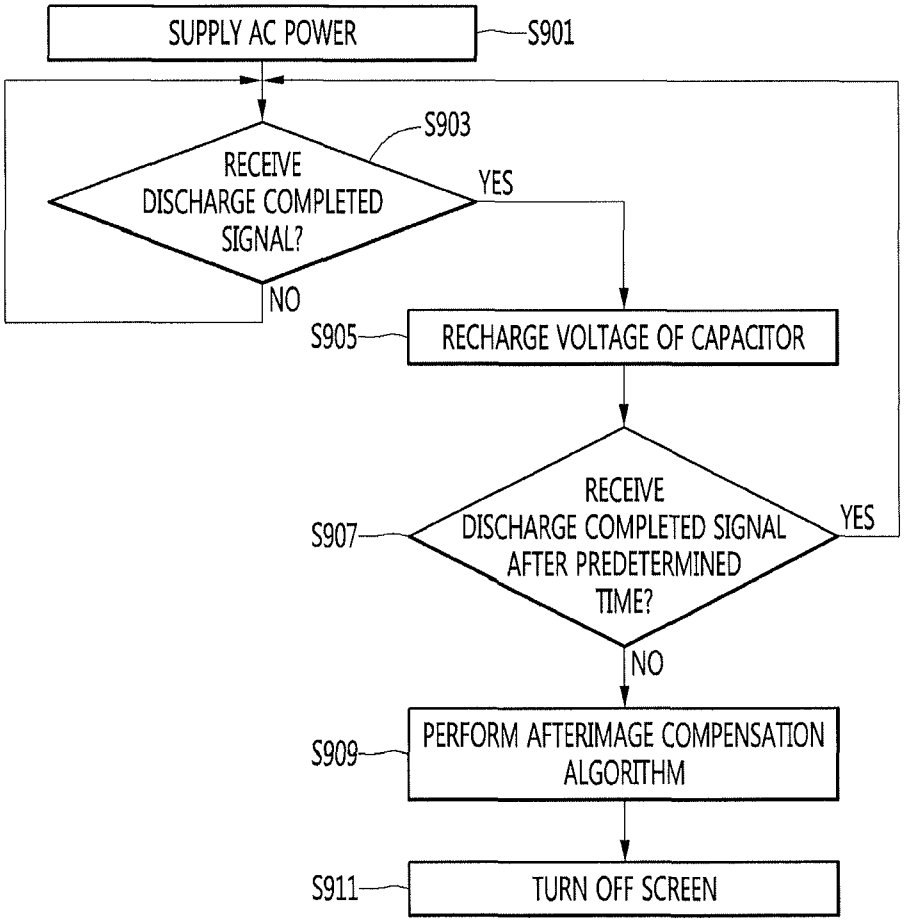

SUPPLY AC POWER
S901
S903
RECEIVE DISCHARGE COMPLETED SIGNAL?
YES
NO
S905
RECHARGE VOLTAGE OF CAPACITOR
S907
RECEIVE DISCHARGE COMPLETED SIGNAL AFTER PREDETERMINED TIME?
YES
NO
S909
PERFORM AFTERIMAGE COMPENSATION ALGORITHM
S911
TURN OFF SCREEN

FIG. 10

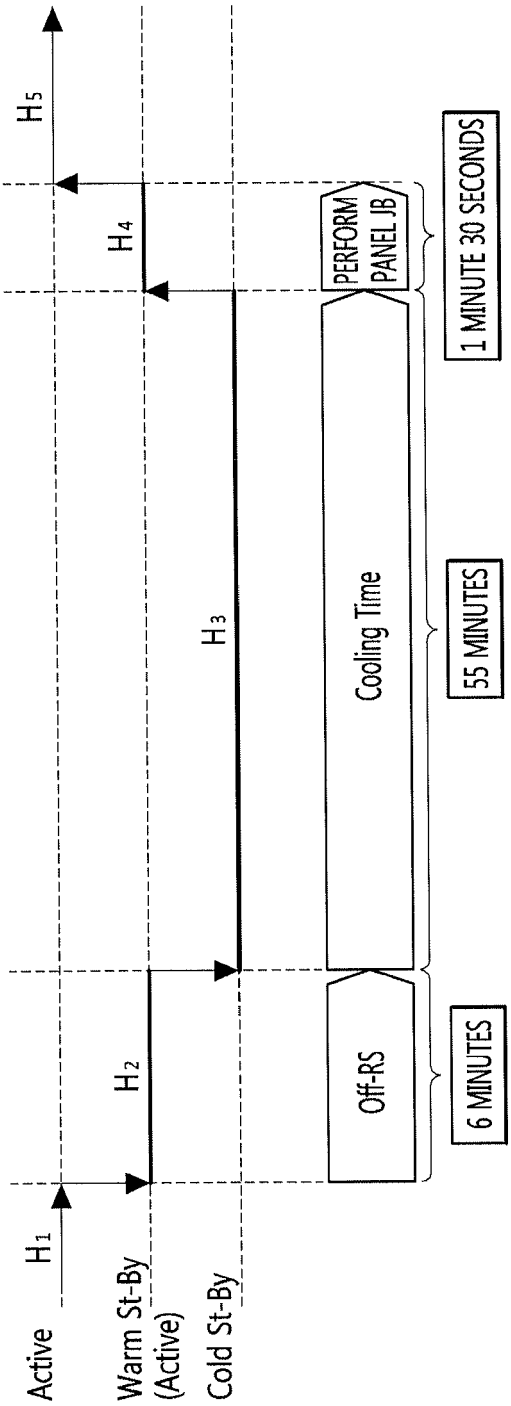

H5
H4
H3
H2
H1
Active
Warm St-By
(Active)
Cold St-By
PERFORM
PANEL JB
Cooling Time
Off-RS
1 MINUTE 30 SECONDS
55 MINUTES
6 MINUTES

FIG. 11A

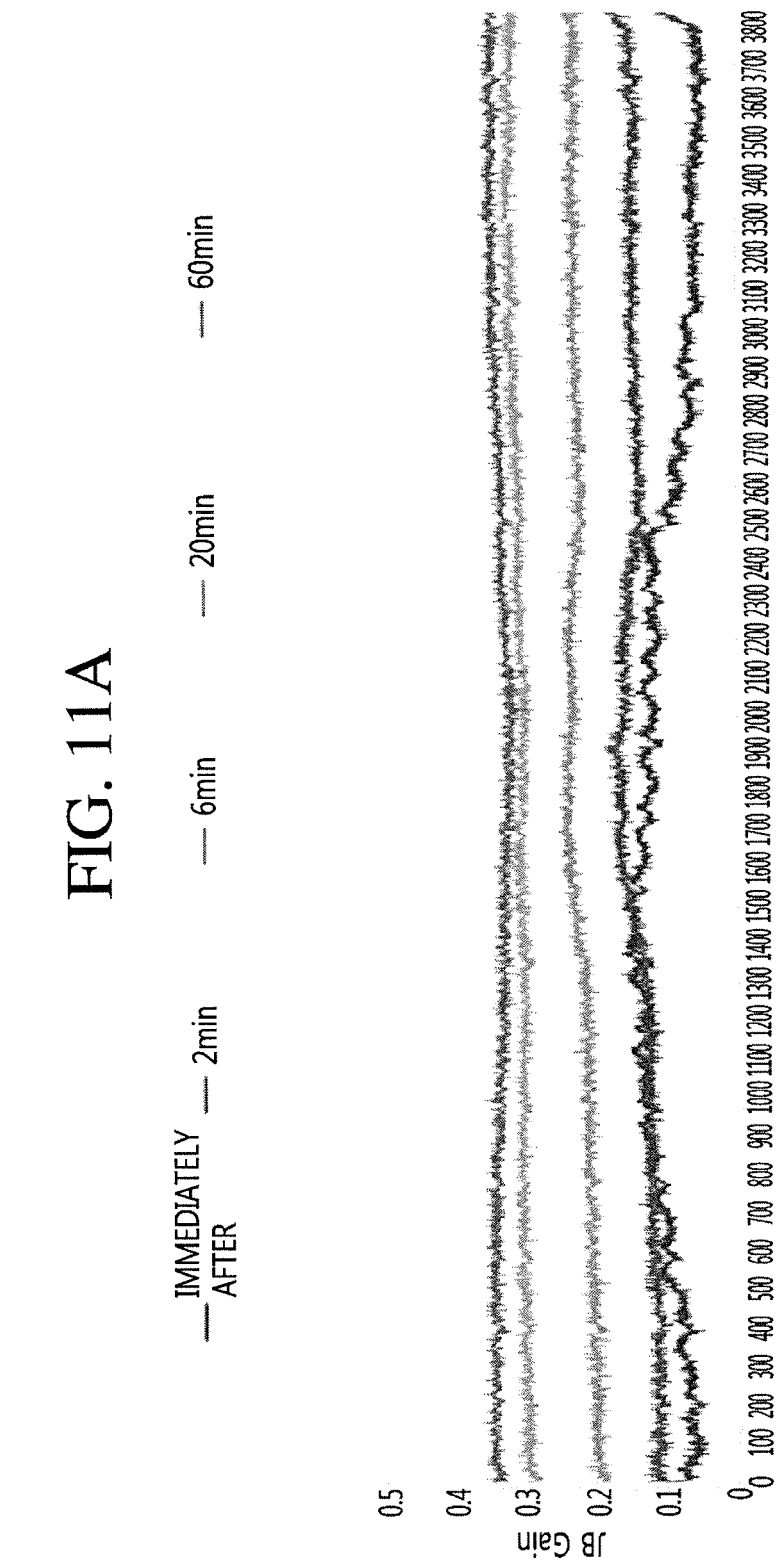

IMMEDIATELY AFTER
2min
6min
20min
60min
JB Gain
0.5
0.4
0.3
0.2
0.1
0
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100 2200 2300 2400 2500 2600 2700 2800 2900 3000 3100 3200 3300 3400 3500 3600 3700 3800
Ws pixel

FIG. 11B

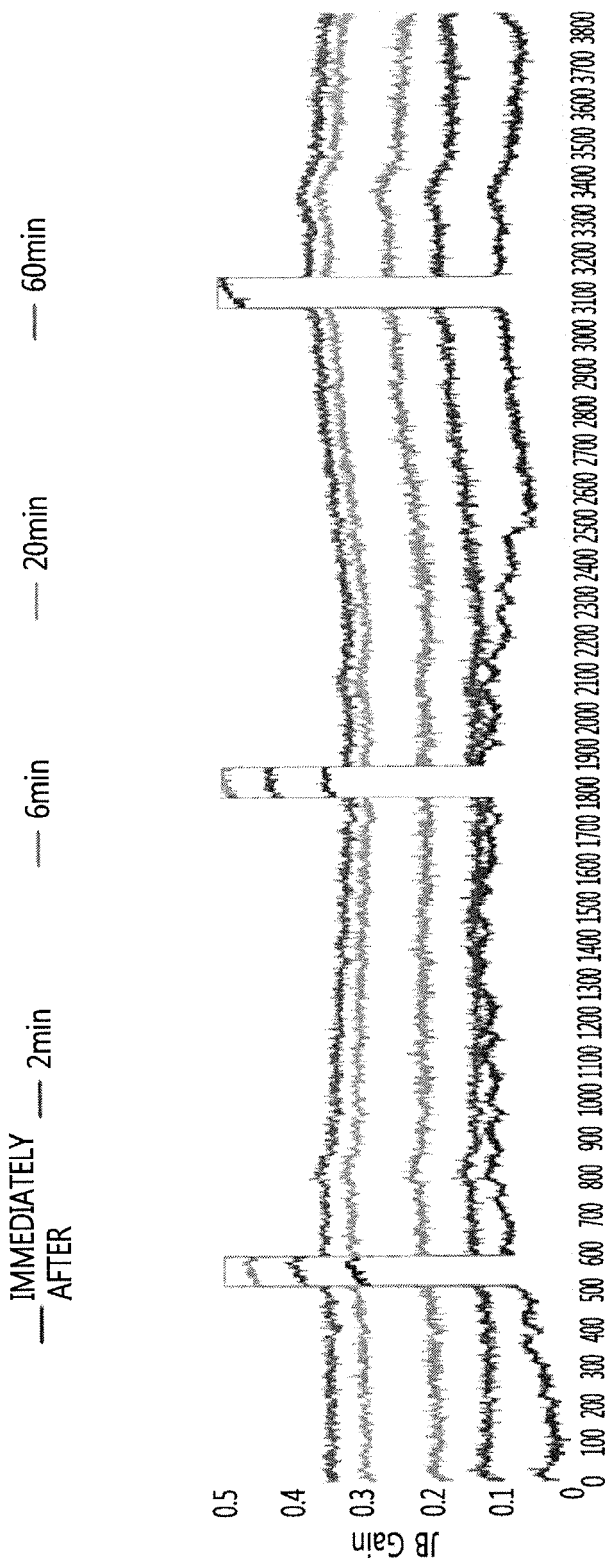

IMMEDIATELY
AFTER
2min
6min
20min
60min
JB Gain
0.5
0.4
0.3
0.2
0.1
0
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100 2200 2300 2400 2500 2600 2700 2800 2900 3000 3100 3200 3300 3400 3500 3600 3700 3800
Ws pixel

FIG. 11C

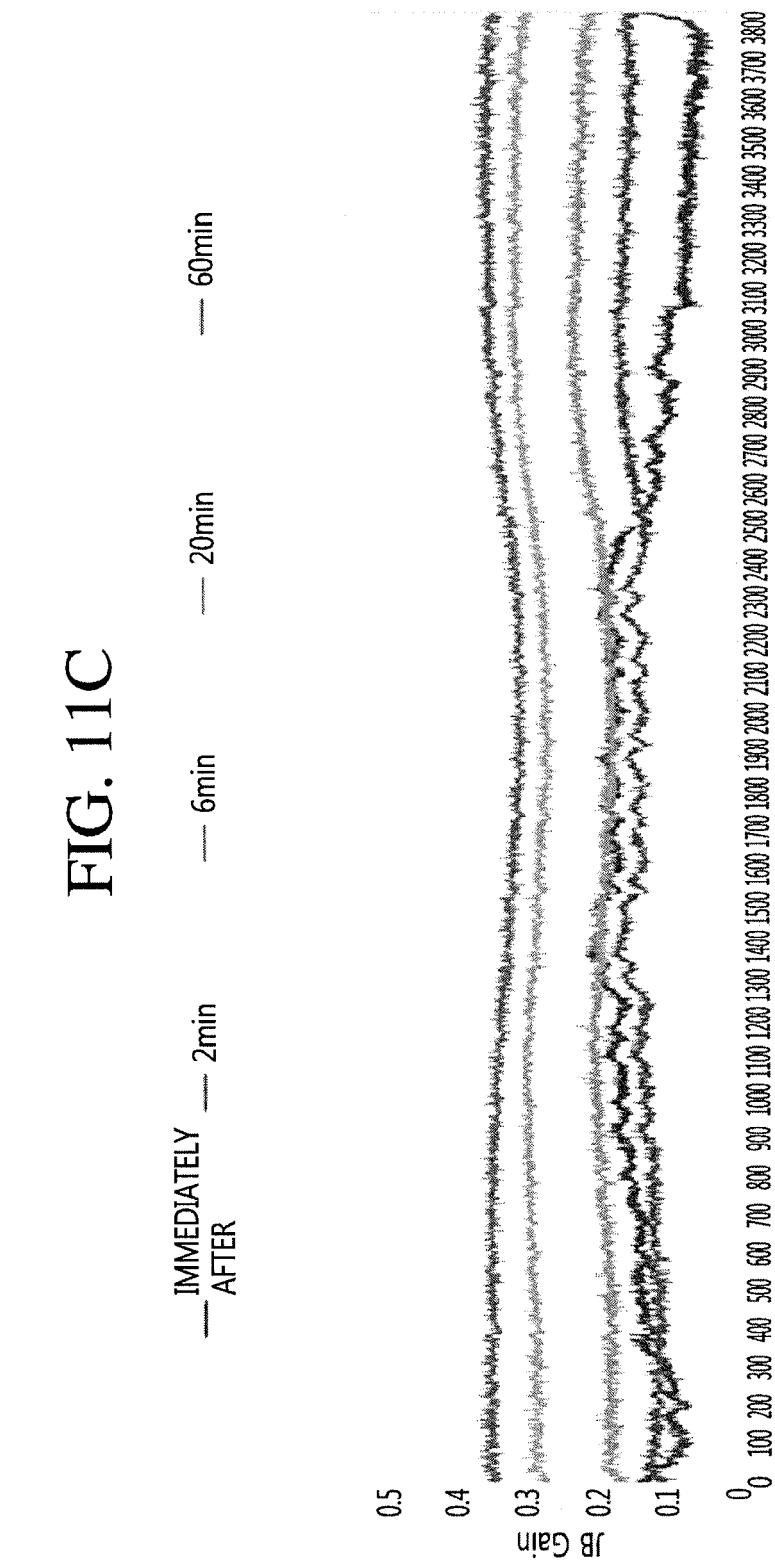

IMMEDIATELY AFTER
2min
6min
20min
60min
JB Gain
0.5
0.4
0.3
0.2
0.1
0
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100 2200 2300 2400 2500 2600 2700 2800 2900 3000 3100 3200 3300 3400 3500 3600 3700 3800
Ws pixel

FIG. 11D

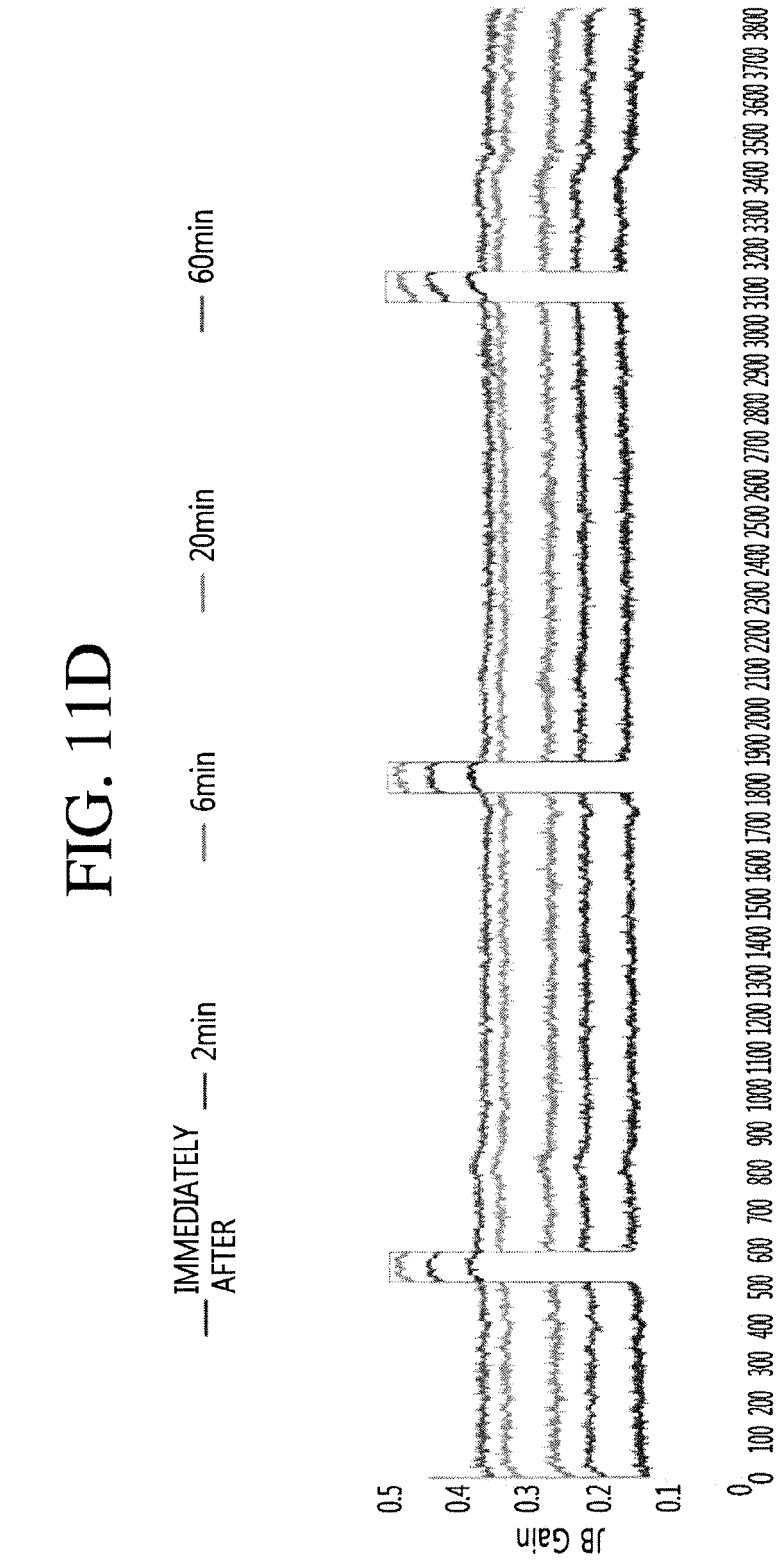

IMMEDIATELY AFTER
2min
6min
20min
60min
JB Gain
0.5
0.4
0.3
0.2
0.1
0
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100 2200 2300 2400 2500 2600 2700 2800 2900 3000 3100 3200 3300 3400 3500 3600 3700 3800
Ws pixel

FIG. 11E

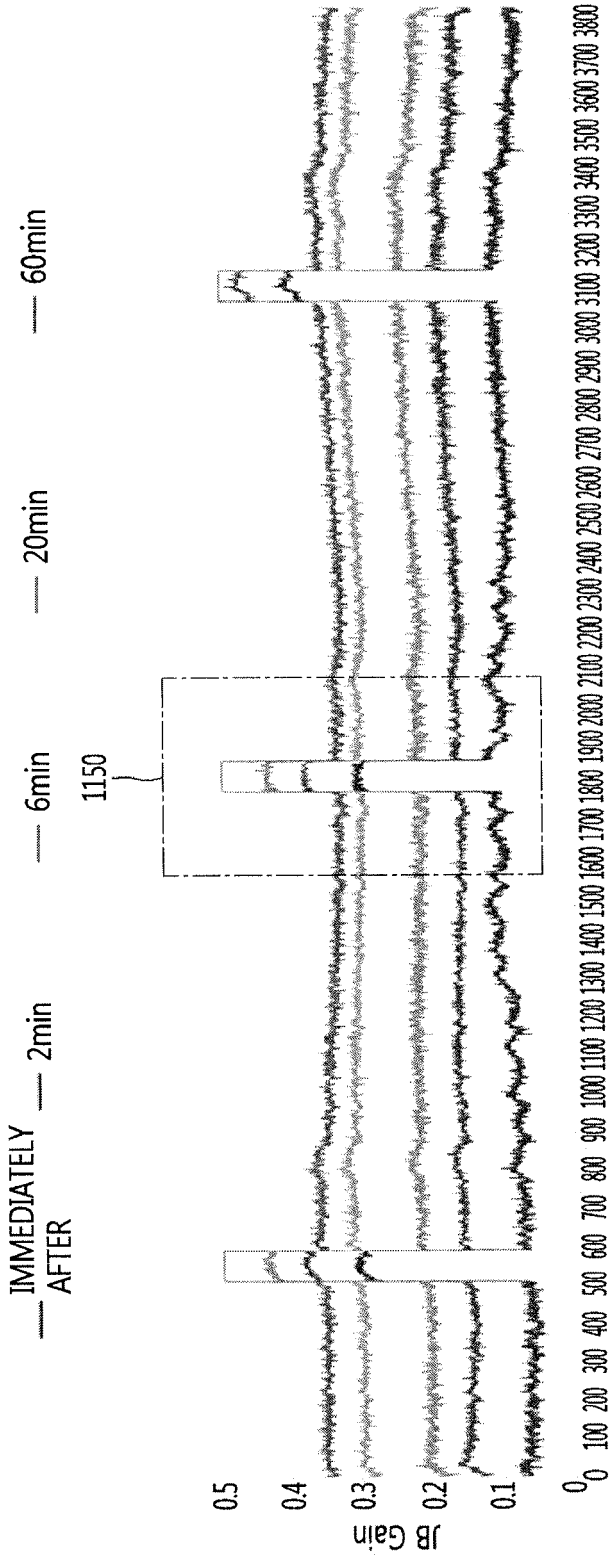

IMMEDIATELY AFTER
2min
6min
20min
60min
1150
JB Gain
0.5
0.4
0.3
0.2
0.1
0
0 100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100 2200 2300 2400 2500 2600 2700 2800 2900 3000 3100 3200 3300 3400 3500 3600 3700 3800
Ws pixel

FIG. 11F

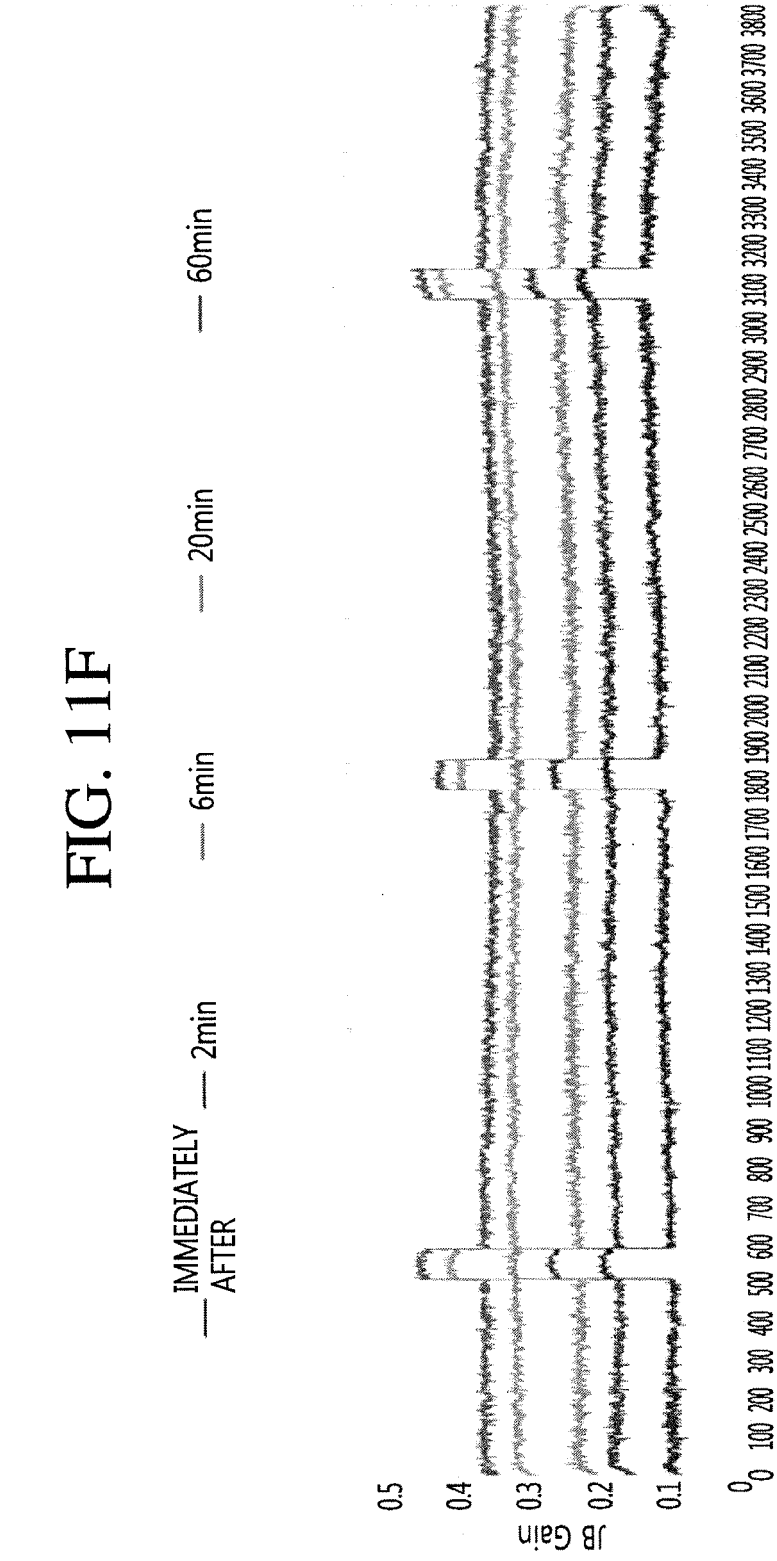
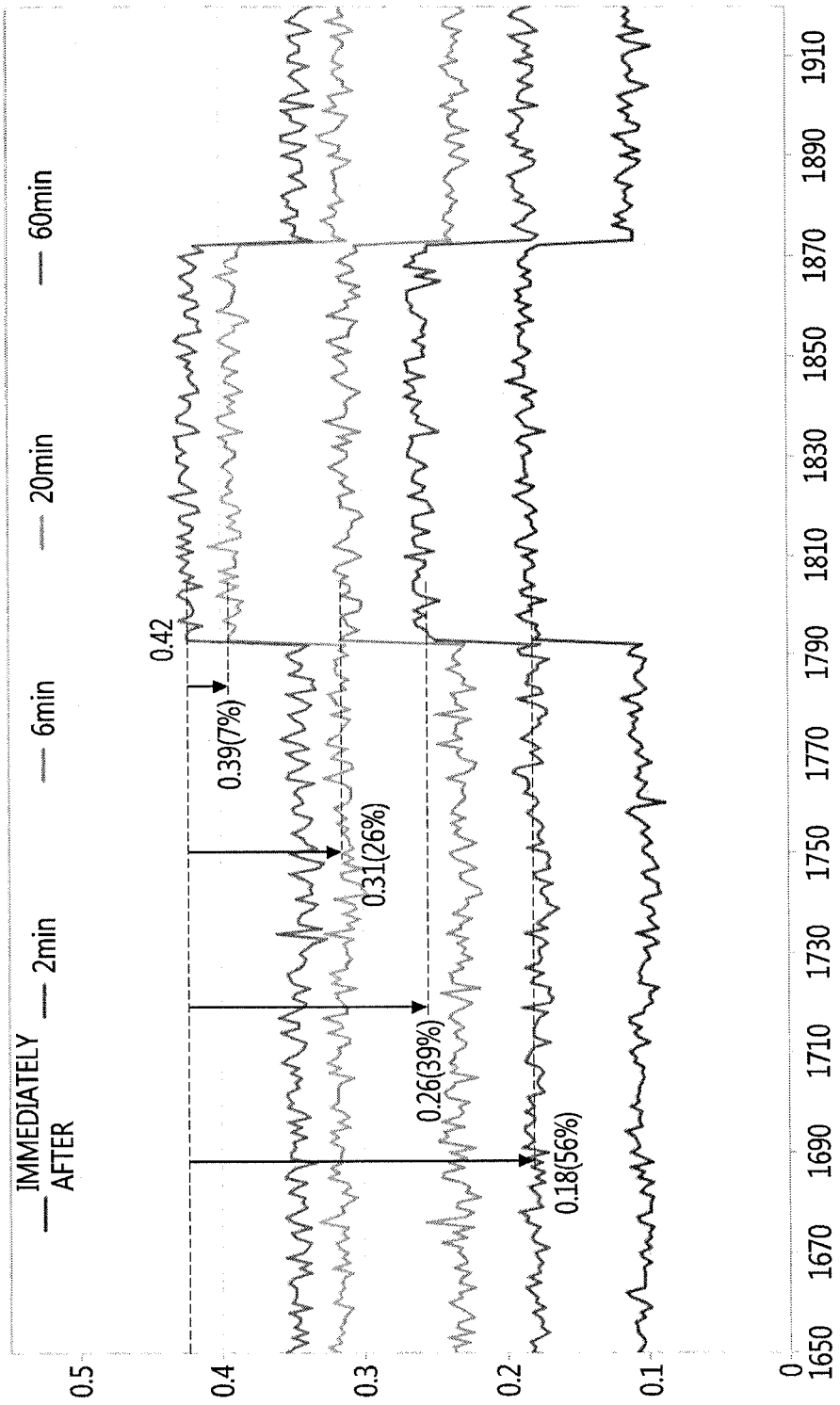

IMMEDIATELY AFTER
2min
6min
20min
60min
JB Gain
0.5
0.4
0.3
0.2
0.1
0
100 200 300 400 500 600 700 800 900 1000 1100 1200 1300 1400 1500 1600 1700 1800 1900 2000 2100 2200 2300 2400 2500 2600 2700 2800 2900 3000 3100 3200 3300 3400 3500 3600 3700 3800
Ws pixel

FIG. 12


IMMEDIATELY
AFTER
2min
6min
20min
60min
0.42
0.39(7%)
0.31(26%)
0.26(39%)
0.18(56%)
0.5
0.4
0.3
0.2
0.1
0
1650
1670
1690
1710
1730
1750
1770
1790
1810
1830
1850
1870
1890
1910

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EUROPEAN SEARCH REPORT

Application Number
EP 18 19 6456

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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Y	US 2008/218451 A1 (MIYAMOTO MITSUHIDE [JP] ET AL) 11 September 2008 (2008-09-11) * paragraph [0053] - paragraph [0062]; figures 3-5 * -----	15	
A	US 2014/092144 A1 (KIM JOONYOUNG [KR] ET AL) 3 April 2014 (2014-04-03) * abstract * * paragraphs [0022] - [0055]; figures 1-4 * -----	1-15	
			TECHNICAL FIELDS SEARCHED (IPC) G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	16 November 2018	Adarska, Veneta

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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16-11-2018

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REFERENCES CITED IN THE DESCRIPTION

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专利名称(译)	有机发光二极管显示装置		
公开(公告)号	EP3460786A1	公开(公告)日	2019-03-27
申请号	EP2018196456	申请日	2018-09-25
申请(专利权)人(译)	LG电子株式会社.		
当前申请(专利权)人(译)	LG电子株式会社.		
发明人	HWANGBO, HANSEOK		
IPC分类号	G09G3/3225		
优先权	62/562499 2017-09-25 US 1020170142738 2017-10-30 KR		
外部链接	Espacenet		

摘要(译)

一种有机发光二极管显示装置，包括：显示面板;放电电路，被配置为如果显示面板被驱动超过预定时间则放电电压并且中断对显示面板的供电，并且处理器被配置为：如果供电，则确定是否满足显示面板的余像补偿所需的冷却时间，如果满足冷却时间，则执行显示面板的余像补偿。

FIG. 1

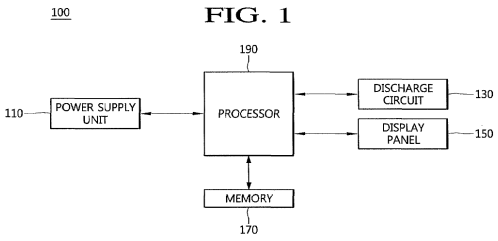

FIG. 2