

(19)



(11)

EP 3 174 042 B1

(12)

EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention
of the grant of the patent:
23.10.2019 Bulletin 2019/43

(51) Int Cl.:
G09G 3/32 (2016.01)

(21) Application number: **16187883.0**

(22) Date of filing: **08.09.2016**

(54) ORGANIC LIGHT EMITTING DIODE DISPLAY

ANZEIGE MIT ORGANISCHEN LICHTEMITTIERENDEN DIODEN

AFFICHAGE À DIODES ÉLECTROLUMINESCENTES ORGANIQUES

(84) Designated Contracting States:
**AL AT BE BG CH CY CZ DE DK EE ES FI FR GB
GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO
PL PT RO RS SE SI SK SM TR**

(30) Priority: **30.11.2015 KR 20150169237**

(43) Date of publication of application:
31.05.2017 Bulletin 2017/22

(73) Proprietor: **LG Display Co., Ltd.
Yeongdeungpo-gu
Seoul
150-721 (KR)**

(72) Inventors:
• **SHIN, Sangil**
Gyeonggi-do, 411-765 (KR)
• **SUK, Jungyoup**
Gyeonggi-do, 413-012 (KR)
• **SHIN, Byongwook**
Daegu, 706-903 (KR)

(74) Representative: **Carpmaels & Ransford LLP
One Southampton Row
London WC1B 5HA (GB)**

(56) References cited:
EP-A1- 2 889 864 EP-A1- 2 980 854
CN-A- 104 614 911 CN-A- 104 977 740
US-A1- 2010 141 630 US-A1- 2014 022 230

EP 3 174 042 B1

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Description

BACKGROUND

Field of the Invention

[0001] The present invention relates to a display device with a free form active area.

Discussion of the Related Art

[0002] With the development of information technology, the market for displays that play an intermediary role between users and information is growing. Thus, display devices such as organic light emitting displays (OLEDs), quantum dot displays (QDDs), liquid crystal displays (LCDs), and plasma display panels (PDPs) are increasingly used.

[0003] Moreover, flexible displays have become commercialized in recent years. The flexible displays come in a variety of designs, and offer benefits such as portability and durability. The flexible displays are applied to various fields including TV (television), automotive displays, and wearable devices, as well as mobile devices like smartphones and tablet PCs. There is a demand for flexible displays in a variety of free forms (unconventional shapes), rather than in traditional square shapes so that they can find applications in many fields.

[0004] Since such a free form display device has a different shape than those of the existing display devices, the arrangement of components of the display device varies. For example, a line arrangement structure required for the free form display device is different from those of the existing display devices. That is, there is a need for the development of a novel, efficient line arrangement structure that suits the characteristics of a free form display device and prevents a short-circuit fault, etc. between different signal lines to which different signals (or voltages) are applied.

[0005] US2014022230A1 relates to a display device including: a first auxiliary electrode coupled to a first power voltage supply line; a second auxiliary electrode coupled to a second power voltage supply line with a first link electrode; an active area, comprising: scan lines; data lines; first voltage lines; second voltage lines; and pixels; and a display drive circuit configured to supply data voltages to data links coupled to the data lines, wherein the first auxiliary electrode, the second auxiliary electrode, the first power voltage supply line, the second power voltage supply line, the data links, and the display drive circuit being in a bezel area corresponding to an area outside the active area, the second auxiliary electrode being between the first auxiliary electrode and the active area, the first auxiliary electrode being between the second auxiliary electrode and the display drive circuit.

[0006] EP2889864A1 relates to a display device that may minimize voltage drop of a power source supplied to a pixel. The display device comprises a power gener-

ator generating a driving power source; a display panel that includes a plurality of pixels and displays images by using the driving power source; and a printed circuit board having a power transfer line for transferring the driving power source output from the power generator to the display panel, wherein the power transfer line is provided in a closed-loop type.

SUMMARY

[0007] The present invention is defined by claim 1 with further details of specific embodiments provided in the dependent claims.

[0008] It is noted that, among all the presented embodiments, only those which fall under the scope of the appended claims are to be intended as embodiments of the invention, whereas the other embodiments shall be understood as examples useful to understand the invention but not forming part of the same.

[0009] Accordingly, the present invention is directed to a free form display device that prevents degradation in luminance uniformity and a short circuit between signals lines to which different signals are applied, by changing signal transmission paths to which a power supply voltage or scan pulses are applied.

[0010] A display device include, a substrate comprising a free form active area having pixels defined by scan lines, data lines, and power supply lines; a bezel area located outside the active area and having a power supply routing line to which a power supply voltage can be applied and a scan routing line to which scan pulses can be applied; and link lines that are disposed in the bezel area, that connect the power supply routing lines to the power supply lines and which are configured to transmit the power supply voltage from the power supply routing lines to the power supply lines, the link lines comprising: a plurality of first link lines; and one or more second link lines that interconnect the first link lines, each of the first link lines comprising one end connected to the power supply routing line and the other end connected to one of the power supply lines.

[0011] The display device may also comprise a plurality of first auxiliary link lines, each of the first auxiliary link lines comprising one end connected to the power supply routing line and the other end connected to one of the second link lines.

[0012] The display device may further comprises second auxiliary link lines, each of the second auxiliary link lines comprising one end that is connected to either one of the second link lines or one of the power supply lines, and the other end that is connected to either one of the second link lines or one of the power supply lines.

[0013] The display device may further comprises a gate drive circuit configured to supply scan pulse to the scan lines and select pixels from the display panel to write a data voltage.

[0014] The scan routing lines may be connected to the lead-in part of a gate drive circuit and the scan routing

lines may be formed on a different layer than the lead-in part of the gate drive circuit and the scan lines.

[0015] The scan routing line may be formed with at least one insulating layer in between the scan routing line and the lead-in part.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is a block diagram illustrating a display device according to the present invention;

FIG. 2 is a view showing a display panel according to the present invention;

FIG. 3 is a view schematically illustrating part of a pixel array;

FIGS. 4 and 5 are views illustrating various patterns of how a gate drive circuit and scan lines are connected, with GIP circuits arranged on either side of the display panel; and

FIG. 6 is a top plan view illustrating a display panel according to the present invention;

FIG. 7 is a top plan view illustrating the AR area of FIG. 6, in the display device according to a first exemplary embodiment of the present invention;

FIG. 8 is a cross-sectional view taken along line I-I' of FIG. 7;

FIG. 9 is a cross-sectional view taken along line II-II' of FIG. 7;

FIG. 10 is a top plan view illustrating the AR area of FIG. 6, in the display device according to a second exemplary embodiment of the present invention;

FIG. 11 is a cross-sectional view taken along line III-III' of FIG. 10;

FIG. 12 is a top plan view illustrating the AR area of FIG. 6, in the display device according to a third exemplary embodiment of the present invention

FIG. 13 is a cross-sectional view taken along line IV-IV' of FIG. 12; and

FIG. 14 is a cross-sectional view taken along line V-V' of FIG. 12.

DETAILED DESCRIPTION

[0017] Reference will now be made in detail to embodiments illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts. Detailed description of known arts will be omitted if it is determined that the arts are not needed to explain the working of the embodiments of the invention. In describing various embodiments, descriptions of the same or like parts will be given with respect to a particular

embodiment and may be omitted in other exemplary embodiments.

[0018] Although terms including ordinal numbers such as first and second may be used to describe various components, the components are not limited by the terms. The terms are used only to distinguish one component from other components.

[0019] When a component is described as being "linked" or "connected" to another component, a component may be directly linked or connected to another component, it should be understood, however, that another component may be present in the middle. Meanwhile, when a component is described as being "directly linked" or "directly connected" to another component, it should be understood that another component may not be present in the middle.

[0020] A display device according to the present invention may be implemented based on display devices such as liquid crystal displays (LCD), field emission displays (FED), plasma display panels (PDP), organic light emitting display (OLED), electrophoresis displays (EPD), etc. For convenience of explanation, the following description will be given with respect to a display device comprising organic light emitting diodes.

[0021] FIG. 1 is a block diagram illustrating a display device according to the present invention. FIG. 2 is a view showing a display panel according to the present invention. FIG. 3 is a view schematically illustrating part of a pixel array. FIGS. 4 and 5 are views illustrating various patterns of how a gate drive circuit and scan lines are connected, with GIP circuits arranged on either side of the display panel.

[0022] Referring to FIGS. 1 through 3, a display device according to the present invention comprises a display driver circuit and a display panel 110.

[0023] The display driver circuit comprises a gate drive circuit 120, a data drive circuit 140, and a timing controller 30, and writes a video data voltage of an input image in the pixels of the display panel 110. The data drive circuit 140 converts digital video data RGB input from the timing controller 30 to an analog gamma compensation voltage to generate a data voltage. The data voltage output from the data drive circuit 140 is supplied to data lines DL. The gate drive circuit 120 sequentially supplies a scan pulse synchronized with the data voltage to scan lines GL and selects pixels from the display panel 110 to write the data voltage.

[0024] The timing controller 30 receives timing signals, such as a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, a data enable signal DE, a main clock MCLK, etc., input from a host system 20, and synchronizes the timings of operation of the data drive circuit 140 and gate drive circuit 120. Data timing control signals for controlling the data drive circuit 140 include a source sampling clock SSC, a source output enable signal SOE, etc. Gate timing control signals for controlling the gate drive circuit 120 include a gate start pulse GSP, a gate shift clock GSC, a gate output enable

signal GOE, etc.

[0025] The host system 20 may be implemented as one among a television system, a set-top box, a navigation system, a DVD player, a Blu-ray player, a personal computer (PC), a home theater system, and a phone system. The host system 20 comprises a system-on-chip (SoC) with a scaler embedded in it, and converts the digital video data RGB of the input image into a data format suitable for display on the display panel 110. The host system 20 transmits the digital video data RGB and the timing signals Vsync, Hsync, DE, and MCLK to the timing controller 30.

[0026] A substrate SUB forming the appearance of the display panel 110 is not limited to particular shapes. That is, although the substrate SUB shown in the drawings will be described with respect to one that is roughly rectangular in shape, but is not limited thereto. The plane of the substrate SUB may vary in shape from polygons and circles to ovals. The following description will be made by taking a circular substrate SUB as an example.

[0027] The display panel 110 comprises an active area AA and a bezel area BZ. The active area AA has an odd shape, rather than traditional rectangular shapes. The plane of the active area AA may be identical to or different from the plane of the substrate SUB. For example, a circular active area AA may be defined on a display panel 10 having a square appearance. The following description will be made by taking a circular active area AA as an example.

[0028] The active area AA comprises data lines DL, scan lines GL crossing the data lines DL, and pixels 10 defined by a matrix of the data lines DL and scan lines GL. Data of an input image is displayed in the active area AA. The active area AA further comprises reference voltage lines (hereinafter, "REF lines") for supplying a reference voltage Vref to the pixels 10, and high voltage lines (hereinafter, "VDD lines") for supplying a high voltage to the pixels 10. The scan lines GL supply scan pulses to the pixels 10. The scan lines GL comprise first scan lines GL1 to which a first scan pulse SCAN1 is applied, and second scan lines GL2 to which a second scan pulse SCAN2 is applied. The data lines DL transmit a data voltage to the pixels 10.

[0029] Each pixel 10 comprises a red subpixel, green subpixel, and blue subpixel for color representation. Each pixel 10 may further comprise a white subpixel. The data lines DL, scan lines GL, REF lines, VDD lines, etc. are connected to each pixel 10.

[0030] Each pixel 10 comprises a driving thin film transistor (hereinafter, TFT) DT for controlling the amount of current flowing through the OLED, and a programming part SC for setting the gate-source voltage of the driving TFT DT. The programming part SC may comprise at least one switching TFT and at least one storage capacitor. The switching TFT turns on in response to a scan pulse from a scan line GL to thereby apply a data voltage from a data line DL to one electrode of the storage capacitor. The driving TFT DT adjusts the amount of light emitted

by the organic light emitting diode (hereinafter, OLED) by controlling the amount of current supplied to the OLED based on the amount of voltage stored in the storage capacitor. The amount of light emitted by the OLED is proportional to the current supplied from the driving TFT DT. Such a pixel is connected to a high voltage source and a low voltage source and takes high voltage VDD and low voltage VSS from a power generator (not shown). The TFTs of the pixel may be implemented as p-type or n-type. Also, a semiconductor layer for the TFTs of the pixel may comprise amorphous silicon, or polysilicon, or oxide. The OLED comprises an anode ANO, a cathode CAT, and an organic compound layer interposed between the anode ANO and the cathode CAT. The anode ANO is connected to the driving TFT DT.

[0031] The bezel area BZ is disposed outside the active area AA. The bezel area BZ may comprise a data routing part 111, a multiplexer 160, a high voltage routing part 112, a reference voltage routing part 113, a gate drive circuit GIC 120, and a low voltage routing part 114. These components may be spaced apart from one another by a certain distance, in order to prevent a short circuit, or discharge, between them. To improve the aesthetic appearance of the display device, the bezel area BZ may be made as small as possible by properly separating, or minimally but adequately separating to prevent discharge, the components from one another.

[0032] The data routing part 111 may extend from a pad part 180 to either side of the bezel area BZ, and may be defined by the shape of the active area AA. The data routing part 111 is provided with a plurality of data routing lines. The data routing lines are electrically connected to the data drive circuit 140, and supply a data voltage output from the data drive circuit 140 to the pixels 10. The data routing lines of the data routing part 111 are electrically connected to pads of the pad part 180, and correspond to output channels of the data drive circuit 140 on a one-to-one basis.

[0033] The data drive circuit 140 may be mounted on a flexible circuit substrate 140a and electrically connected to the pad part 180 through an anisotropic conductive film (ACF). The flexible circuit board 140a may bend toward the back of the display panel 110. In this instance, the data drive circuit 140 may be located on the back of the display panel 110.

[0034] The multiplexer (MUX) 160 is disposed between the active area AA and the data routing part 111. The multiplexer 160 takes a data voltage from the data routing lines of the data routing part 111 and distributes it to the data lines DL in the active area AA. One end of the multiplexer 160 is electrically connected to the data routing lines of the data routing part 111, and the other end is electrically connected to the data lines DL in the active area AA. The multiplexer 160 outputs a data signal output from one output terminal of the data drive circuit 140 to multiple data lines DL by time-division, in response to a MUX enable signal. Accordingly, the multiplexer 160 requires fewer output terminals for the data drive circuit

140 and fewer data routing lines to connect to the output terminals.

[0035] The data routing part 111 and the multiplexer 160 may be disposed adjacent to the active area AA. The data routing part 111 and the multiplexer 160 may be disposed on only one of the upper and lower hemispheres of the active area AA. The upper hemisphere of the active area AA refers to the area above a horizontal line that goes through the center of the active area AA. The lower hemisphere of the active area AA refers to the area below the horizontal line that goes through the center of the active area AA. The data routing part 111 and the multiplexer 160 may be disposed adjacent to the data drive circuit 140.

[0036] An AP (auto probe) switching circuit 115 may be further provided on one side of the bezel area BZ. The AP switching circuit 115 is electrically connected to the scan lines GL and data lines DL in the active area AA and operates to check for the lighting-up of the pixels 10.

[0037] The high voltage routing part 112 may extend from the pad part 180 to either side, that is both left and right hand sides, of the bezel area BZ, and be defined by the shape of the active area AA. The high voltage routing part 112 may be defined outside the data routing part 111. The high voltage routing part 112 is provided with a VDD routing line. The VDD routing line takes a high voltage VDD output from a power generator. The VDD routing line is electrically connected to the VDD lines in the active area AA. The high voltage VDD is transmitted to the VDD lines through the VDD routing line. The high voltage VDD is the voltage required to drive the driving TFT of a compensating pixel or drive the OLED.

[0038] The reference voltage routing part 113 may extend from the pad part 180 to either side, that is both left and right hand sides, of the bezel area BZ, and be defined by the shape of the active area AA. The reference voltage routing part 113 may be defined outside the data routing part 111. The reference voltage routing part 113 is provided with an REF routing line. The REF routing line takes a reference voltage Vref output from a power generator. The REF routing line is electrically connected to the REF lines in the active area AA. The reference voltage Vref is transmitted to the REF lines through the REF routing line. The reference voltage Vref is the voltage required to reset the electric potential at the TFTs and OLED when the compensating pixel is driven. The reference voltage Vref may be an initial voltage VINI.

[0039] As illustrated in the drawing, either the high voltage routing part 112 or the reference voltage routing part 113 may extend from the pad part 180 and be located on the upper hemisphere, and the other one of the high voltage routing part 112 or the reference voltage routing part 113 may extend from the pad part 180 and be located on the upper and lower hemispheres. However, the present invention is not limited to this, and both the high voltage routing part 112 and the reference voltage routing part 113 may extend from the pad part 180 and may be located on the upper and lower hemispheres. In another

example, if upper and lower pad parts connected to a power generator are provided, either the high voltage routing part 112 or the reference voltage routing part 113 may extend from the upper pad part and be located on the upper hemisphere, and the other one may extend from the lower pad part and be located on the lower hemisphere. The VDD routing line and REF routing line respectively disposed in the high voltage routing part 112 and reference voltage routing part 113 may be formed in such a way as to have an area large enough to keep the voltage level stable.

[0040] If the active area AA is free form, the data lines DL in the active area AA are different lengths depending on their positions. A free form shape may be a shape that is not a square. In particular, a free form shape may be a shape that is not a rectangle. A free form shape may be a circle. For a free form active area, the length of the data lines DL disposed at the center of the active area AA may be different from that of the data lines DL disposed on the outer part of the active area AA. Since the data lines DL in the active area AA are different lengths depending on their positions, the number of pixels connected to each data line DL also differs. The differences in length between the data lines DL may create variations on capacitors. This may bring about problems like non-uniform luminance, thereby degrading the display quality of the display device.

[0041] To prevent this, the bezel area BZ may have a compensating capacitor 116. As illustrated in the drawing, the compensating capacitor 116 may be formed in the reference voltage routing part 113. However, the present invention is not limited thereto, and the compensating capacitor 116 may be formed by the overlapping of first and second capacitor electrodes, with at least one insulating layer in between. The first capacitor electrode is electrically connected to the data lines DL in the active area AA. If the compensating capacitor 116 is formed in the reference voltage routing part 113, the second capacitor electrode may be a REF routing line.

[0042] The compensating capacitor 116 may be a dual capacitor that runs vertically. A first capacitor may be formed in the upper part of the compensating capacitor 116 by the overlapping of the first and second capacitor electrodes, and a second capacitor may be formed in the lower part of the compensating capacitor 116 by the overlapping of the first capacitor electrode and a third capacitor electrode. The third capacitor electrode may be an electrode to which scan pulses supplied from the gate drive circuit 120 adjacent to it are applied.

[0043] A plurality of compensating capacitors 116 may be provided if necessary. At least one of the compensating capacitors 116 may have a different capacitance value from another one. That is, the compensating capacitors 116 may have a proper capacitance value that can compensate for variations depending on the length of the corresponding data line DL.

[0044] The gate drive circuit 120 comprises a shift register. The shift register comprises stages connected in

cascade. The stages output scan pulses SCAN1 and SCAN2 in response to a start pulse GSP, and shift the output of the scan pulses SCAN1 and SCAN2 in response to shift clocks GCLK1 to GCLK4. The gate drive circuit 120 may be disposed directly in the bezel area BZ of the display panel 110 depending on the type of a GIP (gate-driver in panel) circuit.

[0045] The gate drive circuit 120 may be disposed in the bezel area BZ along the shape of the active area AA, spaced a certain distance apart from the active area AA. The gate drive circuit 120 supplies scan pulses through scan routing lines to corresponding scan lines GL. The gate drive circuit 120 may be disposed on either side of the bezel area BZ, with the active area AA at the center. However, the present invention is not limited to this, and the gate drive circuit 12 may be disposed on one side of the bezel area BZ. The gate drive circuit 120 may divide the scan lines GL into a predetermined number of groups, and supply scan pulses for each group.

[0046] For example, referring further to FIG. 4, the gate drive circuit 120 may comprise a first GIP circuit GIP(L) disposed on one side of the display panel 110, and a second GIP circuit GIP(R) disposed on the other side of the display panel 110.

[0047] The first and second GIP circuits GIP(L) and GIP(R) may be connected to all scan lines GL1 to GLn. The first and second GIP circuits GIP(L) and GIP(R) receive a start pulse GSP and, at the same time, output scan pulses. Accordingly, the scan pulses output from the first and second GIP circuits GIP(L) and GIP(R) are simultaneously applied to both ends of the same scan line GL, respectively.

[0048] In another example, referring further to FIG. 5, the first GIP circuit GIP(L) is connected to a first group of scan lines GL and sequentially supplies a scan pulse to the first group of scan lines GL. The second GIP circuit GIP(R) is connected to a second group of scan lines GL and sequentially supplies a scan pulse to the second group of scan lines GL. The first group of scan lines GL may comprise odd-numbered scan lines GL1, GL3, ..., GL2n-1. The second group of scan lines GL may comprise even-numbered scan lines GL2, GL4, ..., GL2n. A start pulse GSP may be supplied to the first and second GIP circuits GIP(L) and GIP(R) at different time slots. Accordingly, the first and second GIP circuits GIP(L) and GIP(R) may output a scan pulse or carry signal at different timings. For example, a first scan pulse from the first GIP circuit 120 GIP(L) may be supplied to the first scan lines GL1 first, and then after approximately 1 horizontal period, a second scan pulse from the second GIP circuit GIP(R) may be supplied to the second scan lines GL2.

[0049] The low voltage routing part 114 may extend from the pad part 180, and be defined by the shape of the active area AA. The low voltage routing part 114 may take a low voltage VSS from a power generator and supply it to the pixels 10.

[0050] If the active area AA is free form, the power supply lines (REF lines and VDD lines) in the active area

AA are different lengths depending on their positions. That is, the length of the power supply lines (REF lines and VDD lines) disposed at the center of the active area AA may be different from that of the power supply lines (REF lines and VDD lines) disposed on the outer part of the active area AA. Since the power supply lines (REF lines and VDD lines) in the active area AA are different lengths depending on their positions, the number of pixels connected to each power supply line (REF lines and VDD lines) also differs. Accordingly, there may be load variations between the power supply lines (REF lines and VDD lines). This may bring about problems like non-uniform luminance, thereby degrading the display quality and product reliability of the display device.

[0051] Exemplary embodiments of the present invention, which are devised to reduce load variations caused by differences in length between power supply lines, will be described below with reference to the accompanying drawings. For ease of explanation, a signal transmission path for applying the reference voltage Vref, among the power supply voltages VDD and Vref, will be described by way of example. It should be noted that the present invention is not limited to such an example.

<First Exemplary Embodiment>

[0052] A display device according to a first exemplary embodiment of the present invention will be described below with reference to FIGS. 6 through 9. FIG. 6 is a top plan view illustrating a display panel according to the present invention. FIG. 7 is a top plan view illustrating the AR area of FIG. 6, in the display device according to the first exemplary embodiment of the present invention. FIG. 8 is a cross-sectional view taken along line I-I' of FIG. 7. FIG. 9 is a cross-sectional view taken along line II-II' of FIG. 7.

[0053] Referring to FIGS. 6 and 7, the display panel according to the present invention comprises a substrate SUB and link lines LNL1 and LNL2. The substrate SUB comprises a free form active area AA and a bezel area BZ located outside the active area AA. Pixels 10 defined by scan lines GL, data lines DL, and REF lines RFL are arranged in the free form active area AA. A gate drive circuit 120, a reference voltage routing part 113, and a link area LN are located in the bezel area BZ.

[0054] The gate drive circuit 120 may be formed on the substrate SUB of the display panel by GIP technology. The gate drive circuit 120 generates scan pulses. The gate drive circuit 120 supplies scan pulses SCAN1 and SCAN2 to the scan lines GL in the active area AA under control of a timing controller 30. The gate drive circuit 120 and the scan lines GL are electrically connected through scan routing lines GRL provided in between them. The scan pulses from the gate drive circuit 120 are supplied to the scan lines GL through the scan routing lines GRL.

[0055] The reference voltage routing part 113 is provided with an REF routing line RFR. The REF routing line

RFR receives a reference voltage V_{ref} from a power generator. A plurality of driving elements and a plurality of electrodes to which different signals (or voltages) are applied are disposed in a space (hereinafter, "link area") LN between the reference voltage routing part 113 and the active area AA, with insulating layers of organic and/or inorganic insulating materials interposed between the driving elements and the electrodes. For example, AP switching circuit elements 115, the link lines LNL1 and LNL2, and the scan routing lines GRL may be disposed in the link area LN. The link lines LNL1 and LNL2 and the scan routing lines GRL run across the link area LN.

[0056] The link lines LNL1 and LNL2 are disposed in the bezel area BZ, and connect the REF routing line RFR to the REF lines RFL to transmit the reference voltage V_{ref} from the REF routing line RFR to the REF lines RFL. That is, the reference voltage V_{ref} is supplied to the REF lines RFL in the active area AA through a signal transmission path connecting to the REF routing line RFR and the link lines LNL1 and LNL2.

[0057] The link lines LNL1 and LNL2 comprise first link lines LNL1 and second link lines LNL2. The first link lines LNL1 extend from the reference voltage routing part 113 through the link area LN and are electrically connected to the REF lines RFL. To this end, one end of the first link lines LNL1 is connected to the REF routing line RFR of the reference voltage routing part 113, and the other end of the first link lines LNL1 is connected to the REF lines RFL in the active area AA.

[0058] The second link lines LNL2 electrically connect n first link lines LNL1 (n is an integer greater than or equal to 2). One end and the other end of the second link lines LNL2 are connected to different first link lines LNL1, respectively. The second link lines LNL2 may serve as a bridge that connects the first link lines LNL1. The second link lines LNL2 may be disposed adjacent to the active area AA. The second link lines LNL2 may compensate for load variations caused by differences in length between the REF lines RFL in the active area AA. Accordingly, the first exemplary embodiment of the present invention may provide a display device that prevents degradation in luminance uniformity.

[0059] The bezel area BZ may have a large number of second link lines LNL2 to interconnect multiple first link lines LNL1. The term interconnect may be taken to mean the joining of two components in such a way that electrical contact is formed between the two components. The larger the number of second lines LNL2, the easier for the REF lines RFL to be equipotential. The reference voltage can be supplied uniformly to the REF lines RFL by having a sufficient number of second link lines LNL2.

[0060] In order for the REF lines RFL to be equipotential, the display device may further comprise first auxiliary link lines LNA1. Unlike the first link lines LNL1 connecting the REF routing line RFR and the REF lines RFL, the first auxiliary link lines LNA1 connect the REF routing line RFR and the second link lines LNL2. A large number of

first auxiliary link lines LNA1 may be provided in the bezel area BZ. The larger the number of first auxiliary link lines LNA1, the easier for the REF lines RFL to be equipotential. The reference voltage can be supplied uniformly to the REF lines RFL by having a sufficient number of first auxiliary link lines LNA1.

[0061] Reference numeral 118 of FIG. 6 schematically illustrates an example in which link lines to which the reference voltage V_{ref} is applied are interconnected in an area adjacent to the active area AA. Link lines to which the high voltage VDD is applied may be connected, as indicated by reference numeral 117 of FIG. 6. However, the present invention is not limited to this example.

[0062] Reference numerals M1, M2, M3, and M4 put in brackets in the drawing denote first, second, third, and fourth conductive layers, respectively, to which different signals (or voltages) are applied, and which serve as transmission paths for these signals. The reference numerals in brackets are used to distinguish the layers where each signal line is formed, and the same reference numeral in brackets denotes signal lines on the same layer. It should be noted that the same reference numeral in brackets does not necessarily mean that the same signal is applied to the signal lines.

[0063] Referring further to FIGS. 7 and 8, connections among the REF routing line RFR, link lines LNL1 and LNL2, and REF lines RFL will be described using a stack structure.

[0064] Referring further to FIGS. 7 and 8, numerous insulating layers are disposed on the substrate SUB. For example, a buffer layer BUF, a gate insulating layer GI, a first insulating layer IN1, and a second insulating layer IN2 may be disposed on the substrate SUB.

[0065] The scan routing lines GRL are disposed between the gate insulating layer GI and the first insulating layer IN1. The scan routing lines GRL transmit scan pulses to the scan lines GL disposed between the gate insulating layer GI and the first insulating layer IN1. The first link lines LNL1 and the second link lines LNL2 are disposed between the first insulating layer IN1 and the second insulating layer IN2.

[0066] The REF routing line RFR and the REF lines RFL are disposed on the second insulating layer IN2. The RFR routing line RFR is connected to the first link lines LNL1 via contact holes RH1 penetrated into the second insulating layer IN2. The REF lines RFL are connected to the first link lines LNL1 via contact holes RH2 penetrated into the second insulating layer IN2. The contact holes RH2 that bring the REF lines RFL and the first link lines LNL1 into contact with each other may be disposed on the outer part of the active area AA, adjacent to the active area AA. However, the present invention is not limited to this.

[0067] The display device may prevent load variations caused by differences in length depending on the positions of the REF lines RFL by having the first link lines LNL1, second lines LNL2, and first auxiliary link lines LNA1. The present invention may provide a display de-

vice that is improved in display quality and product reliability by preventing degradation in luminance uniformity.

[0068] However, because a plurality of signal lines to which different signals are applied and a plurality of driving elements are disposed in the link area LN, a short circuit or interference may occur between the signals lines to which different signals are applied.

[0069] Specifically, in the link area LN, the scan routing lines GRL, to which scan pulses are applied, and the link lines LNL1 and LNL2, to which the reference voltage Vref is applied, are disposed on different layers, with the first insulating layer IN1 in between. Especially, the second link lines LNL2 cross the scan routing lines GRL, with only the first insulating layer IN1 in between. The distance G1 between the second link lines LNL2 and the scan routing lines GRL is very short since the second link lines LNL2 are vertically adjacent to the scan routing lines GRL.

[0070] If the second link lines LNL2 and the scan routing lines GRL, to which different signals are applied, are disposed adjacent to each other, the insulating layer, e.g., first insulating layer IN1, between the second link lines LNL2 and the scan routing lines GRL may be fused due to applied static electricity, etc., thus resulting in an insulation breakdown. Therefore, a short circuit may occur between the second link lines LNL2 and the scan routing lines GRL. Moreover, a large current flows into the gate drive circuit 120 and/or power generator through the adjacent second link lines LNL2 and scan routing lines GRL, thereby causing circuit damage.

<Second Exemplary Embodiment>

[0071] A second exemplary embodiment of the present invention provides a display device which compensates for load variations caused by differences in length between REF lines RFL by having first and second link lines LNL2, and which prevents a short circuit caused by the proximity between second link lines LNL2 and scan routing lines GRL to which different signals are applied.

[0072] Referring to FIGS. 10 and 11, a display device according to the second exemplary embodiment of the present invention will be described below. FIG. 10 is a top plan view illustrating the AR area of FIG. 6, in the display device according to the second exemplary embodiment of the present invention. FIG. 11 is a cross-sectional view taken along line III-III' of FIG. 10.

[0073] Referring to FIGS. 6 and 10, a display panel according to the present invention comprises a substrate SUB and link lines LNL1 and LNL2. The substrate SUB comprises a free form active area AA and a bezel area BZ located outside the active area AA. Pixels 10 defined by scan lines GL, data lines DL, and REF lines RFL are arranged in the free form active area AA. A gate drive circuit 120, a reference voltage routing part 113, and a link area LN are located in the bezel area BZ.

[0074] The gate drive circuit 120 may be formed on the substrate SUB of the display panel by GIP technology.

The gate drive circuit 120 generates scan pulses. The gate drive circuit 120 supplies scan pulses SCAN1 and SCAN2 to the scan lines GL in the active area AA under control of a timing controller 30. The gate drive circuit 120 and the scan lines GL are electrically connected through scan routing lines GRL provided in between them. The scan pulses from the gate drive circuit 120 are supplied to the scan lines GL through the scan routing lines GRL.

[0075] The reference voltage routing part 113 is provided with an REF routing line RFR. The REF routing line RFR receives a reference voltage Vref from a power generator. A plurality of driving elements and a plurality of electrodes to which different signals (or voltages) are applied are disposed in a space (hereinafter, "link area") LN between the reference voltage routing part 113 and the active area AA, with insulating layers of organic and/or inorganic insulating materials interposed between the driving elements and the electrodes. For example, AP switching circuit elements 115, the link lines LNL1 and LNL2, and the scan routing lines GRL may be disposed in the link area LN. The link lines LNL1 and LNL2 and the scan routing lines GRL run across the link area LN.

[0076] The link lines LNL1 and LNL2 are disposed in the bezel area BZ, and connect the REF routing line RFR to the REF lines RFL to transmit the reference voltage Vref from the REF routing line RFR to the REF lines RFL. That is, the reference voltage Vref is supplied to the REF lines RFL in the active area AA through a signal transmission path connecting to the REF routing line RFR and the link lines LNL1 and LNL2.

[0077] The link lines LNL1 and LNL2 comprise first link lines LNL1 and second link lines LNL2. The first link lines LNL1 extend from the reference voltage routing part 113 through the link area LN and are electrically connected to the REF lines RFL. To this end, one end of the first link lines LNL1 is connected to the REF routing line RFR of the reference voltage routing part 113 via contact holes RH1, and the other end of the first link lines LNL1 is connected to the REF lines RFL in the active area AA via contact holes RH2.

[0078] The second link lines LNL2 electrically connect n first link lines LNL1 (n is an integer greater than or equal to 2). The second link lines LNL2 extend from the REF lines RFL toward the outer part of the active area AA. That is, the second link lines LNL2 and the REF lines RFL are formed as a single body. Accordingly, the REF lines RFL run through the active area AA, and extend toward the bezel area BZ. One end of the second link lines LNL2 is connected to the REF lines RFL. The other end of the second link lines LNL2 is connected to the first link lines LNL1 via contact holes RH3. Accordingly, the first link lines LNL1 may be connected to the REF lines RFL via the contact holes RH2, and connected to the second link lines LNL2 extending from the REF lines RFL via the contact holes RH3. One first link line LNL2 may be connected to an REF line RFL via a contact hole RH2,

and at the same time connected to a second link line LNL2 via a contact hole RH3.

[0079] The second link lines LNL2 may compensate for load variations caused by differences in length between the REF lines RFL in the active area AA by interconnecting the first link lines LNL1. The present invention provides a display device that can prevent degradation in luminance uniformity.

[0080] The bezel area BZ may have a large number of second link lines LNL2 to interconnect multiple first link lines LNL1. The larger the number of second lines LNL2, the easier for the REF lines RFL to be equipotential. The reference voltage can be supplied uniformly to the REF lines RFL by having a sufficient number of second link lines LNL2.

[0081] In order for the REF lines RFL to be equipotential, the present invention may further comprise first auxiliary link lines LNA1. Unlike the first link lines LNL1 connecting the REF routing line RFR and the REF lines RFL, the first auxiliary link lines LNA1 connect the REF routing line RFR and the second link lines LNL2. A large number of first auxiliary link lines LNA1 may be provided in the bezel area BZ. The larger the number of first auxiliary link lines LNA1, the easier for the REF lines RFL to be equipotential. The reference voltage can be supplied uniformly to the REF lines RFL by having a sufficient number of first auxiliary link lines LNA1.

[0082] In order for the REF lines RFL to be equipotential, the present invention may further comprise second auxiliary link lines LNA2. One end of the second auxiliary link lines LNA2 is connected to either the second link lines LNL2 or the REF lines RFL, and the other end of the second auxiliary link lines LNA2 is connected to either the second link lines LNL2 or the REF lines RFL. In an example, the second auxiliary link lines LNA2 connect the second link lines LNL2 and the REF lines RFL. In another example, the second auxiliary link lines LNA2 connect the REF lines RFL. That is, the second auxiliary link lines LNA2 are not directly connected to the REF routing line RFR. The second auxiliary link lines LNA2 are different from the first link lines LNL1 connecting the REF routing line RFR and the REF lines RFL. The second auxiliary link lines LNA2 are different from the second link lines LNL2 connecting the REF lines RFL and the first link lines LNL1. A large number of second auxiliary link lines LNA2 may be provided in the bezel area BZ. The larger the number of second auxiliary link lines LNA2, the easier for the REF lines RFL to be equipotential. The reference voltage can be supplied uniformly to the REF lines RFL by having a sufficient number of second auxiliary link lines LNA2.

[0083] Referring further to FIGS. 11, connections among the REF routing line RFR, link lines, and REF lines RFL will be described using a stack structure.

[0084] Referring further to FIGS. 11, numerous insulating layers are disposed on the substrate SUB. For example, a buffer layer BUF, a gate insulating layer GI, a first insulating layer IN1, and a second insulating layer

IN2 may be disposed on the substrate SUB.

[0085] The scan routing lines GRL are disposed between the gate insulating layer GI and the first insulating layer IN1. The scan routing lines GRL transmit scan pulses to the scan lines GL disposed between the gate insulating layer GI and the first insulating layer IN1. The first link lines LNL1 and the second auxiliary link lines LNA2 are disposed between the first insulating layer IN1 and the second insulating layer IN2.

[0086] The REF routing line RFR, the REF lines RFL, and the second link lines LNL2 are disposed on the second insulating layer IN2. The REF routing line RFR is connected to the first link lines LNL1 via contact holes RH1 penetrated into the second insulating layer IN2. The REF lines RFL are connected to the first link lines LNL1 via contact holes RH2 penetrated into the second insulating layer IN2. The REF lines RFL are connected to the second auxiliary link lines LNA2 via contact holes RH2 penetrated into the second insulating layer IN2. The contact holes RH2 that bring the REF lines RFL and the first link lines LNL1 into contact with each other may be disposed on the outer part of the active area AA, adjacent to the active area AA. However, the present invention is not limited to this.

[0087] The second link lines LNL2 are formed on the same layer as the REF lines RFL, and directly connected to the REF lines RFL. The second link lines LNL2 and the REF lines RFL are formed as a single body. The second link lines LNL2 are connected to the first link lines LNL1 via contact holes RH3 penetrated into the second insulating layer IN2. The second link lines LNL2 are connected to the second auxiliary link lines LNA2 via contact holes RH3 penetrated into the second insulating layer IN2.

[0088] In the second exemplary embodiment of the present invention, the first link lines LNL1 and the second link lines LNL2 are disposed on different layers. That is, the second link lines LNL2 are disposed above the first link lines LNL1, with an insulating layer in between. Accordingly, in the link area LN, the second link lines LNL2 and the scan routing lines GRL cross each other, with the first and second insulating layers IN1 and IN2 in between.

[0089] The second exemplary embodiment of the present invention can prevent a short circuit between the second link lines LNL2 and scan routing lines GRL to which different signals are applied, as compared to the first exemplary embodiment, by keeping enough distance G2 between the second link lines LNL2 and the scan routing lines GRL.

[0090] The present invention may prevent load variations caused by differences in length depending on the positions of the REF lines RFL by having the first link lines LNL1, second lines LNL2, first auxiliary link lines LNA1, and second auxiliary link lines LNA2. Accordingly, the present invention may provide a display device that is improved in display quality and product reliability by preventing degradation in luminance uniformity.

<Third Exemplary Embodiment>

[0091] A third exemplary embodiment of the present invention provides a display device which more efficiently prevents a short circuit caused by the proximity between second link lines LNL2 and scan routing lines GRL to which different signals are applied, as compared to the second exemplary embodiment. In describing the third exemplary embodiment, redundancies between the second and third exemplary embodiments will be omitted.

[0092] Referring to FIGS. 12 and 14, a display device according to the third exemplary embodiment of the present invention will be described below. FIG. 12 is a top plan view illustrating the AR area of FIG. 6, in the display device according to a third exemplary embodiment of the present invention. FIG. 13 is a cross-sectional view taken along line IV-IV' of FIG. 12. FIG. 14 is a cross-sectional view taken along line V-V' of FIG. 12.

[0093] Referring to FIG. 12, the gate drive circuit 120 may be formed on the substrate SUB of the display panel by GIP technology. The gate drive circuit 120 generates scan pulses. The gate drive circuit 120 supplies scan pulses SCAN1 and SCAN2 to the scan lines GL in the active area AA under control of a timing controller 30. The gate drive circuit 120 and the scan lines GL are electrically connected through scan routing lines GRL provided in between them. The scan pulses from the gate drive circuit 120 are supplied to the scan lines GL through the scan routing lines GRL.

[0094] The scan routing lines GRL extend from a lead-in part GLI of the gate drive circuit 120, and are connected to the scan lines GL in the active area AA. One end of the scan routing lines GRL is connected to the lead-in part GLI of the gate drive circuit 120, and the other end is connected to the scan lines GL. Scan pulses are generated from the gate drive circuit 120 and supplied to the scan lines GL through the lead-in part GLI of the gate drive circuit 120 and the scan routing lines GRL. The scan routing lines GRL run across the reference voltage routing part 113 and the link area LN.

[0095] Referring further to FIG. 13, the third exemplary embodiment of the present invention is characterized in that the scan routing lines GRL are formed on a different layer than the lead-in part GLI of the gate drive circuit 120 and the scan lines GL. The scan routing lines GRL are formed below the lead-in part GLI of the gate drive circuit 120 and the scan lines GL, with at least one insulating layer in between.

[0096] One end of the scan routing lines GRL is connected to the lead-in part GLI of the gate drive circuit 120 via contact holes GH1 penetrated into the gate insulating layer GI and buffer layer BUF. The other end of the scan routing lines GRL is connected to the scan lines GL via contact holes GH2 penetrated into the gate insulating layer GI and buffer layer BUF.

[0097] Referring further to FIG. 14, in the third exemplary embodiment of the present invention, the first link lines LNL1 and the second link lines LNL2 are disposed

on different layers. That is, the second link lines LNL2 are disposed above the first link lines LNL1, with an insulating layer in between. Also, in the third exemplary embodiment of the present invention, the scan routing lines GRL, the lead-in part GLI of the gate drive circuit 120, and the scan lines GL are disposed on different layers. That is, the scan routing lines GRL are disposed below the lead-in part GLI of the gate drive circuit 120 and the scan lines GL, with an insulating layer in between. Accordingly, in the link area LN, the second link lines LNL2 and the scan routing lines GRL cross each other, with the buffer layer BUF, gate insulating layer GI, first insulating layer IN1, and second insulating layer IN2 in between.

[0098] The third exemplary embodiment of the present invention can more efficiently prevent a short circuit between the second link lines LNL2 and scan routing lines GRL to which different signals are applied, as compared to the second exemplary embodiment, by keeping enough distance G2 between the second link lines LNL2 and the scan routing lines GRL.

[0099] The present invention can prevent a short circuit between signal lines to which different signals are applied, by using novel signal transmission paths.

[0100] Moreover, the present invention can compensate for load variations caused by differences in length depending on the positions of the scan lines by adding or changing signal transmission paths to which a power supply voltage is applied. Accordingly, the present invention provides a display device that is improved in display quality and product reliability by preventing degradation in luminance uniformity.

[0101] Although embodiments have been described with reference to a number of illustrative embodiments thereof, it should be understood that numerous other modifications and embodiments can be devised by those skilled in the art that will fall within the scope of the claims of this disclosure. More particularly, numerous variations and modifications are possible in the component parts and/or arrangements of the subject combination arrangement within the scope of the appended claims. In addition to variations and modifications in the component parts and/or arrangements, alternative uses will also be apparent to those skilled in the art.

[0102] One exemplary aspect of the present invention would be a display device comprising:

a substrate comprising an free form active area having pixels defined by scan lines, data lines, and power supply lines, and a bezel area located outside the active area and having power supply routing lines to which a power supply voltage is applied and scan routing lines to which scan pulses are applied; and link lines that are disposed in the bezel area, and that connect the power supply routing lines to the power supply lines and transmit the power supply voltage from the power supply routing lines to the power supply lines,

the link lines comprising:

a plurality of first link lines; and
one or more second link lines that interconnect
the first link lines,
each of the first link lines comprising one end
connected to the power supply routing lines and
the other end connected to the power supply
lines.

Claims

1. A display device (110) comprising:

a substrate (SUB), pixels, scan lines (GL), data
lines (DL), power supply lines (RFL), a power
supply routing line (RFR), a scan routing line
(GRL), first link lines (LNL1), second link lines
(LNL2), first auxiliary link lines (LNA1), second
auxiliary link lines (LNA2), a first insulating layer
(IN1), a second insulating layer (IN2), a gate in-
sulating layer (GI), a buffer layer (BUF), which
are disposed on the substrate,
wherein the pixels are formed in a free form ac-
tive area (AA) of the substrate, the pixels being
located at the crossing of the scan lines (GL)
and the data lines (DL), and connected to re-
spective power supply lines (RFL),
wherein the power supply lines in the free form
active area have different lengths and are con-
nected to different numbers of pixels depending
on their positions;
wherein the power supply routing line (RFR) to
which a power supply voltage (REF) can be ap-
plied and the scan routing line (GRL) to which
scan pulses can be applied are formed in a bezel
area (BZ) of the substrate which is outside the
active area (AA);
wherein the first and second link lines (LNL1,
LNL2) are disposed in the bezel area (BZ) and
are configured to connect the power supply rout-
ing line (RFR) to the power supply lines (RFL)
so as to transmit the power supply voltage (REF)
from the power supply routing line (RFR) to the
power supply lines (RFL),
wherein each of the first link lines (LNL1) com-
prises one end connected to the power supply
routing line (RFR) and the other end connected
to one of the power supply lines (RFL),
wherein the second link lines (LNL2) intercon-
nect the first link lines (LNL1),
wherein each of the first auxiliary link lines
(LNA1) comprises one end connected to the
power supply routing line (RFR) and the other
end connected to one of the second link lines
(LNL2),
wherein each of the second auxiliary link lines

(LNA2) comprises one end that is connected to
one of the power supply lines (RFL) and the oth-
er end that is connected to one of the second
link lines (LNL2),
wherein the first insulating layer (IN1) is dis-
posed on the scan routing line (GRL);
the first link lines (LNL1), the first auxiliary link
lines (LNA1) and the second auxiliary link lines
(LNA2) are disposed between the first insulating
layer (IN1) and the second insulating layer (IN2);
and
the power supply routing line (RFR), the power
supply lines (RFL), and the second link lines
(LNL2) are formed on a same layer disposed on
the second insulating layer (IN2), and
wherein the power supply routing line (RFR) is
connected to the first link lines (LNL1) via con-
tact holes (RH1) penetrated into the second in-
sulating layer (IN2),
the power supply lines (RFL) are connected to
the first link lines (LNL1) and to the second aux-
iliary link lines (LNA2) via contact holes (RH2)
penetrated into the second insulating layer
(IN2), and
the second link lines (LNL2) are connected to
the first link lines (LNL1) and to the second aux-
iliary link lines (LNA2) via contact holes (RH3)
penetrated into the second insulating layer
(IN2).

2. The display device of claim 1, wherein the scan rout-
ing line (GRL) is disposed between the gate insulat-
ing layer (GI) and the first insulating layer (IN1).

3. The display device of claim 1, wherein:

the display device further comprises a gate drive
circuit (120) configured to supply scan pulses to
the scan lines (GL) and select pixels from the
display panel (110) to write a data voltage;
the scan routing line (GRL) is connected to a
lead-in part (GLI) of the gate drive circuit (120);
and
the scan routing line (GRL) is formed on a dif-
ferent layer than the lead-in part (GLI) of the gate
drive circuit (120) and the scan lines (GL).

4. The display device of claim 3, wherein there is at
least one insulating layer in between the scan routing
line (GRL) and the lead-in part (GLI).

5. The display device of claim 1, wherein when the sec-
ond link lines (LNL2) and the scan routing lines (GRL)
cross each other, the buffer layer (BUF), the gate
insulating layer (GI), the first insulating layer (IN1),
and the second insulating layer (IN2) are in between.

Patentansprüche

1. Anzeigevorrichtung (110), die Folgendes umfasst:

ein Substrat (SUB), Pixel, Abtastleitungen (GL), 5
Datenleitungen (DL), Leistungsversorgungslei-
tungen (RFL), eine Leistungsversorgungsfüh-
rungsleitung (RFR), eine Abtastführungsleitung
(GRL), erste Verbindungsleitungen (LNL1), 10
zweite Verbindungsleitungen (LNL2), erste
Hilfsverbindungsleitungen (LNA1), zweite Hilfs-
verbindungsleitungen (LNA2), eine erste Isolier-
schicht (IN1), eine zweite Isolierschicht (IN2),
eine Gate-Isolierschicht (GI) und eine Puffer-
schicht (BUF), die auf dem Substrat angeordnet 15
sind,
wobei die Pixel in einer Freiformaktivfläche (AA)
des Substrats gebildet sind, wobei sich die Pixel
an der Kreuzung der Abtastleitungen (GL) und
der Datenleitungen (DL) befinden und mit den 20
jeweiligen Leistungsversorgungsleitungen
(RFL) verbunden sind,
wobei die Leistungsversorgungsleitungen in der
Freiformaktivfläche unterschiedliche Längen
aufweisen und abhängig von ihren Positionen 25
mit unterschiedlich vielen Pixeln verbunden
sind;
wobei die Leistungsversorgungsführungslei-
tung (RFR), an die eine Leistungsversorgungs-
spannung (REF) angelegt werden kann, und die 30
Abtastführungsleitung (GRL), an die Abtastim-
pulse angelegt werden können, in einer Einfas-
sungsfläche (BZ) des Substrats gebildet sind,
die sich außerhalb der Aktivfläche (AA) befindet;
wobei die ersten und zweiten Verbindungslei- 35
tungen (LNL1, LNL2) in der Einfassungsfläche
(BZ) angeordnet sind und konfiguriert sind, die
Leistungsversorgungsführungsleitung (RFR)
mit den Leistungsversorgungsleitungen (RFL)
zu verbinden, um die Leistungsversorgungs- 40
spannung (REF) von der Leistungsversor-
gungsführungsleitung (RFR) an die Leistungs-
versorgungsleitungen (RFL) zu übertragen,
wobei jede der ersten Verbindungsleitungen
(LNL1) ein Ende, das mit der Leistungsversor- 45
gungsführungsleitung (RFR) verbunden ist, und
das andere Ende, das mit einer der Leistungs-
versorgungsleitungen (RFL) verbunden ist, um-
fasst,
wobei die zweiten Verbindungsleitungen (LNL2) 50
die ersten Verbindungsleitungen (LNL1) zu-
sammenschalten,
wobei jede der ersten Hilfsverbindungsleitun-
gen (LNA1) ein Ende, das mit der Leistungsver-
sorgungsführungsleitung (RFR) verbunden ist, 55
und das andere Ende, das mit einer der zweiten
Verbindungsleitungen (LNL2) verbunden ist,
umfasst,

wobei jede der zweiten Hilfsverbindungsleitun-
gen (LNA2) ein Ende, das mit einer der Leis-
tungsversorgungsleitungen (RFL) verbunden
ist, und das andere Ende, das mit einer der zwei-
ten Verbindungsleitungen (LNL2) verbunden
ist, umfasst,

wobei die erste Isolierschicht (IN1) auf der Ab-
tastführungsleitung (GRL) angeordnet ist;
die ersten Verbindungsleitungen (LNL1), die
ersten Hilfsverbindungsleitungen (LNA1) und
die zweiten Hilfsverbindungsleitungen (LNA2)
zwischen der ersten Isolierschicht (IN1) und der
zweiten Isolierschicht (IN2) angeordnet sind und
die Leistungsversorgungsführungsleitung
(RFR), die Leistungsversorgungsleitungen
(RFL) und die zweiten Verbindungsleitungen
(LNL2) auf derselben Schicht gebildet sind, die
auf der zweiten Isolierschicht (IN2) angeordnet
ist, und

wobei die Leistungsversorgungsführungslei-
tung (RFR) mit den ersten Verbindungsleitun-
gen (LNL1) über Kontaktlöcher (RH1) verbun-
den ist, die durch die zweite Isolierschicht (IN2)
hindurchgehen,

die Leistungsversorgungsleitungen (RFL) mit
den ersten Verbindungsleitungen (LNL1) und
mit den zweiten Hilfsverbindungsleitungen
(LNA2) über Kontaktlöcher (RH2) verbunden
sind, die durch die zweite Isolierschicht (IN2)
hindurchgehen, und

die zweiten Verbindungsleitungen (LNL2) mit
den ersten Verbindungsleitungen (LNL1) und
mit den zweiten Hilfsverbindungsleitungen
(LNA2) über Kontaktlöcher (RH3) verbunden
sind, die durch die zweite Isolierschicht (IN2)
hindurchgehen.

2. Anzeigevorrichtung nach Anspruch 1, wobei die Ab-
tastführungsleitung (GRL) zwischen der Gate-Iso-
lierschicht (GI) und der ersten Isolierschicht (IN1)
angeordnet ist.

3. Anzeigevorrichtung nach Anspruch 1, wobei:

die Anzeigevorrichtung ferner eine Gate-Trei-
berschaltung (120) umfasst, die konfiguriert ist,
Abtastimpulse an die Abtastleitungen (GL) zu
liefern und Pixel aus der Anzeigetafel (110) aus-
zuwählen, um eine Datenspannung zu schrei-
ben;

die Abtastführungsleitung (GRL) mit einem Zu-
leitungsteil (GLI) der Gate-Treiberschaltung
(120) verbunden ist und

die Abtastführungsleitung (GRL) auf einer an-
deren Schicht als der Zuleitungsteil (GLI) der
Gate-Treiberschaltung (120) und die Abtastlei-
tungen (GL) gebildet ist.

4. Anzeigevorrichtung nach Anspruch 3, wobei mindestens une Isolierschicht zwischen der Abtastführungsleitung (GRL) und dem Zuleitungsteil (GLI) vorhanden ist.
5. Anzeigevorrichtung nach Anspruch 1, wobei dann, wenn die zweiten Verbindungsleitungen (LNL2) und die Abtastführungsleitungen (GRL) einander kreuzen, sich die Pufferschicht (BUF), die Gate-Isolierschicht (GI), die erste Isolierschicht (IN1) und die zweite Isolierschicht (IN2) dazwischen befinden.

Revendications

1. Dispositif (110) d'affichage comportant :

un substrat (SUB), des pixels, des lignes de balayage (GL), des lignes de données (DL), des lignes d'alimentation électrique (RFL), une ligne d'acheminement d'alimentation électrique (RFR), une ligne d'acheminement de balayage (GRL), des premières lignes de liaison (LNL1), des deuxièmes lignes de liaison (LNL2), des premières lignes de liaison auxiliaires (LNA1), des deuxièmes lignes de liaison auxiliaires (LNA2), une première couche isolante (IN1), une deuxième couche isolante (IN2), une couche d'isolation de grille (GI), une couche tampon (BUF), qui sont disposées sur le substrat, les pixels étant formés dans une zone active (AA) de forme libre du substrat, les pixels étant situés à l'intersection des lignes de balayage (GL) et des lignes de données (DL), et reliés à des lignes d'alimentation électrique (RFL) respectives, les lignes d'alimentation électrique dans la zone active de forme libre présentant des longueurs différentes et étant reliées à différents nombres de pixels en fonction de leurs positions ; la ligne d'acheminement d'alimentation électrique (RFR) à laquelle une tension d'alimentation électrique (REF) peut être appliquée et la ligne d'acheminement de balayage (GRL) à laquelle des impulsions de balayage peuvent être appliquées étant formées dans une zone d'encadrement (BZ) du substrat qui est à l'extérieur de la zone active (AA) ; les premières et deuxièmes lignes de liaison (LNL1, LNL2) étant disposées dans la zone d'encadrement (BZ) et étant configuré pour relier la ligne d'acheminement d'alimentation électrique (RFR) aux lignes d'alimentation électrique (RFL) de façon à transmettre la tension d'alimentation électrique (REF) de la ligne d'acheminement d'alimentation électrique (RFR) aux lignes d'alimentation électrique (RFL), chacune des premières lignes de liaison (LNL1)

comportant une extrémité reliée à la ligne d'acheminement d'alimentation électrique (RFR) et l'autre extrémité reliée à une des lignes d'alimentation électrique (RFL), les deuxièmes lignes de liaison (LNL2) interconnectant les premières lignes de liaison (LNL1), chacune des premières lignes de liaison auxiliaires (LNA1) comportant une extrémité reliée à la ligne d'acheminement d'alimentation électrique (RFR) et l'autre extrémité reliée à une des deuxièmes lignes de liaison (LNL2), chacune des deuxièmes lignes de liaison auxiliaires (LNA2) comportant une extrémité qui est reliée à une des lignes d'alimentation électrique (RFL) et l'autre extrémité qui est reliée à une des deuxièmes lignes de liaison (LNL2), la première couche isolante (IN1) étant disposée sur la ligne d'acheminement de balayage (GRL) ; les premières lignes de liaison (LNL1), les premières lignes de liaison auxiliaires (LNA1) et les deuxièmes lignes de liaison auxiliaires (LNA2) étant disposées entre la première couche isolante (IN1) et la deuxième couche isolante (IN2) ; et la ligne d'acheminement d'alimentation électrique (RFR), les lignes d'alimentation électrique (RFL), et les deuxièmes lignes de liaison (LNL2) étant formées sur une même couche disposée sur la deuxième couche isolante (IN2), et la ligne d'acheminement d'alimentation électrique (RFR) étant reliée aux premières lignes de liaison (LNL1) via des trous de contact (RH1) pénétrant dans la deuxième couche isolante (IN2), les lignes d'alimentation électrique (RFL) étant reliées aux premières lignes de liaison (LNL1) et aux deuxièmes lignes de liaison auxiliaires (LNA2) via des trous de contact (RH2) pénétrant dans la deuxième couche isolante (IN2), et les deuxièmes lignes de liaison (LNL2) étant reliées aux premières lignes de liaison (LNL1) et aux deuxièmes lignes de liaison auxiliaires (LNA2) via des trous de contact (RH3) pénétrant dans la deuxième couche isolante (IN2).

2. Dispositif d'affichage selon la revendication 1, la ligne d'acheminement de balayage (GRL) étant disposée entre la couche d'isolation de grille (GI) et la première couche isolante (IN1).
3. Dispositif d'affichage selon la revendication 1 :

le dispositif d'affichage comportant en outre un circuit (120) de commande de grille configuré pour fournir des impulsions de balayage aux lignes de balayage (GL) et sélectionner des pixels à partir du panneau (110) d'affichage pour

écrire une tension de données ;
la ligne d'acheminement de balayage (GRL)
étant reliée à une partie d'entrée (GLI) du circuit
(120) de commande de grille ; et
la ligne d'acheminement de balayage (GRL) 5
étant formée sur une couche différente de celle
de la partie d'entrée (GLI) du circuit (120) de
commande de grille et des lignes de balayage
(GL).

10

4. Dispositif d'affichage selon la revendication 3, **caractérisé en ce qu'il** existe au moins une couche isolante entre la ligne d'acheminement de balayage (GRL) et la partie d'entrée (GLI).

15

5. Dispositif d'affichage selon la revendication 1, **caractérisé en ce que**, lorsque les deuxièmes lignes de liaison (LNL2) et les lignes d'acheminement de balayage (GRL) se croisent, la couche tampon (BUF), la couche d'isolation de grille (GI), la première 20
couche isolante (IN1), et la deuxième couche isolante (IN2) se trouvent entre elles.

25

30

35

40

45

50

55

60

65

FIG. 1

100

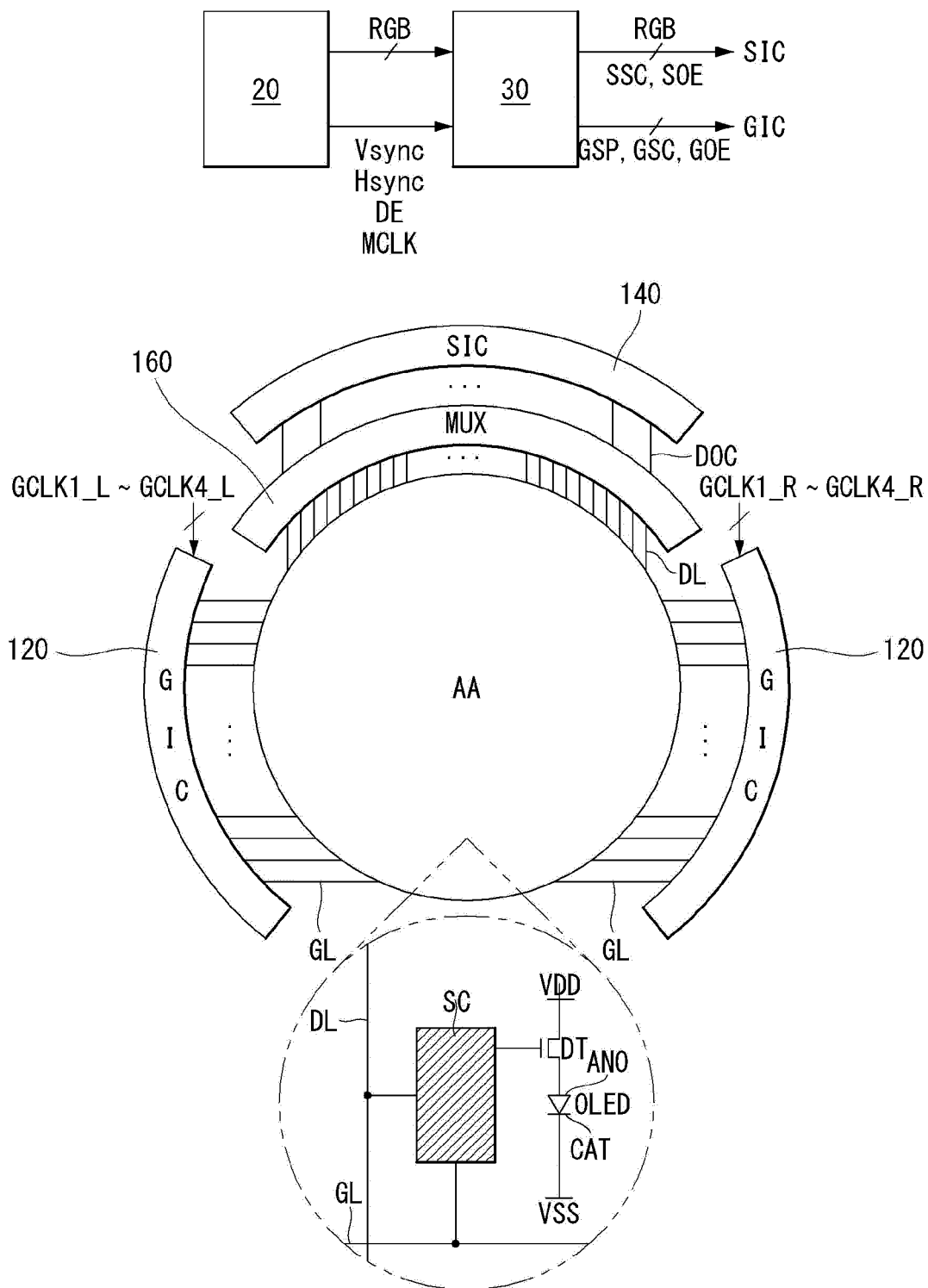


FIG. 2

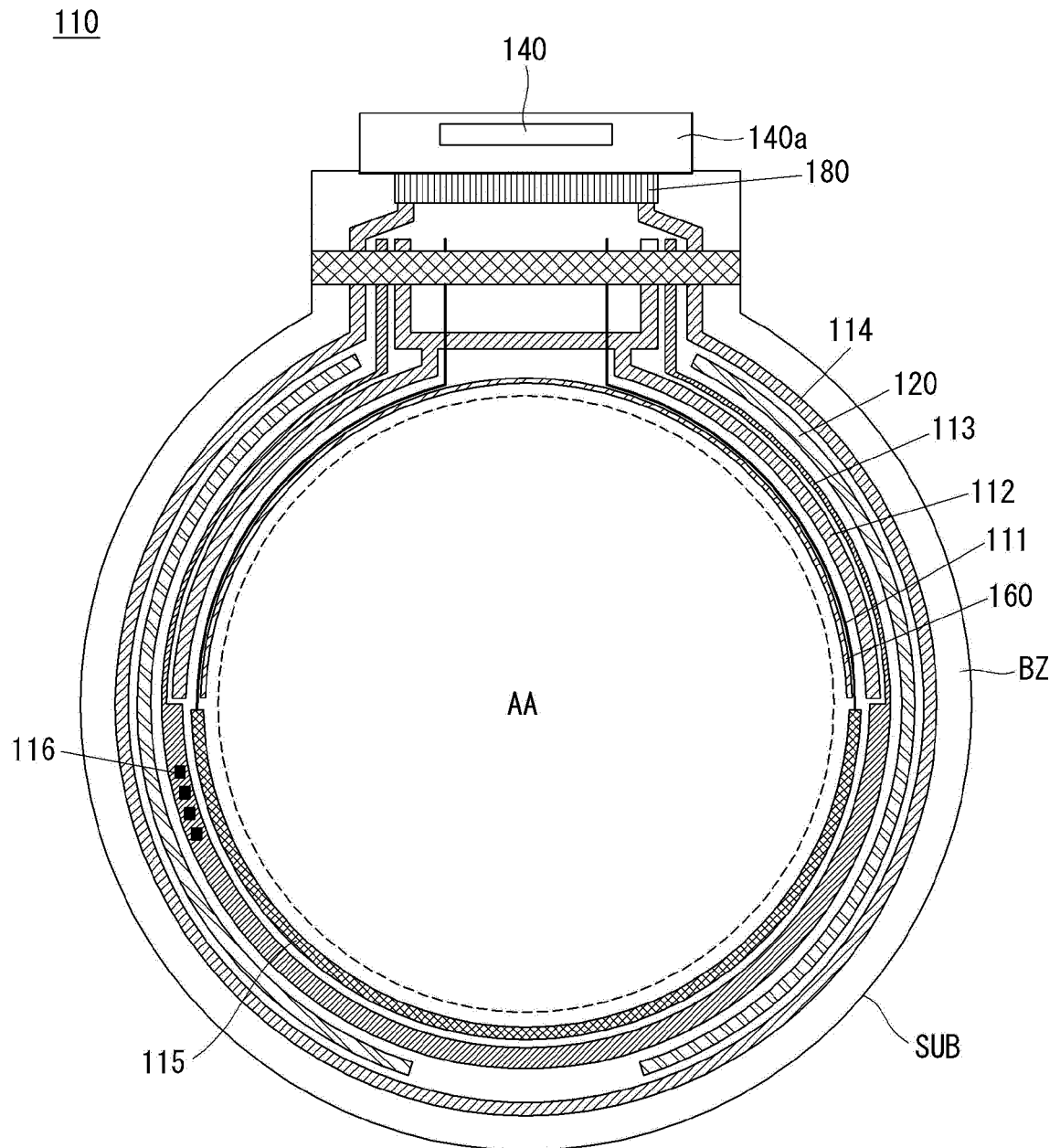


FIG. 3

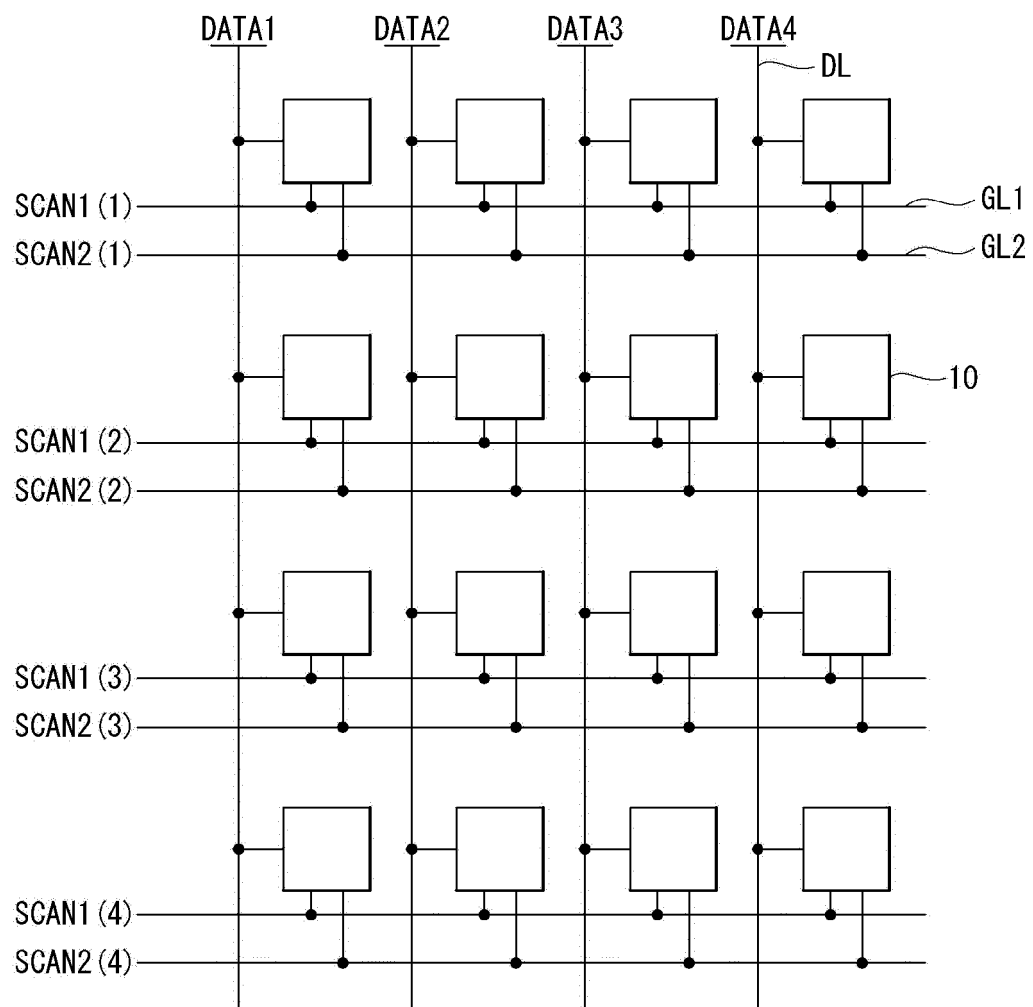


FIG. 4

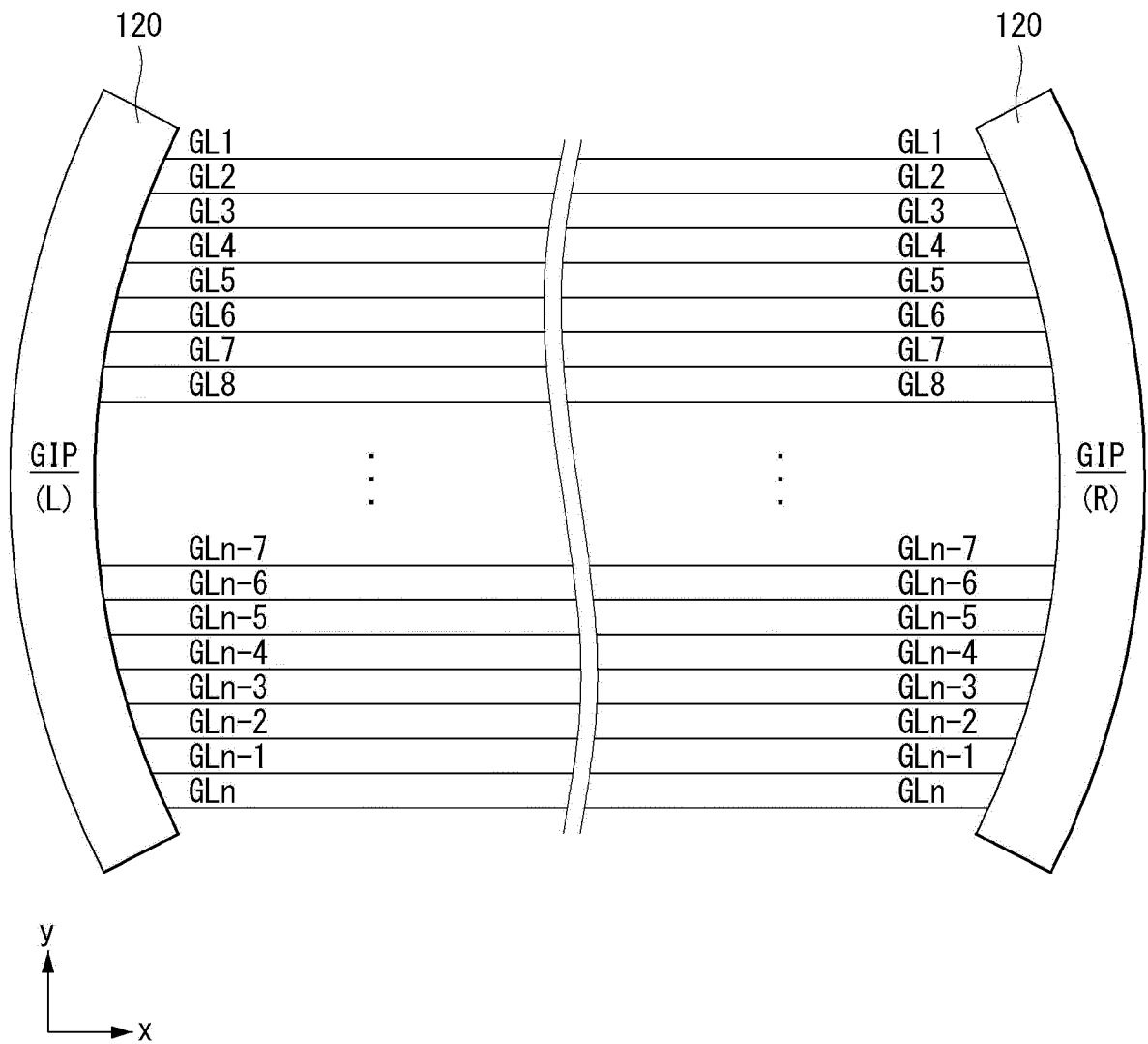


FIG. 5

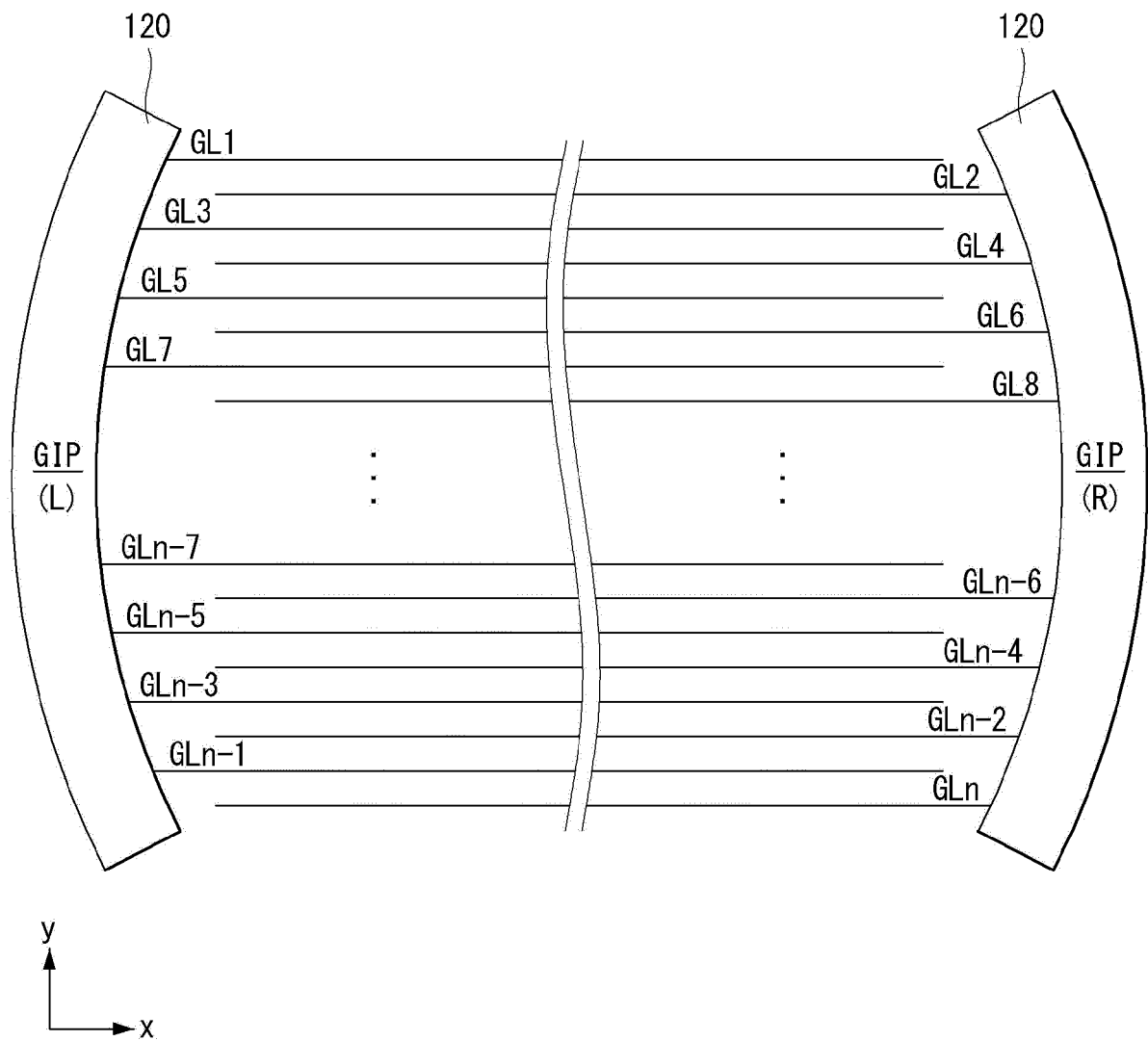


FIG. 6

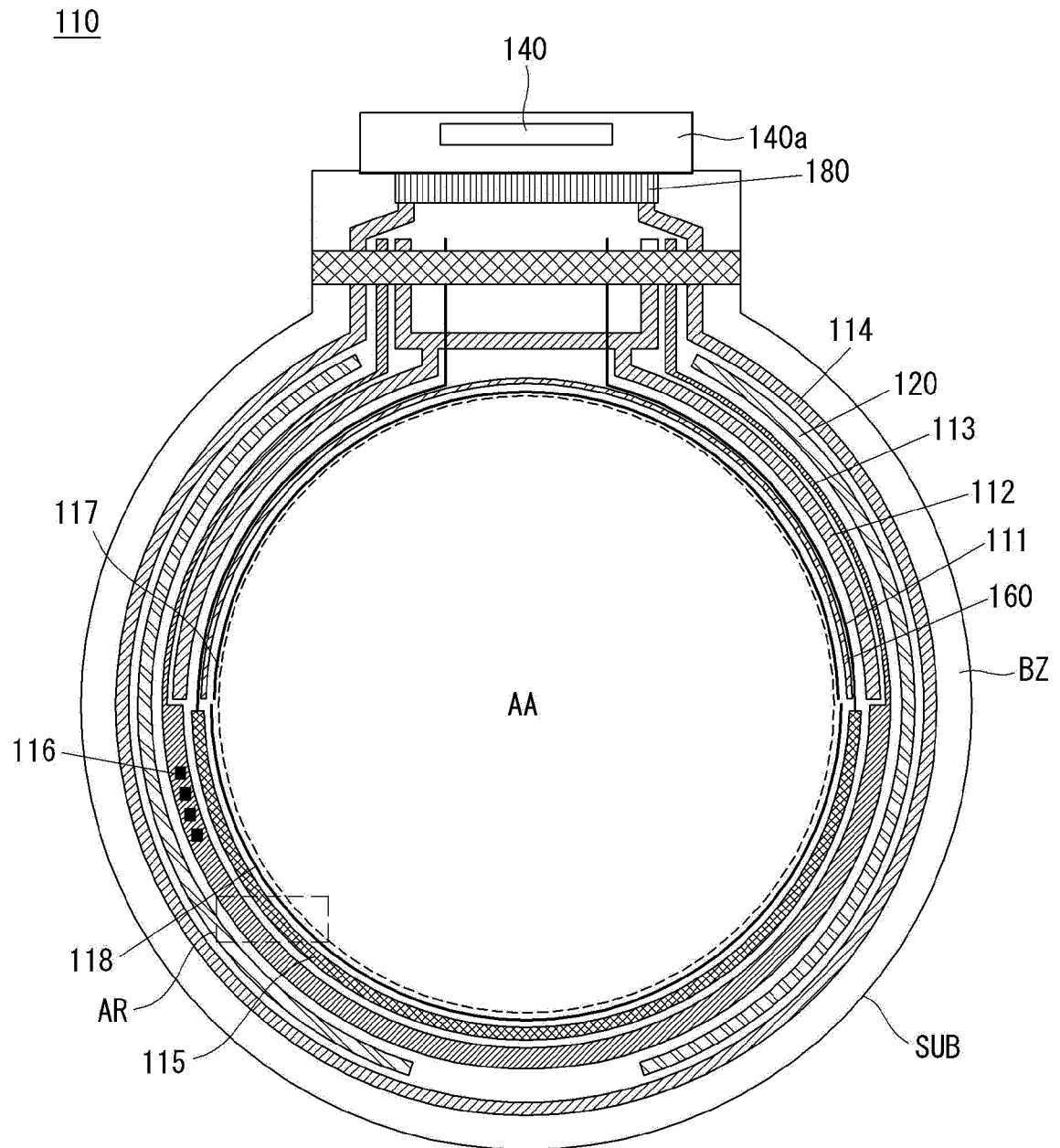


FIG. 7

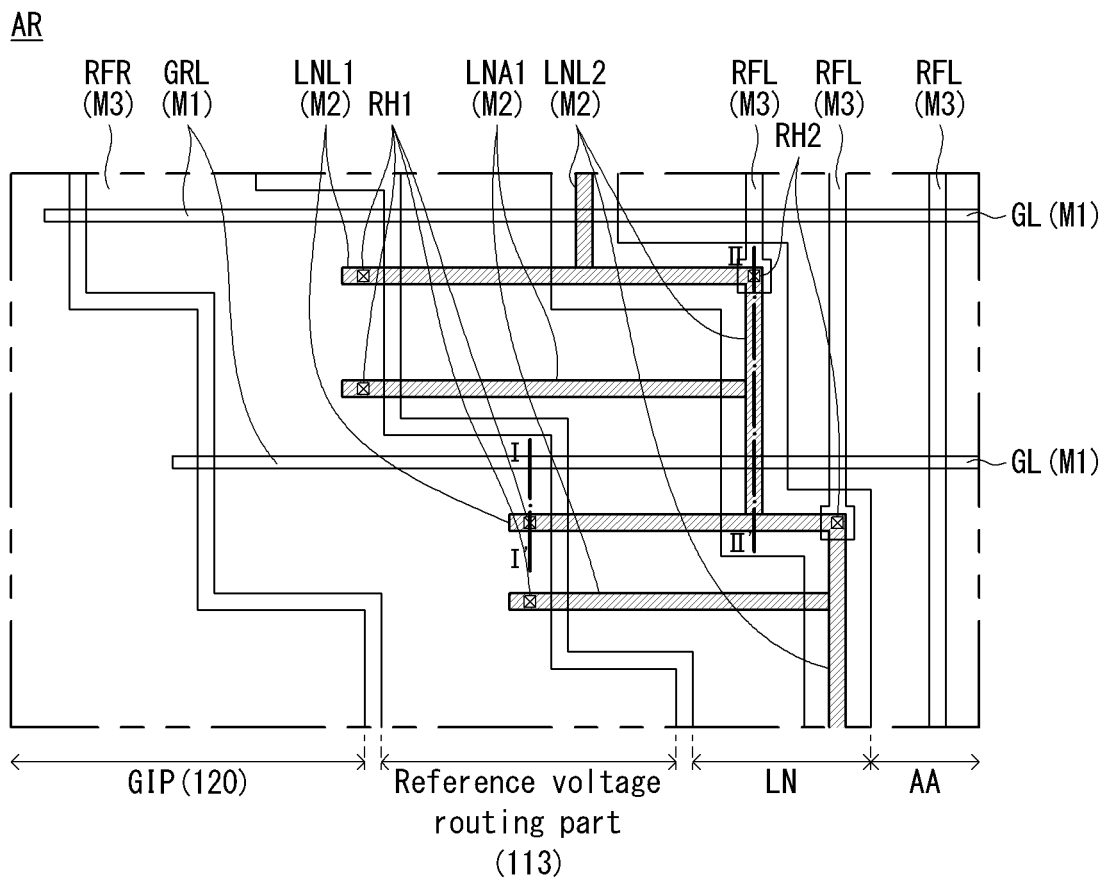


FIG. 8

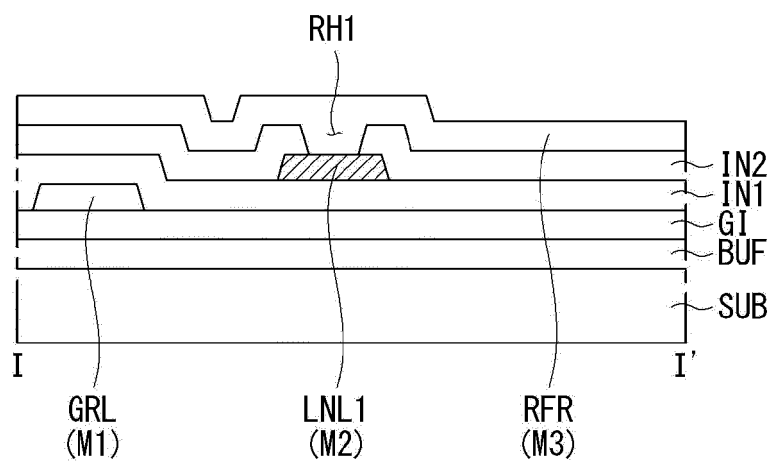


FIG. 9

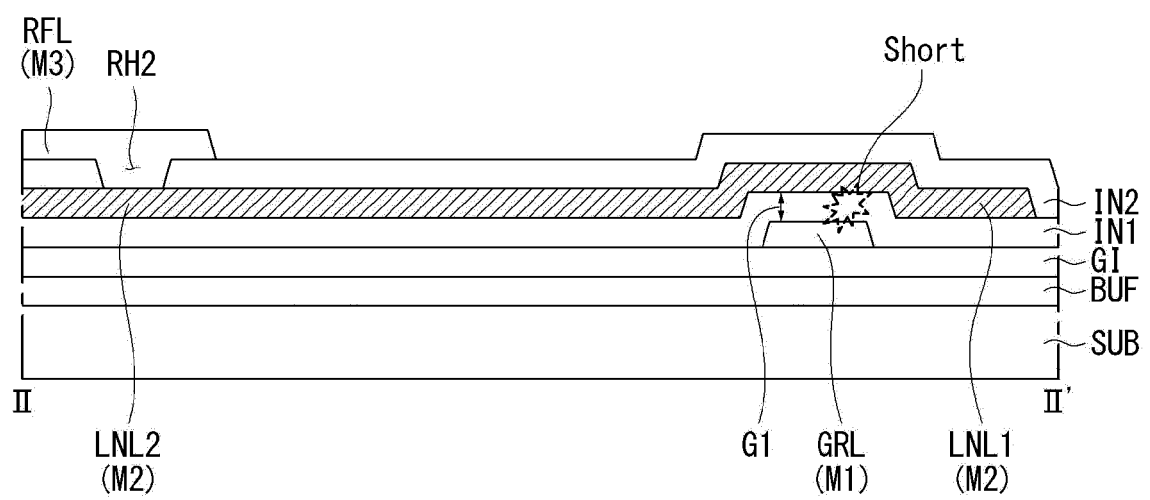


FIG. 10

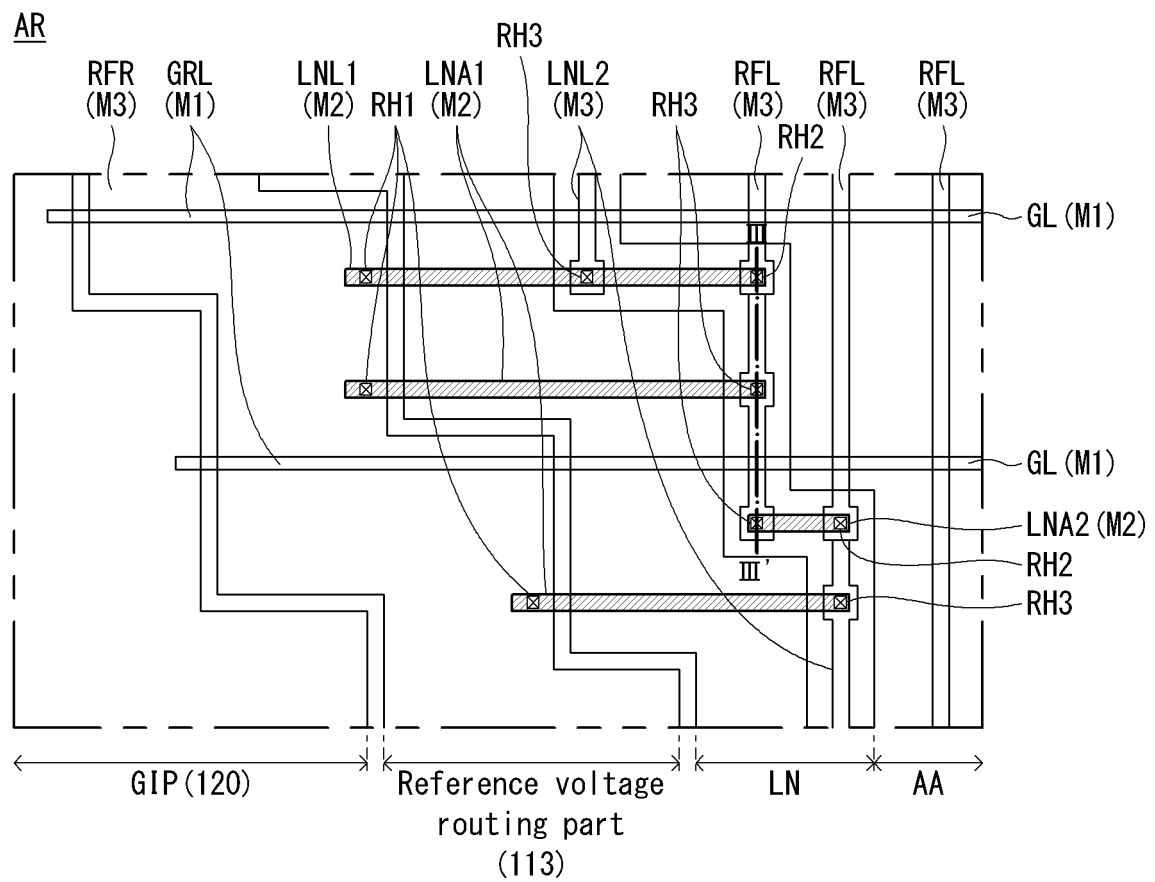


FIG. 11

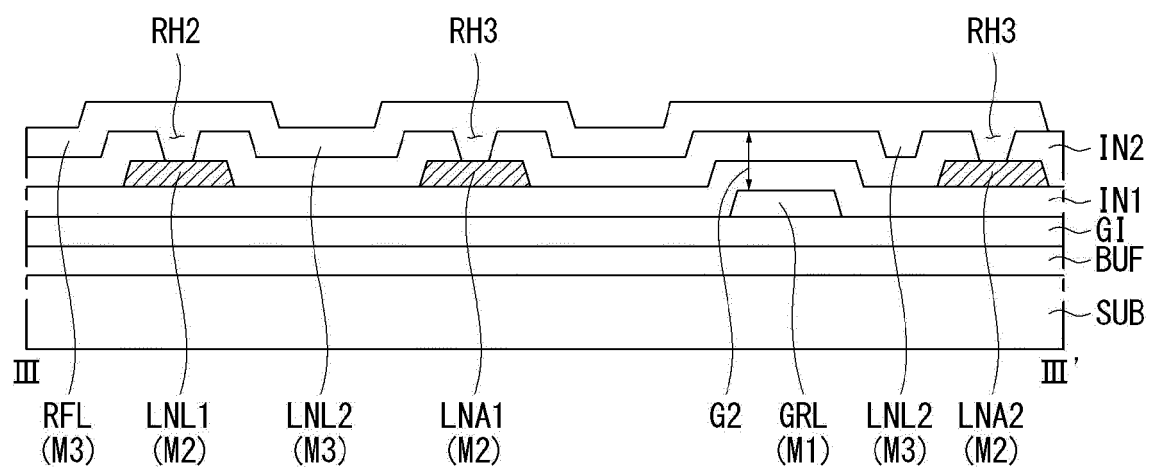


FIG. 12

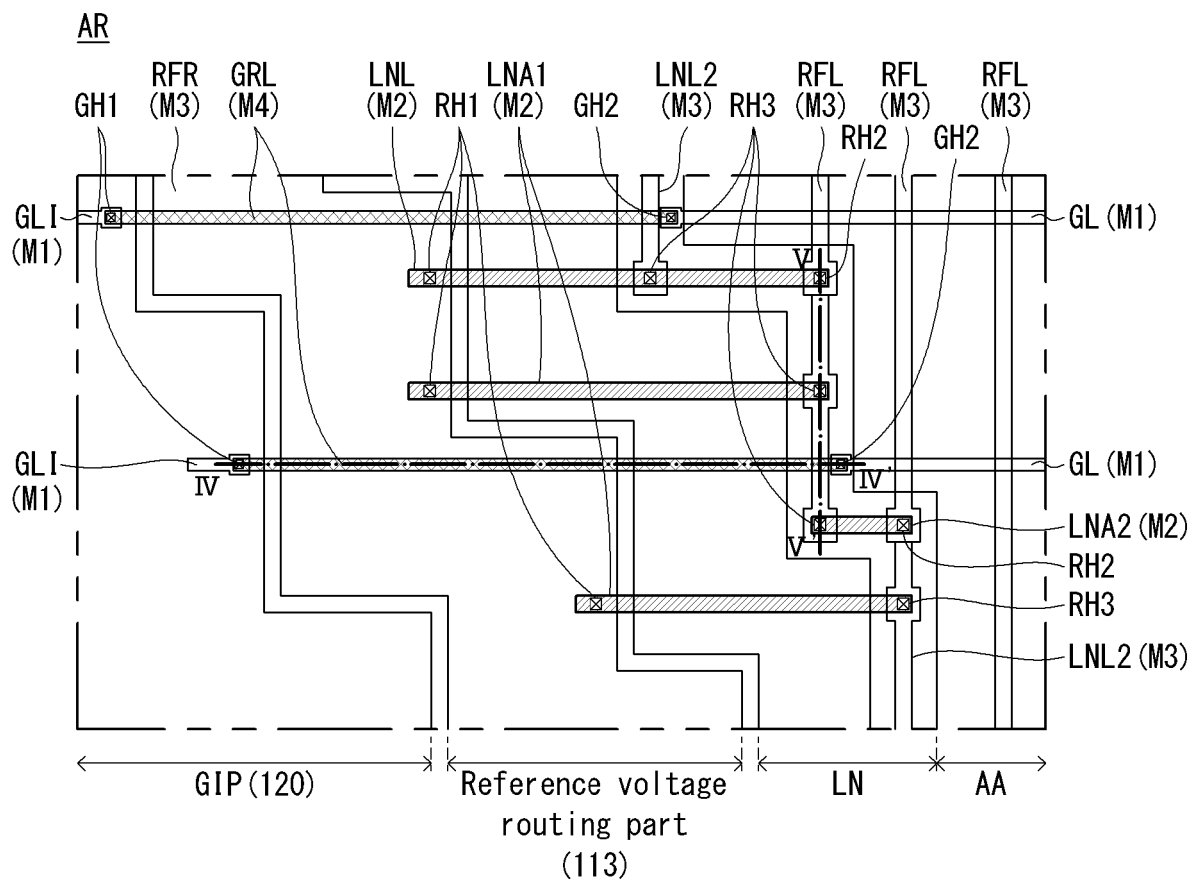


FIG. 13

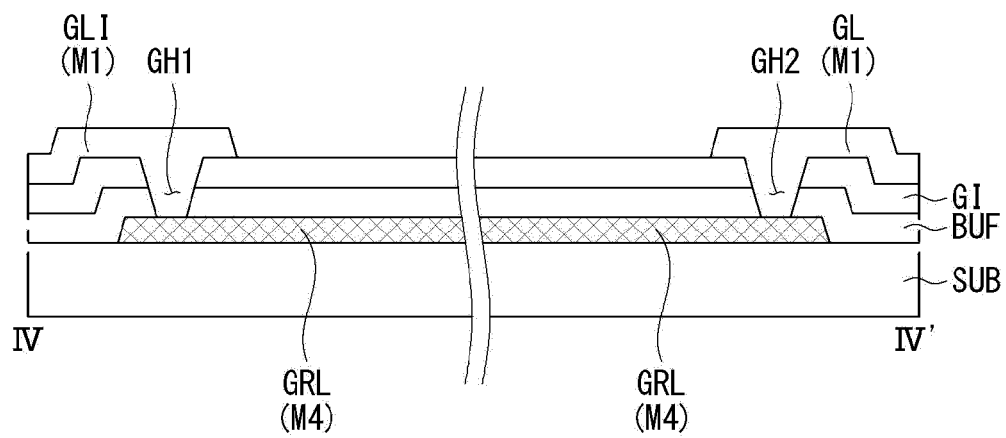
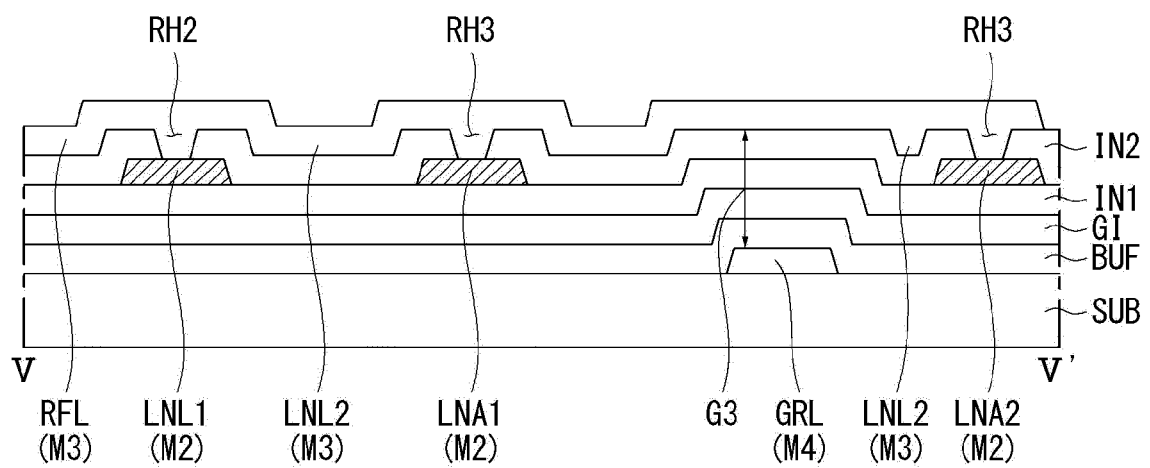


FIG. 14



REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 2014022230 A1 [0005]
- EP 2889864 A1 [0006]

一种显示装置，包括：基板，其包括：自由形式的有源区域，其具有由扫描线，数据线和电源线限定的像素；以及边框区域，其位于有源区域之外，并且具有被施加了电源电压的电源布线线施加扫描脉冲的扫描布线；布置在边框区域中的连接线和连接线，所述连接线将电源路由线连接到电源线并将电源电压从电源路由线传输到电源线，所述链接线包括：第一链接线；一条或多条将第一条链接线互连的第二条链接线，每个第一条链接线的一端连接到电源路由线，另一端连接到电源线。