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(54) **OLED DISPLAY DEVICE**

(57) Provided is an OLED display device including a circuit that controls a voltage of an Nth row unit pixel and a voltage of anodes of pixel lines adjacent to the Nth row unit pixel in order to minimize a voltage difference between the Nth row unit pixel and the pixel lines adjacent to the Nth row unit pixel to suppress a decrease in luminance of the Nth row unit pixel caused by a leakage current introduced to the Nth row unit pixel. The circuit is configured to set the voltage of the anodes of pixel lines adjacent to the Nth row unit pixel to be equal to or lower than a voltage of an anode of the Nth row unit pixel when the Nth row unit pixel is in a sampling period or a programming period during a driving timing of an OLED display device.. Accordingly, it is possible to minimize flow of an unintended leakage current toward a low-potential anode via a common single layer caused by a voltage difference in anode between a pixel including a high-potential anode and a pixel including the low-potential anode.

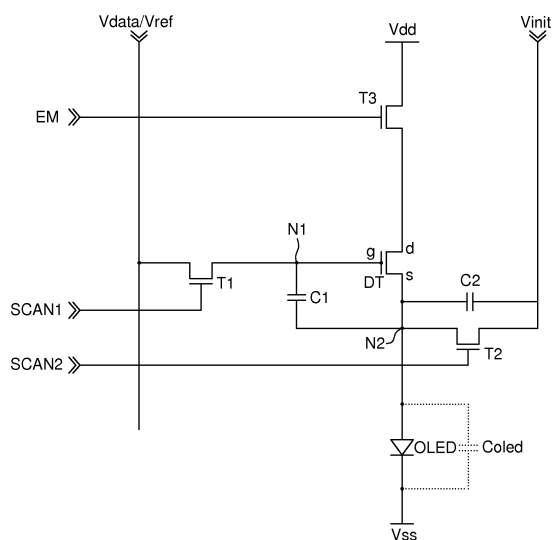


FIG. 3

Description

[Technical Field]

[0001] The present disclosure relates to an organic light emitting diode (hereinafter, referred to as "OLED") display device.

[Background Art]

[0002] Each of a plurality of pixels constituting an OLED display device includes an OLED having an organic light emitting layer between an anode and a cathode and a pixel circuit that independently drives the OLED. The pixel circuit includes a switching thin film transistor (hereinafter, referred to as "TFT"), a capacitor, and a driving TFT. The switching TFT charges the capacitor with a data voltage in response to a scan pulse. The driving TFT regulates emission of the OLED by controlling the amount of current supplied to the OLED according to the data voltage charged in the capacitor.

[0003] Such an OLED display device is comprised of an X*Y matrix including x number of row unit pixels and y number of column unit pixels on a screen. That is, each horizontal pixel line is comprised of x number of pixels and each vertical pixel line is comprised of y number of pixels. The OLED display device displays an image in a single frame by writing data in order from a first row unit pixel to a lowermost xth row unit pixel on a screen.

[0004] Meanwhile, in the organic light emitting layer constituting the OLED, a hole injection layer and a hole transporting layer adjacent to the anode is configured as a common single layer in all of the pixels constituting the OLED display device. However, while the OLED display device writes data to the first row unit pixel through the lowermost row unit pixel in order, there is a time when a voltage difference is generated between anodes of adjacent pixels. Due to a voltage difference in anode between a pixel including a high-potential anode and a pixel including a low-potential anode, an unintended leakage current flows toward the pixel including a low-potential anode through the common single layer. The leakage current may cause a set value of a data voltage applied to an Nth pixel line to be deviated from the manufacturer's intention. Such a data voltage deviation caused by the leakage current becomes a big problem when a resistance of the common single layer decreases.

[0005] Meanwhile, in the OLED display device, a problem occurs as pixels may have different driving TFT threshold voltages V_{th} and mobility due to process variation. Further, a voltage drop of a high-potential voltage VDD occurs, causing an amount of current driving the OLED to be changed. Thus, a luminance deviation is generated between pixels. Generally, an initial driving TFT characteristic deviation generates stain or patterns on a screen and a driving TFT characteristic deviation due to deterioration that occurs over time when driving the OLED reduces the lifespan of an OLED display panel

or generates a residual image. Accordingly, there have been continued attempts to reduce a luminance deviation between pixels and thus improve an image quality by introducing a compensation circuit that compensates a driving TFT characteristic deviation and a drop voltage of a high-potential voltage VDD.

[Disclosure]

10 [Technical Problem]

[0006] The present disclosure is conceived to solve the above-described problem. In the present disclosure, at a time when data are written to an Nth row unit pixel and an image is displayed, an influence of adjacent pixel lines on the Nth row unit pixel is minimized by using a voltage compensation circuit. Accordingly, an object of the present disclosure is to provide an OLED display device that solves a luminance deviation problem caused by a voltage difference generated due to a leakage current during a data writing period.

[Technical Solution]

25 **[0007]** In order to achieve the above-described object, in the OLED display device according to an exemplary embodiment of the present disclosure, each of a plurality of pixels includes the OLED as a light emitting element and a pixel driving circuit that drives the light emitting element. Further, the pixel driving circuit includes: the driving element connected in series between a high-potential voltage supply line and a low-potential voltage supply line, together with the light emitting element; a first switching element that connects a data line with a first node connected with a gate of the driving element in response to a first scan signal; a second switching element that connects an initialization voltage supply line with a second node connected with a source of the driving element in response to a second scan signal; a third switching element that connects the high-potential voltage supply line with a drain of the driving element in response to an emission signal; and a first capacitor connected between the first node and the second node, and the pixel driving circuit operates in a period divided into an initialization period in which when the third switching element is in an off state, the pixel driving circuit turns on the first and second switching elements, to initialize the first and second nodes, a sampling period in which the pixel driving circuit turns on the first and third switching elements, to sense a threshold voltage of the driving element, a programming period in which when the third switching element is in an off state, the pixel driving circuit turns on the first switching element, to write a data voltage to the pixel, a holding period from after completion of writing of a data voltage to the pixel to before the pixel emits a light, and an emission period in which the pixel driving circuit turns on the third switching element, to cause the driving element to supply a drive current to the

light emitting element.

[0008] The present disclosure provides an OLED display device that has a reduced luminance deviation between pixels since a driving TFT characteristic deviation and a drop voltage of a high-potential voltage VDD are compensated.

[0009] The present disclosure provides an OLED display device that has an improved image quality since a luminance deviation between pixels is reduced.

[0010] The present disclosure provides an OLED display device that has an increased margin of a data driving voltage since even when a relatively low data driving voltage is applied, an equivalent luminance is achieved.

[0011] Further, the present disclosure provides an OLED display device that has an excellent response characteristic since three frames displaying the same image in order have a constant and stable luminance regardless of images are displayed in their respective previous frames.

[Description of Drawings]

[0012]

FIG. 1 is a configuration view of an OLED display device according to an exemplary embodiment of the present disclosure;

FIG. 2 is a driving waveform diagram of each pixel P illustrated in FIG. 1;

FIG. 3 is a circuit diagram of each pixel P illustrated in FIG. 1;

FIGS. 4a and 4b are circuit diagrams of each pixel P according to other exemplary embodiments of the present disclosure, respectively;

FIG. 5a is a schematic diagram illustrating an inflow direction of a leakage current introduced to an Nth row unit pixel corresponding to an Nth gate line from pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel while a frame in a display panel of an OLED display device realizes a black image and a next frame realizes a white image;

FIG. 5b is a graph illustrating a simulation result of a V_{gs} value in an Nth row unit pixel corresponding to an Nth gate line while a frame in a display panel of an OLED display device realizes a black image and a next frame realizes a white image;

FIG. 6a is a schematic diagram illustrating an inflow direction of a leakage current introduced to an Nth row unit pixel corresponding to an Nth gate line from pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel while a frame in a display panel of an OLED display device realizes a white image and a next frame also realizes a white image;

FIG. 6b is a graph illustrating a simulation result of a V_{gs} value in an Nth row unit pixel corresponding to an Nth gate line while a frame in a display panel

of an OLED display device realizes a white image and a next frame also realizes a white image;

FIGS. 7, 9, 11, and 13 are schematic diagrams illustrating that when an Nth row unit pixel corresponding to an Nth gate line in a display panel of an OLED display device is in a sampling period t_2 or a programming period t_3 , pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel is in an emission state according to an exemplary embodiment of the present disclosure;

FIGS. 8a, 8b, 10a, 10b, 12a, 12b, 14a, and 14b respectively corresponding to FIGS. 7, 9, 11, and 13 are driving waveform diagrams illustrating a driving method of an Nth row unit pixel corresponding to an Nth gate line in a display panel of an OLED display device and pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel according to an exemplary embodiment of the present disclosure;

FIG. 15 is a graph comparing an I-V curve between a case where a pixel of an OLED display device is driven by a driving method of the present disclosure according to the driving waveform diagram of FIG. 8a and a case where the pixel is driven by a driving method of the prior art; and

FIG. 16 is a graph comparing a response characteristic between a case where a driving method of the present disclosure is applied and a case where a driving method of the prior art is applied.

[Detailed Description Of The Preferred Embodiment]

[0013] Hereinafter, an OLED display device and a method for driving the same according to an exemplary embodiment of the present disclosure will be described in detail with reference to the accompanying drawings.

[0014] A thin film transistor (TFT) employed in the present disclosure may be of a P type or an N type. In the following exemplary embodiment, there will be described a case where a TFT is of an N type, for convenience in explanation. In this regard, a gate high voltage VGH is a gate-on voltage to turn on a TFT, and a gate low voltage VGL is a gate-off voltage to turn off a TFT. In explaining pulse type signals, a gate high voltage (VGH) state is defined as a "high state", and a gate low voltage (VGL) state is defined as a "low state".

[0015] FIG. 1 is a configuration view of an OLED display device according to an exemplary embodiment of the present disclosure.

[0016] As illustrated in FIG. 1, the OLED display device includes a display panel 2 including a plurality of pixels P defined in accordance with intersection of a plurality of gate lines GL and a plurality of data lines DL, a gate driver 4 for driving the plurality of gate lines GL, a data driver 6 for driving the plurality of data lines DL, and a timing controller 8 for arranging image data RGB input from the outside, supplying the arranged image data RGB to the

data driver 6, and outputting gate control signals GCS and data control signals DCS to control the gate driver 4 and data driver 6.

[0017] Each pixel P includes an OLED and a pixel driving circuit including a driving TFT DT configured to supply a drive current to the OLED. Each pixel driving circuit independently drives the OLEDs of the respective pixels P. Further, the pixel driving circuit is configured to compensate for a characteristic deviation between the driving TFTs DTs and compensate for a voltage drop of a high-potential voltage VDD. Thus, it is possible to reduce a luminance deviation between the pixels P. The pixels P according to the present disclosure will be described in detail with reference to FIGS. 2 to 6.

[0018] The display panel 2 includes the plurality of gate lines GL and the plurality of data lines DL intersecting each other. The pixels P are disposed in intersection regions of the gate lines GL and the data lines DL.

[0019] The gate driver 4 supplies a plurality of gate signals to the plurality of gate lines GL in response to a plurality of gate control signals GCS supplied from the timing controller 8. The plurality of gate signals includes first and second scan signals SCAN1 and SCAN2, and an emission signal EM. These signals are supplied to each pixel P by the plurality of gate lines GL. A high-potential voltage VDD has a higher level than a low-potential voltage VSS. The low-potential voltage VSS may be a ground voltage. An initialization voltage Vinit has a lower level than a threshold voltage of the OLED of each pixel P.

[0020] The data driver 6 converts digital image data RGB input from the timing controller 8 into a data voltage Vdata in response to a plurality of data control signals DCS supplied from the timing controller 8, using a reference gamma voltage. Further, the data driver 6 supplies the converted data voltage Vdata to the plurality of data lines DL. Meanwhile, the data driver 6 outputs the data voltage Vdata only in a programming period t3 (refer to FIG. 2) of each pixel P. In a period other than the programming period, the data driver 6 outputs a reference voltage Vref.

[0021] The timing controller 8 aligns the externally input image data RGB so as to be matched to the size and resolution of the display panel 2, and then supplies the aligned image data to the data driver 6. The timing controller 8 generates a plurality of gate control signals GCS and a plurality of data control signals DCS by using synchronization signals SYNC input from the outside, for example, a dot clock DCLK, a data enable signal DE, a horizontal synchronization signal Hsync, and a vertical synchronization signal Vsync. Further, the timing controller 8 supplies the generated gate control signals GCS and data control signals DCS to the gate driver 4 and data driver 6, respectively, in order to control the gate driver 4 and data driver 6.

[0022] Hereinafter, each pixel P according to an exemplary embodiment of the present disclosure will be described in more detail with reference to FIG. 2 to FIG. 4.

[0023] Referring to FIG. 2, each pixel P according to an exemplary embodiment of the present disclosure operates in a plurality of periods divided into an initialization period t1, a sampling period t2, a programming period t3, a holding period t4, and an emission period t5, in response to pulse timings of a plurality of gate signals supplied to the pixel P.

[0024] The initialization period t1 may include a first initialization period t11. In the first initialization period t11, a voltage difference between a gate node (a first node N1 in FIG. 3) and a source node (a second node N2 in FIG. 3) of a driving TFT in the pixel P has a higher value than a threshold voltage of the driving TFT. For example, as for the pixel P driven by the pixel driving circuit according to a circuit diagram of FIG. 3, in the first initialization period t11, when the first scan signal SCAN1 is output at a high state, the second scan signal SCAN2 may be output at a high state and then output at a low state, and the emission signal EM may be output at a low state at the same time.

[0025] Meanwhile, although not illustrated in FIG. 2, the initialization period t1 may include a second initialization period t12 in addition to the first initialization period t11. In the second initialization period t12, a voltage applied between an anode and a cathode of the OLED has a lower value than a threshold driving voltage of the OLED. Herein, the threshold driving voltage of the OLED means a minimum voltage for driving the OLED. The threshold driving voltage of the OLED is an eigen value of the OLED depending on a design of the OLED (a kind of a material, an interfacial characteristic, a thickness, and the like). When the first initialization period t11 does not arrive yet, the second initialization period t12 may start. For example, as for the pixel P driven by the pixel driving circuit according to the circuit diagram of FIG. 3, in the second initialization period t12, when the first scan signal SCAN1 is output at a low state, the second scan signal SCAN2 may be output at a high state and the emission signal EM may be output at a low state at the same time.

[0026] In the sampling period t2, a threshold voltage of the driving TFT in the pixel P is sensed or sampled. For example, as for the pixel P driven by the pixel driving circuit according to the circuit diagram of FIG. 3, in the sampling period t2, the first scan signal SCAN1 and emission signal EM may be output at a high state and the second scan signal SCAN2 may be output at a low state at the same time.

[0027] In the programming period t3, the pixel P writes data to a capacitor. For example, as for the pixel P driven by the pixel driving circuit according to the circuit diagram of FIG. 3, in the programming period t3, the first scan signal SCAN1 may be output at a high state and the second scan signal SCAN2 and emission signal EM may be output at a low state at the same time.

[0028] The holding period t4 is a period between the programming period t3 and the emission period t5. For example, as for the pixel P driven by the pixel driving

circuit according to the circuit diagram of FIG. 3, in the holding period t_4 , all of the first scan signal SCAN1, the second scan signal SCAN2, and the emission signal EM may be output at a low state.

[0029] In the emission period t_5 , the pixel P is supplied with a current corresponding to the written data and emits light. For example, as for the pixel P driven by the pixel driving circuit according to the circuit diagram of FIG. 3, in the emission period t_5 , the emission signal EM may be output at a high state and the first and second scan signals SCAN1 and SCAN2 may be output at a low state.

[0030] Meanwhile, the data driver 6 supplies data voltage Vdata to the plurality of data lines DL in sync with the programming period t_3 of each pixel P. In periods other than the programming period t_3 , the data driver 6 supplies a reference voltage Vref to the plurality of data lines DL.

[0031] Referring to FIG. 3, each pixel P includes an OLED and a pixel driving circuit including four TFTs and two capacitors, to drive the OLED. To be specific, the pixel driving circuit includes a driving TFT DT, first to third TFTs T1 to T3, and first and second capacitors C1 and C2.

[0032] The driving TFT DT is connected in series between the VDD supply line and the VSS supply line, together with the OLED. In the emission period t_5 , the driving TFT DT supplies a drive current to the OLED.

[0033] The first TFT T1 is turned on or off in response to the first scan signal SCAN1. When the first TFT T1 is turned on, the data line DL is connected with a first node N1 connected with a gate of the driving TFT DT. The first TFT T1 supplies, to the first node N1, the reference voltage Vref supplied from the data line DL in the initialization period t_1 and sampling period t_2 . Further, in the programming period t_3 , the driving TFT DT supplies, to the first node N1, the data voltage Vdata supplied from the data line DL.

[0034] The second TFT T2 is turned on or off in response to the second scan signal SCAN2. When the second TFT T2 is turned on, the initialization voltage (Vinit) supply line is connected with a second node N2 connected with a source of the driving TFT DT. The second TFT T2 supplies, to the second node N2, the initialization voltage Vinit supplied from the Vinit supply line in the initialization period t_1 .

[0035] The third TFT T3 is turned on or off in response to the emission signal EM. When the third TFT T3 is turned on, the high-potential voltage (VDD) supply line is connected with a drain of the driving TFT DT. In the sampling period t_2 and emission period t_5 , the third TFT T3 supplies, to the drain of the driving TFT DT, the high-potential voltage VDD supplied from the VDD supply line.

[0036] The first capacitor C1 is disposed between the first node N1 and the second node N2 so as to connect the first node N1 with the second node N2. The first capacitor C1 stores the threshold voltage Vth of the driving TFT DT in the sampling period t_2 .

[0037] The second capacitor C2 is disposed between

the Vinit supply line and the second node N2 so as to connect the Vinit supply line with the second node N2. The second capacitor C2 is connected to the first capacitor C1 in series and thus relatively reduces a capacity ratio of the first capacitor C1. Thus, the second capacitor C2 functions to enhance the luminance of the OLED with respect to the data voltage Vdata applied to the first node N1 in the programming period t_3 . Meanwhile, as illustrated in FIG. 4a, the second capacitor C2 may be disposed between the VDD supply line and the second node N2 so as to connect VDD supply line with the second node N2. Alternatively, as illustrated in FIG. 4b, the second capacitor C2 may be disposed between the VSS supply line and the second node N2 so as to connect the VSS supply line with the second node N2.

[0038] Hereinafter, a method for driving each pixel P according to an exemplary embodiment of the present disclosure will be described with reference to FIGS. 2 and 3.

[0039] First, in the initialization period t_1 (without, for example, the second initialization period t_{12}), the first and second TFTs T1 and T2 are turned on in the first initialization period t_{11} . Then, the reference voltage Vref is supplied to the first node N1 via the first TFT T1, and the initial voltage Vinit is supplied to the second node N2. As a result, the pixel P is initialized. The initialization period t_1 refers to a period before the third TFT T3 is turned on, and in this period, the second TFT T2 is turned off.

[0040] Subsequently, in the sampling period t_2 , the first and third TFTs T1 and T3 are turned on. Then, the first node N1 sustains the reference voltage Vref. And, when the drain of the driving TFT DT is floated, the high-potential voltage VDD is applied to the drain of the driving TFT DT. At the same time, a current flows from the drain toward the source of the driving TFT DT. When a source voltage of the driving TFT DT is equal to "Vref-Vth", the driving TFT DT is turned off. Herein, "Vth" represents the threshold voltage of the driving TFT DT. In this period, the third TFT T3 is turned off.

[0041] Thereafter, in the programming period t_3 , the third TFT T3 is turned off and the first TFT T1 sustains the turn-on state. Then, the data voltage Vdata is supplied to the first node N1 via the first TFT T1 in the turn-on state.

[0042] As a result, the voltage of the second node N2 is changed to "Vref-Vth+C' (Vdata-Vref)" due to a coupling phenomenon caused by voltage distribution according to in-series connection of the first and second capacitors C1 and C2. Herein, "C'" represents " $C1/(C1+C2+C_{oled})$ ". "Coled" represents the capacitance of the OLED. In accordance with the present disclosure, the capacity ratio of the first capacitor C1 is relatively reduced since the second capacitor C2 connected in series with the first capacitor C1 is provided. Accordingly, it is possible to enhance the luminance of the OLED with respect to the data voltage Vdata applied to the first node N1 in the programming period t_3 .

[0043] Then, in the holding period t_4 , no TFT is turned on. That is, the first TFT T1 is turned off and the second

and third TFTs T2 and T3 sustain the turn-off state. As a result, the data voltage Vdata and the threshold voltage written to the pixel P in the programming period t3 are maintained. That is, the holding period t4 refers to a period after the programming period t3 and before the emission period t5.

[0044] Subsequently, in the emission period t5, the third TFT T3 is turned on. Then the high-potential voltage VDD is applied to the drain of the driving TFT DT via the third TFT T3. As a result, the driving TFT DT supplies a drive current to the OLED. In this case, the drive current supplied from the driving TFT DT to the OLED is expressed by an expression " $K(V_{data}-V_{ref}-C'(V_{data}-V_{ref}))^2$ ". Referring to this expression, it can be seen that the drive current of the OLED is not influenced by the threshold voltage Vth of the driving TFT DT and the high-potential voltage VDD. Accordingly, it is possible to reduce a luminance deviation between the pixels P by compensating for a driving TFT characteristic deviation in each pixel P and a voltage drop of the high-potential voltage VDD. Meanwhile, in accordance with the present disclosure, it may be possible to compensate for a mobility deviation between the driving TFTs DT by adjusting an ascending time of the emission signal EM transitioning from a low state to a high state at a starting point of the emission period t5.

[0045] The inventors of the present disclosure found that a luminance drop generated when the pixel P is driven by a method of the prior art is caused by a leakage current between the anodes of the adjacent pixels P. This will be described in more detail with reference to FIG. 5a, FIG. 5b, FIG. 6a, and FIG. 6b.

[0046] FIG. 5a is a schematic diagram illustrating an inflow direction of a leakage current introduced to an Nth row unit pixel corresponding to an Nth gate line from pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel while a frame in a display panel of an OLED display device realizes a black image and a next frame realizes a white image.

[0047] FIG. 5b is a graph illustrating a simulation result of a Vgs value in an Nth row unit pixel corresponding to an Nth gate line while a frame in a display panel of an OLED display device realizes a black image and a next frame realizes a white image.

[0048] FIG. 6a is a schematic diagram illustrating an inflow direction of a leakage current introduced to an Nth row unit pixel corresponding to an Nth gate line from pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel while a frame in a display panel of an OLED display device realizes a white image and a next frame also realizes a white image.

[0049] FIG. 6b is a graph illustrating a simulation result of a Vgs value in an Nth row unit pixel corresponding to an Nth gate line while a frame in a display panel of an OLED display device realizes a white image and a next frame also realizes a white image.

[0050] An Nth row unit pixel shares a hole injection layer and a hole transporting layer of an organic light

emitting layer as a so-called common layer with adjacent pixel lines (for example, an N-1th row unit pixel and an N+1th row unit pixel and their subsequent adjacent pixel lines).

[0051] Meanwhile, while data are written to the Nth row unit pixel, row unit pixels (for example, N-1th and N-2th row unit pixels) before the Nth row unit pixel display an image corresponding to data desired to be displayed on a corresponding frame, and row unit pixels (for example, N+1th and N+2th row unit pixels) after the Nth row unit pixel display an image corresponding to data desired to be displayed on a previous frame. FIG. 5a and FIG. 6a illustrate inflow directions of a leakage current introduced to an Nth row unit pixel from pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel in a case where data are written to the Nth row unit pixel to emit a light in a display panel of an OLED display device. FIG. 5a corresponds to a case where a frame in a display panel realizes a black image and a next frame realizes a white image, and FIG. 6a corresponds to a case where a frame realizes a white image and a next frame also realizes a white image.

[0052] While data are written to the Nth row unit pixel, an anode voltage of the Nth row unit pixel is lowered to be equal to or less than a cathode voltage in order not to allow a current to flow to the OLED. In this case, as compared with a voltage applied to an anode of the Nth row unit pixel, a voltage applied to anodes of adjacent pixel lines is relatively high. Therefore, a voltage difference is generated between the anode of the Nth row unit pixel and the anodes of its adjacent pixel lines.

[0053] To be more specific, referring to FIG. 5a, if a frame of a display panel realizes a black image and a next frame realizes a white frame, an N+1 row unit pixel realizes a black state (i.e., a non-emission state) of the frame, and, thus, an anode voltage is low. However, an N-1th row unit pixel realizes a white state (i.e., an emission state typically with a luminance of 300 nit) of the next frame, and, thus, an anode voltage is relatively higher than the anode voltage of the N+1th row unit pixel. Therefore, a difference between the voltage applied to the anode of the Nth row unit pixel and the voltage applied to the anode of the N+1th row unit pixel is not great. Thus, a leakage current flows in a small amount, whereas a difference between the voltage applied to the anode of the Nth row unit pixel and the voltage applied to the anode of the N-1th row unit pixel is relatively very great, and, thus, a leakage current flows in a large amount. In other words, a large amount of leakage current is introduced from the high-potential anode of the N-1th row unit pixel to the low-potential anode of the Nth row unit pixel via the common layer of the organic light emitting layer. Referring to FIG. 5b, it can be seen that in the programming period t3 of the Nth row unit pixel, a voltage value of the second node is not constant but exhibits a slight increase. Vgs as a voltage difference between the first node (gate node) and the second node (source node) of the driving TFT DT is 3.31 V.

[0054] Meanwhile, referring to FIG. 6a, if a frame of a display panel realizes a white image and a next frame also realizes a white frame, an N+1 row unit pixel and an N-1th row unit pixel are in a white state, and, thus, an anode voltage of the N+1th row unit pixel and an anode voltage of the N-1th row unit pixel are high. Therefore, a difference between the voltage applied to the anode of the Nth row unit pixel and the voltage applied to the anode of the N-1th row unit pixel is great and a difference between the voltage applied to the anode of the Nth row unit pixel and the voltage applied to the anode of the N+1th row unit pixel is also very great. Thus, a large amount of leakage current is introduced from the high-potential anodes of the N-1th and N+1th row unit pixels to the low-potential anode of the Nth row unit pixel (i.e., in a positive direction) via the common layer of the organic light emitting layer. Referring to FIG. 6b, it can be seen that in the programming period t3 of the Nth row unit pixel, a voltage value of the second node is not constant but exhibits a slight increase. In this case, V_{gs} is 3.12 V.

[0055] By comparing FIG. 5b and FIG. 6b, V_{gs} (for example, 3.12 V) in the case where a frame of a display panel realizes a white image and a next frame also realizes a white image is lower than V_{gs} (for example, 3.31 V) in the case where a frame of a display panel realizes a black image and a next frame realizes a white image. That is, it can be seen that an influence of a leakage current is greater in the case where a frame of a display panel realizes a white image and a next frame also realizes a white image as compared with the case where a frame of a display panel realizes a black image (i.e., a non-emission state) and a next frame realizes a white image (i.e., an emission state typically with a luminance of 300 nit). As a result, it can be seen that while data are written to an Nth row unit pixel, when pixel lines adjacent to the Nth row unit pixel are in an emission state, as anode voltages of the adjacent pixel lines increase, an influence of a leakage current increases.

[0056] Meanwhile, when FIG. 5a and FIG. 6a are described, only an influence of N-1th and N+1th row unit pixels most adjacent to an Nth row unit pixel has been described for convenience in explanation. However, actually, the present disclosure is not limited thereto. N-2th and N+2th row unit pixels or N-3th or N+3th row unit pixels also have an influence. In other words, as a pixel line is more adjacent to the Nth row unit pixel, the pixel line has a greater influence on the Nth row unit pixel, and as a pixel line is less adjacent to the Nth row unit pixel, the pixel line has a smaller influence on the Nth row unit pixel.

[0057] The following is the reason why a leakage current flows when there is a voltage difference between anodes of adjacent pixel lines. An Nth row unit pixel shares a hole injection layer and a hole transporting layer of an organic light emitting layer as a so-called common layer with adjacent pixel lines (for example, an N-1th row unit pixel and an N+1th row unit pixel and their subsequent adjacent pixel lines). However, the hole injection

layer and the hole transporting layer of the organic light emitting layer are connected with an anode of an OLED. Therefore, if there is a voltage difference between an anode of the Nth row unit pixel and anodes of its adjacent pixel lines, a current flows through a so-called common layer.

[0058] Such a flow of a leakage current is increased as a resistance of the common layer is decreased. Further, particularly when the common layer is doped with a small amount of impurity in order to improve the element performance of the OLED, a flow of a leakage current is increased. Since the impurity has conductivity, as a doping concentration of the impurity is increased, a resistance of the common layer is decreased, and, thus, a larger amount of leakage current is generated. If a doping concentration is lowered in consideration of a leakage current, it is impossible to improve the element performance of the OLED.

[0059] In other words, in order to minimize inflow of a leakage current, an increase in resistance may be considered. However, such an approach may deteriorate the element performance of an OLED.

[0060] Thus, the inventors of the present disclosure conceived a method for driving an OLED display device, which solves a leakage current problem simply by manipulating a method for driving a pixel driving circuit without undergoing any modification in a structure of an OLED element or a structure of the pixel driving circuit. This will be described in detail below. Herein, application of the concept of the present disclosure in which when the Nth row unit pixel is in a programming period t3, a voltage of an anode of each pixel is controlled in order for other adjacent row unit pixels to realize a non-emission state is not limited in the kind of a pixel driving circuit.

[0061] FIGS. 7, 9, 11, and 13 are schematic diagrams illustrating that when an Nth row unit pixel corresponding to an Nth gate line in a display panel of an OLED display device is in a sampling period t2 or a programming period t3, pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel is in an emission state according to an exemplary embodiment of the present disclosure.

[0062] FIGS. 8a, 8b, 10a, 10b, 12a, 12b, 14a, and 14b respectively corresponding to FIGS. 7, 9, 11, and 13 are driving waveform diagrams illustrating a driving method of an Nth row unit pixel corresponding to an Nth gate line in a display panel of an OLED display device and pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel according to an exemplary embodiment of the present disclosure.

[0063] At a time when an Nth row unit pixel corresponding to an Nth gate line in a display panel of an OLED display device moves on from a frame to a next frame, if an Nth row unit pixel is driven in the sampling period t2 or in the programming period t3, a voltage which is lower than a voltage applied to a cathode of an OLED is applied to a second node. That is, a voltage lower than a cathode voltage is applied to the anode of the OLED

in the Nth row unit pixel. Therefore, the Nth row unit pixel is in a non-emission state in the sampling period t2 or in the programming period t3. In this case, adjacent pixel lines are set to be in a non-emission state, and, thus, a leakage current introduced from the adjacent pixel lines (or adjacent row unit pixels) to the Nth row unit pixel is minimized. To be more specific, when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, anode voltages of the adjacent pixel lines are set to be equal to or less than an anode voltage of the Nth row unit pixel in order to suppress a voltage difference. Thus, a leakage current introduced from the adjacent pixel lines to the Nth row unit pixel is minimized. According to this method, for example, when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, (1) an N-1th row unit pixel is in the holding period t4, (2) an N+1th row unit pixel is in any one of the first initialization period t11 and the second initialization period t12, or in the first initialization period t11 and the second initialization period t12.

[0064] FIG. 7 illustrates a case where when an Nth row unit pixel is in the sampling period t2 or in the programming period t3, N-1th and N+1th row unit pixels among its adjacent pixel lines are in a non-emission state. Herein, a dotted arrow indicates an inflow route of a leakage current. Although FIG. 7 illustrates a line comprised of six pixels and five lines including an Nth line and previous and next two lines most adjacent to the Nth line, it is obvious that such illustration is provided only for convenience in explanation and a configuration of lines and columns is not limited thereto.

[0065] To be more specific, when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, (1) the N-1th row unit pixel is in the holding period t4, (2) the N+1th row unit pixel is in any one of the first initialization period t11 and the second initialization period t12, or in the first initialization period t11 and the second initialization period t12.

[0066] FIG. 8a and FIG. 8b are driving waveform diagrams illustrating a driving method of an Nth row unit pixel and pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel. FIG. 8a and FIG. 8b are driving waveform diagrams for driving a display panel as illustrated in FIG. 7 if a pixel P adopts a 4T2C structure illustrated in FIG. 3 as a pixel driving circuit. This is just an example. The driving method according to an exemplary embodiment of the present disclosure as illustrated in FIG. 7 can also be applied to a pixel driving circuit of any other structure which drives a display panel as illustrated in FIG. 7 and operates in the initialization period t1, the sampling period t2, the programming period t3, the holding period t4, and the emission period t5 as described with reference to FIG. 2.

[0067] Referring to FIG. 8a, a driving timing may be controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, the N-1th row unit pixel is in the holding period t4 and the N+1th row unit pixel is in the second initialization period

t12.

[0068] Here, the first initialization period t11, in which a voltage difference between the first node N1 and the second node N2 of the driving TFT DT is higher than a threshold voltage of the driving TFT DT, corresponds to a period from when a TFT configured to allow the first scan signal SCAN1 to flow and a TFT configured to allow the second scan signal SCAN2 to flow are turned on at the same time to before a TFT configured to allow the EM signal EM to flow is turned on. In this case, the TFT configured to allow the second scan signal SCAN2 to flow may be turned off before the TFT configured to allow the EM signal EM to flow is turned on or may be turned off at the same time as when the TFT configured to allow the EM signal EM to flow is turned on.

[0069] Further, the second initialization period t12, in which a voltage between an anode and a cathode of the OLED is lower than an OLED threshold driving voltage, corresponds to a period from when the TFT configured to allow the second scan signal SCAN2 to flow is turned on to before the TFT configured to allow the first scan signal SCAN1 to flow is turned on. The second initialization period t12 may be present earlier in time than the first initialization period t11, but cannot be present later in time than the first initialization period t11. That is, it is possible to drive from the second initialization period t12 to the first initialization period t11, but impossible to drive from the first initialization period t11 to the second initialization period t12. The same explanation for the first initialization period t11 and the second initialization period t12 applies to FIGS. 10, 12, and 14.

[0070] That is, referring to FIG. 8a, a driving timing may be controlled such that the second initialization period t12 starts earlier than the first initialization period t11 in each pixel P constituting a display panel of an OLED display device.

[0071] Referring to FIG. 8b, a driving timing may be controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, the N-1th row unit pixel is in the holding period t4 and the N+1th row unit pixel is in the first initialization period t11. In other words, a driving timing may be controlled such that each pixel P constituting a display panel of an OLED display device goes through the first initialization period t11 without the second initialization period t12.

[0072] If each pixel P constituting a display panel of an OLED display device goes through the second initialization period t12 between the emission period t5 and the first initialization period t11, a voltage (for example, an initialization voltage Vinit) lower than the threshold voltage of the driving TFT DT is already applied to the second node N2 of the driving TFT DT in the pixel before the first initialization period t11. As compared with (1) a case where each pixel P constituting a display panel of an OLED display device goes through only the first initialization period t11 as the initialization period t1, in (2) a case where the pixel P goes through the second initialization period t12 in addition to the first initialization period

t11 as the initialization period t1, a period in which an anode voltage is lower than a voltage applied to the driving TFT DT is increased by the second initialization period t12. Thus, it is possible to effectively suppress inflow of a leakage current to an Nth row unit pixel.

[0073] If a pixel P adopts a 4T2C structure illustrated in FIG. 3 as a pixel driving circuit, the first initialization period t11 and the second initialization period t12 cannot be completely overlapped in time. However, if a pixel P adopts a pixel driving circuit of another structure, the first initialization period t11 and the second initialization period t12 may be completely overlapped in time, i.e., the initialization period t1 may be the first initialization period t11 or the second initialization period t12. That is, the first initialization period t11 and the second initialization period t12 may start and end at the same time. In other words, each pixel P may be driven such that an anode voltage of an OLED is lower than an OLED driving voltage while a voltage difference between a gate node and a source node of a driving TFT in each pixel P is higher than a threshold voltage of the driving TFT.

[0074] Then, FIG. 9 illustrates a case where when an Nth row unit pixel is in the sampling period t2 or in the programming period t3, N-1th, N+1th, and N+2 row unit pixels among its adjacent pixel lines are in a non-emission state. Herein, a dotted arrow indicates an inflow route of a leakage current. Although FIG. 9 illustrates a line comprised of six pixels and five lines including an Nth line and previous and next two lines most adjacent to the Nth line, it is obvious that such illustration is provided only for convenience in explanation and a configuration of lines and columns is not limited thereto.

[0075] To be more specific, when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, (1) the N-1th row unit pixel is in the holding period t4, (2) the N+1th row unit pixel and the N+2th row unit pixel are in any one of the first initialization period t11 and the second initialization period t12, or in the first initialization period t11 and the second initialization period t12.

[0076] FIG. 10a and FIG. 10b are driving waveform diagrams illustrating a driving method of an Nth row unit pixel and pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel. FIG. 10a and FIG. 10b are driving waveform diagrams for driving a display panel as illustrated in FIG. 9 if a pixel P adopts a 4T2C structure illustrated in FIG. 3 as a pixel driving circuit. That is, this is just an example, and the driving method according to an exemplary embodiment of the present disclosure as illustrated in FIG. 9 can also be applied to a pixel driving circuit of any other structure which drives a display panel as illustrated in FIG. 9 and operates in the first initialization period t11, the second initialization period t12, the initialization period t1, the sampling period t2, the programming period t3, the holding period t4, and the emission period t5 as described with reference to FIG. 2.

[0077] Referring to FIG. 10a, a driving timing may be controlled such that when the Nth row unit pixel is in the

sampling period t2 or in the programming period t3, the N-1th row unit pixel is in the holding period t4 and all of the N+1th and N+2th row unit pixels are in the second initialization period t12.

[0078] That is, a driving timing may be controlled such that each pixel P constituting a display panel of an OLED display device goes through the second initialization period t12 over two horizontal periods 2H. Herein, a horizontal period 1H refers to a period obtained by dividing a period allotted for displaying a single frame by M if a display panel is comprised of M gate lines GL to display the single frame. The two horizontal periods 2H are twice the horizontal period 1H.

[0079] Further, referring to FIG. 10a, a driving timing may be controlled such that the second initialization period t12 of the Nth row unit pixel constituting a display device of an OLED display device to start before writing the sampling period t2 of the N-1th row unit pixel.

[0080] Otherwise, referring to FIG. 10a, a driving timing may be controlled such that the second initialization period t12 starts earlier than the first initialization period t11 in each pixel P constituting a display panel of an OLED display device. However, in any case, the first initialization period t11 does not end earlier than the second initialization period t12.

[0081] Referring to FIG. 10b, a driving timing may be controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, the N-1th row unit pixel is in the holding period t4 and all of the N+1th and N+2th row unit pixels are in the first initialization period t11.

[0082] That is, referring to FIG. 10b, a driving timing may be controlled such that each pixel P constituting a display panel of an OLED display device goes through the first initialization period t11 over the two horizontal periods 2H.

[0083] Further, referring to FIG. 10b, a driving timing may be controlled such that the first initialization period t11 of the Nth row unit pixel constituting a display panel of an OLED display device to start before writing the sampling period t2 of the N-1th row unit pixel.

[0084] Otherwise, referring to FIG. 10b, a driving timing may be controlled such that each pixel P constituting a display panel of an OLED display device goes through only the first initialization period t11.

[0085] If a 4T2C structure illustrated in FIG. 3 is adopted as a pixel driving circuit, the first initialization period t11 and the second initialization period t12 cannot be completely overlapped in time. However, if a pixel driving circuit of another structure is adopted, the first initialization period t11 and the second initialization period t12 may be completely overlapped in time, i.e., the initialization period t1 may be the first initialization period t11 or the second initialization period t12. That is, the first initialization period t11 and the second initialization period t12 may start and end at the same time. In other words, each pixel P may be driven such that an anode voltage of an OLED is lower than an OLED driving voltage while

a voltage difference between a gate node and a source node of a driving TFT in each pixel P is higher than a threshold voltage of the driving TFT.

[0086] Then, FIG. 11 illustrates a case where when an Nth row unit pixel is in the sampling period t2 or in the programming period t3, N-1th, N-2th, and N+1 row unit pixels among its adjacent pixel lines are in a non-emission state. Herein, a dotted arrow indicates an inflow route of a leakage current. Although FIG. 11 illustrates a line comprised of six pixels and five lines including an Nth line and previous and next two lines most adjacent to the Nth line, it is obvious that such illustration is provided only for convenience in explanation and a configuration of lines and columns is not limited thereto.

[0087] To be more specific, when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, (1) the N-2th and N-1th row unit pixels are in the holding period t4, (2) the N+1th row unit pixel is in any one of the first initialization period t11 and the second initialization period t12, or in the first initialization period t11 and the second initialization period t12.

[0088] FIG. 12a and FIG. 12b are driving waveform diagrams illustrating a driving method of an Nth row unit pixel and pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel. FIG. 12a and FIG. 12b are driving waveform diagrams for driving a display panel as illustrated in FIG. 11 if a pixel P adopts a 4T2C structure illustrated in FIG. 3 as a pixel driving circuit. That is, this is just an example, and the driving method according to an exemplary embodiment of the present disclosure as illustrated in FIG. 11 can also be applied to a pixel driving circuit of any other structure which drives a display panel as illustrated in FIG. 11 and operates in the first initialization period t11, the second initialization period t12, the initialization period t1, the sampling period t2, the programming period t3, the holding period t4, and the emission period t5 as described with reference to FIG. 2.

[0089] Referring to FIG. 12a, a driving timing may be controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, the N-2th and N-1th row unit pixels are in the holding period t4 and the N+1th row unit pixel is in the second initialization period t12.

[0090] That is, referring to FIG. 12a, a driving timing may be controlled such that the second initialization period t12 starts earlier than the first initialization period t11 in each pixel P constituting a display panel of an OLED display device. However, in any case, the first initialization period t11 does not end earlier than the second initialization period t12.

[0091] Referring to FIG. 12b, a driving timing may be controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, the N-2th and N-1th row unit pixels are in the holding period t4 and the N+1th row unit pixel is in the first initialization period t11.

[0092] That is, referring to FIG. 12b, a driving timing

may be controlled such that each pixel P constituting a display panel of an OLED display device goes through only the first initialization period t11.

[0093] If a pixel P adopts a 4T2C structure illustrated in FIG. 3 as a pixel driving circuit, the first initialization period t11 and the second initialization period t12 cannot be completely overlapped in time, but if a pixel P adopts a pixel driving circuit of another structure, the first initialization period t11 and the second initialization period t12 may be completely overlapped in time, i.e., the initialization period t11 may be the first initialization period t11 or the second initialization period t12. That is, the first initialization period t11 and the second initialization period t12 may start and end at the same time. In other words, each pixel P may be driven such that an anode voltage of an OLED is lower than an OLED driving voltage while a voltage difference between a gate node and a source node of a driving TFT in each pixel P is higher than a threshold voltage of the driving TFT.

[0094] Then, FIG. 13 illustrates a case where when an Nth row unit pixel is in the sampling period t2 or in the programming period t3, N-1th, N-2th, N+1th, and N+2th row unit pixels among its adjacent pixel lines are in a non-emission state. Herein, a dotted arrow indicates an inflow route of a leakage current. Although FIG. 13 illustrates a line comprised of six pixels and five lines including an Nth line and previous and next two lines most adjacent to the Nth line, it is obvious that such illustration is provided only for convenience in explanation and a configuration of lines and columns is not limited thereto.

[0095] To be more specific, when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, (1) the N-2th and N-1th row unit pixels are in the holding period t4, (2) the N+1th and N+2th row unit pixels are in any one of the first initialization period t11, the second initialization period t12, and the initialization period t1, or in the first initialization period t11 and the second initialization period t12.

[0096] FIG. 14a and FIG. 14b are driving waveform diagrams illustrating a driving method of an Nth row unit pixel and pixel lines (for example, N-2th, N-1th, N+1th, and N+2th row unit pixels) adjacent to the Nth row unit pixel. FIG. 14a and FIG. 14b are driving waveform diagrams for driving a display panel as illustrated in FIG. 13 if a pixel P adopts a 4T2C structure illustrated in FIG. 3 as a pixel driving circuit. That is, this is just an example, and the driving method according to an exemplary embodiment of the present disclosure as illustrated in FIG. 13 can also be applied to a pixel driving circuit of any other structure which drives a display panel as illustrated in FIG. 13 and operates in the first initialization period t11, the second initialization period t12, the initialization period t1, the sampling period t2, the programming period t3, the holding period t4, and the emission period t5 as described with reference to FIG. 2.

[0097] Referring to FIG. 14a, a driving timing may be controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, the

N-2th and N-1th row unit pixels are in the holding period t4 and the N+1th and N+2th row unit pixels are in the second initialization period t12.

[0098] That is, referring to FIG. 14a, a driving timing may be controlled such that each pixel P constituting a display panel of an OLED display device goes through the holding period t4 over two horizontal periods 2H.

[0099] Further, referring to FIG. 14a, a driving timing may be controlled such that the second initialization period t12 starts earlier than the first initialization period t11 in each pixel P constituting a display panel of an OLED display device. However, in any case, the first initialization period t11 does not end earlier than the second initialization period t12.

[0100] Furthermore, referring to FIG. 14a, a driving timing may be controlled such that each pixel P constituting a display panel of an OLED display device goes through the second initialization period t12 over the two horizontal periods 2H.

[0101] Referring to FIG. 14b, a driving timing may be controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, the N-2th and N-1th row unit pixels are in the holding period t4 and the N+1th and N+2th row unit pixels are in the first initialization period t11.

[0102] That is, referring to FIG. 14b, a driving timing may be controlled such that each pixel constituting a display panel of an OLED display device goes through the holding period t4 over the two horizontal periods 2H.

[0103] Otherwise, referring to FIG. 14b, a driving timing may be controlled such that each pixel constituting a display panel of an OLED display device goes through only the first initialization period t11.

[0104] Further, referring to FIG. 14b, a driving timing may be controlled such that each pixel constituting a display panel of an OLED display device goes through the first initialization period t11 over the two horizontal periods 2H.

[0105] If a 4T2C structure illustrated in FIG. 3 is adopted as a pixel driving circuit, the first initialization period t11 and the second initialization period t12 cannot be completely overlapped in time. However, if a pixel driving circuit of another structure is adopted, the first initialization period t11 and the second initialization period t12 may be completely overlapped in time, i.e., the initialization period t1 may be the first initialization period t11 or the second initialization period t12. That is, the first initialization period t11 and the second initialization period t12 may start at the same time and end at the same time. In other words, each pixel P may be driven such that an anode voltage of an OLED is lower than an OLED driving voltage while a voltage difference between a gate node and a source node of a driving TFT in each pixel P is higher than a threshold voltage of the driving TFT.

[0106] In short, when an Nth row unit pixel constituting a display panel of an OLED display device is in the sampling period t2 or in the programming period t3, pixel lines adjacent to the Nth row unit pixel are set to be in a non-

emission state. Thus, anode voltages of the adjacent pixel lines are set to be equal to or less than an anode voltage of the Nth row unit pixel, so that a leakage current introduced from the adjacent pixel lines to the Nth row unit pixel is minimized. In order to do so, a driving timing is controlled such that when the Nth row unit pixel is in the sampling period t2 or in the programming period t3, at least one of the previous row unit pixels (for example, N-1th, N-2th, and N-3th row unit pixels) adjacent to the Nth row unit pixel is in the holding period t4 and at least one of the next adjacent row unit pixels (for example, N+1th, N+2th, and N+3th row unit pixels) adjacent to the Nth row unit pixel is in any one of the first initialization period t11 or the second initialization period t12, or in the first initialization period t11 and the second initialization period t12.

[0107] Next, FIG. 15 is a graph comparing an I-V curve between a case where a pixel driving circuit configured according to a circuit diagram of FIG. 3 is driven by a driving method of the prior art (hereinafter, referred to as "prior art") and a case where the pixel driving circuit is driven by a driving method of an OLED display device of the present disclosure as illustrated in FIG. 7, according to the driving waveform diagram of FIG. 8a (hereinafter, referred to as "present disclosure").

[0108] It can be seen from FIG. 15 that when the same data driving voltage is applied, a higher current flows to the OLED in the present disclosure as compared with the prior art. Under the same data driving voltage condition, as a current flowing to the OLED is increased, a luminance is increased. This means that as compared with the prior art, in the present disclosure, even when a relatively low data driving voltage is applied, an equivalent luminance can be achieved. Thus, according to the present disclosure, it is possible to increase a margin of a data driving voltage.

[0109] Next, FIG. 16 is a graph comparing a response characteristic between a case where a driving method of the present disclosure is applied and a case where a driving method of the prior art is applied when a display panel including a pixel driving circuit configured according to a circuit diagram of FIG. 3 starts from a state where a black image is realized. Then it realizes a white image in a first frame, realizes a white image in a second frame, and realizes a white image in a third frame.

[0110] Referring to FIG. 16, it can be seen that in the prior art, the luminance of the second frame and the third frame in which a white image is converted into a white image is lower than the luminance of the first frame in which a black image is converted into a white image. That is, the three frames displaying the same image are different in luminance depending on images displayed in their respective previous frames. However, it can be seen that in the present disclosure, the luminance of the first frame is not different from the luminance of the second frame and the third frame and has an equivalent luminance. That is, it can be seen that the three frames displaying the same image have a constant and stable luminance

regardless of images displayed in their respective previous frames.

[0111] In an OLED display device according to an exemplary embodiment of the present disclosure, when an Nth row unit pixel is in a sampling period or a programming period, at least one row unit pixel of a previous row unit pixel or a next row unit pixel adjacent to the Nth row unit pixel is in any one of a holding period from after completion of writing data voltage to each of the at least one row unit pixel to before each of the at least one row unit pixel emits light, a first initialization period in which a voltage of an anode of an OLED included in each of the at least one row unit pixel has a lower value than an OLED driving voltage, and a second initialization period in which a voltage difference between a gate node and a source node of a driving element that regulates an OLED driving voltage applied to an OLED included in each of the at least one row unit pixel has a higher value than a threshold voltage of the driving element, or in the first initialization period and the second initialization period.

[0112] As another feature of the OLED display device according to an exemplary embodiment of the present disclosure, when the Nth row unit pixel is in a sampling period or a programming period, the previous row unit pixel adjacent to the Nth row unit pixel is in a holding period.

[0113] As yet another feature of the OLED display device according to an exemplary embodiment of the present disclosure, when the Nth row unit pixel is in a sampling period or a programming period, the next row unit pixel adjacent to the Nth row unit pixel is in a second initialization period.

[0114] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, in the Nth row unit pixel, a second initialization period starts earlier than a first initialization period.

[0115] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, in the Nth row unit pixel, a first initialization period and a second initialization period start at the same time.

[0116] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, when the previous row unit pixel adjacent to the Nth row unit pixel is in a sampling period, a first initialization period or a second initialization period starts in the Nth row unit pixel.

[0117] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, when an N-1th or N-2th row unit pixel is in a sampling period, a first initialization period or a second initialization period starts in the Nth row unit pixel.

[0118] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, in the Nth row unit pixel, a first initialization period and a second initialization period end at the same time.

[0119] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, a first initialization period or a second initialization period of the Nth row unit pixel starts before a sampling period of an N-1th row unit pixel.

[0120] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, the Nth row unit pixel goes through the first initialization period t11 over two horizontal periods 2H, the second initialization period t12 over two horizontal periods 2H, or the holding period t4 over two horizontal periods 2H.

[0121] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, when the Nth row unit pixel is in a sampling period or a programming period, an N-1th row unit pixel and an N-2th row unit pixel are in a holding period.

[0122] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, the OLED is a light emitting element and each of a plurality of pixels includes a pixel driving circuit that drives the light emitting element. The pixel driving circuit includes: the driving element connected in series between a high-potential voltage supply line and a low-potential voltage supply line, together with the light emitting element; a first switching element that connects a data line with a first node connected with a gate of the driving element in response to a first scan signal; a second switching element that connects an initialization voltage supply line with a second node connected with a source of the driving element in response to a second scan signal; a third switching element that connects the high-potential voltage supply line with a drain of the driving element in response to an emission signal; and a first capacitor connected between the first node and the second node, and the pixel driving circuit operates in a period divided into an initialization period in which when the third switching element is in an off state, the pixel driving circuit turns on the first and second switching elements, to initialize the first and second nodes, a sampling period in which the pixel driving circuit turns on the first and third switching elements, to sense a threshold voltage of the driving element, a programming period in which when the third switching element is in an off state, the pixel driving circuit turns on the first switching element, to write a data voltage to the pixel, a holding period from after completion of writing of a data voltage to the pixel to before the pixel emits a light, and an emission period in which the pixel driving circuit turns on the third switching element, to cause the driving element to supply a drive current to the light emitting element.

[0123] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, the initialization period includes a first initialization period or a second initialization period. The first initialization period is a period from when the first switching element and the second switching element are

turned on in response to a first scan signal and a second scan signal, respectively, to before the third switching element is turned on in response to an emission signal. The second initialization period is a period in which the second switching element is turned on in response to the second scan signal before the first switching element is turned on in response to the first scan signal.

[0124] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, in the first initialization period, before the third switching element is turned on in response to the emission signal, the second switching element is turned off in response to the second scan signal. Or when the third switching element is turned on in response to the emission signal, the second switching element is turned off in response to the second scan signal.

[0125] An OLED display device according to an exemplary embodiment of the present disclosure includes a circuit that controls a voltage of an Nth row unit pixel and a voltage of anodes of pixel lines adjacent to the Nth row unit pixel in order to minimize a voltage difference between the Nth row unit pixel and the pixel lines adjacent to the Nth row unit pixel to suppress a decrease in luminance of the Nth row unit pixel caused by a leakage current introduced to the Nth row unit pixel, and the circuit is configured to set the voltage of the anodes of pixel lines adjacent to the Nth row unit pixel to be equal to or lower than a voltage of an anode of the Nth row unit pixel when the Nth row unit pixel is in the sampling period or the programming period during a driving timing of the OLED display device.

[0126] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, to make a time delay secured between after completion of writing of a data voltage to a pixel and before the pixel emits a light in order for at least one of previous pixel lines adjacent to the Nth row unit pixel to be in a non-emission state when the Nth row unit pixel is in the programming period, control of a voltage of the anode by the circuit is supported by a timing controller, and the timing controller receives image data and synchronization signals from an external source, outputs the image data and a generated data control signal to a data driver through a plurality of data lines, and outputs a generated gate control signal to a gate driver through a plurality of gate lines, and, thus, the holding period is added between the programming period and the emission period during the driving timing of the OLED display device.

[0127] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, to secure a period in which a voltage applied between an anode and a cathode of an OLED of a pixel is lower than a threshold driving voltage of the OLED of the pixel after the pixel emits a light in order for at least one of next pixel lines adjacent to the Nth row unit pixel to be in a non-emission state when the Nth row unit pixel is in the programming period, control of a volt-

age of the anode by the circuit is supported by a timing controller, and the timing controller receives image data and synchronization signals from an external source, outputs the image data and a generated data control signal to a data driver through a plurality of data lines, and outputs a generated gate control signal to a gate driver through a plurality of gate lines, and, thus, an initialization period in which the pixel is initialized during the driving timing of the OLED display device includes a second initialization period, and the second initialization period is a period in which a second switching element connected with an initialization voltage supply line is turned on in response to a second scan signal before a first switching element connected with a data line is turned on in response to a first scan signal.

[0128] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, control of a voltage of the anode by the circuit is supported by a gate driver, and the gate driver receives a gate control signal from a timing controller, and each gate control signal includes a first scan signal, a second scan signal, and an emission signal to be output to each pixel through a plurality of gate lines.

[0129] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, control of a voltage of the anode by the circuit is supported by a data driver, and the data driver receives image data and a data control signal from a timing controller and outputs a converted data voltage to each pixel through a plurality of data lines.

[0130] As still another feature of the OLED display device according to an exemplary embodiment of the present disclosure, control of a voltage of the anode by the circuit is supported by a display panel including a plurality of pixels, and each of the plurality of pixels respectively provided in intersection regions of a plurality of gate lines and a plurality of data lines includes a pixel driving circuit connected with an OLED, a gate line, a data line, a high-potential voltage supply line, a low-potential voltage supply line, and an initialization voltage supply line.

[0131] The present disclosure is not limited to the above-described exemplary embodiment and the accompanying drawings, and it is obvious to those skilled in the art that various substitutions, modifications, and changes can be made without departing from the scope of the present disclosure.

Claims

1. An OLED display device in which when an Nth row unit pixel is in a sampling period or a programming period, at least one row unit pixel of a previous row unit pixel or a next row unit pixel adjacent to the Nth row unit pixel is in any one of a holding period from after completion of writing of a data voltage to each of the at least one row unit pixel to before each of

the at least one row unit pixel emits a light, a first initialization period in which a voltage of an anode of an OLED included in each of the at least one row unit pixel has a lower value than an OLED driving voltage, and a second initialization period in which a voltage difference between a gate node and a source node of a driving element that regulates an OLED driving voltage applied to an OLED included in each of the at least one row unit pixel has a higher value than a threshold voltage of the driving element, or in the first initialization period and the second initialization period.

2. The OLED display device according to claim 1, wherein when the Nth row unit pixel is in the sampling period or the programming period, the previous row unit pixel adjacent to the Nth row unit pixel is in the holding period.
3. The OLED display device according to claim 1, wherein when the Nth row unit pixel is in the sampling period or the programming period, the next row unit pixel adjacent to the Nth row unit pixel is in the second initialization period.
4. The OLED display device according to claim 1, wherein in the Nth row unit pixel, the second initialization period starts earlier than the first initialization period.
5. The OLED display device according to claim 1, wherein in the Nth row unit pixel, the first initialization period and the second initialization period start at the same time.
6. The OLED display device according to claim 1, wherein when the previous row unit pixel adjacent to the Nth row unit pixel is in the sampling period, the first initialization period or the second initialization period starts in the Nth row unit pixel.
7. The OLED display device according to claim 6, wherein when an N-1th or N-2th row unit pixel is in the sampling period, the first initialization period or the second initialization period starts in the Nth row unit pixel.
8. The OLED display device according to claim 5, wherein in the Nth row unit pixel, the first initialization period and the second initialization period end at the same time.
9. The OLED display device according to claim 1, wherein the first initialization period or the second initialization period of the Nth row unit pixel starts before the sampling period of an N-1th row unit pixel.
10. The OLED display device according to claim 1,

wherein the Nth row unit pixel goes through the first initialization period over two horizontal periods, the second initialization period over two horizontal periods, or the holding period over two horizontal periods.

11. The OLED display device according to claim 1, wherein when the Nth row unit pixel is in the sampling period or the programming period, an N-1th row unit pixel and an N-2th row unit pixel are in the holding period.
12. The OLED display device according to claim 1, wherein the OLED is a light emitting element and each of a plurality of pixels includes a pixel driving circuit that drives the light emitting element, and the pixel driving circuit includes:

the driving element connected in series between a high-potential voltage supply line and a low-potential voltage supply line, together with the light emitting element;
 a first switching element that connects a data line with a first node connected with a gate of the driving element in response to a first scan signal;
 a second switching element that connects an initialization voltage supply line with a second node connected with a source of the driving element in response to a second scan signal;
 a third switching element that connects the high-potential voltage supply line with a drain of the driving element in response to an emission signal; and
 a first capacitor connected between the first node and the second node, and
 the pixel driving circuit operates in a period divided into an initialization period in which when the third switching element is in an off state, the pixel driving circuit turns on the first and second switching elements, to initialize the first and second nodes,
 the sampling period in which the pixel driving circuit turns on the first and third switching elements, to sense a threshold voltage of the driving element,
 the programming period in which when the third switching element is in an off state, the pixel driving circuit turns on the first switching element, to write a data voltage to the pixel,
 the holding period from after completion of writing of a data voltage to the pixel to before the pixel emits a light, and
 an emission period in which the pixel driving circuit turns on the third switching element, to cause the driving element to supply a drive current to the light emitting element.

13. The OLED display device according to claim 12, wherein the initialization period includes the first initialization period or the second initialization period, the first initialization period is a period from when the first switching element and the second switching element are turned on in response to a first scan signal and a second scan signal, respectively, to before the third switching element is turned on in response to an emission signal, and the second initialization period is a period in which the second switching element is turned on in response to the second signal before the first switching element is turned on in response to the first scan signal.

14. The OLED display device according to claim 13, wherein in the first initialization period, before the third switching element is turned on in response to the emission signal, the second switching element is turned off in response to the second scan signal, or when the third switching element is turned on in response to the emission signal, the second switching element is turned off in response to the second scan signal.

15. A device comprising:

a circuit that controls a voltage of an Nth row unit pixel and a voltage of anodes of pixel lines adjacent to the Nth row unit pixel in order to minimize a voltage difference between the Nth row unit pixel and the pixel lines adjacent to the Nth row unit pixel to suppress a decrease in luminance of the Nth row unit pixel caused by a leakage current introduced to the Nth row unit pixel, wherein the circuit is configured to set the voltage of the anodes of pixel lines adjacent to the Nth row unit pixel to be equal to or lower than a voltage of an anode of the Nth row unit pixel when the Nth row unit pixel is in the sampling period or the programming period during a driving timing of an OLED display device.

16. The device according to claim 15, wherein to make a time delay secured between after completion of writing of a data voltage to a pixel and before the pixel emits a light in order for at least one of previous pixel lines adjacent to the Nth row unit pixel to be in a non-emission state when the Nth row unit pixel is in the programming period, control of a voltage of the anode by the circuit is supported by a timing controller, and the timing controller receives image data and synchronization signals from an external source, outputs the image data and a generated data control signal to a data driver through a plurality of data lines, and outputs a generated gate control signal to a gate driver through a plurality of gate lines, and, thus, the holding period

is added between the programming period and the emission period during the driving timing of the OLED display device.

17. The device according to claim 15, wherein to secure a period in which a voltage applied between an anode and a cathode of an OLED of a pixel is lower than a threshold driving voltage of the OLED of the pixel after the pixel emits a light in order for at least one of next pixel lines adjacent to the Nth row unit pixel to be in a non-emission state when the Nth row unit pixel is in the programming period, control of a voltage of the anode by the circuit is supported by a timing controller, and the timing controller receives image data and synchronization signals from an external source, outputs the image data and a generated data control signal to a data driver through a plurality of data lines, and outputs a generated gate control signal to a gate driver through a plurality of gate lines, and, thus, an initialization period in which the pixel is initialized during the driving timing of the OLED display device includes a second initialization period, and the second initialization period is a period in which a second switching element connected with an initialization voltage supply line is turned on in response to a second scan signal before a first switching element connected with a data line is turned on in response to a first scan signal.

18. The device according to claim 15, wherein control of a voltage of the anode by the circuit is supported by a gate driver, and the gate driver receives a gate control signal from a timing controller, and each gate control signal includes a first scan signal, a second scan signal, and an emission signal to be output to each pixel through a plurality of gate lines.

19. The device according to claim 15, wherein control of a voltage of the anode by the circuit is supported by a data driver, and the data driver receives image data and a data control signal from a timing controller and outputs a converted data voltage to each pixel through a plurality of data lines.

20. The device according to claim 15, wherein control of a voltage of the anode by the circuit is supported by a display panel including a plurality of pixels, and each of the plurality of pixels respectively provided in intersection regions of a plurality of gate lines and a plurality of data lines includes a pixel driving circuit connected with an OLED, a gate line, a data line, a high-potential voltage supply line, a low-potential voltage supply line, and an initialization voltage supply line.

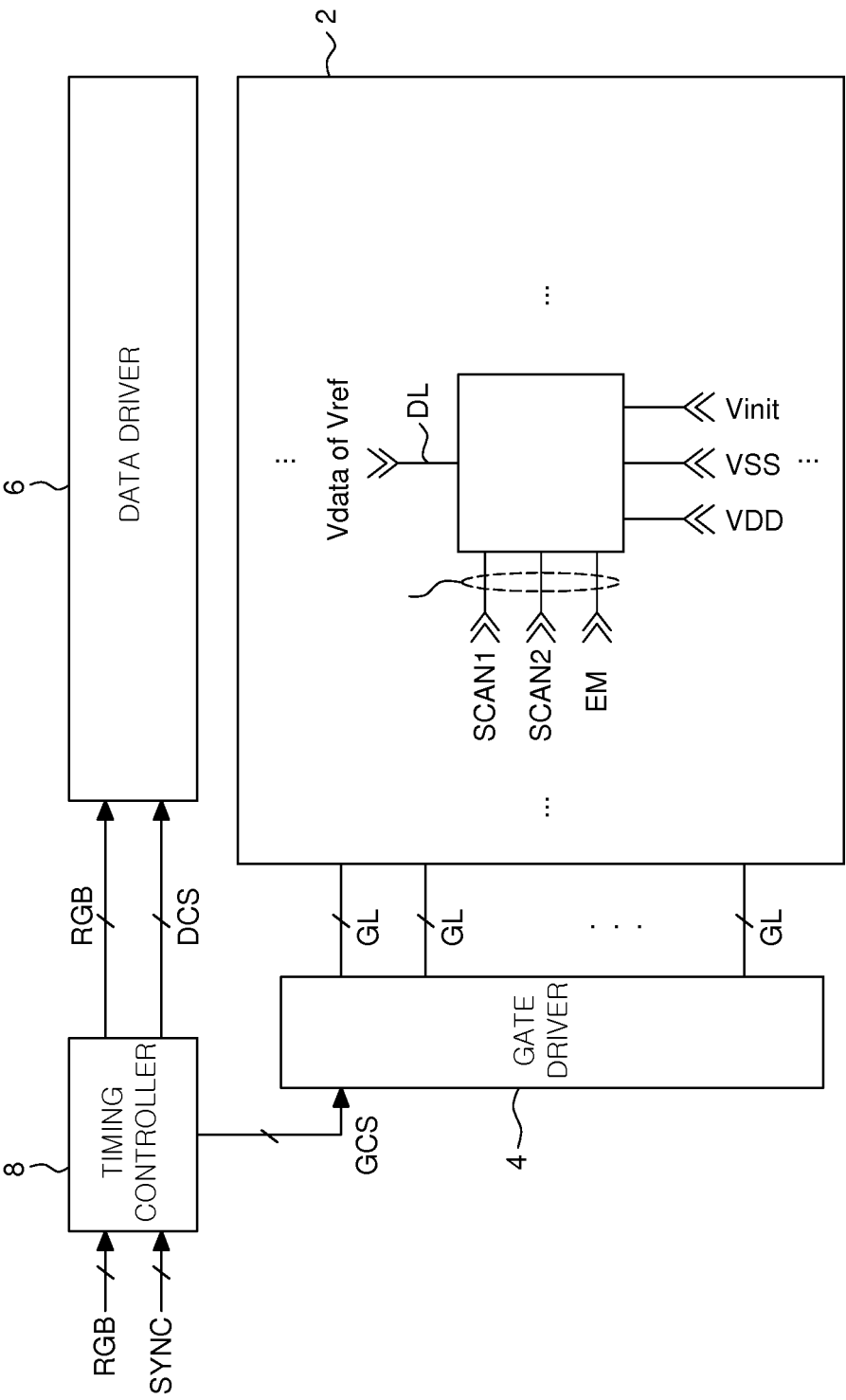


FIG. 1

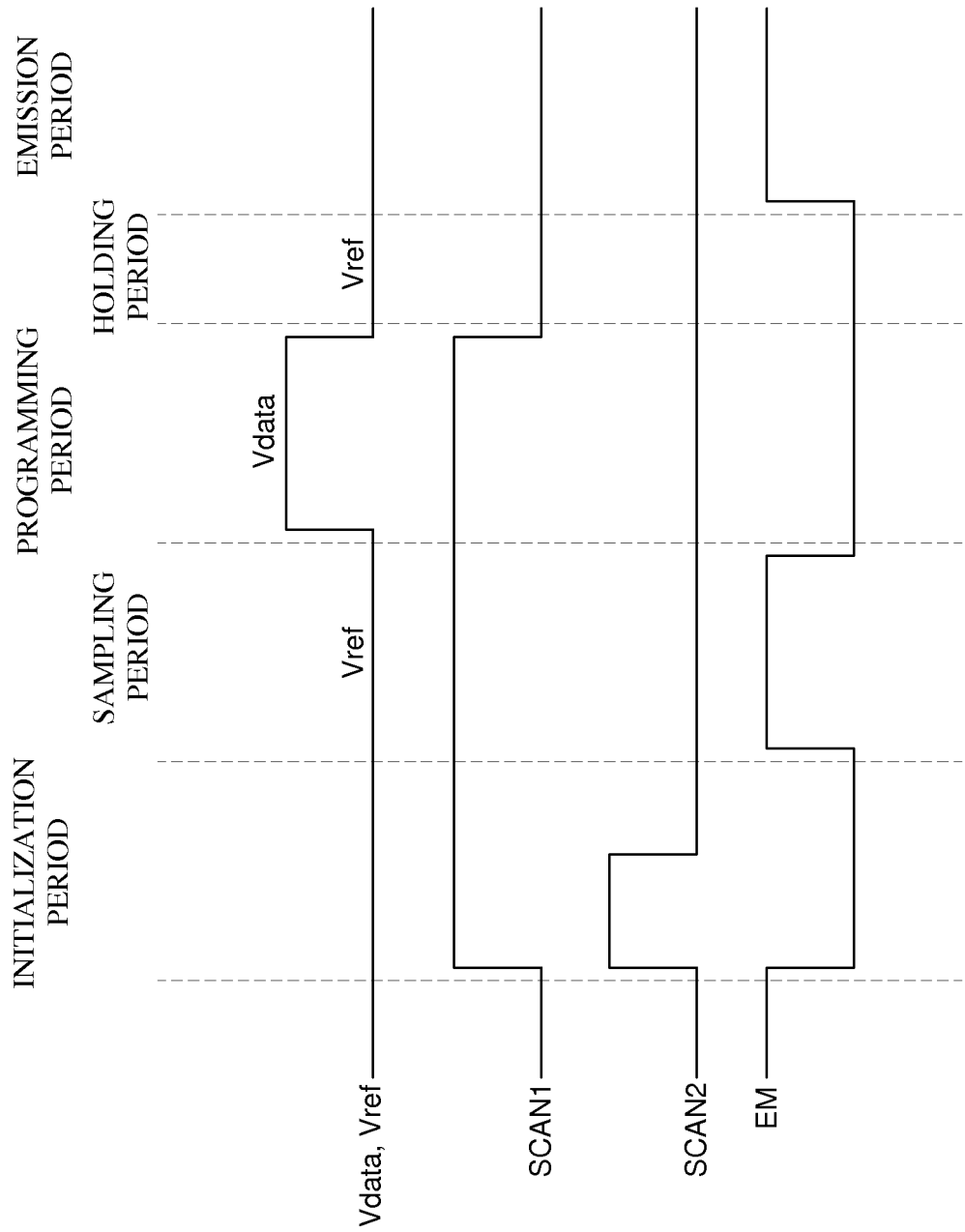


FIG. 2

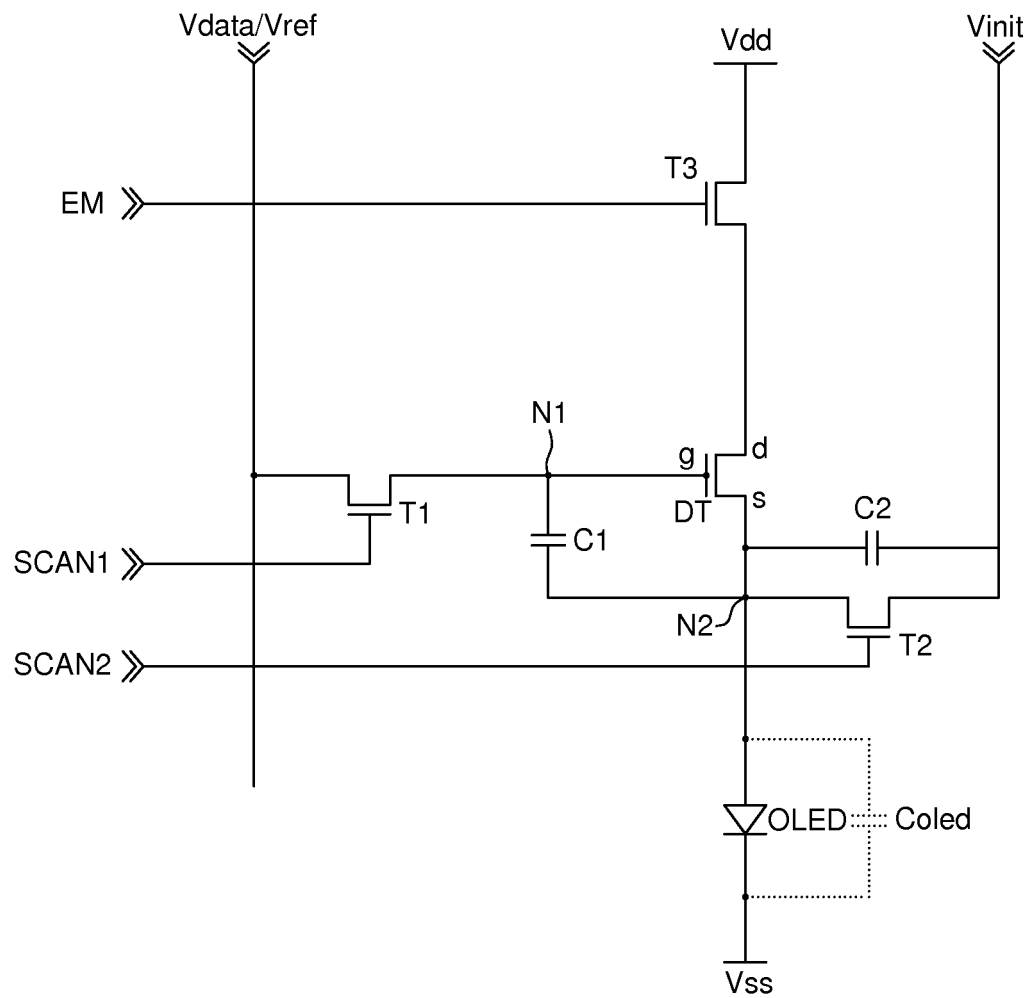


FIG. 3

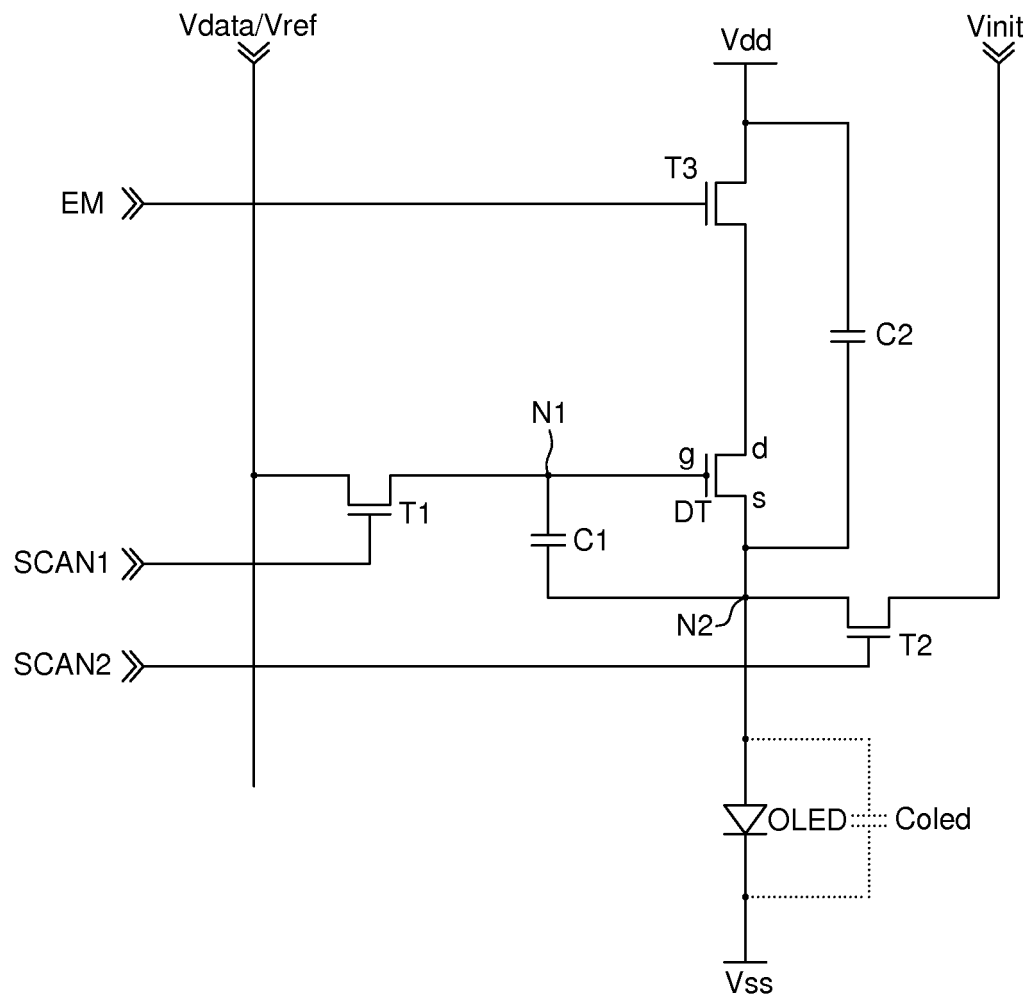


FIG. 4a

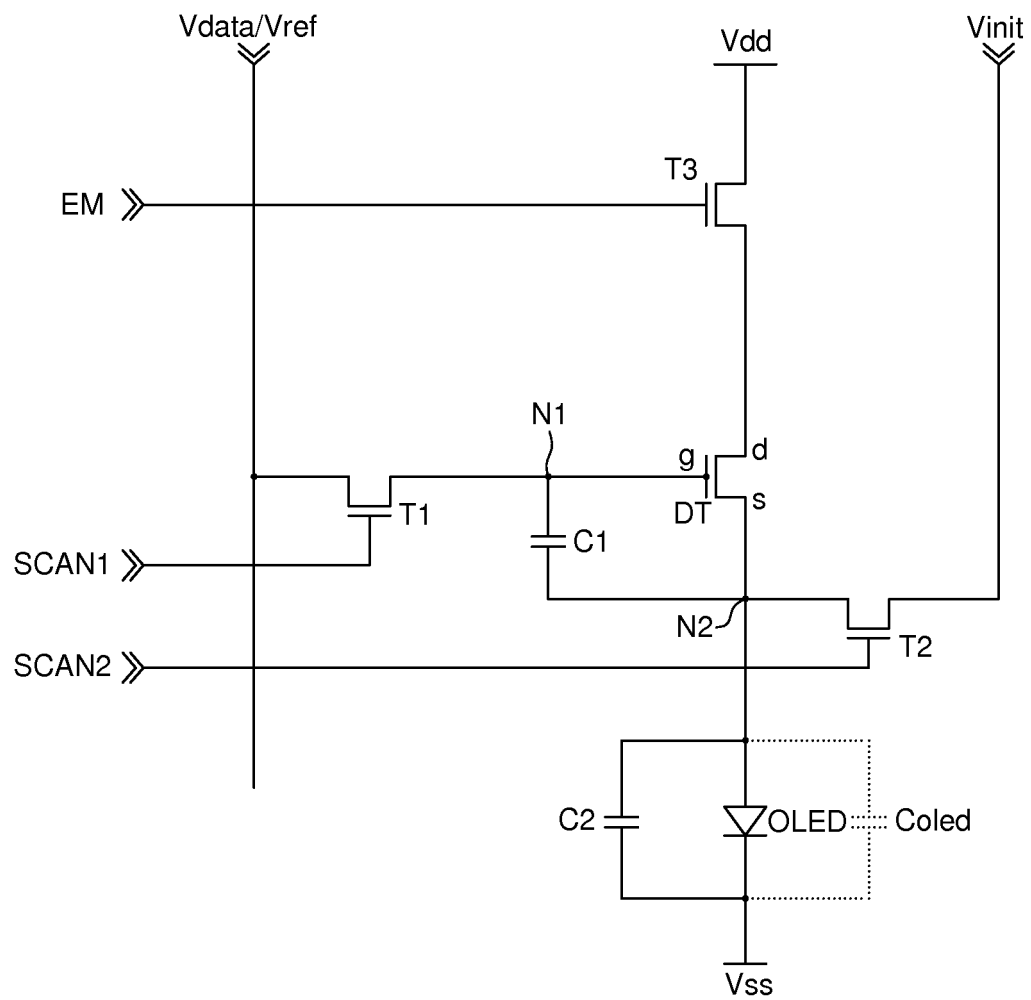


FIG. 4b

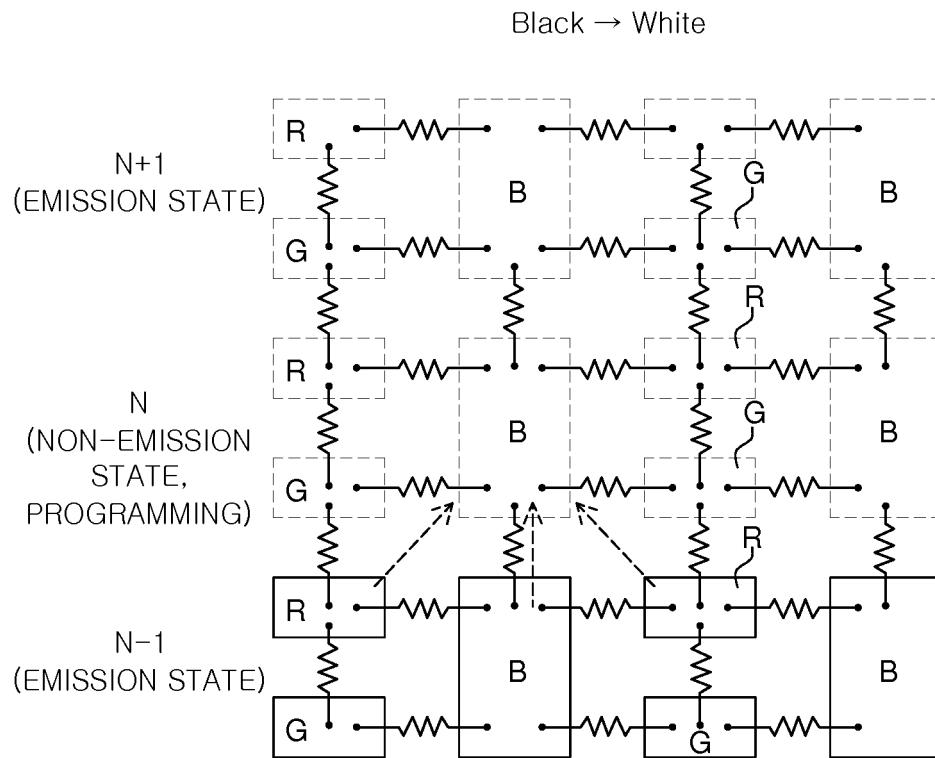


FIG. 5a

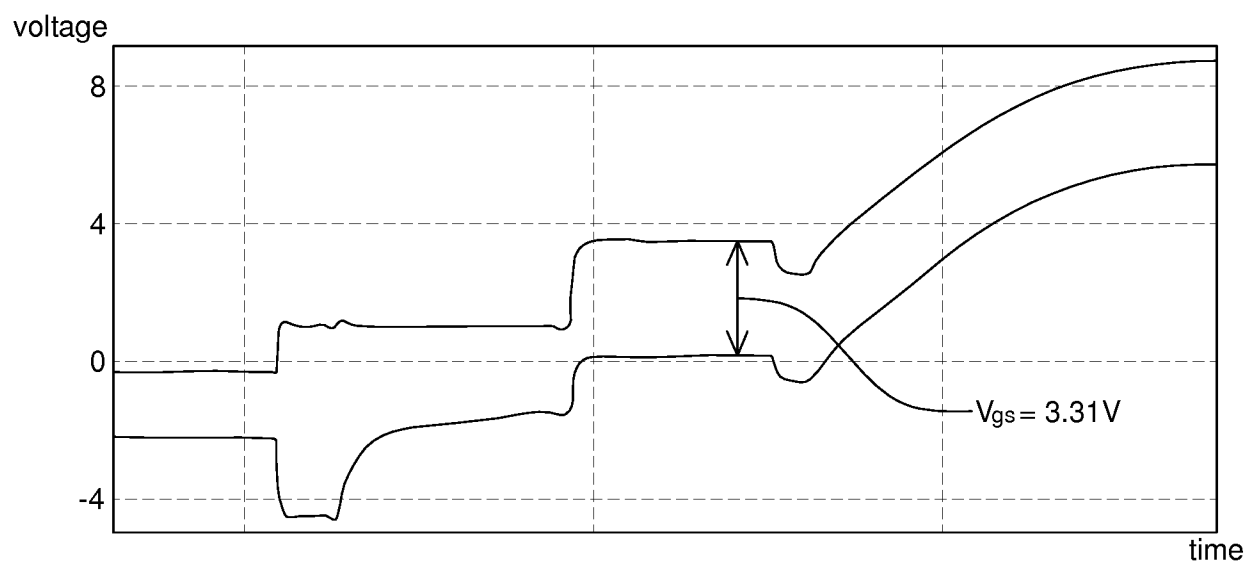


FIG. 5b

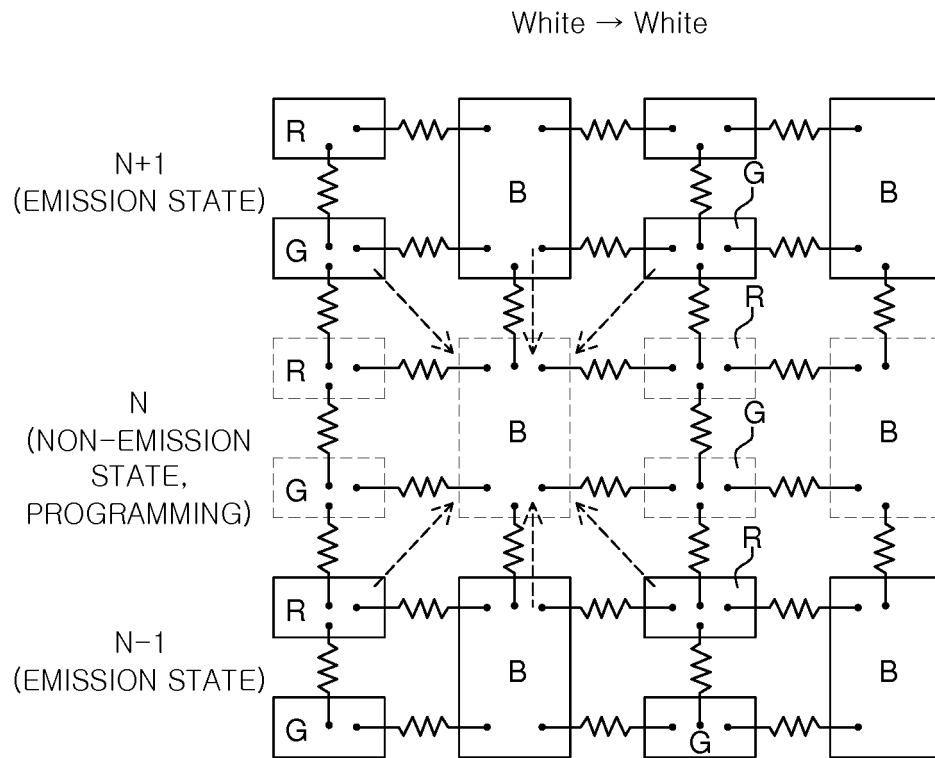


FIG. 6a

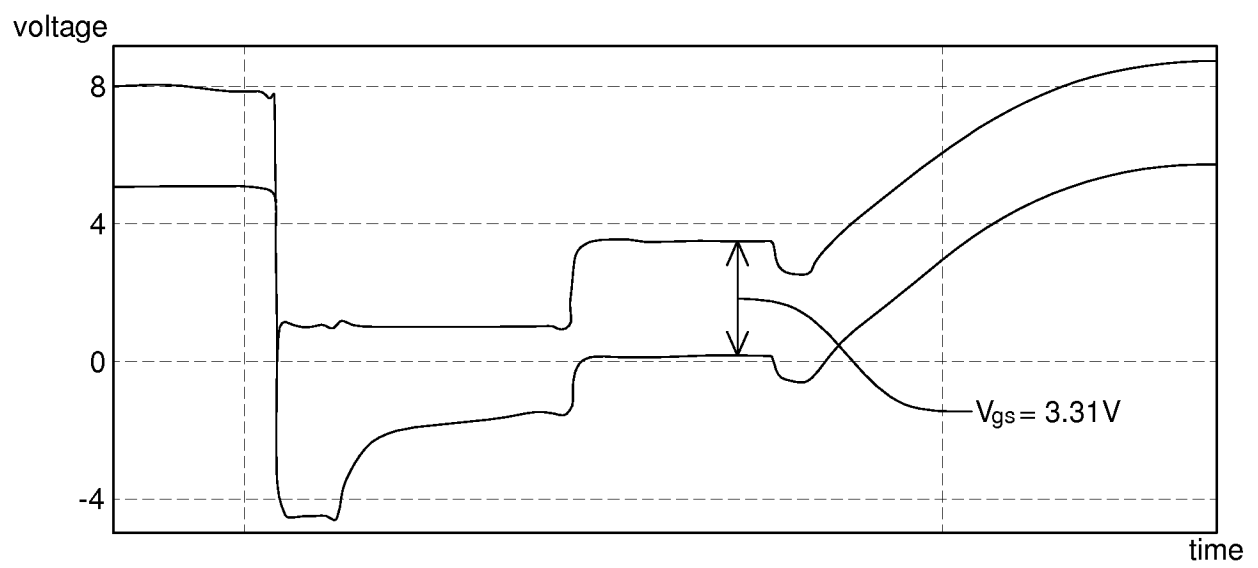


FIG. 6b

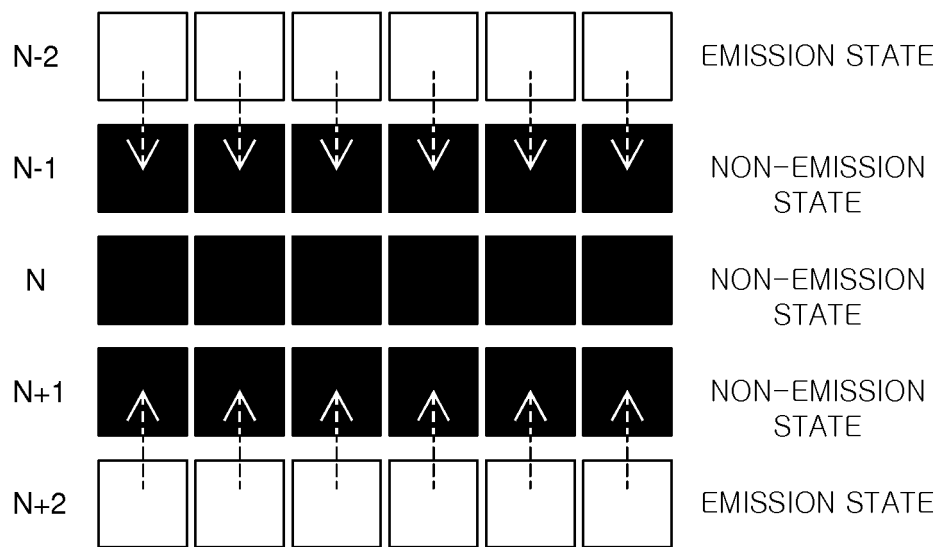


FIG. 7

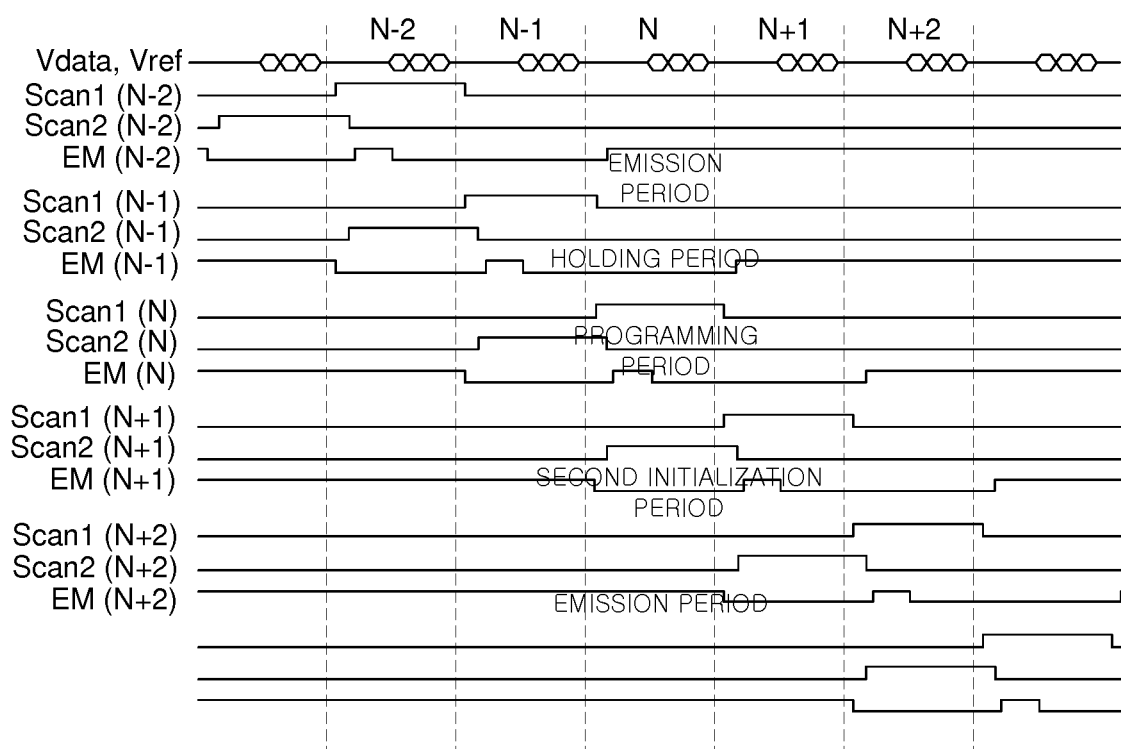


FIG. 8a

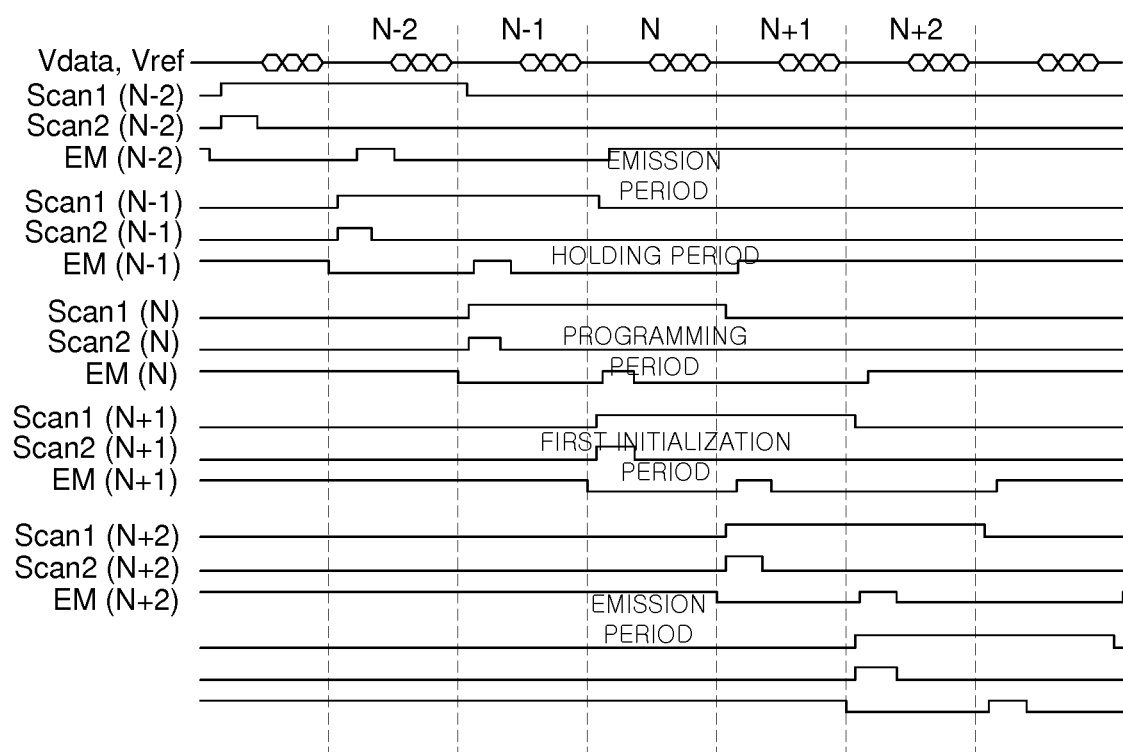


FIG. 8b

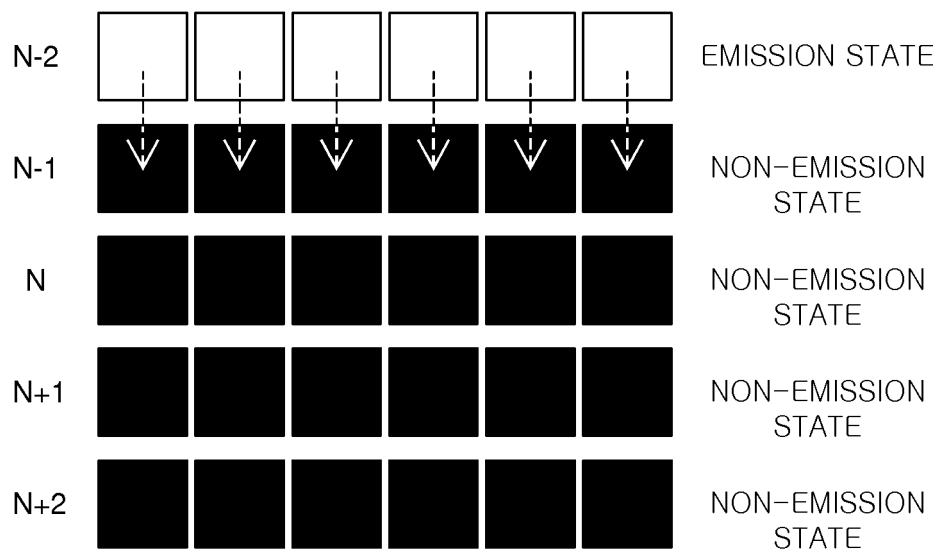


FIG. 9

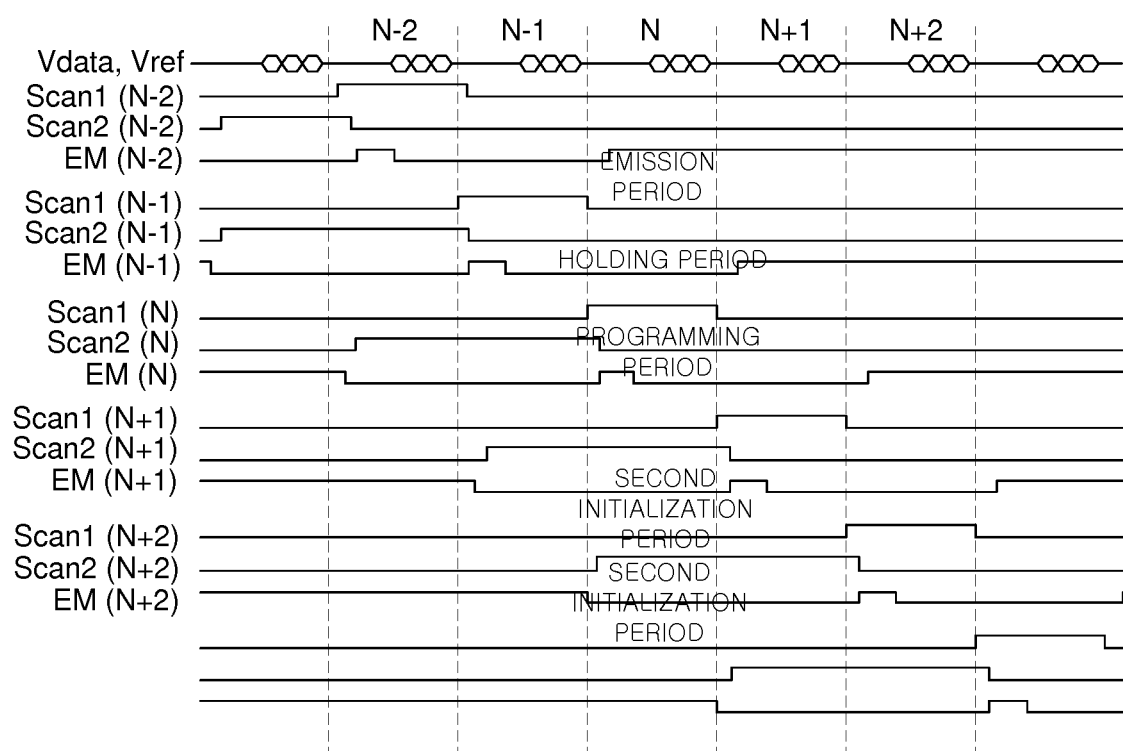


FIG. 10a

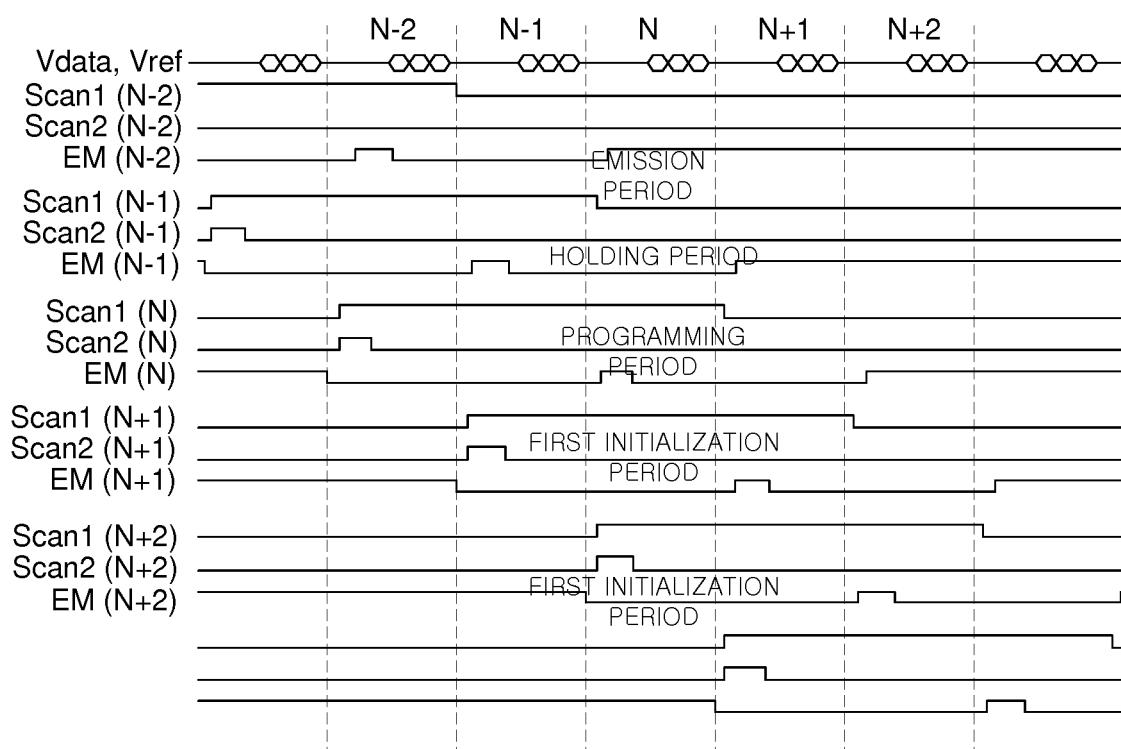


FIG. 10b

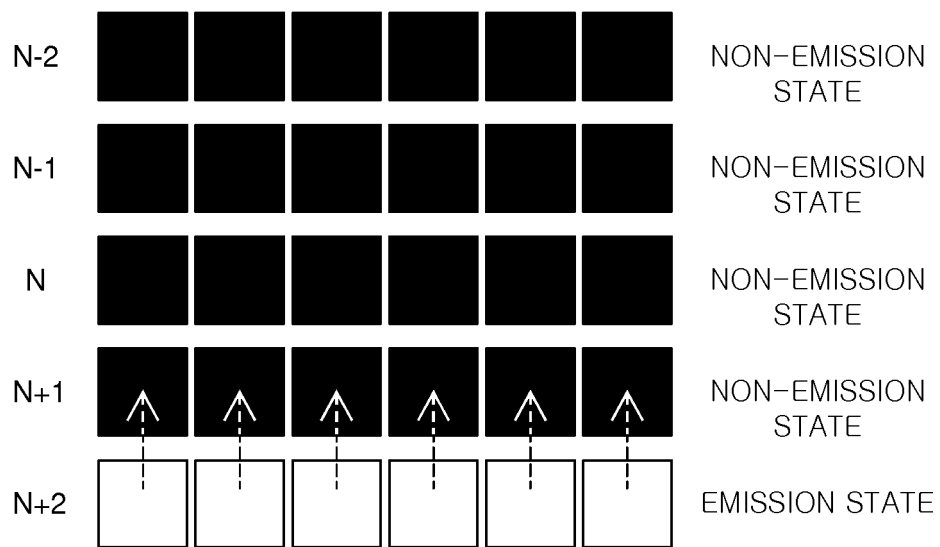


FIG. 11

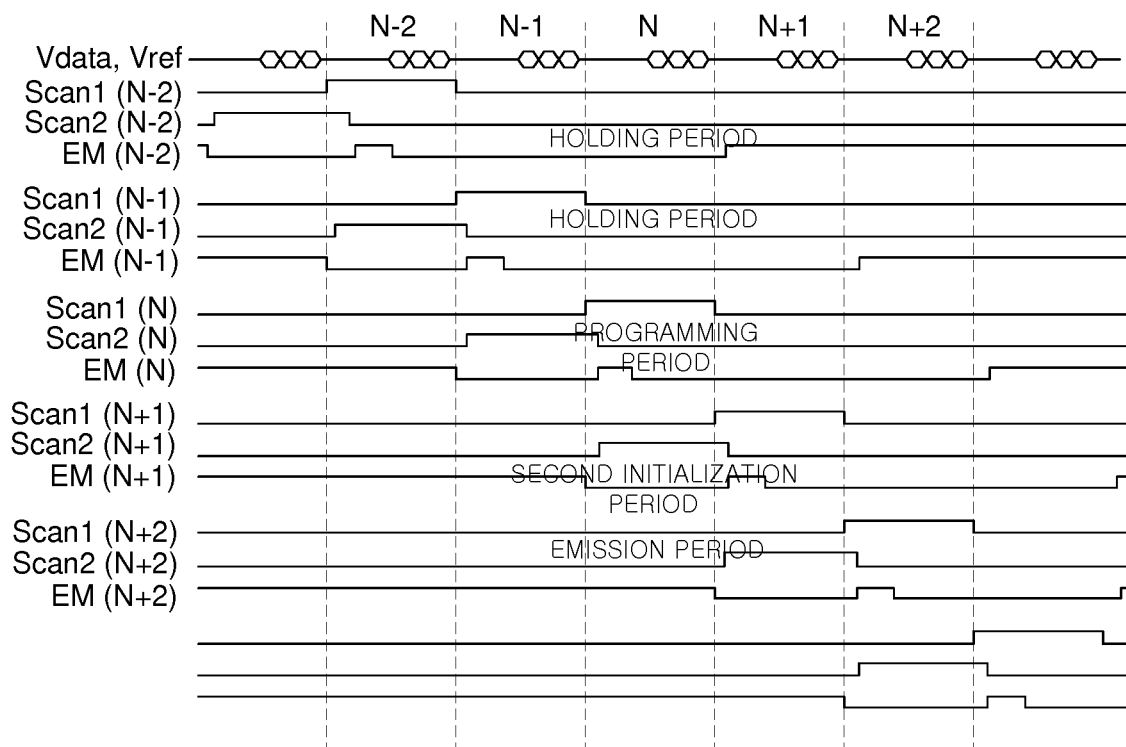


FIG.12a

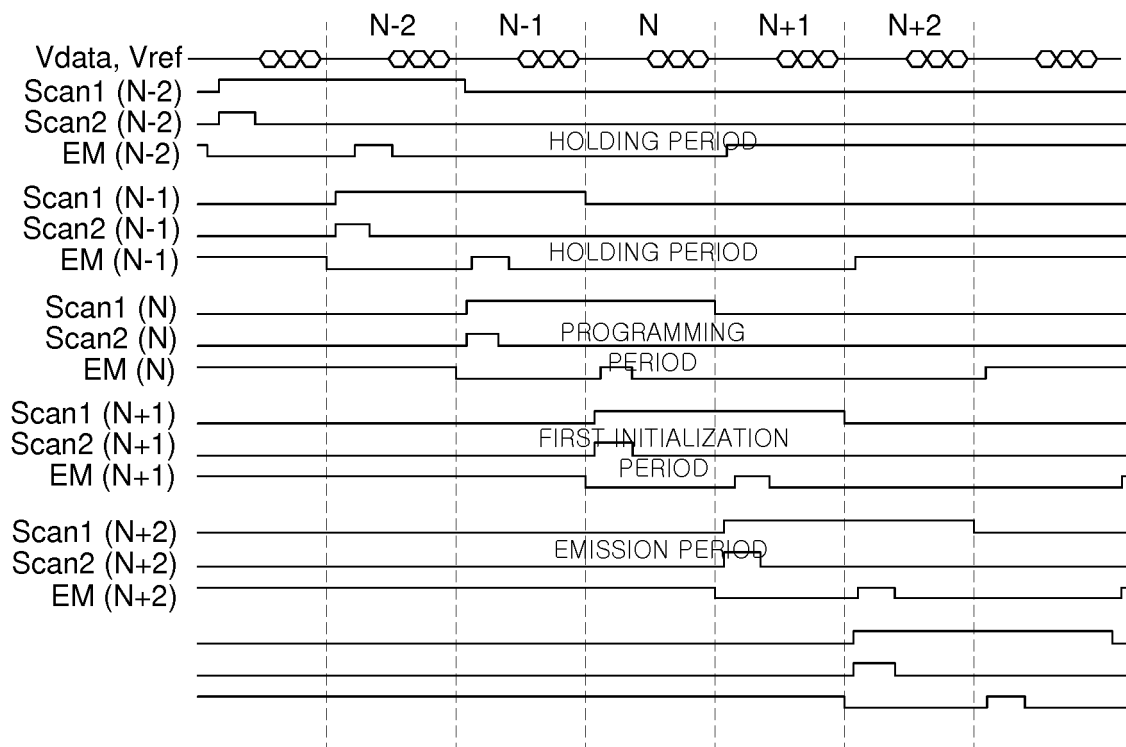


FIG.12b

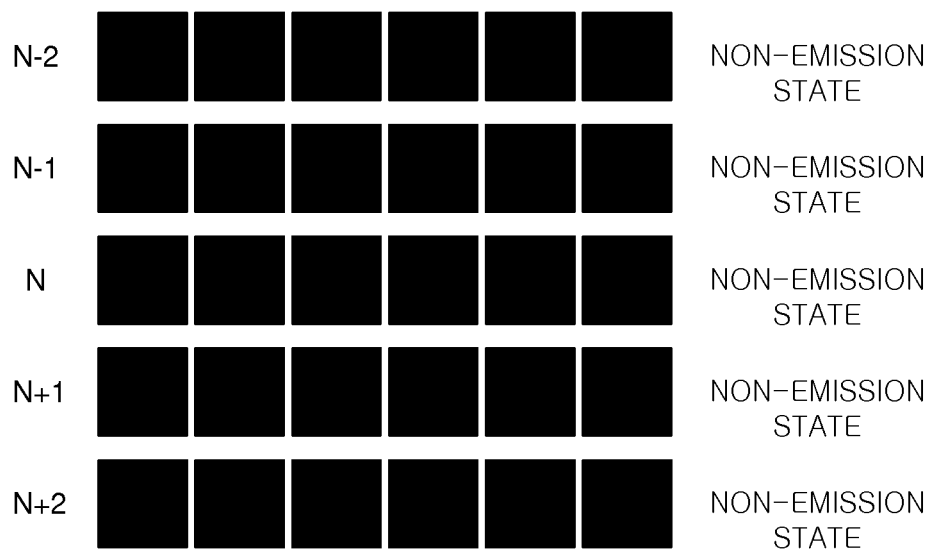


FIG. 13

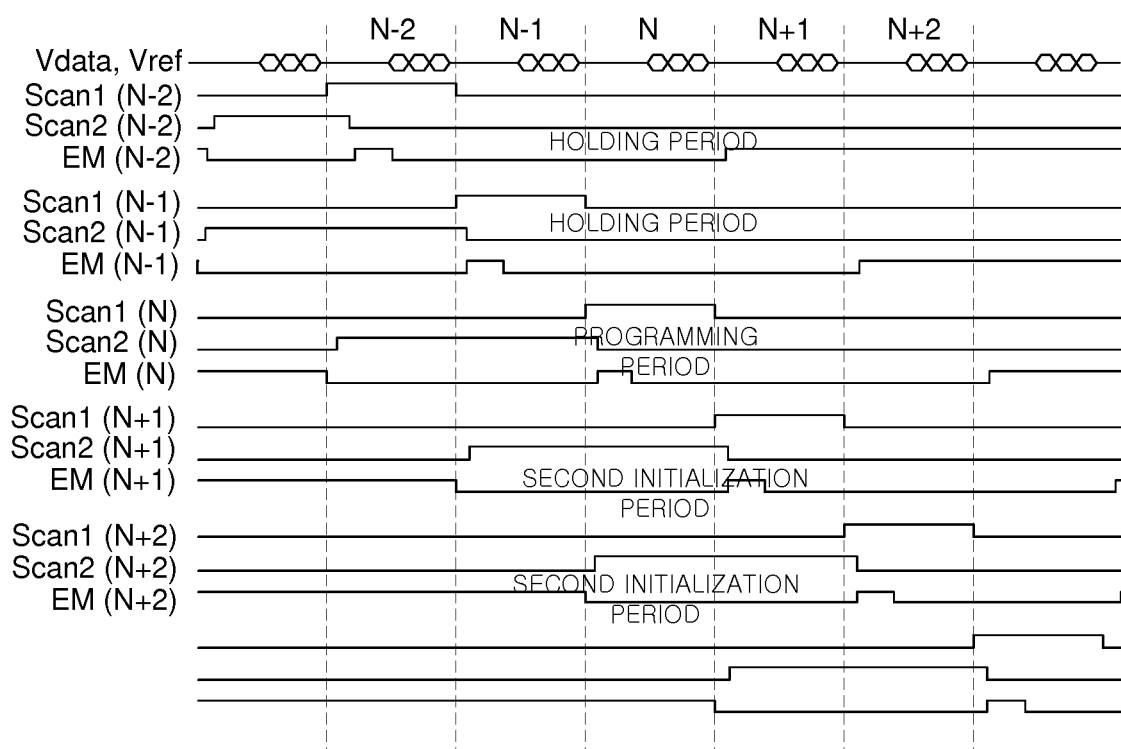


FIG. 14a

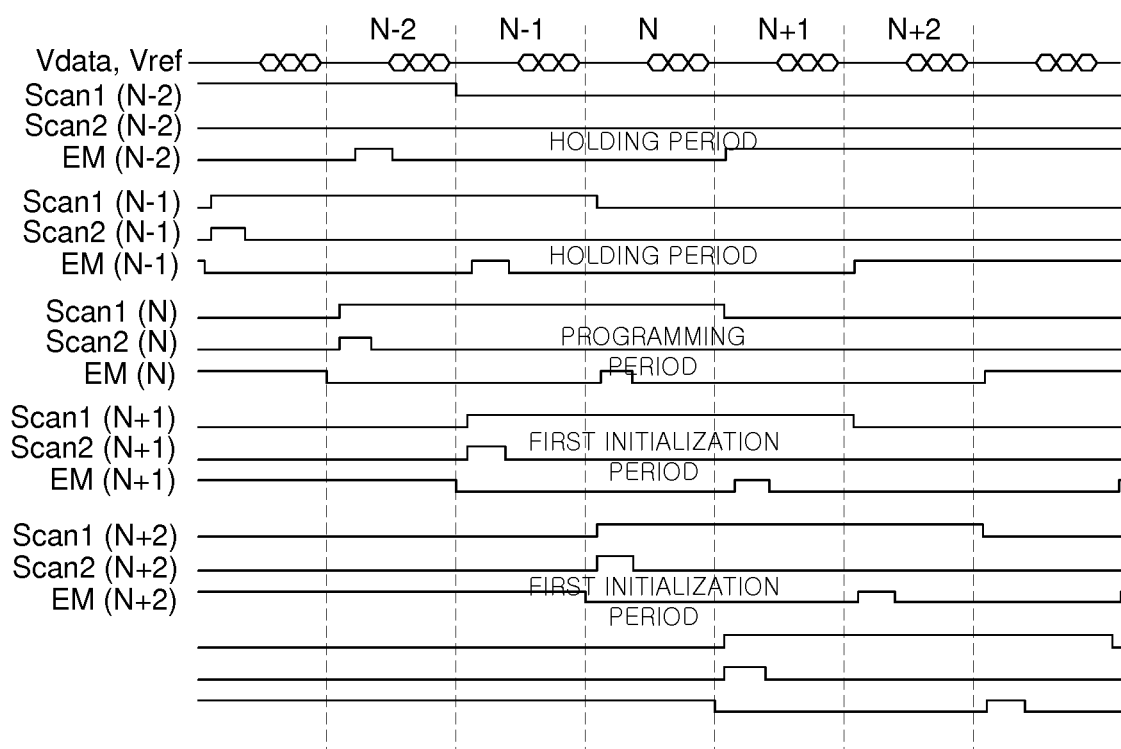


FIG. 14b

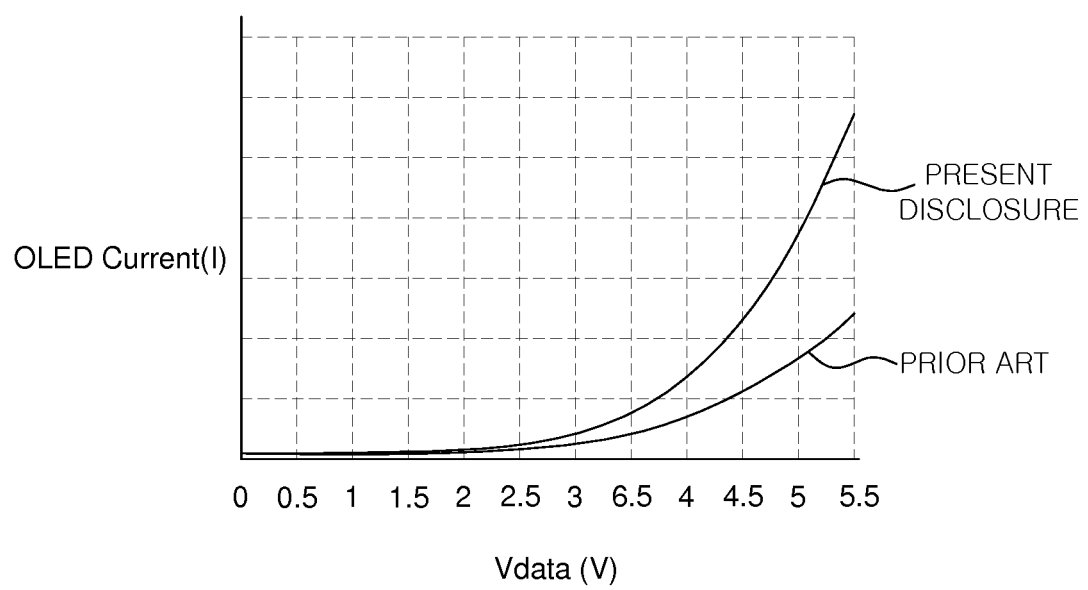


FIG. 15

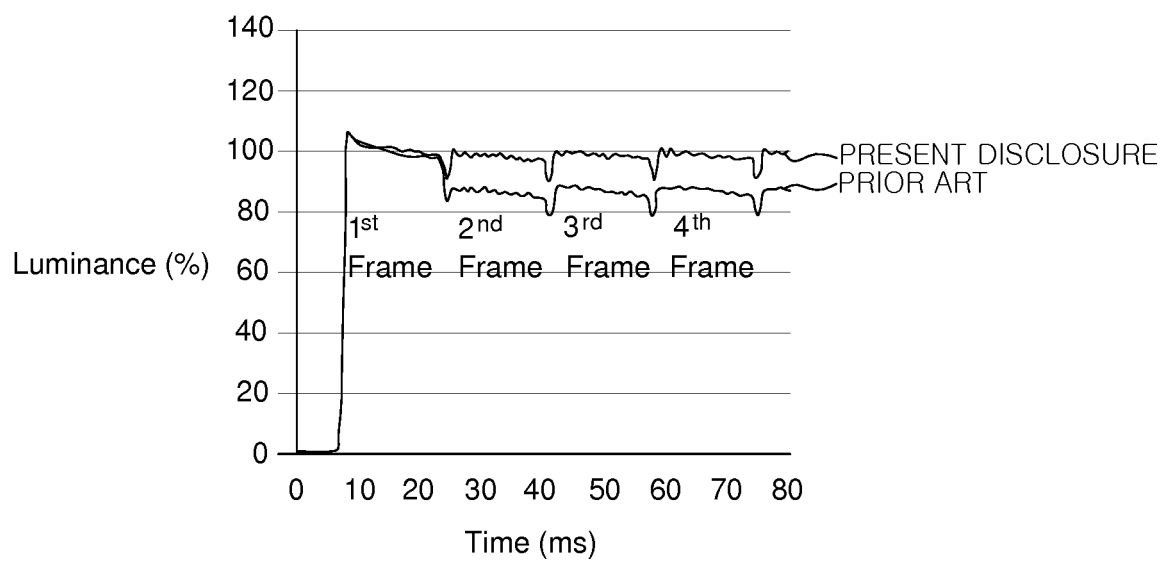


FIG. 16

INTERNATIONAL SEARCH REPORT

International application No.

PCT/KR2015/006896

A. CLASSIFICATION OF SUBJECT MATTER

G09G 3/32(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G09G 3/32; G09G 3/22; G09G 3/20; G09G 3/30; G09G 5/10; H01J 1/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean Utility models and applications for Utility models: IPC as above

Japanese Utility models and applications for Utility models: IPC as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS (KIPO internal) & Keywords: OLED, luminance, fall, anode voltage, threshold voltage, period, votagle difference

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KR 10-2013-0055450 A (LG DISPLAY CO., LTD.) 28 May 2013 See paragraphs [0007]-[0026]; claims 1, 4, 6; and figure 1.	1-20
A	KR 10-2013-0029992 A (LG DISPLAY CO., LTD.) 26 March 2013 See abstract; claim 1; and figure 2.	1-20
A	US 2012-0169794 A1 (UCHINO, Katsuhide et al.) 05 July 2012 See abstract; claims 1, 9; and figures 37-38.	1-20
A	KR 10-2012-0072816 A (LG DISPLAY CO., LTD.) 04 July 2012 See abstract; claims 2, 3; and figures 6, 8.	1-20
A	KR 10-2004-0045341 A (CANON KABUSHIKI KAISHA) 01 June 2004 See abstract; claim 1; and figure 7.	1-20

☐ Further documents are listed in the continuation of Box C.
 ☒ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"G" document member of the same patent family

Date of the actual completion of the international search

08 OCTOBER 2015 (08.10.2015)

Date of mailing of the international search report

08 OCTOBER 2015 (08.10.2015)

Name and mailing address of the ISA/KR


 Korean Intellectual Property Office
 Government Complex-Daejeon, 189 Seonsa-ro, Daejeon 302-701,
 Republic of Korea

Facsimile No. 82-42-472-7140

Authorized officer

Telephone No.

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/KR2015/006896

Patent document cited in search report	Publication date	Patent family member	Publication date
KR 10-2013-0055450 A	28/05/2013	NONE	
KR 10-2013-0029992 A	26/03/2013	NONE	
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		US 8988326 B2	24/03/2015
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		CN 1503209 C	09/06/2004
		EP 1422685 A2	26/05/2004
		EP 1422685 A3	26/12/2007
		JP 2004-170774 A	17/06/2004
		US 2004-0130539 A1	08/07/2004
		US 7145528 B2	05/12/2006

专利名称(译)	OLED显示器件		
公开(公告)号	EP3166100A1	公开(公告)日	2017-05-10
申请号	EP2015815759	申请日	2015-07-03
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	YOON SANG HUN KANG CHANG HEON LEE JUNG MIN		
发明人	YOON, SANG HUN KANG, CHANG HEON LEE, JUNG MIN		
IPC分类号	G09G3/32		
CPC分类号	G09G3/3291 G09G3/3233 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2310/0256 G09G2320/0214 G09G2320/0223		
优先权	1020140084053 2014-07-04 KR		
其他公开文献	EP3166100A4		
外部链接	Espacenet		

摘要(译)

提供一种OLED显示装置，包括控制第N行单位像素的电压的电路和与第N行单位像素相邻的像素行的阳极的电压，以使第N行单位像素与像素之间的电压差最小化与第N行单位像素相邻的线，以抑制由引入第N行单位像素的漏电流引起的第N行单位像素的亮度降低。该电路被配置为当第N行单位像素处于采样周期时将第N行单位像素相邻的像素行的阳极的电压设置为等于或低于第N行单位像素的阳极的电压。或者，在OLED显示装置的驱动时序期间的编程时段。因此，可以使由包括在像素之间的阳极中的电压差引起的公共单层朝向低电位阳极的非预期漏电流的流动最小化。高电位阳极和包括低电位阳极的像素。

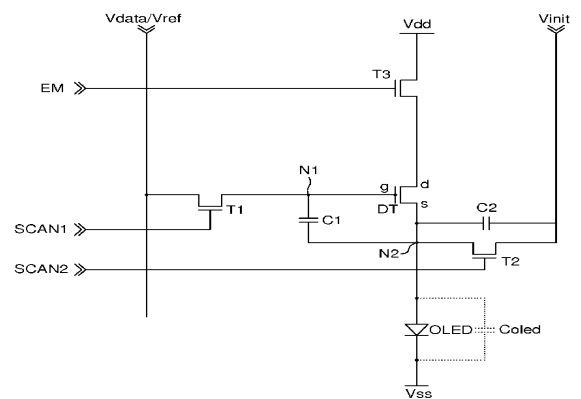


FIG. 3