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(54) **Array substrate, manufacturing method thereof and OLED display device**

(57) An array substrate, a manufacturing method thereof and an OLED display device are provided. The array substrate comprises a plurality of pixel units disposed on a substrate, wherein each pixel unit includes a TFT structure formed on the substrate and an OLED driven by the TFT structure; the TFT structure includes a drive TFT. A drain electrode of the drive TFT is connected with the OLED; a gate electrode and the drain electrode

of the drive TFT are at least partially overlapped to form a storage capacitor. A recess is formed in an insulating layer interposed between the gate electrode and the drain electrode corresponding to the overlapped area, so that the distance between the gate electrode and the drain electrode is less than the thickness of the insulating layer corresponding to the non-overlapped area.

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Description

BACKGROUND

[0001] Embodiments of the present invention relate to an array substrate, a manufacturing method thereof and an organic light-emitting diode (OLED) display device.

[0002] OLED is considered to be one of the most important display technologies in the future due to the advantages of simple manufacturing process, low cost, free adjustment of emission colors within visible regions, large scale, flexible bending and the like. More particularly, the power efficiency of a white OLED (WOLED) has exceeded 60 lm/W and the service life of the WOLED has reached 20,000 hours or more, greatly promoting the development of the WOLED.

[0003] FIG. 1 is a schematic structural view of the traditional OLED array substrate, which specifically illustrates a structure of a pixel unit. The structure comprises (from bottom to top): a first gate electrode 2, a second gate electrode 2' and gate lines (not illustrated in the figure) formed on a substrate 1, a gate insulating layer 3 formed on the first gate electrode 2, the second gate electrode 2' and the gate lines, a first active layer 4 and a second active layer 4' formed on the gate insulating layer 3, an insulating interlayer 5 formed on the first active layer 4 and the second active layer 4', a first source-drain layer 6 (including a first source electrode and a first drain electrode) and a second source-drain layer 6' (including a second source electrode and a second drain electrode) formed on the insulating interlayer 5, and a passivation layer 7 formed on the first source-drain layer 6 and the second source-drain layer 6'. The first gate electrode 2, the gate insulating layer 3, the first active layer 4, the insulating interlayer 5 and the first source-drain layer 6 constitute a switch thin-film transistor (switch TFT); the second gate electrode 2', the gate insulating layer 3, the second active layer 4', the insulating interlayer 5 and the second source-drain layer 6' constitute a drive thin-film transistor (drive TFT). The passivation layer 7, a color filter 9, a resin layer 10, a first electrode 11 of an OLED, a pixel defining layer 12, an organic emission layer 13, and a second electrode 14 of the OLED are disposed above the first source-drain layer 6 and the second source-drain layer 6' in sequence. The first electrode 11 is a transparent electrode, and light emitted by the organic emission layer is emitted after running through the first electrode and various layers under the first electrode. The OLED is disposed in a pixel region of the pixel unit (in general, a display area of the pixel unit, except for a TFT).

[0004] In the structure, as illustrated by dotted lines in FIG. 1, a storage capacitor is formed between the second gate electrode 2' and the second source-drain layer 6'. An equivalent circuit diagram of the pixel unit is as illustrated in FIG. 2, in which Cs refers to the storage capacitor. As the WOLED requires a large driving current, a WOLED display device has large power consumption. In

order to reduce the power consumption, a structure of the storage capacitor is formed on the substrate. The storage capacitor has the function of supplying one part of driving current for the WOLED in such a way that the driving current supplied by an electric power source can be correspondingly reduced, and hence the power consumption can be reduced. However, it can be seen from FIG. 1 that as two insulating layers are interposed between the second gate electrode 2' and the drain electrode of the second source-drain layer 6', the distance is large and the capacitance is small.

SUMMARY

[0005] One embodiment of the present invention provides an array substrate, comprising a plurality of pixel units disposed on a substrate, each pixel unit comprising a thin-film transistor (TFT) structure formed on the substrate and an organic light-emitting diode (OLED) driven by the TFT structure, the TFT structure comprising a drive TFT, wherein a drain electrode of the drive TFT is connected with the OLED; a gate electrode and the drain electrode of the drive TFT are at least partially overlapped to form a storage capacitor; and a recess is formed in an insulating layer interposed between the gate electrode and the drain electrode corresponding to an overlapped area of the gate electrode and the drain electrode of the drive TFT, so that a distance between the gate electrode and the drain electrode is less than a thickness of a part of the insulating layer in an area other than the non-overlapped area.

[0006] In one example, the drain electrode is disposed over the gate electrode; and a part of the drain electrode is formed in the recess.

[0007] In one example, the TFT structure comprises: a first gate electrode and a second gate electrode formed on the substrate, a gate insulating layer formed on the first gate electrode and the second gate electrode, a first active layer and a second active layer formed on the gate insulating layer, a first source electrode and a first drain electrode formed on the first active layer, and a second source electrode and a second drain electrode formed on the second active layer; the first drain electrode is connected with the second gate electrode; the first gate electrode, the gate insulating layer, the first active layer, the first source electrode and the first drain electrode constitute a switch TFT; and the second gate electrode, the gate insulating layer, the second active layer, the second source electrode and the second drain electrode constitute the drive TFT; and the OLED is disposed in a pixel region of the pixel unit and comprises a transparent first electrode, an emission layer and a second electrode; the first electrode is connected with the second drain electrode; the second drain electrode and the second gate electrode are at least partially overlapped to form the storage capacitor; and the insulating layer interposed between the second drain electrode and the second gate electrode comprises the gate insulating layer.

[0008] In one example, an insulating interlayer is further formed between the second active layer and the second drain electrode; the insulating layer comprises the insulating interlayer and the gate insulating layer; the recess is formed in a surface of the insulating interlayer close to the second drain electrode; and the depth of the recess is less than the thickness of the insulating interlayer.

[0009] In one example, an insulating interlayer is further formed between the second active layer and the second drain electrode; the insulating layer comprises the insulating interlayer and the gate insulating layer; a through hole is formed in the insulating interlayer corresponding to the overlapped area; and the through hole and a surface of the gate insulating layer form the recess.

[0010] In one example, an insulating interlayer is further formed between the second active layer and the second drain electrode; the insulating layer comprises the insulating interlayer and the gate insulating layer; a through hole is formed in the insulating interlayer corresponding to the overlapped area; a sub-recess is formed in the gate insulating layer corresponding to the overlapped area; the through hole and the sub-recess form the recess; and the depth of the sub-recess is less than the thickness of the gate insulating layer.

[0011] In one example, the pixel unit further comprises: a color filter formed between a layer provided with the OLED and a layer provided with the TFT structure.

[0012] In one example, the color filter is disposed on a passivation layer above the drive TFT.

[0013] Another embodiment of the invention provides a method for manufacturing an array substrate, comprising the following steps of: forming patterns of a first gate electrode, a second gate electrode, an insulating layer, a first active layer and a second active layer on a substrate; forming patterns of a through hole and a recess in the insulating layer; forming patterns of a first source electrode, a first drain electrode, a second source electrode and a second drain electrode in such a way that the second drain electrode and the second gate electrode are at least partially overlapped and an overlapped area of the second drain electrode and the second gate electrode corresponds to the recess, so that a distance between the second gate electrode and the second drain electrode is less than the thickness of a part of the insulating layer in an area other than the non-overlapped area; and forming patterns of a color filter and an OLED.

[0014] In one example, the insulating layer comprises a gate insulating layer; and forming the patterns of the through hole and the recess in the insulating layer comprises: by patterning process, forming the through hole in the gate insulating layer corresponding to a connection area of the first drain electrode and the second gate electrode, and forming the recess in the gate insulating layer corresponding to the overlapped area of the second drain electrode and the second gate electrode.

[0015] In one example, the insulating layer comprises a gate insulating layer formed on the first gate electrode

and the second gate electrode and an insulating interlayer formed on the first active layer and the second active layer; and the patterns of the through hole and the recess are formed in the insulating layer by one patterning process.

[0016] In one example, forming the patterns of the through hole and the recess in the insulating layer comprises: by patterning process, forming a first through hole running through the gate insulating layer and the insulating interlayer at a connection area of the first drain electrode and the second gate electrode; forming a second through hole running through the insulating interlayer at a connection area of the first source electrode and the first active layer; forming a third through hole running through the insulating interlayer at a connection area of the first drain electrode and the first active layer; forming a fourth through hole running through the insulating interlayer at a connection area of the second source electrode and the second active layer; and forming the recess at the overlapped area of the second drain electrode and the second gate electrode.

[0017] In one example, forming the recess at the overlapped area of the second drain electrode and the second gate electrode comprises: forming the recess in the insulating interlayer corresponding to the overlapped area; or, forming a through hole in the insulating interlayer corresponding to the overlapped area, and the through hole and a surface of the gate insulating layer forming the recess; or, forming a through hole at the corresponding overlapped area on the insulating interlayer, forming a sub-recess in the gate insulating layer corresponding to overlapped area, and the through hole and the sub-recess forming the recess.

[0018] Another embodiment of the present invention provides an OLED display device, which comprises the array substrate according to any embodiment of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] In order to clearly illustrate the technical solution of the embodiments of the invention, the drawings of the embodiments will be briefly described in the following; it is obvious that the described drawings are only related to some embodiments of the invention and thus are not limitative of the invention.

FIG. 1 is a schematic structural view of a traditional array substrate;

FIG. 2 is an equivalent circuit diagram of a pixel unit in the array substrate in FIG. 1;

FIG. 3 is a schematic structural view of an array substrate provided by an embodiment of the present invention;

FIG. 4 is an enlarged view of a recess of the array substrate in FIG. 3;

FIG. 5 is a schematic diagram of a substrate obtained by forming patterns of a gate electrode, an insulating

layer and an active layer in manufacturing the array substrate in FIG. 3;

FIG. 6 is a schematic diagram of a substrate obtained by forming a through hole and a recess on the substrate in FIG. 5; and

FIG. 7 is a schematic diagram of a substrate obtained by forming source/drain electrodes on the substrate in FIG. 6.

DETAILED DESCRIPTION

[0020] In order to make objects, technical details and advantages of the embodiments of the invention apparent, the technical solutions of the embodiment will be described in a clearly and fully understandable way in connection with the drawings related to the embodiments of the invention. It is obvious that the described embodiments are just a part but not all of the embodiments of the invention. Based on the described embodiments herein, those skilled in the art can obtain other embodiment(s), without any inventive work, which should be within the scope of the invention.

[0021] The array substrate provided by the present invention comprises a plurality of pixel units disposed on a substrate, wherein each pixel unit includes a TFT structure formed on the substrate and an OLED driven by the TFT structure and disposed in a pixel region of the pixel unit. In addition, the TFT structure includes a drive TFT, wherein a drain electrode of the drive TFT is connected with the OLED; a gate electrode and the drain electrode of the drive TFT are at least partially overlapped to form a storage capacitor; and a recess is formed an insulating layer interposed between the gate electrode and the drain electrode corresponding to an overlapped area of the gate electrode and the drain electrode of the drive TFT, so that the distance between the gate electrode and the drain electrode is less than the thickness of a part of the insulating layer corresponding to the non-overlapped area (in an area other than the overlapped area). The structure reduces the distance between the gate electrode and the drain electrode and hence increases the storage capacitance formed between the gate electrode and the drain electrode and reduces the driving power of the array substrate. Description will be given below by taking a bottom-gate TFT WOLED array substrate as an example.

[0022] As illustrated in FIG. 3, the array substrate comprises (from bottom to top): a first gate electrode 2, a second gate electrode 2' and gate lines (not illustrated in the figure) formed on a substrate 1, a gate insulating layer 3 formed on the first gate electrode 2, the second gate electrode 2' and the gate lines, a first active layer 4 and a second active layer 4' formed on the gate insulating layer 3, an insulating interlayer 5 formed on the first active layer 4 and the second active layer 4', a first source-drain layer 6 (including a first source electrode and a first drain electrode) and a second source-drain layer 6' (including a second source electrode and a second drain electrode)

formed on the insulating interlayer 5, and a passivation layer 7 formed on the first source-drain layer 6 and the second source-drain layer 6'. The first gate electrode 2, the gate insulating layer 3, the first active layer 4, the insulating interlayer 5 and the first source-drain layer 6 constitute a switch TFT. The second gate electrode 2', the gate insulating layer 3, the second active layer 4', the insulating interlayer 5 and the second source-drain layer 6' constitute a drive TFT. The passivation layer 7, a color filter 9, a resin layer 10, a first electrode 11 of an OLED, a pixel defining layer 12, an organic emission layer 13, and a second electrode 14 of the OLED are disposed on the first source-drain layer 6 and the second source-drain layer 6' in sequence. The first electrode 11 is a transparent electrode; and light emitted by the organic emission layer is emitted after running through the first electrode and various layers under the first electrode.

[0023] For instance, the color filter 9 is formed between a layer provided with the OLED and a layer provided with the TFT structure.

[0024] In the structure, the second gate electrode 2' and a drain electrode (hereinafter referred to as the second drain electrode) of the second source-drain layer 6' are at least partially overlapped to form a storage capacitor; and an insulating layer formed by the gate insulating layer 3 and the insulating interlayer 5 is interposed between the second gate electrode 2' and the second drain electrode. In order to increase the storage capacitance, a recess is formed in the insulating layer at position corresponding to the overlapped area and one part of the second drain electrode is formed in the recess, so that the distance between the second gate electrode 2' and the second drain electrode is less than the thickness of the insulating layer corresponding to the non-overlapped area. That is to say, compared to the traditional storage capacitor structure, the distance between two plate electrodes (the second gate electrode 2' and the second drain electrode) of the storage capacitor is reduced and the storage capacitance is increased.

[0025] In the embodiment, the insulating layer between the two plate electrodes of the storage capacitor consists of the gate insulating layer 3 and the insulating interlayer 5, and the recess has three structures:

[0026] Structure 1: the recess is formed on a surface of the insulating interlayer 5 close to the second drain electrode, and the depth of the recess is less than the thickness of the insulating interlayer 5, namely the recess is formed in the insulating interlayer 5;

[0027] Structure 2: a through hole is formed in the insulating interlayer 5 corresponding to the overlapped area, and the through hole and a surface of the gate insulating layer 3 form the recess; and

[0028] Structure 3: as illustrated in FIG. 4, a through hole 16 is formed in the insulating interlayer 5 corresponding to the overlapped area; a sub-recess 15 is formed in the gate insulating layer 3 corresponding to the overlapped area; the through hole 16 and the sub-recess 15 form the recess. The depth of the sub-recess 15 is

less than the thickness of the gate insulating layer 3.

[0029] In the three structures, as for the recess with the structure 3, the distance between the second gate electrode 2' and the second drain electrode is minimum, and the formed storage capacitance is maximum. The storage capacitance corresponding to the structure 2 is secondary. The storage capacitance corresponding to the structure 1 has the smallest increase.

[0030] The insulating layer between the two plate electrodes (the second gate electrode 2' and the second drain electrode) of the storage capacitor may also only include the gate insulating layer 3. At this point, only the recess is formed in the surface of the gate insulating layer 3, so that one part of the second drain electrode is formed in the recess.

[0031] The embodiment of the present invention further provides a method for manufacturing the array substrate, which comprises:

[0032] Step 1: as illustrated in FIG. 5, forming patterns of a first gate electrode 2, a second gate electrode 2', an insulating layer, a first active layer 4 and a second active layer 4'. The insulating layer includes a gate insulating layer 3 and an insulating interlayer 5. The step is mainly as follows: corresponding film layers are formed (by coating, sputtering, deposition and the like), and hence patterns of the corresponding layers are formed by patterning process (the patterning process generally includes photoresist coating, exposure, development, etching, photoresist removing and the like). The step is basically the same with the step in the traditional method for manufacturing the array substrate, and will not be further described.

[0033] Step 2: forming patterns of a through hole and a recess in the insulating layer. More specifically, as illustrated in FIG. 6, by patterning process, a first through hole 21 running through the gate insulating layer and the insulating interlayer is formed at a connection area of the first drain electrode and the second gate electrode; a second through hole 22 running through the insulating interlayer is formed at a connection area of the first source electrode and the first active layer; a third through hole 23 running through the insulating interlayer is formed at a connection area of the first drain electrode and the first active layer; a fourth through hole 24 running through the insulating interlayer is formed at a connection area of the second source electrode and the second active layer; and a recess 25 is formed at an overlapped area of the second drain electrode and the second gate electrode. In the step, as the through holes have different depths, a half-tone mask may be adopted to achieve the development and exposure of photoresist. The through hole 21 is formed by a first etching process and then the through holes 22, 23 and 24 are formed by a second etching process. In addition, the recess 25 is also formed by the second etching process. The etching of the recess 25 includes the following three modes:

[0034] Mode 1: forming the recess 25 in the insulating interlayer 5 corresponding to the overlapped area. As the

depth of the recess is preferably the same with that of the through holes 22, 23 and 24, the phenomenon of over-etching in the etching process of the recess 25 can be avoided.

[0035] Mode 2: forming the through hole in the insulating interlayer 5 corresponding to the overlapped area, and the through hole 16 (as illustrated in FIG. 4) and a surface of the gate insulating layer 3 forming the recess 25. In the mode, the overlapped area must be over-etched to form the recess 25.

[0036] Mode 3: forming the through hole 16 in the insulating interlayer 5 corresponding to the overlapped area, forming a sub-recess 15 (as illustrated in FIG. 4) in the gate insulating layer 3 corresponding to the overlapped area, and the through hole 16 and the sub-recess 15 forming the recess 25. The mode 3 is as illustrated in FIG. 6.

[0037] In the above three modes for forming the recess, the patterns of the through hole and the recess are formed in the insulating layer only by one patterning process no matter which mode is adopted.

[0038] Step 3: as illustrated in FIG. 7, forming patterns of the first source-drain layer 6 (including the first source electrode and the first drain electrode) and the second source-drain layer 6' (including the second source electrode and the second drain electrode). The second drain electrode and the second gate electrode are at least partially overlapped, and one part of the second drain electrode is formed in the recess 25 (that is to say, the overlapped area of the second drain electrode and the second gate electrode corresponds to the recess 25), so that the distance between the second gate electrode and the second drain electrode is less than the thickness of the insulating layer corresponding to the non-overlapped area.

[0039] Step 4: forming patterns of a color filter and an OLED. The finally formed array substrate is as illustrated in FIG. 3.

[0040] If only the gate insulating layer 3 is formed in the step 1, in the step 2, the through hole is only formed in the gate insulating layer 3 at the connection area of the first drain electrode and the second gate electrode, and the recess is formed in the gate insulating layer at the overlapped area of the second drain electrode and the second gate electrode.

[0041] The embodiment of the present invention further provides an OLED display device, which comprises the foregoing array substrate. The display device may be electronic paper, an OLED panel, an OLED display, an OLED TV, a digital picture frame, a mobile phone, a tablet PC or any other product or component with display function.

[0042] The foregoing is merely exemplary embodiments of the invention, but is not used to limit the protection scope of the invention. The protection scope of the invention shall be defined by the attached claims.

Claims

1. An array substrate, comprising a plurality of pixel units disposed on a substrate, each pixel unit comprising a thin-film transistor (TFT) structure formed on the substrate and an organic light-emitting diode (OLED) driven by the TFT structure, the TFT structure comprising a drive TFT, wherein
 a drain electrode of the drive TFT is connected with the OLED; a gate electrode and the drain electrode of the drive TFT are at least partially overlapped to form a storage capacitor; and
 a recess is formed in an insulating layer interposed between the gate electrode and the drain electrode corresponding to an overlapped area of the gate electrode and the drain electrode of the drive TFT, so that a distance between the gate electrode and the drain electrode is less than a thickness of a part of the insulating layer in an area other than the non-overlapped area.
2. The array substrate according to claim 1, wherein the drain electrode is disposed over the gate electrode; and a part of the drain electrode is formed in the recess.
3. The array substrate according to claim 1 or 2, wherein the TFT structure comprises: a first gate electrode and a second gate electrode formed on the substrate, a gate insulating layer formed on the first gate electrode and the second gate electrode, a first active layer and a second active layer formed on the gate insulating layer, a first source electrode and a first drain electrode formed on the first active layer, and a second source electrode and a second drain electrode formed on the second active layer; the first drain electrode is connected with the second gate electrode; the first gate electrode, the gate insulating layer, the first active layer, the first source electrode and the first drain electrode constitute a switch TFT; and the second gate electrode, the gate insulating layer, the second active layer, the second source electrode and the second drain electrode constitute the drive TFT; and
 the OLED is disposed in a pixel region of the pixel unit and comprises a transparent first electrode, an emission layer and a second electrode; the first electrode is connected with the second drain electrode; the second drain electrode and the second gate electrode are at least partially overlapped to form the storage capacitor; and the insulating layer interposed between the second drain electrode and the second gate electrode comprises the gate insulating layer.
4. The array substrate according to claim 3, wherein an insulating interlayer is further formed between the second active layer and the second drain electrode;

the insulating layer comprises the insulating interlayer and the gate insulating layer; the recess is formed in a surface of the insulating interlayer close to the second drain electrode; and the depth of the recess is less than the thickness of the insulating interlayer.
5. The array substrate according to claim 3, wherein an insulating interlayer is further formed between the second active layer and the second drain electrode; the insulating layer comprises the insulating interlayer and the gate insulating layer; a through hole is formed in the insulating interlayer corresponding to the overlapped area; and the through hole and a surface of the gate insulating layer form the recess.
6. The array substrate according to claim 3, wherein an insulating interlayer is further formed between the second active layer and the second drain electrode; the insulating layer comprises the insulating interlayer and the gate insulating layer; a through hole is formed in the insulating interlayer corresponding to the overlapped area; a sub-recess is formed in the gate insulating layer corresponding to the overlapped area; the through hole and the sub-recess form the recess; and the depth of the sub-recess is less than the thickness of the gate insulating layer.
7. The array substrate according to any one of claims 1 to 6, wherein the pixel unit further comprises:

a color filter formed between a layer provided with the OLED and a layer provided with the TFT structure.
8. The array substrate according to claim 7, wherein the color filter is disposed on a passivation layer above the drive TFT.
9. A method for manufacturing an array substrate, comprising the following steps of:

forming patterns of a first gate electrode, a second gate electrode, an insulating layer, a first active layer and a second active layer on a substrate;
 forming patterns of a through hole and a recess in the insulating layer;
 forming patterns of a first source electrode, a first drain electrode, a second source electrode and a second drain electrode in such a way that the second drain electrode and the second gate electrode are at least partially overlapped and an overlapped area of the second drain electrode and the second gate electrode corresponds to the recess, so that a distance between the second gate electrode and the second drain electrode is less than the thickness of a part of the insulating layer in an area other than the non-

overlapped area; and
forming patterns of a color filter and an OLED.

10. The method for manufacturing the array substrate according to claim 9, wherein the insulating layer comprises a gate insulating layer; and forming the patterns of the through hole and the recess in the insulating layer comprises:

by patterning process, forming the through hole in the gate insulating layer corresponding to a connection area of the first drain electrode and the second gate electrode, and forming the recess in the gate insulating layer corresponding to the overlapped area of the second drain electrode and the second gate electrode.

11. The method for manufacturing the array substrate according to claim 9, wherein the insulating layer comprises a gate insulating layer formed on the first gate electrode and the second gate electrode and an insulating interlayer formed on the first active layer and the second active layer; and the patterns of the through hole and the recess are formed in the insulating layer by one patterning process.

12. The method for manufacturing the array substrate according to claim 11, wherein forming the patterns of the through hole and the recess in the insulating layer comprises:

by patterning process, forming a first through hole running through the gate insulating layer and the insulating interlayer at a connection area of the first drain electrode and the second gate electrode; forming a second through hole running through the insulating interlayer at a connection area of the first source electrode and the first active layer; forming a third through hole running through the insulating interlayer at a connection area of the first drain electrode and the first active layer; forming a fourth through hole running through the insulating interlayer at a connection area of the second source electrode and the second active layer; and forming the recess at the overlapped area of the second drain electrode and the second gate electrode.

13. The method for manufacturing the array substrate according to claim 12, wherein forming the recess at the overlapped area of the second drain electrode and the second gate electrode comprises:

forming the recess in the insulating interlayer corresponding to the overlapped area; or, forming a through hole in the insulating interlayer corresponding to the overlapped area, and the through hole and a surface of the gate insulating

layer forming the recess; or, forming a through hole at the corresponding overlapped area on the insulating interlayer, forming a sub-recess in the gate insulating layer corresponding to overlapped area, and the through hole and the sub-recess forming the recess.

14. An OLED display device, comprising the array substrate according to any one of claims 1 to 8.

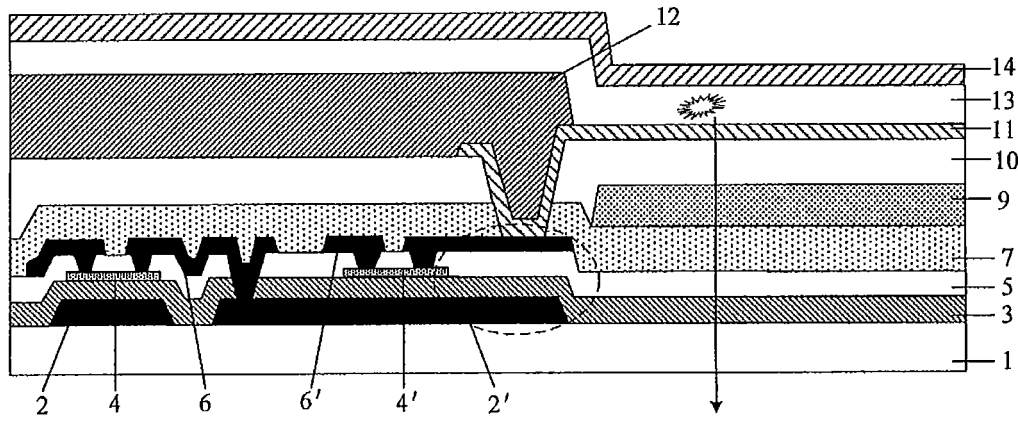


FIG. 1

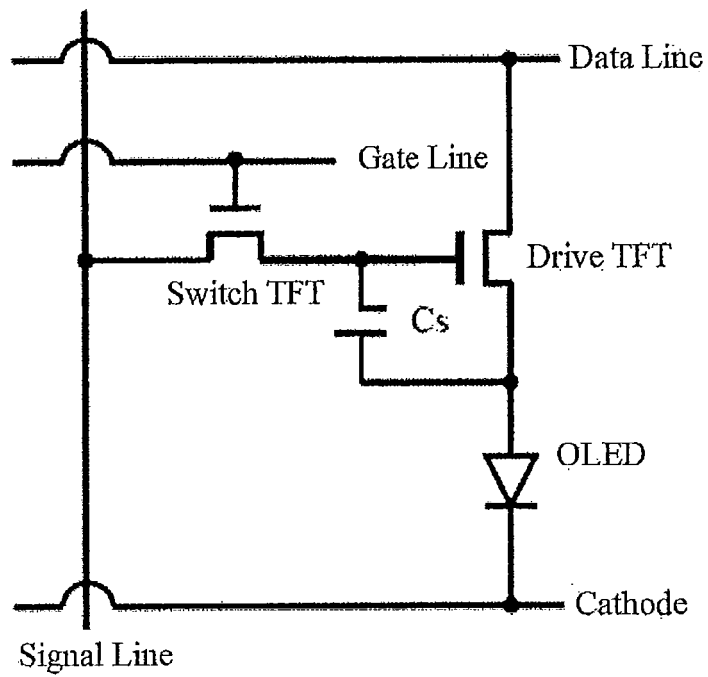


FIG. 2

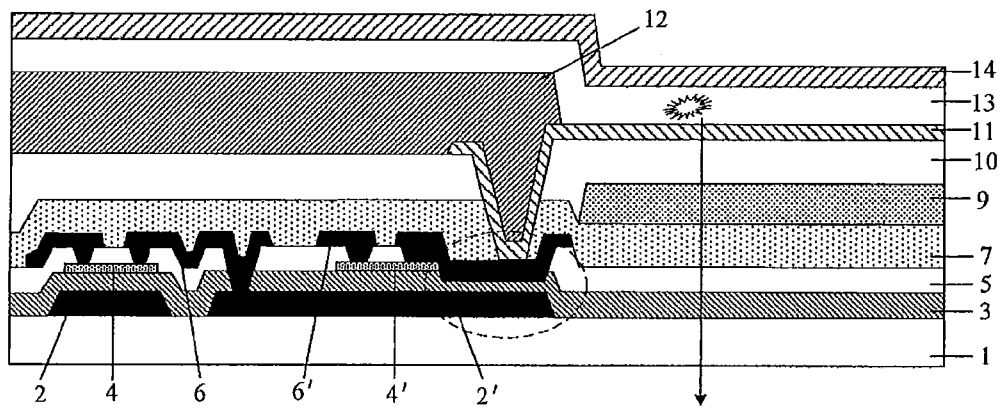


FIG. 3

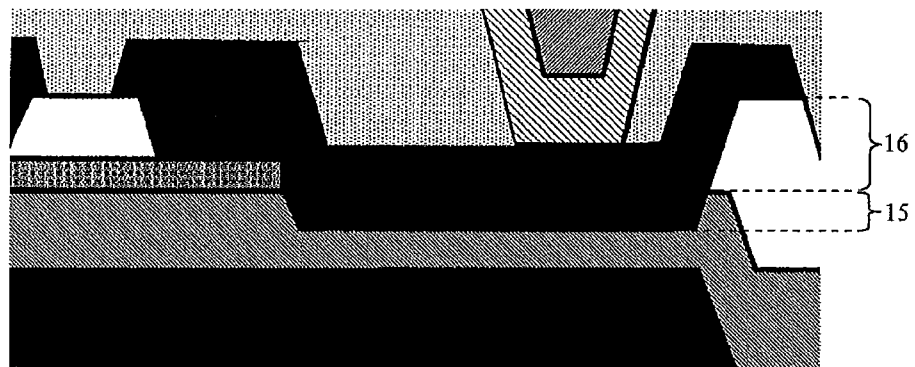


FIG. 4

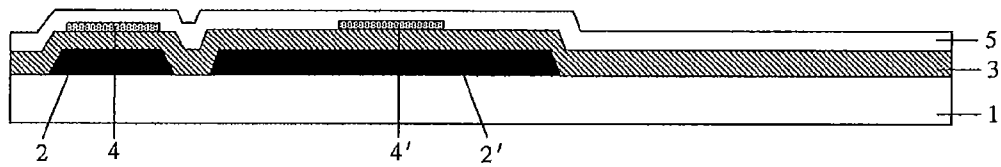


FIG. 5

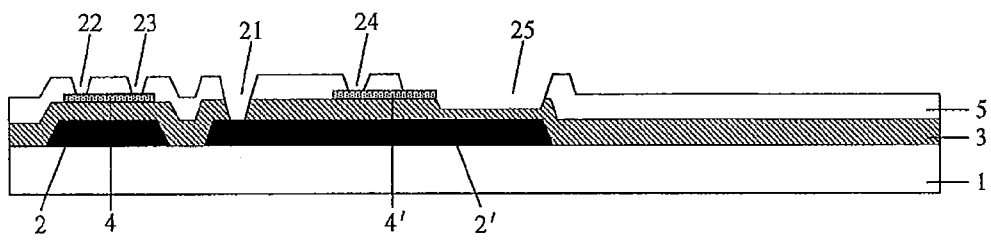


FIG. 6

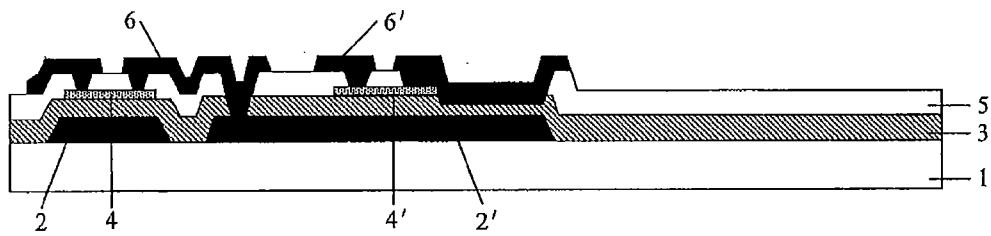


FIG. 7



EUROPEAN SEARCH REPORT

Application Number
EP 13 19 6455

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 2007/263164 A1 (KUMAGAI MINORU [JP]) 15 November 2007 (2007-11-15) * paragraph [0050]; figures 2,5,7A-10B *	1-14	INV. H01L27/12
Y	EP 1 865 371 A2 (SAMSUNG ELECTRONICS CO LTD [KR]) 12 December 2007 (2007-12-12) * the whole document *	1-14	
A	JP H03 280018 A (SONY CORP) 11 December 1991 (1991-12-11) * abstract *	1-14	
Y	US 2007/109453 A1 (KANEKO HIDEKI [JP] ET AL) 17 May 2007 (2007-05-17) * paragraph [0004] * * paragraph [0009] - paragraph [0011] * * figures 4,8 *	1-14	
Y	US 2011/074749 A1 (HIGASHI TOSHIAKI [JP]) 31 March 2011 (2011-03-31) * figures 3,6A,6B,10A-19 *	1-14	
A	US 2012/211750 A1 (KAKINUMA NOBUAKI [JP]) 23 August 2012 (2012-08-23) * figures 1,4 *	1-14	TECHNICAL FIELDS SEARCHED (IPC)
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A	JP 2008 170664 A (EPSON IMAGING DEVICES CORP) 24 July 2008 (2008-07-24) * figures 2,4,5 *	1-14	
A	GB 2 431 504 A (LG PHILIPS LCD CO LTD [KR] LG PHILIPH LCD CO LTD [KR]; LG DISPLAY CO L) 25 April 2007 (2007-04-25) * the whole document *	1-14	
The present search report has been drawn up for all claims			
Place of search Berlin		Date of completion of the search 7 March 2014	Examiner Hoffmann, Niels
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 13 19 6455

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07-03-2014

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专利名称(译)	阵列基板，其制造方法和OLED显示装置		
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申请号	EP2013196455	申请日	2013-12-10
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优先权	201210536938.6 2012-12-12 CN		
外部链接	Espacenet		

摘要(译)

提供一种阵列基板，其制造方法以及OLED显示装置。阵列基板包括设置在基板上的多个像素单元，其中每个像素单元包括形成在基板上的TFT结构和由TFT结构驱动的OLED；TFT结构包括驱动TFT。驱动TFT的漏极与OLED连接；驱动TFT的栅电极和漏电极至少部分重叠以形成存储电容器。在对应于重叠区域的介于栅电极和漏电极之间的绝缘层中形成凹槽，使得栅电极和漏电极之间的距离小于对应于非重叠的绝缘层的厚度。区。

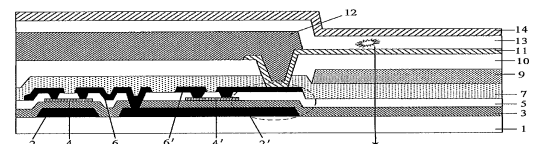


FIG. 1

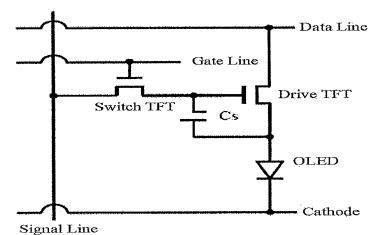


FIG. 2