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(54) Display device

(57) According to one embodiment, a display device (110, 112, 114, 210, 212) includes a substrate (10), a thin film transistor (12), a passivation film (13), a hydrogen barrier film (14), a pixel electrode (16), an organic light emitting layer (18), an opposite electrode (20), and a sealing film (22). The thin film transistor (12) is provided on a major surface of the substrate (10). The thin film transistor (12) includes a gate electrode (33), a gate insulating film (34), a semiconductor film (35), a first conducting portion (31), and a second conducting portion

(32). The passivation film (13) is provided on the thin film transistor (12). The hydrogen barrier film (14) is provided on the passivation film (13). The pixel electrode (16) is electrically connected to one of the first conducting portion (31) and the second conducting portion (32). The organic light emitting layer (18) is provided on the pixel electrode (16). The opposite electrode (20) is provided on the organic light emitting layer (18). The sealing film (22) is provided on the hydrogen barrier film (14) and the opposite electrode (20).

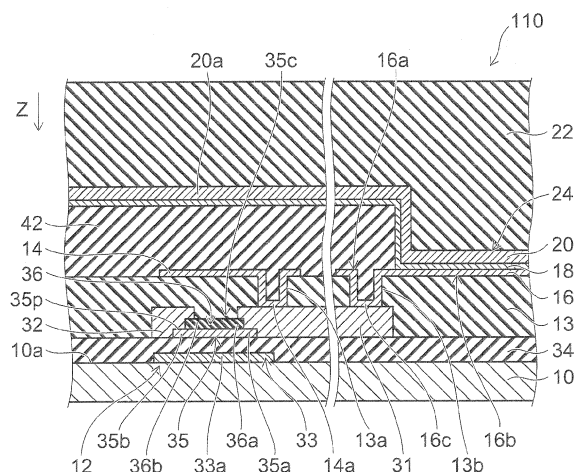


FIG. 1

Description

FIELD

[0001] Embodiments described herein relate generally to a display device.

BACKGROUND

[0002] There is an active matrix display device in which a switching element such as a thin film transistor controls a current passing through an organic EL (Electro-Luminescent) device. It is desired to improve image quality in this display device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003]

FIG. 1 is a schematic cross-sectional view illustrating the configuration of a display device according to a first embodiment;

FIG. 2 is an equivalent circuit diagram illustrating the configuration of the display device according to the first embodiment;

FIG. 3 is a graph illustrating the characteristics of a display device according to a reference sample;

FIG. 4A to FIG. 4D are schematic cross-sectional views illustrating a method for manufacturing the display device according to the first embodiment;

FIG. 5 is a flowchart illustrating a method for manufacturing the display device according to the first embodiment;

FIG. 6 is an equivalent circuit diagram illustrating the configuration of another display device according to the first embodiment;

FIG. 7 is a schematic cross-sectional view illustrating the configuration of still another display device according to the first embodiment;

FIG. 8A and FIG. 8B are schematic views illustrating the configuration of a display device according to a second embodiment; and

FIG. 9 is a schematic cross-sectional view illustrating the configuration of another display device according to the second embodiment.

DETAILED DESCRIPTION

[0004] According to one embodiment, a display device includes a substrate, a thin film transistor, a passivation film, a hydrogen barrier film, a pixel electrode, an organic light emitting layer, an opposite electrode, and a sealing film. The substrate has a major surface. The substrate is light transmissive. The thin film transistor is provided on the major surface. The thin film transistor includes a gate electrode, a gate insulating film, a semiconductor film, a first conducting portion, and a second conducting portion. The gate electrode is provided on the major sur-

face. The gate insulating film is provided on the gate electrode. The semiconductor film is provided on the gate insulating film. The semiconductor film includes a first region, a second region apart from the first region, and a third region provided between the first region and the second region. The first conducting portion is electrically connected to the first region. The second conducting portion is electrically connected to the second region. The second conducting portion is provided apart from the first conducting portion. The passivation film is provided on the thin film transistor. The passivation film is insulative. The hydrogen barrier film is provided on the passivation film. The hydrogen barrier film overlaps with the semiconductor film when projected onto a plane parallel with the major surface. The pixel electrode is electrically connected to one of the first conducting portion and the second conducting portion. The pixel electrode is light transmissive. The organic light emitting layer is provided on the pixel electrode. The opposite electrode is provided on the organic light emitting layer. The sealing film is provided on the hydrogen barrier film and the opposite electrode.

[0005] Various embodiments will be described hereinafter with reference to the accompanying drawings.

[0006] It is noted that the drawings are schematic or conceptual. The relationship between the thicknesses and widths of portions, a ratio of size between portions, or the like are not necessarily the same as real ones. Moreover, even in the case of expressing the same portions, dimensions and ratios between the portions are sometimes expressed differently depending on the drawings.

[0007] In the specification and drawings, components similar to those described or illustrated in a drawing thereinafter are marked with the identical reference numerals, and a detailed description is omitted as appropriate.

First Embodiment

[0008] FIG. 1 is a schematic cross-sectional view illustrating the configuration of a display device according to a first embodiment.

[0009] As shown in FIG. 1, a display device 110 according to the embodiment includes a substrate 10, a thin film transistor 12, a passivation film 13, a hydrogen barrier film 14, a pixel electrode 16, an organic light emitting layer 18, an opposite electrode 20, and a sealing film 22.

[0010] The pixel electrode 16, the organic light emitting layer 18, and the opposite electrode 20 form an organic EL light emitting element portion 24. In this example, the pixel electrode 16 is served as an anode and the opposite electrode 20 is served as a cathode. In the embodiment, the pixel electrode 16 may be served as a cathode and the opposite electrode 20 may be served as an anode. The light emission of the light emitting element portion 24 is driven by the thin film transistor 12. In the display device 110, the combinations of the thin film transistors

12 and the light emitting element portions 24 are disposed in a matrix configuration. The drive of the thin film transistors 12 and the light emission of the light emitting element portions 24 in association with the drive are controlled to display pictures. The display device 110 is an active matrix display device using an organic EL device.

[0011] The substrate 10 has a major surface 10a. A light transmissive material, for example, is used for the substrate 10. A glass material or a resin material, for example, is used for the substrate 10. A light transmissive and flexible material is used for the substrate 10. A resin material such as polyimide, for example, is used for the substrate 10.

[0012] The thin film transistor 12 is provided on a major surface 10a of the substrate 10.

[0013] The thin film transistor 12 includes a first conducting portion 31, a second conducting portion 32, a gate electrode 33, a gate insulating film 34, a semiconductor film 35, and a channel protection film 36.

[0014] The gate electrode 33 is provided on the major surface 10a of the substrate 10. A high melting point metal such as molybdenum tungsten (MoW), molybdenum tantalum (MoTa) and tungsten (W), for example, is used for the gate electrode 33.

[0015] The gate insulating film 34 is provided on the gate electrode 33. In this example, the gate insulating film 34 is provided on throughout the major surface 10a so as to cover the gate electrode 33. An insulative and light transmissive material, for example, is used for the gate insulating film 34. One of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, for example, is used for the gate insulating film 34.

[0016] The semiconductor film 35 is provided on the gate insulating film 34. The gate insulating film 34 is provided between the gate electrode 33 and the semiconductor film 35, and insulates the gate electrode 33 from the semiconductor film 35. An oxide semiconductor including at least one of In, Ga, and Zn, for example, is used for the semiconductor film 35. Namely, an In-Ga-Zn-O oxide semiconductor, an In-Ga-O oxide semiconductor, and an In-Zn-O oxide semiconductor, for example, are used for the semiconductor film 35. The semiconductor film 35 is of an n-type or of a p-type. In the following, in this example, the case will be described where the semiconductor film 35 is of an n-type.

[0017] The first conducting portion 31 is provided on the gate insulating film 34. A part of the first conducting portion 31 is provided on the semiconductor film 35, and contacts the semiconductor film 35. Consequently, the first conducting portion 31 is electrically connected to the semiconductor film 35. The second conducting portion 32 is provided on the gate insulating film 34. The second conducting portion 32 is disposed apart from the first conducting portion 31. A part of the second conducting portion 32 is provided on the semiconductor film 35, and contacts the semiconductor film 35. Consequently, the second conducting portion 32 is electrically connected to the semiconductor film 35. Ti, Al, Mo, and the like, for

example, are used for the first conducting portion 31 and the second conducting portion 32. The first conducting portion 31 and the second conducting portion 32 may be a stacked body including at least one of Ti, Al and Mo, for example. The first conducting portion 31 is one of the source electrode and drain electrode of the thin film transistor 12. The second conducting portion 32 is the other of the source electrode and drain electrode of the thin film transistor 12. In the following, in this example, the case will be described where the first conducting portion 31 is the source electrode and the second conducting portion 32 is the drain electrode.

[0018] The channel protection film 36 is provided on the semiconductor film 35. The channel protection film 36 protects the semiconductor film 35. A silicon oxide film, for example, is used for the channel protection film 36.

[0019] The first conducting portion 31 covers a first portion 36a of the channel protection film 36. The second conducting portion 32 covers a second portion 36b of the channel protection film 36. The first conducting portion 31 covers a first region 35a of the semiconductor film 35. The second conducting portion 32 covers a second region 35b of the semiconductor film 35. The second region 35b is apart from the first region in a direction perpendicular to the major surface 10a. The semiconductor film 35 has a third region 35c provided between the first region and the second region. The third region 35c is not covered with the first conducting portion 31 and the second conducting portion 32. The gate electrode 33 has a portion 33a between the first conducting portion 31 and the second conducting portion 32 when seen in a direction perpendicular to a film surface 35p of the semiconductor film 35 (in the following, referred to as a Z-axis direction). Namely, the gate insulating film 34 is disposed between the gate electrode 33 and the third region 35c of the semiconductor film 35. The channel protection film 36 is provided at least on the third region 35c. When a voltage is applied to the gate electrode 33, a channel is generated in the semiconductor film 35 and a current passes between the first conducting portion 31 and the second conducting portion 32.

[0020] The passivation film 13 is provided on the thin film transistor 12. In this example, the passivation film 13 is provided on throughout the major surface 10a. The passivation film 13 covers the thin film transistor 12. The passivation film 13 is insulative. The passivation film 13 is also light transmissive. One of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, for example, is used for the passivation film 13.

[0021] The hydrogen barrier film 14 is provided on the passivation film 13. Namely, the passivation film 13 is provided between the thin film transistor 12 and the hydrogen barrier film 14. The hydrogen barrier film 14 overlaps with the semiconductor film 35 when projected onto a plane parallel with the major surface 10a. The hydrogen barrier film 14 covers the semiconductor film 35 through the passivation film 13. The hydrogen barrier film 14 cov-

ers at least the third region 35c in the semiconductor film 35. A conductive material with hydrogen barrier properties to suppress the penetration of hydrogen is used for the hydrogen barrier film 14. A metal material including one of Ti, Ta, TiN, and TaN, for example, is used for the hydrogen barrier film 14. An oxide including at least one of In, Zn, Ga, Ti, and Al, for example, is used for the hydrogen barrier film 14. For the oxide of the hydrogen barrier film 14, ITO (In-Ti-O), IZO (In-Zn-O), AZO (Al-Zn-O), IGZO (In-Ga-Zn-O), ZnO, and the like are used, for example.

[0022] The passivation film 13 is provided with a first opening 13a and a second opening 13b, and a part of the first conducting portion 31 is exposed from the first opening 13a and the second opening 13b. A part 14a of the hydrogen barrier film 14 contacts the first conducting portion 31 in the first opening 13a. Consequently, the hydrogen barrier film 14 is electrically connected to the first conducting portion 31.

[0023] The pixel electrode 16 is electrically connected to one of the first conducting portion 31 and the second conducting portion 32. In this example, the pixel electrode 16 is electrically connected to the first conducting portion 31.

[0024] The pixel electrode 16 is provided on the passivation film 13. The pixel electrode 16 has an opposing region 16a opposing the thin film transistor 12 and a non-opposing region 16b not opposing the thin film transistor 12 in the Z-axis direction. An electrically conductive and light transmissive material, for example, is used for the pixel electrode 16. ITO or the like, for example, is used for the pixel electrode 16. A part 16c of the opposing region 16a of the pixel electrode 16 contacts the first conducting portion 31 in the second opening 13b. Consequently, the pixel electrode 16 is electrically connected to the first conducting portion 31.

[0025] Consequently, the hydrogen barrier film 14 is electrically connected to the pixel electrode 16 through the first conducting portion 31. As described above, the hydrogen barrier film 14 is electrically connected to one of the first conducting portion 31 and the second conducting portion 32.

[0026] A planarization film 42 is provided on the hydrogen barrier film 14 and the opposing region 16a of the pixel electrode 16. An insulative material, for example, is used for the planarization film 42. One of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, for example, is used for the planarization film 42.

[0027] The organic light emitting layer 18 is provided on the non-opposing region 16b of the pixel electrode 16 and the planarization film 42. The organic light emitting layer 18 contacts the pixel electrode 16 in the non-opposing region 16b, for example. The planarization film 42 prevents the hydrogen barrier film 14 from contacting the organic light emitting layer 18, and prevents the opposing region 16a from contacting the organic light emitting layer 18. A stacked body having a hole transport layer, a light emitting layer, and an electron transport layer

er stacked on each other, for example, is used for the organic light emitting layer 18.

[0028] The opposite electrode 20 is provided on the organic light emitting layer 18. The opposite electrode 20 is provided on the planarization film 42, and has a portion 20a extending on the semiconductor film 35 and the hydrogen barrier film 14. A conductive material is used for the opposite electrode 20. Al, MgAg, or the like, for example, is used for the opposite electrode 20. The light emitting element portion 24 is formed in the non-opposing region 16b, for example. In the light emitting element portion 24, a voltage is applied across the pixel electrode 16 and the opposite electrode 20 to emit light from the organic light emitting layer 18. The light emitted from the organic light emitting layer 18 passes through the passivation film 13, the gate insulating film 34, and the substrate 10, and goes to the outside. The display device 110 is a lower surface emitting display device.

[0029] The sealing film 22 is provided on the opposite electrode 20. The sealing film 22 covers the organic light emitting layer 18 and the opposite electrode 20. The sealing film 22 covers the thin film transistor 12 and the hydrogen barrier film 14. The sealing film 22 protects the organic light emitting layer 18 and the opposite electrode 20. One of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film, for example, is used for the sealing film 22. In the case of using these materials, the sealing film 22 includes hydrogen of 10^{19} atoms/cm³ or more.

[0030] The hydrogen barrier film 14 suppresses hydrogen included in the sealing film 22 that reaches the semiconductor film 35 and adversely affects the performance of the thin film transistor 12.

[0031] FIG. 2 is an equivalent circuit diagram illustrating the configuration of the display device according to the first embodiment.

[0032] As shown in FIG. 2, the display device 110 includes the thin film transistor 12, the hydrogen barrier film 14, the light emitting element portion 24, a switch transistor 50, a signal line 51, a gate line 52, and a power supply line 53.

[0033] A source 12S (the first conducting portion 31) of the thin film transistor 12 is electrically connected to an anode 24A (the pixel electrode 16) of the light emitting element portion 24. A drain 12D (the second conducting portion 32) of the thin film transistor 12 is electrically connected to the power supply line 53 that supplies a supply voltage. A gate 12G (the gate electrode 33) of the thin film transistor 12 is electrically connected to a source 50S of the switch transistor 50.

[0034] An opposite electrode 24C (the opposite electrode 20) of the light emitting element portion 24 is connected to a common power supply 25 (a ground, for example). A drain 50D of the switch transistor 50 is electrically connected to the signal line 51. A gate 50G of the switch transistor 50 is electrically connected to the gate line 52.

[0035] The hydrogen barrier film 14 contacts the first conducting portion 31 through the part 14a, and is elec-

trically connected to the source 12S of the thin film transistor 12 as described above. The hydrogen barrier film 14 is electrically connected to the anode 24A of the light emitting element portion 24 through the source 12S.

[0036] In the display device 110, a voltage is applied to the gate 50G of the switch transistor 50 through the gate line 52 to turn the switch transistor 50 in the ON state. A voltage is simultaneously applied to the signal line 51, and the voltage is applied to the gate 12G of the thin film transistor 12 through the signal line 51 and the switch transistor 50 in the ON state. Consequently, a current according to the voltage of the gate 12G passes through the light emitting element portion 24, and light is emitted from the light emitting element portion 24 at luminance according to the voltage of the gate 12G.

[0037] In the following, an exemplary deterioration in the performance of the thin film transistor 12 will be described.

[0038] FIG. 3 is a graph illustrating the characteristics of a display device according to a reference sample.

[0039] The horizontal axis in FIG. 3 represents a gate voltage V_g to be applied to the gate 12G of the thin film transistor 12. The vertical axis in FIG. 3 represents a current I_d passing across the drain 12D and the source 12S of the thin film transistor 12.

[0040] A sample L1 shown in FIG. 3 is a sample in which the thin film transistor 12 was formed on the substrate 10 and the passivation film 13 was formed thereon. A sample L2 is a sample in which SiN was further formed on the sample L1 by PE-CVD (Plasma-Enhanced Chemical Vapor Deposition) as the sealing film 22. In the sample L2, the hydrogen barrier film 14 was not provided. A sample L3 is a sample in which the sample L2 was annealed at a temperature of 100°C for one hour.

[0041] As shown in FIG. 3, in the sample L1, appropriate threshold characteristics are obtained in the thin film transistor 12. In the sample L2, the threshold voltage of the thin film transistor 12 is greatly shifted to the negative side. When annealing is performed as in the sample L3, the threshold voltage is reducing to turn into the normally on state.

[0042] From the comparison between the sample 1 and the sample L2, it can be considered that the shift of the threshold voltage is caused by the sealing film 22. Since a reduction in the resistance of the semiconductor film 35 further advances by annealing at a low temperature of about 100°C, it can be considered that a faulty mode occurs in which some impurity is diffused. More specifically, it can be considered that hydrogen included in the sealing film 22 is diffused to the lower side to deoxidize the IGZO film in the channel for a reduction in the resistance and the threshold voltage of the thin film transistor 12 fluctuates.

[0043] In an actual display device in which the thin film transistor 12 and the organic light emitting layer 18 are combined, the opposite electrode 20 including a metal material (Al, for example) is provided between the thin film transistor 12 and the sealing film 22. It is usually

considered that hydrogen included in the sealing film 22 is blocked at the opposite electrode 20 and does not reach the semiconductor film 35 of the thin film transistor 12.

[0044] However, even in the case where the opposite electrode 20 is provided between the semiconductor film 35 and the sealing film 22, the shift of the threshold voltage is insufficiently suppressed. Namely, the opposite electrode 20 made of a metal material such as Al does not provide effect enough to block hydrogen in the sealing film 22.

[0045] On the contrary, in the configuration in which the hydrogen barrier film 14 with a low hydrogen permeability is formed on the thin film transistor 12 other than the opposite electrode 20 such as Al, the fluctuation of the threshold voltage is reduced after forming the sealing film 22.

[0046] In the display device 110 according to the embodiment provided with the hydrogen barrier film 14, the shift of the threshold voltage after annealing can be suppressed after forming the sealing film 22. Thereby, a high image quality can be obtained in the display device 110.

[0047] As described above, the hydrogen barrier film 14 with a low hydrogen permeability (that is, the hydrogen barrier properties are high) is provided to suppress the fluctuation of the threshold voltage.

[0048] Ti, Ta, TiN, TaN, and the like have a low hydrogen permeability. An oxide including at least one of In, Zn, Ga, Ti, and Al has a low hydrogen permeability. These materials are used for the hydrogen barrier film 14 to effectively suppress the fluctuation of the threshold voltage.

[0049] In the case of using a metal material including one of Ti, Ta, TiN, and TaN for the hydrogen barrier film 14, the thin film transistor 12 can be shielded from the light. Thereby, the characteristic variation (optical leakage) of the thin film transistor 12 caused by light incident to the thin film transistor 12 can be suppressed.

[0050] In the embodiment, the hydrogen barrier film 14 is electrically connected to the source 12S of the thin film transistor 12. Thereby, such an event that the hydrogen barrier film 14 provided on the thin film transistor 12 is charged and the thin film transistor 12 is turned into the ON state unintentionally can be suppressed, for example. A change in the characteristics of the thin film transistor 12 can also be suppressed, which is caused by the unnecessary back gate effect from the potential of the opposite electrode 24C of the light emitting element portion 24.

[0051] FIG. 4A to FIG. 4D are schematic cross-sectional views illustrating a method for manufacturing the display device according to the first embodiment.

[0052] As shown in FIG. 4A, in the manufacture of the display device 110, the thin film transistor 12 is formed on the major surface 10a of the substrate 10. In forming the thin film transistor 12, the gate electrode 33 is formed on the major surface 10a. The gate insulating film 34 is formed on the major surface 10a and the gate electrode

33. The semiconductor film 35 is formed on the gate insulating film 34. The channel protection film 36 is formed on the semiconductor film 35. The first conducting portion 31 and the second conducting portion 32 are formed on the gate insulating film 34, the semiconductor film 35, and the channel protection film 36.

[0053] As shown in FIG. 4B, the passivation film 13 is formed on the thin film transistor 12. For example, a SiO_2 film to be the passivation film 13 is formed by PE-CVD. The first opening 13a and the second opening 13b are formed on the SiO_2 film. The thickness of the passivation film 13 is 200 nm (100 nm or more and 300 nm or less), for example. The hydrogen barrier film 14 and the pixel electrode 16 are formed on the passivation film 13. For example, a Ti film to be the hydrogen barrier film 14 is formed by sputtering, and processed in a predetermined shape to obtain the hydrogen barrier film 14. The thickness of the hydrogen barrier film 14 is 50 nm (20 nm or more and 150 nm or less), for example. An ITO film to be the pixel electrode 16 is formed by sputtering or the like, and processed in a predetermined shape to obtain the pixel electrode 16. The thickness of the pixel electrode 16 is 200 nm (100 nm or more and 200 nm or less), for example. The order of forming the hydrogen barrier film 14 and forming the pixel electrode 16 is optional. In the case where a material used for the pixel electrode 16 is used for the hydrogen barrier film 14, these process steps are simultaneously performed.

[0054] As shown in FIG. 4C, the planarization film 42 is formed on the hydrogen barrier film 14 and the opposing region 16a of the pixel electrode 16. For example, an organic resin to be the planarization film 42 is applied and patterned to obtain the planarization film 42. The organic light emitting layer 18 is formed on the planarization film 42 and the non-opposing region 16b of the pixel electrode 16. The organic light emitting layer 18 is formed by vapor deposition, for example.

[0055] As shown in FIG. 4D, the opposite electrode 20 is formed on the organic light emitting layer 18. For example, a stacked film of a LiF film and an Al film to be the opposite electrode 20 is formed by vapor deposition, and processed in a predetermined shape. The sealing film 22 is formed on the opposite electrode 20. As described above, the display device 110 is fabricated.

[0056] FIG. 5 is a flowchart illustrating a method for manufacturing the display device according to the first embodiment.

[0057] As shown in FIG. 5, the method for manufacturing the display device 110 includes Step S110 of forming the thin film transistor 12, Step S115 of forming the passivation film 13, Step S120 of forming the hydrogen barrier film 14 and the pixel electrode 16, Step S130 of forming the organic light emitting layer 18, Step S140 of forming the opposite electrode 20, and Step S150 of forming the sealing film 22.

[0058] In Step S110, the process described with reference to FIG. 4A is performed, for example. In Step 115 and Step S120, the process described with reference to

FIG. 4B is performed, for example. In Step S130, the process described with reference to FIG. 4C is performed, for example. In Step S140 and Step S150, the process described with reference to FIG. 4D is performed, for example.

[0059] The process step of forming the thin film transistor 12 (Step S110) can include forming the channel protection film 36 to cover the top surface of the semiconductor film 35.

[0060] In the manufacturing method, the hydrogen barrier film 14 can include one of Ti, Ta, TiN, and TaN. The hydrogen barrier film 14 can include an oxide including at least one of In, Zn, Ga, Ti, and Al.

[0061] The process step of forming the hydrogen barrier film 14 and the pixel electrode 16 (Step S120) can include electrically connecting the hydrogen barrier film 14 to one of the first conducting portion 31 and the second conducting portion 32 (the source 12S, for example). In the case where the semiconductor film 35 is of an n-type, the process step of forming the hydrogen barrier film 14 and the pixel electrode 16 (Step S120) can include electrically connecting the hydrogen barrier film 14 to the pixel electrode 16.

[0062] In the manufacturing method, the semiconductor film 35 can include an oxide semiconductor including at least one of In, Ga, and Zn. The sealing film 22 includes hydrogen of 10^{19} atoms/cm³ or more. In this case, the hydrogen barrier film 14 is provided to effectively suppress the fluctuation of the threshold voltage.

[0063] FIG. 6 is an equivalent circuit diagram illustrating the configuration of another display device according to the first embodiment.

[0064] As shown in FIG. 6, in a display device 112, a semiconductor film 35 of a thin film transistor 12 is of a p-type. A pixel electrode 16 is electrically connected to one of a first conducting portion 31 and a second conducting portion 32. In this example, the pixel electrode 16 is electrically connected to the first conducting portion 31 (a drain 12D). A hydrogen barrier film 14 is connected to the second conducting portion 32 (a source 12S), which is the other of the first conducting portion 31 and the second conducting portion 32. The hydrogen barrier film 14 is electrically connected to a power supply line 53 through the source 12S.

[0065] For example, like this example, in the case where the semiconductor film 35 is of a p-type, the process step of forming the hydrogen barrier film 14 and the pixel electrode 16 (Step S120) can include electrically connecting the hydrogen barrier film 14 to the other of the first conducting portion 31 and the second conducting portion 32 (the source 12S is the second conducting portion 32).

[0066] Also in the display device 112, since the hydrogen barrier film 14 is provided, the fluctuation of the characteristics of the thin film transistor 12 can be suppressed, and a display device with a high image quality can be provided.

[0067] FIG. 7 is a schematic cross-sectional view illus-

trating the configuration of still another display device according to the first embodiment.

[0068] As shown in FIG. 7, a display device 114 further includes a color filter 44. The color filter 44 is provided between a hydrogen barrier film 14 and a planarization film 42, and between a pixel electrode 16 and a passivation film 13. The color filter 44 has a different color for every pixel. For example, the color filter 44 is formed in which one of red, green, and blue color resin films (a color resist, for example) is applied and the color resin film is patterned. The film thickness of the color filter 44 is 2 μm , for example (1 μm or more and 3 μm or less, for example).

[0069] As described above, also in the display device 114 provided with the color filter 44 on the hydrogen barrier film 14, a change in the characteristics of the thin film transistor 12 can be suppressed, and a high image quality can be obtained.

[0070] The display device 114 can be manufactured as follows, for example.

[0071] After forming the thin film transistor 12, the passivation film 13 is formed. A SiO_2 film having a thickness of 100 nm or more and 300 nm or less, for example, is formed by PE-CVD as the passivation film 13. A SiN film, or a SiON_x film may be used for the passivation film 13. A Ti film to be the hydrogen barrier film 14 (a thickness of 20 nm or more and 100 nm or less) is further formed by sputtering, for example. This Ti film is processed to obtain the hydrogen barrier film 14. Red, green, and blue color resists are applied and processed to form the color filter 44. The pixel electrode 16 is formed on the color filter 44. The planarization film 42 is formed on the color filter 44 and the pixel electrode 16. An organic light emitting layer 18 and an opposite electrode 20 are sequentially formed on the pixel electrode 16 to form a sealing film 22. As described above, the display device 114 is fabricated.

Second Embodiment

[0072] FIG. 8A and FIG. 8B are schematic views illustrating the configuration of a display device according to a second embodiment.

[0073] FIG. 8A is a schematic cross-sectional view illustrating a display device 210. FIG. 8B is a schematic plan view illustrating the display device 210.

[0074] As shown in FIG. 8A and FIG. 8B, in the display device 210, a material to be a pixel electrode 16 is used for the material of a hydrogen barrier film 14. Namely, the material of the hydrogen barrier film 14 is substantially the same as the material of the pixel electrode 16. In this case, a metal oxide such as ITO, IZO, AZO, IGZO, and ZnO, for example, is used for the hydrogen barrier film 14 and the pixel electrode 16. The hydrogen barrier film 14 continues to the pixel electrode 16.

[0075] Also in the display device 210, the hydrogen barrier film 14 is provided to suppress the movement of hydrogen included in the sealing film 22 to the semicon-

ductor film 35 for improving image quality. Moreover, in the display device 210, the hydrogen barrier film 14 and the pixel electrode 16 can be formed simultaneously. Thereby, additional processes can be eliminated, and providing a high productivity.

[0076] In this example, the hydrogen barrier film 14 can include an oxide including at least one of In, Zn, Ga, Ti, and Al. These materials are a material used for the pixel electrode 16.

[0077] The process step of forming the hydrogen barrier film 14 and the pixel electrode 16 (Step S120) can include forming the hydrogen barrier film 14 using a material to be the pixel electrode 16. The hydrogen barrier film 14 continues to the pixel electrode 16. Thereby a high productivity can be obtained.

[0078] FIG. 9 is a schematic cross-sectional view illustrating the configuration of another display device according to the second embodiment.

[0079] As shown in FIG. 9, in a display device 212, a pixel electrode 16 and a hydrogen barrier film 14 continuing to the pixel electrode 16 are provided on a color filter 44. Also in the display device 212, the hydrogen barrier film 14 suppresses the movement of hydrogen included in a sealing film 22 to a semiconductor film 35 for improving image quality. Additional processes are also unnecessary, and productivity is also high.

[0080] According to the embodiment, a display device with a high image quality can be provided.

[0081] In the specification of the application, "perpendicular" and "parallel" refer to not only strictly perpendicular and strictly parallel but also include, for example, the fluctuation due to manufacturing processes, etc. It is sufficient to be substantially perpendicular and substantially parallel.

[0082] In the specification of the application, a state in which "a component is provided on another component" includes a state in which a component is directly provided on another component as well as a state in which a component is provided on another component with a different element inserted between the component and another component. A state in which "a component is stacked on another component" includes a state in which a component is stacked on another component to contact each other as well as a state in which a component is stacked on another component with a different element inserted between the component and another component. A state in which "a component opposes another component" includes a state in which a component directly faces another component as well as a state in which a component faces another component with a different element inserted between the component and another component.

[0083] As described above, the embodiments of the invention are described with reference to specific examples.

[0084] However, the embodiments of the invention are not limited to these specific examples. For example, the specific configurations of the components such as the substrate, the thin film transistor, the passivation film, the

hydrogen barrier film, the pixel electrode, the organic light emitting layer, the opposite electrode, the sealing film, the gate electrode, the gate insulating film, the semiconductor film, the first conducting portion, and the second conducting portion included in the display device are incorporated in the scope of the invention as long as a person skilled in the art appropriately selects components from the publicly known range to similarly implement the invention for obtaining the similar effect.

[0085] Further, any two or more components of the specific examples may be combined within the extent of technical feasibility and are included in the scope of the invention to the extent that the purport of the invention is included.

[0086] Moreover, all display devices practicable by an appropriate design modification by one skilled in the art based on the display device described above as embodiments of the invention also are within the scope of the invention to the extent that the spirit of the invention is included.

[0087] Various other variations and modifications can be conceived by those skilled in the art within the spirit of the invention, and it is understood that such variations and modifications are also encompassed within the scope of the invention.

[0088] While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the invention.

Claims

1. A display device (110, 112, 114, 210, 212) comprising:

a substrate (10) having a major surface (10a), the substrate (10) being light transmissive;
a thin film transistor (12) provided on the major surface (10), the thin film transistor (12) including:

a gate electrode (33) provided on the major surface (10a);
a gate insulating film (34) provided on the gate electrode (33);
a semiconductor film (35) provided on the gate insulating film (34), the semiconductor film (35) including a first region (35a), a second region (35b) apart from the first region (35a), and a third region (35c) provided be-

tween the first region (35a) and the second region (35b);

a first conducting portion (31) electrically connected to the first region (35a); and
a second conducting portion (32) electrically connected to the second region (35b) and provided apart from the first conducting portion (31);

a passivation film (13) provided on the thin film transistor (12), the passivation film (13) being insulative;

a hydrogen barrier film (14) provided on the passivation film (13) and overlapping with the semiconductor film (35) when projected onto a plane parallel with the major surface (10a);

a pixel electrode (16) electrically connected to one of the first conducting portion (31) and the second conducting portion (32), the pixel electrode (16) being light transmissive;

an organic light emitting layer (18) provided on the pixel electrode (16);

an opposite electrode (20) provided on the organic light emitting layer (18); and

a sealing film (22) provided on the hydrogen barrier film (14) and on the opposite electrode (20).

2. The device (110, 112, 114, 210, 212) according to claim 1, wherein the hydrogen barrier film (14) includes one of Ti, Ta, TiN and TaN.
3. The device (110, 112, 114, 210, 212) according to claim 1, wherein the hydrogen barrier film (14) includes an oxide including at least one of In, Zn, Ga, Ti, and Al.
4. The device (110, 112, 114, 210, 212) according to any of claims 1-3, wherein the hydrogen barrier film (14) is electrically connected to the one of the first conducting portion (31) and the second conducting portion (32).
5. The device (110, 114, 210, 212) according to any of claims 1-4, wherein
the semiconductor film (35) is of an n-type, and
the hydrogen barrier film (14) is electrically connected to the pixel electrode (16).
6. The device (112) according to any of claims 1-3, wherein
the semiconductor film (35) is of a p-type, and
the hydrogen barrier film (14) is electrically connected to the other of the first conducting portion (31) and the second conducting portion (32).
7. The device (110, 112, 114, 210, 212) according to any of claims 1-6, wherein the hydrogen barrier film (14) includes a material the same as a material of

the pixel electrode (16).

8. The device (210, 212) according to claim 7, wherein the hydrogen barrier film (14) continues to the pixel electrode (16). 5
9. The device (110, 112, 114, 210, 212) according to any of claims 7 and 8, wherein the pixel electrode (16) includes at least one of ITO, IZO, AZO, IGZO, and ZnO. 10
10. The device (110, 112, 114, 210, 212) according to any of claims 1-9, wherein the semiconductor film (35) includes an oxide semiconductor including at least one of In, Ga, and Zn. 15
11. The device (110, 112, 114, 210, 212) according to any of claims 1-10, wherein the sealing film (22) includes hydrogen of 10^{19} atoms/cm³ or more. 20
12. The device (110, 112, 114, 210, 212) according to claim 11, wherein the sealing film (22) includes at least one of a silicon oxide film, a silicon nitride film, and a silicon oxynitride film. 25
13. The device (110, 112, 114, 210, 212) according to any of claims 1-12, wherein the opposite electrode (20) extends on the semiconductor film (35) and on the hydrogen barrier film (14). 30
14. The device (110, 112, 114, 210, 212) according to any of claims 1-13, wherein the substrate (10) includes a resin material and is flexible. 35
15. The device (110, 112, 114, 210, 212) according to any of claims 1-14, wherein the gate insulating film (34) is disposed between the gate electrode (33) and the third region (35c). 40
16. The device (110, 112, 114, 210, 212) according to claim 15, wherein the thin film transistor (12) further includes a channel protection film (36) provided at least on the third region (35c). 45
17. The device (110, 112, 114, 210, 212) according to any of claims 1-16, wherein the opposite electrode (20) includes a metal material. 50
18. The device (110, 112, 114, 210, 212) according to any of claims 1-17, wherein a thickness of the hydrogen barrier film (14) is 20 nm or more and 150 nm or less. 55
19. The device (114) according to any of claims 1-18, further comprising a color filter (44), the passivation film (13) extending between the pixel electrode (16) and the major surface (10a), and the color filter (44) being provided between the pixel

electrode (16) and the passivation film (13) and on the hydrogen barrier film (14).

20. The device (212) according to any of claims 1-18, further comprising a color filter (44), the passivation film (13) extending between the pixel electrode (16) and the major surface (10a), and the color filter (44) being disposed between the pixel electrode (16) and the passivation film (13) and extending between the passivation film (13) and the hydrogen barrier film (14).

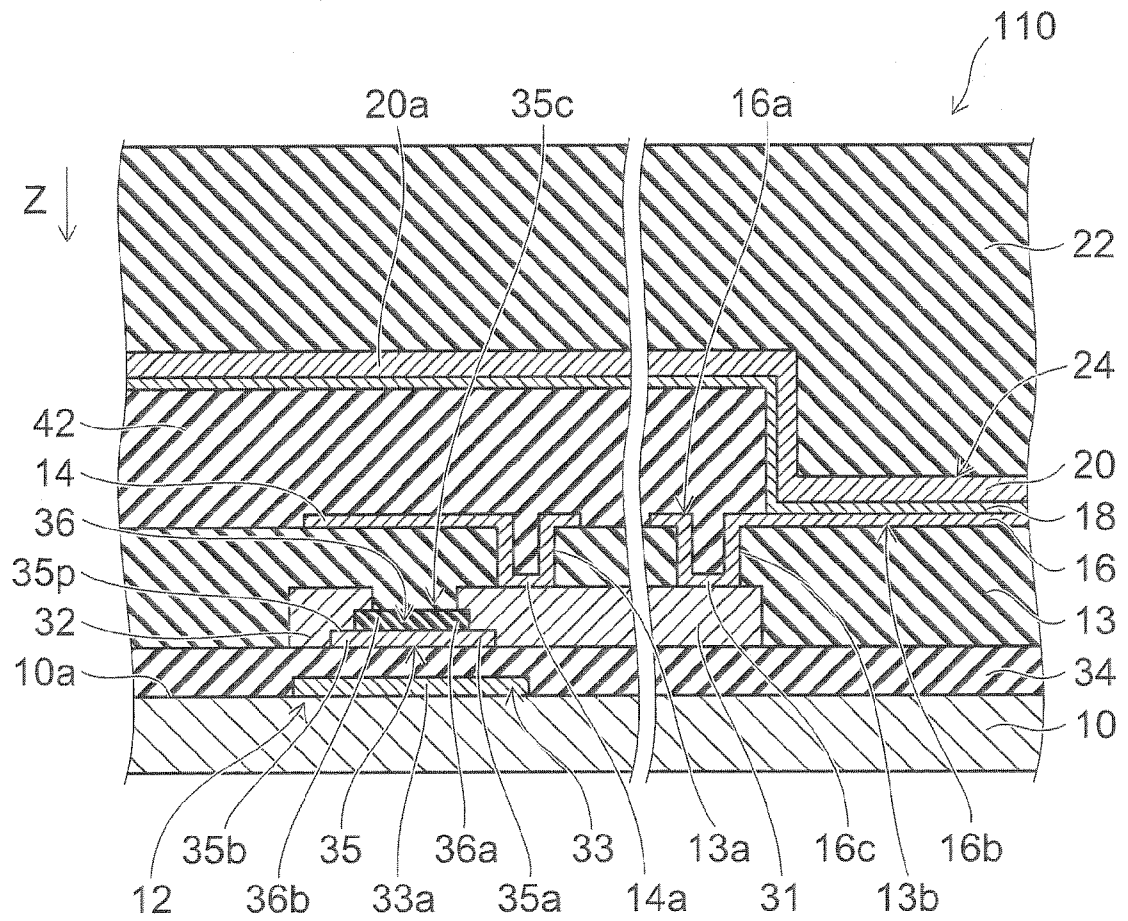


FIG. 1

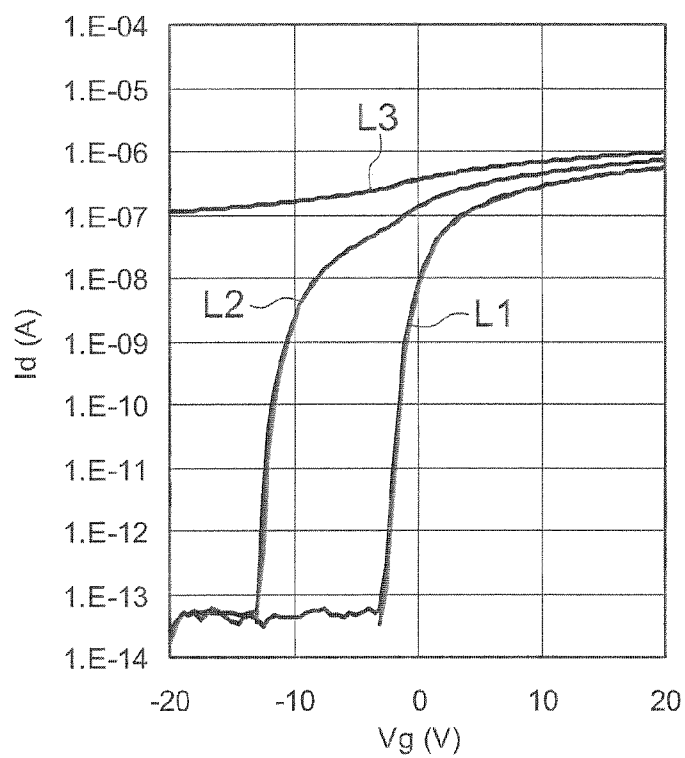
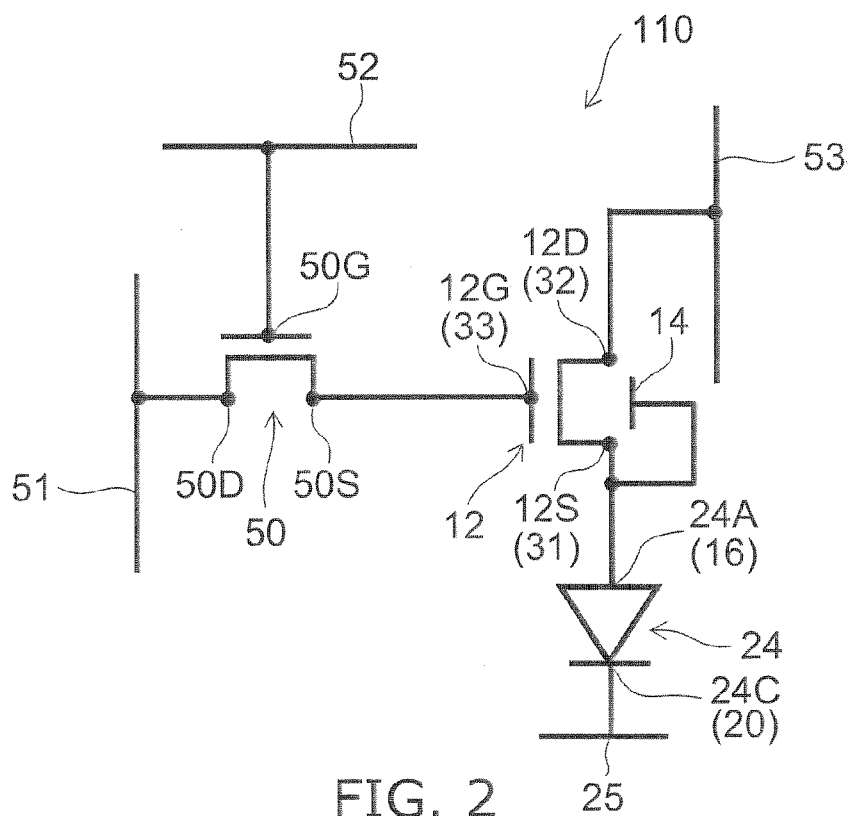


FIG. 3

FIG. 4A

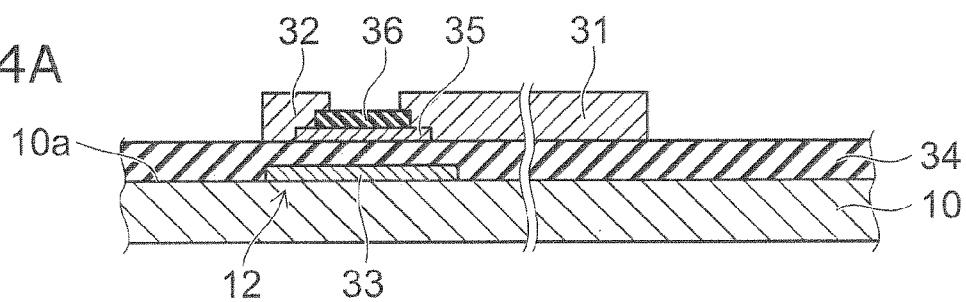


FIG. 4B

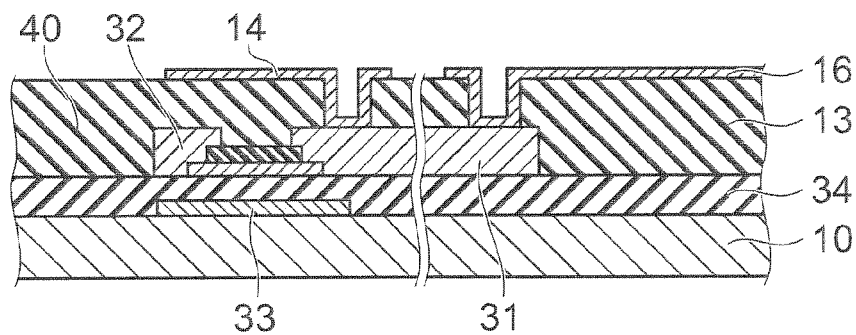


FIG. 4C

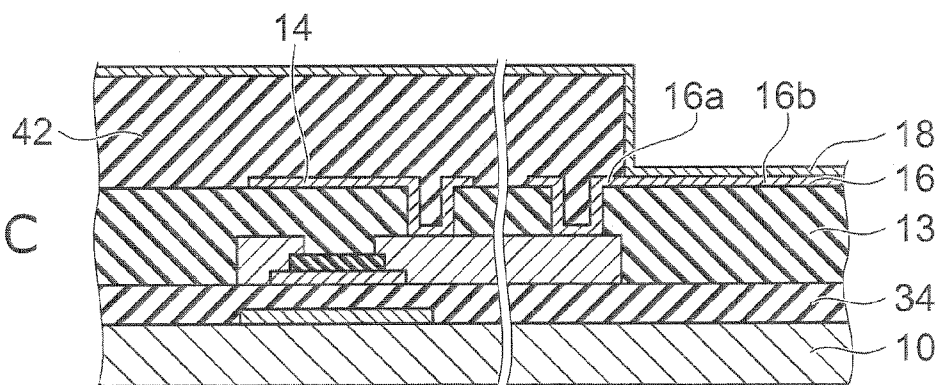
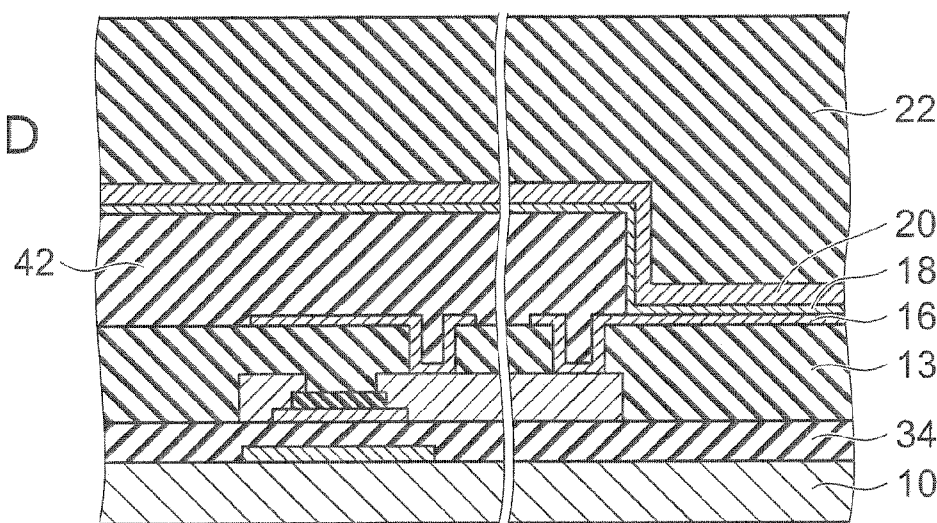


FIG. 4D



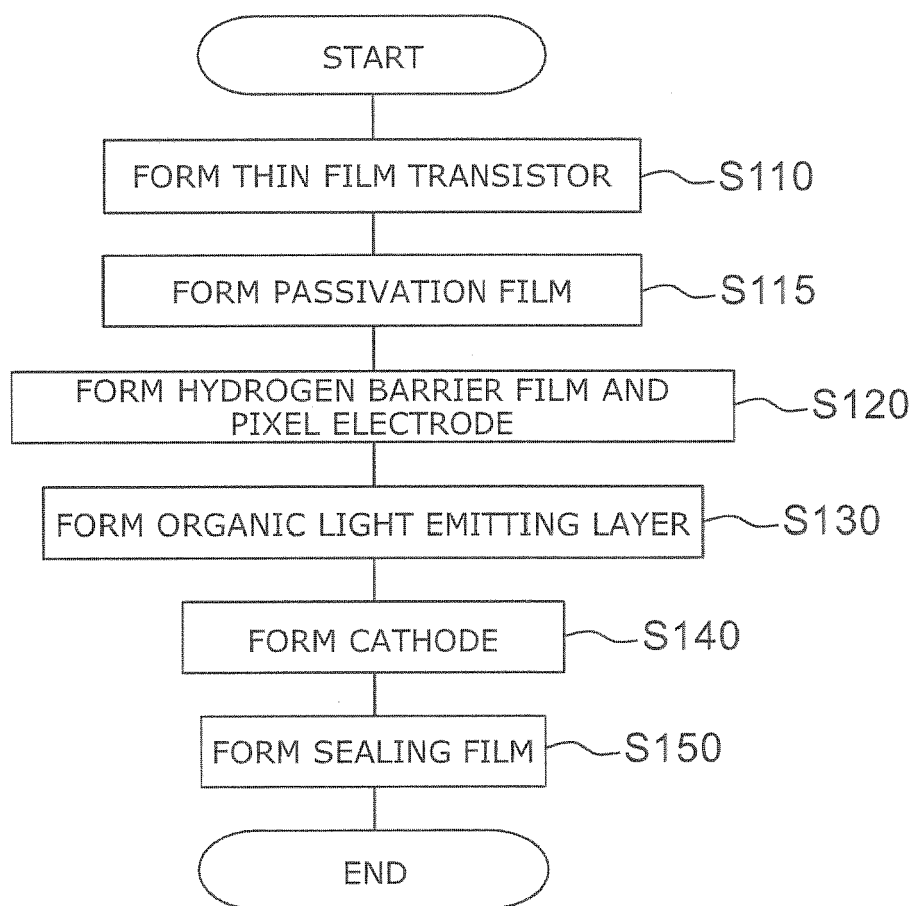


FIG. 5

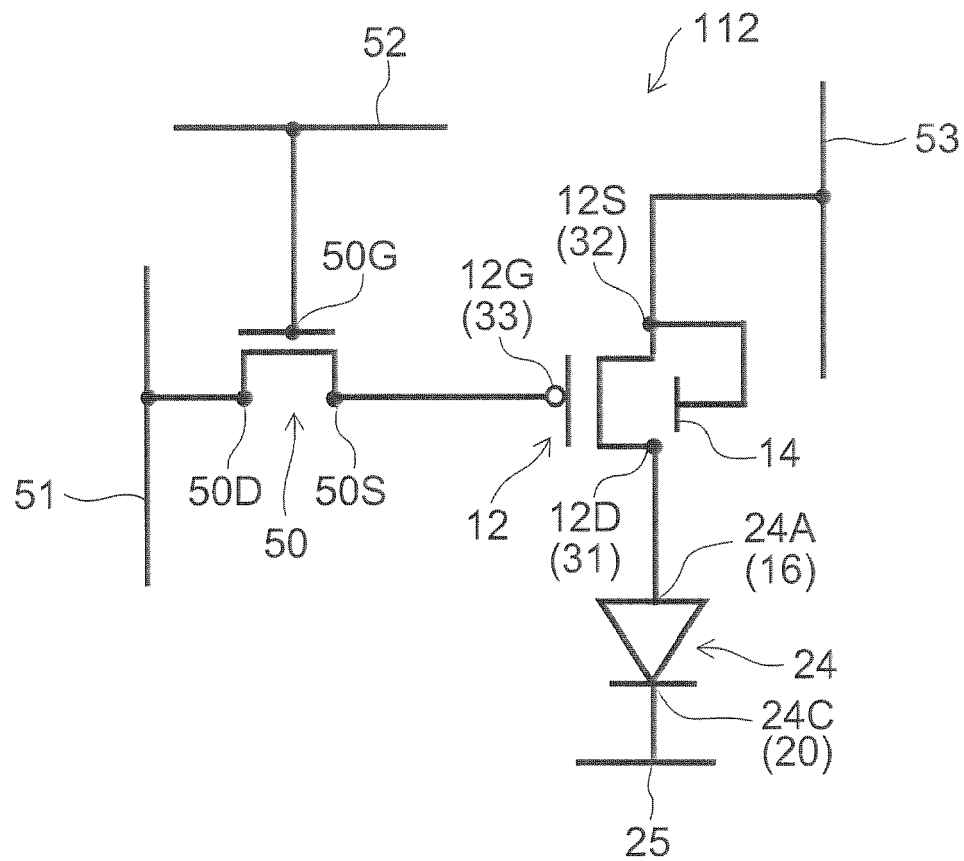


FIG. 6

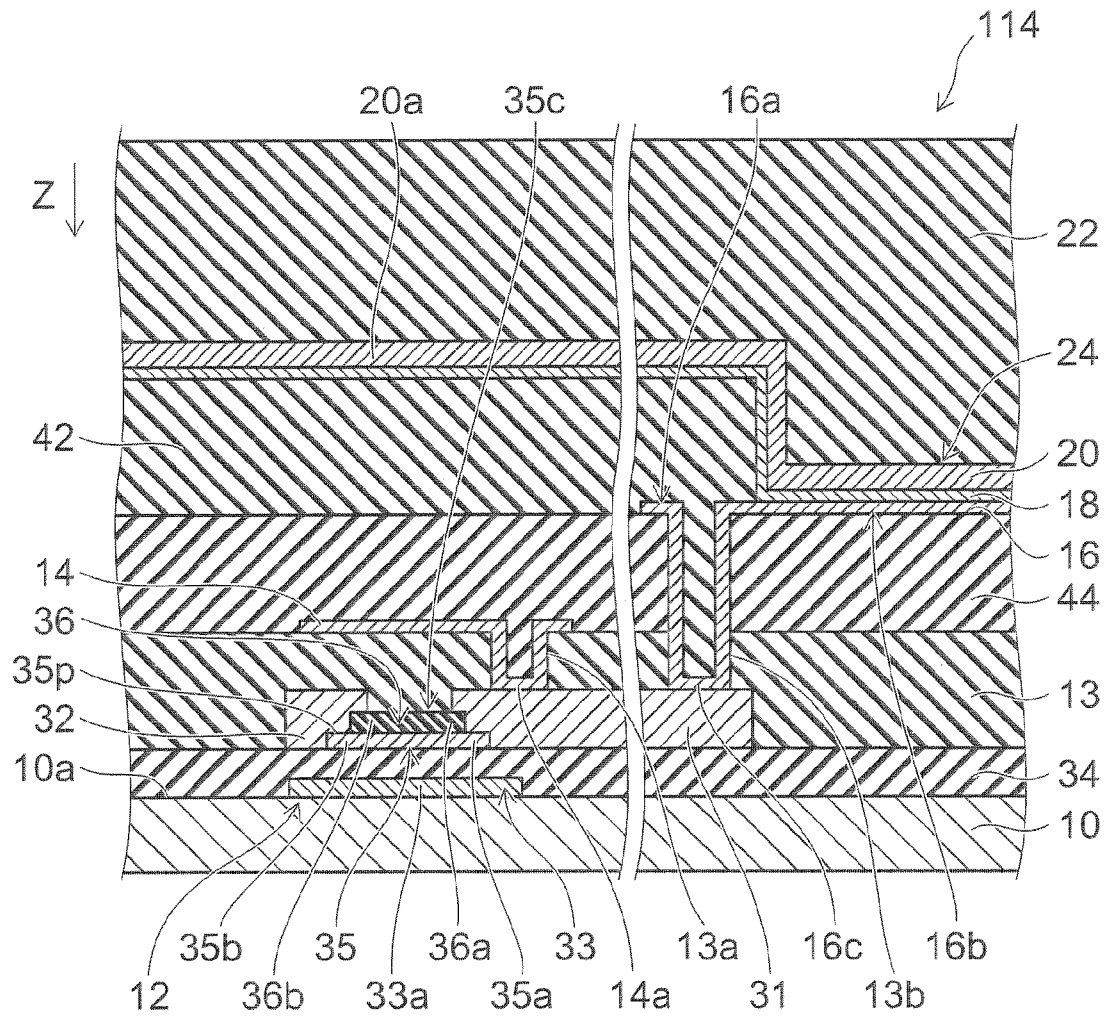


FIG. 7

FIG. 8A

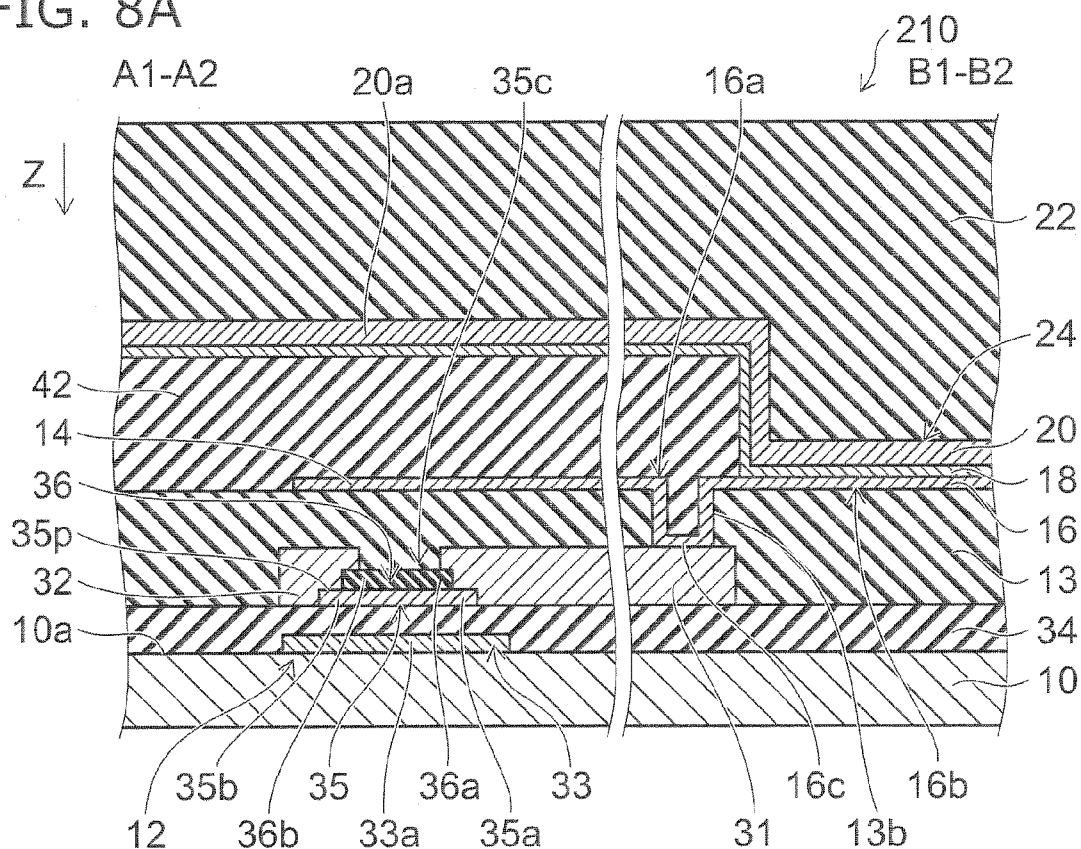
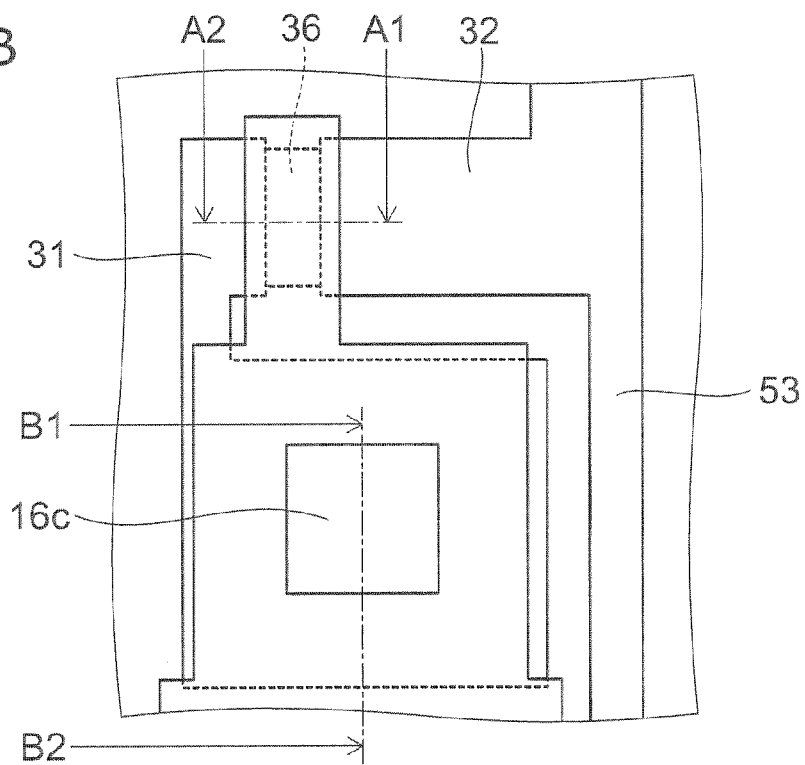


FIG. 8B



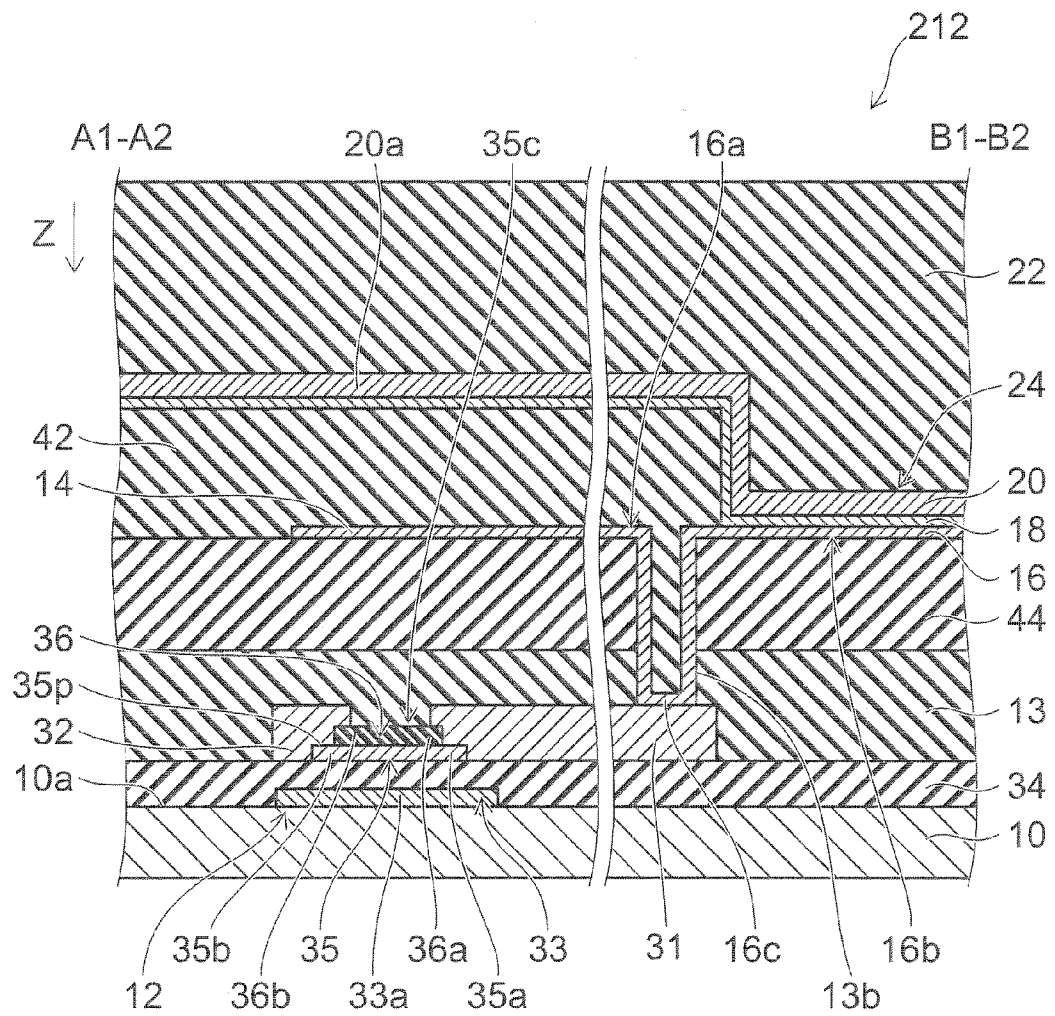


FIG. 9

专利名称(译)	显示设备		
公开(公告)号	EP2667413A2	公开(公告)日	2013-11-27
申请号	EP2013163916	申请日	2013-04-16
[标]申请(专利权)人(译)	株式会社东芝		
申请(专利权)人(译)	株式会社东芝		
当前申请(专利权)人(译)	株式会社东芝		
[标]发明人	SAITO NOBUYOSHI MIURA KENTARO NAKANO SHINTARO SAKANO TATSUNORI UEDA TOMOMASA YAMAGUCHI HAJIME		
发明人	SAITO, NOBUYOSHI MIURA, KENTARO NAKANO, SHINTARO SAKANO, TATSUNORI UEDA, TOMOMASA YAMAGUCHI, HAJIME		
IPC分类号	H01L27/32		
CPC分类号	H01L51/5203 H01L27/3262 H01L29/7869		
优先权	2012118789 2012-05-24 JP		
外部链接	Espacenet		

摘要(译)

根据一个实施例，显示装置（110,112,114,210,212）包括基板（10），薄膜晶体管（12），钝化膜（13），氢阻挡膜（14），像素电极（16），有机发光层（18），相对电极（20）和密封膜（22）。薄膜晶体管（12）设置在基板（10）的主表面上。薄膜晶体管（12）包括栅电极（33），栅极绝缘膜（34），半导体膜（35），第一导电部分（31）和第二导电部分（32）。钝化膜（13）设置在薄膜晶体管（12）上。氢阻挡膜（14）设置在钝化膜（13）上。像素电极（16）电连接到第一导电部分（31）和第二导电部分（32）中的一个。有机发光层（18）设置在像素电极（16）上。对电极（20）设置在有机发光层（18）上。密封膜（22）设置在氢阻挡膜（14）和相对电极（20）上。

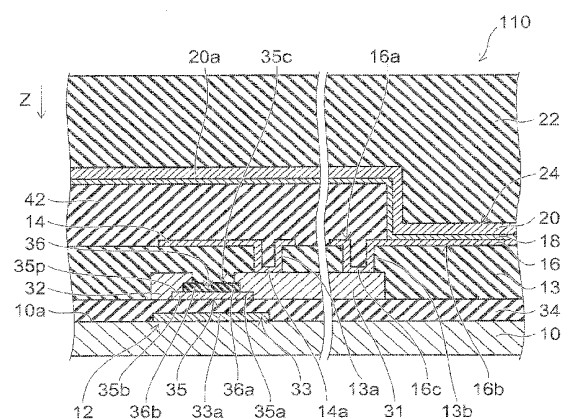


FIG. 1