(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 704 554 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
02.05.2012 Bulletin 2012/18

(21) Application number: **05702559.5**

(22) Date of filing: **04.01.2005**

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(86) International application number:
PCT/IB2005/050027

(87) International publication number:
WO 2005/069266 (28.07.2005 Gazette 2005/30)

(54) **ELECTROLUMINESCENT DISPLAY DEVICES WITH AN ACTIVE MATRIX**

ELEKTROLUMINESZENZ-DISPLAY-EINRICHTUNGEN MIT EINER AKTIVMATRIX

DISPOSITIFS D'AFFICHAGE ELECTROLUMINESCENTS

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU MC NL PL PT RO SE SI SK TR

(30) Priority: **07.01.2004 GB 0400213**

(43) Date of publication of application:
27.09.2006 Bulletin 2006/39

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EP 1 704 554 B1

Description

[0001] This invention relates to electroluminescent display devices, particularly active matrix display devices having thin film switching transistors associated with each pixel.

[0002] Matrix display devices employing electroluminescent, light-emitting, display elements are well known. The display elements may comprise organic thin film electroluminescent elements, for example using polymer materials, or else light emitting diodes (LEDs) using traditional III-V semiconductor compounds. Recent developments in organic electroluminescent materials, particularly polymer materials, have demonstrated their ability to be used practically for video display devices. These materials typically comprise one or more layers of a semiconducting conjugated polymer sandwiched between a pair of electrodes, one of which is transparent and the other of which is of a material suitable for injecting holes or electrons into the polymer layer.

[0003] The polymer material can be fabricated using a CVD process, or simply by a spin coating technique using a solution of a soluble conjugated polymer. Ink-jet printing may also be used. Organic electroluminescent materials exhibit diode-like I-V properties, so that they are capable of providing both a display function and a switching function, and can therefore be used in passive type displays. Alternatively, these materials may be used for active matrix display devices, with each pixel comprising a display element and a switching device for controlling the current through the display element.

[0004] Display devices of this type have current-driven display elements, so that a conventional, analogue drive scheme involves supplying a controllable current to the display element. It is known to provide a current source transistor as part of the pixel configuration, with the gate voltage supplied to the current source transistor determining the current through the display element. A storage capacitor holds the gate voltage after the addressing phase.

[0005] Figure 1 shows a known pixel circuit for an active matrix addressed electroluminescent display device. The display device comprises a panel having a row and column matrix array of regularly-spaced pixels, denoted by the blocks 1 and comprising electroluminescent display elements 2 together with associated switching means, located at the intersections between crossing sets of row (selection) and column (data) address conductors 4 and 6. Only a few pixels are shown in the Figure for simplicity. In practice there may be several hundred rows and columns of pixels. The pixels 1 are addressed via the sets of row and column address conductors by a peripheral drive circuit comprising a row, scanning, driver circuit 8 and a column, data, driver circuit 9 connected to the ends of the respective sets of conductors.

[0006] The electroluminescent display element 2 comprises an organic light emitting diode, represented here as a diode element (LED) and comprising a pair of electrodes between which one or more active layers of organic electroluminescent material is sandwiched. The display elements of the array are carried together with the associated active matrix circuitry on one side of an insulating support. Either the cathodes or the anodes of the display elements are formed of transparent conductive material. The support is of transparent material such as glass and the electrodes of the display elements 2 closest to the substrate may consist of a transparent conductive material such as ITO so that light generated by the electroluminescent layer is transmitted through these electrodes and the support so as to be visible to a viewer at the other side of the support. Typically, the thickness of the organic electroluminescent material layer is between 100 nm and 200nm. Typical examples of suitable organic electroluminescent materials which can be used for the elements 2 are known and described in EP-A-0 717446. Conjugated polymer materials as described in WO96/36959 can also be used.

[0007] Figure 2 shows in simplified schematic form a known pixel and drive circuitry arrangement for providing voltage-programmed operation. Each pixel 1 comprises the EL display element 2 and associated driver circuitry. The driver circuitry has an address transistor 16 which is turned on by a row address pulse on the row conductor 4. When the address transistor 16 is turned on, a voltage on the column conductor 6 can pass to the remainder of the pixel. In particular, the address transistor 16 supplies the column conductor voltage to a current source 20, which comprises a drive transistor 22 and a storage capacitor 24. The column voltage is provided to the gate of the drive transistor 22, and the gate is held at this voltage by the storage capacitor 24 even after the row address pulse has ended. The drive transistor 22 draws a current from the power supply line 26.

[0008] The drive transistor 22 in this circuit is implemented as a p-type TFT, for example a low temperature polysilicon TFT, so that the storage capacitor 24 holds the gate-source voltage fixed. This results in a fixed source-drain current through the transistor, which therefore provides the desired current source operation of the pixel.

[0009] One problem with voltage-programmed pixels, particularly using polysilicon thin film transistors, is that different transistor characteristics across the substrate (particularly the threshold voltage) give rise to different relationships between the gate voltage and the source-drain current, and artefacts in the displayed image result.

[0010] Various techniques have been proposed for compensating for these threshold voltage variations. Some techniques perform in-pixel measurement of the drive transistor threshold voltage, and add this threshold voltage to the pixel drive signal, so that the combined drive voltage takes account of the threshold voltage. A pixel circuit to perform this can use two storage capacitors, one for the threshold voltage and one for the pixel drive voltage. Additional switching transistors are also required to enable the threshold voltage to be measured,

for example by discharging a capacitance across the gate-source junction of the drive transistor until it turns off.

[0011] This type of threshold compensation pixel circuit has two phases to the address cycle. In the first phase, the threshold voltage is stored on a threshold capacitor. In the second phase, the pixel data voltage is stored on a data capacitor. One problem with the known arrangement is that the column line is used for the threshold voltage measurement operation, and this column line is coupled to the pixel through the address transistor controlled by the row. This means that the threshold voltage measurement and the supply of pixel data to the pixel must take place within a row address period.

[0012] One of These Techniques is disclosed by document WO 03/07729.

[0013] According to the invention, there is provided an active matrix device comprising an array of display pixels, each pixel comprising:

a current driven light emitting display element;
a drive transistor for driving a current through the display element;
first and second capacitors connected in series between the gate and source or drain of the drive transistor, a data input to the pixel being provided to the junction between the first and second capacitors thereby to charge the second capacitor to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the first capacitor; and
a discharge transistor connected between the junction between the first and second capacitors and a common line for all pixels of the display.

[0014] This device uses a common line as a discharge sink/source for the threshold voltage measurement operation. By avoiding the use of a data line for this purpose, the pixel can be in a non-addressed state when the threshold measurement takes place.

[0015] Each pixel may further comprise an input transistor connected between an input data line and the junction between the first and second capacitors.

[0016] Each pixel is then preferably operable in two modes, a first mode in which the input transistor is off and the voltage derived from the drive transistor threshold voltage is stored on the first capacitor, and a second mode in which the input transistor is on and a data input to the pixel charges the second capacitor to the voltage derived from the pixel data voltage.

[0017] This input transistor is the address transistor for the circuit, and is off during the threshold measurement stage.

[0018] The drive transistor may be a p-type transistor and the source of the drive transistor is then connected to a power supply line. The common line may then be this power supply line, or it may be a separate line.

[0019] Each pixel may further comprise a second transistor connected between the gate and drain of the drive transistor. This is used to control the supply of current from the drain. Thus, by turning on the second transistor, the first capacitor can be charged to the gate-source voltage. The second transistor may be controlled by a first gate control line which is shared between a row of pixels.

[0020] In one example, the first and second capacitors are connected in series between the gate and source of the drive transistor.

[0021] Each pixel may further comprise a third transistor connected between the drive transistor and the display element. This can be used to isolate the display element during the pixel programming stage.

[0022] The display element may comprise an electroluminescent display element

[0023] The invention also provides a method of driving an active matrix display device comprising an array of current driven light emitting display pixels, each pixel comprising an display element and a drive transistor for driving a current through the display element, the method comprising, for each pixel:

isolating a data line from the pixel, and while the data line is isolated:

driving a current through the drive transistor, and charging a first capacitor to a resulting gate-source voltage;
discharging the first capacitor through a discharge transistor connected between one terminal of the first capacitor and a common line, until the drive transistor turns off, the first capacitor thereby storing a threshold voltage;

coupling a data line to the pixel, and while the data line is coupled:

charging a second capacitor, in series with the first capacitor between the gate and source or drain of the drive transistor, to a data input voltage from the data line; and
using the drive transistor to drive a current through the display element using a gate voltage that is derived from the voltages across the first and second capacitors.

[0024] This method uses a common line as a discharge sink/source for the threshold voltage measurement operation. As mentioned above, avoiding the use of a data line for this purpose enables the pixel to be in a non-addressed state when the threshold measurement takes place.

[0025] The isolating and coupling preferably comprises switching an address transistor connected between the data line and an input to the pixel, and this address transistor for each pixel in a row is switched on simultaneously by a common row address control line.

[0026] When the data line is isolated from the pixel and the first capacitor is being charged, the data line is pref-

erably used to provide a data input voltage to another pixel associated with the data line. This provides a pipelined addressing sequence.

[0027] The invention will now be described by way of example with reference to the accompanying drawings, in which:

Figure 1 shows a known EL display device;
Figure 2 is a schematic diagram of a known pixel circuit for current-addressing the EL display pixel using an input drive voltage;
Figure 3 shows a schematic diagram of a known threshold compensation circuit;
Figure 4 shows a schematic diagram of an example of pixel layout for a display device of the invention;
Figure 5 is a timing diagram for operation of the pixel layout of Figure 5; and
Figure 6 is used to show how the circuit of the invention enables pipelining to be carried out.

[0028] The same reference numerals are used in different figures for the same components, and description of these components will not be repeated.

[0029] Figure 3 shows a known threshold compensation pixel arrangement. Each pixel again has an electroluminescent (EL) display element 2 and a drive transistor T_D in series between a power supply line 26 and a grounded common cathode 28. The drive transistor T_D is for driving a current through the display element 2.

[0030] First and second capacitors C_1 and C_2 are connected in series between the gate and source of the drive transistor T_D. A data input to the pixel is provided to the junction 30 between the first and second capacitors and charges the second capacitor C_2 to a pixel data voltage as will be explained below. The first capacitor C_1 is for storing the drive transistor threshold voltage.

[0031] An address transistor A_1 is connected between an input data line 6 and the junction 30 between the first and second capacitors. This address transistor times the application of a data voltage to the pixel, for storage on the second capacitor C_2.

[0032] A second, shorting, transistor A_2 is connected between the gate and drain of the drive transistor T_D. This is used to control a flow of current between the power supply line 26 and the first capacitor C_1 when the drive transistor T_D is on.

[0033] A third, isolating, transistor A_3 is connected between the drive transistor T_D and the anode of the display element 2. This is used to turn off the display element 2 during the threshold measurement operation of the pixel programming sequence.

[0034] The transistors A_1 to A_3 are controlled by respective row conductors which connect to their gates.

[0035] The addressing of an array of pixels involves addressing rows of pixels in turn, with a full row of pixels addressed simultaneously, in conventional manner. The data line 6 comprises a column conductor,

[0036] The circuit of Figure 3 can be operated in a number of different ways. One basic operation will be described, and the problems associated with the circuit will be explained.

[0037] Only the drive transistor T_D is used in constant current mode. All other TFTs A_1 to A_3 in the circuit are used as switches that operate on a short duty cycle.

[0038] The circuit operation is to store the threshold voltage of the drive transistor T_D on C_1, and then store the data voltage on C_2 so that the gate-source voltage of T_D is the data voltage plus the threshold voltage.

[0039] During the threshold voltage measurement, the address transistor A_1 is turned on as is the shorting transistor A_2. The isolation transistor A_3 is initially on, so that current is driven through the display element for a short time, in order to establish a large gate-source voltage on the drive transistor which turns the drive transistor on.

[0040] The isolating transistor A_3 is then turned off, and the current sourced by the drive transistor passes from the source to the drain, through the transistor A_2, the capacitor C_1 and the address transistor A_1 to the data line 6. A suitable voltage is provided on the data line 6 for this operation, for example the same voltage as the power supply line voltage, and this all takes place within the row address period (namely while the address transistor A_1 is turned on).

[0041] The flow of charge changes the voltage stored across the capacitor C_1 until the gate-source voltage approaches the threshold voltage. At this time, the drive transistor turns off. With the capacitor C_2 shorted out (because the power supply line voltage is on the data line 6), the capacitor C_1 then stores and holds the threshold voltage.

[0042] Subsequently, the shorting transistor A_2 is turned off, and the pixel data is stored on the capacitor C_2 through the address transistor A_1. The transistor A_3 is turned on for the illumination period.

[0043] Variations to this circuit are of course possible, for example to avoid the need for a pulse of light to be output during the threshold measurement operation. However, a problem remains that a significant part of the address cycle is taken up by the threshold measurement.

[0044] The invention provides a pipelined addressing sequence, so that there can be some timing overlap between the control signals of adjacent rows.

[0045] Figure 4 shows an example of pixel circuit of the invention. The circuit is identical to that shown in Figure 3. but additionally has a discharge transistor A_4 connected between the junction 30 and the power supply line 26. The function of this transistor is to allow the address transistor A_1 to be turned off during the threshold voltage measurement cycle, so as to free up the column conductor for use in providing pixel data to the pixels in another row.

[0046] The operation of the circuit is explained with reference to Figure 5.

[0047] At the beginning of the graphs shown in Figure 5, the display is emitting light from the previous address period. At the beginning of the programming phase, the

shorting and discharge transistors A_2, A_4 are turned on. The junction 30 is then lifted to the power rail voltage, and the gate and drain of the drive transistor T_D are connected together. A short pulse of light is emitted while the gate voltage of the drive transistor is stabilised, and then the isolating transistor A_3 is turned off (plot A_3 in Figure 5 goes high). This directs the drive transistor source-drain current to its own gate. In the same way as for the circuit described above, the gate charges up until the drive transistor gate reaches its threshold voltage, and this is stored on the capacitor C_1.

[0048] This charging of the gate has a relatively long time constant. The invention allows this to be carried out with the address transistor turned off (during period 40), so that the time can be "pipelined" with the programming of other rows of pixels with pixel data.

[0049] The shorting and discharge transistors A_2, A_4 are then turned off, so that the gate of the drive transistor can float, with the threshold voltage of the drive transistor stored across the capacitor C_1. The isolation transistor A_3 can also be turned on at that time, and no current will flow to the display element until the pixel is addressed with the data voltage.

[0050] A short address pulse for the address transistor A_1 is needed at a subsequent time, synchronised with the data on the column (the non-hatched part of the data plot in Figure 5). The column is at a lower voltage than the power line voltage, which pulls down the drive transistor gate voltage, storing the pixel data voltage on C_2. The combined voltage across the source-gate junction is thus the measured threshold voltage added to the pixel drive voltage.

[0051] It can be seen that the plots for transistors A_2 and A_4 are the same, so that they can be controlled by a shared control line.

[0052] This pipelining of the addressing sequence allows more than one row of pixels can be programmed at any one time. Thus, the addressing signals on lines A_2 to A_4 can overlap with the same signals for different rows. The length of the addressing sequence does not then imply long pixel programming times, and the effective line time is only limited by the time required to charge the second capacitor C_2 when the address line A_1 is high. This time period is the same as for a standard active matrix addressing sequence. The other parts of the addressing mean that the overall frame time will only be lengthened slightly by the set-up required for the first few rows of the display. However this set up can easily be done within the frame-blanking period so the time required for the threshold voltage measurement is not a problem.

[0053] Pipelined addressing is shown more clearly in the timing diagrams of Figure 6. The control signals for the transistors A_2 to A_4 have been combined into a single plot, but the operation is as described with reference to Figures 4 and 5. The "Data" plot in Figure 6 shows that the data line 6 is used almost continuously to provide data to successive rows.

[0054] In the method of Figures 4 and 5, the threshold measurement operation is combined with the display operation, so that the threshold measurement and display is performed for each row of pixels in turn.

[0055] It is possible instead to perform all of the threshold measurements for the full display, and then to address.

[0056] There are many variations to the specific circuit layout described above which can work in the same way. Differences may be desired to prevent the flash of light during pixel programming. For example, an additional transistor may be provided which gives the drain of the drive transistor a path to ground so that this path can be used to ensure current flow immediately before threshold measurement, instead of using current flow through the display element.

[0057] The circuits can be used for currently available LED devices. However, the electroluminescent (EL) display element may comprise an electrophosphorescent organic electroluminescent display element.

[0058] The circuit above has been shown implemented with a p-type drive transistor. The invention enables larger area polysilicon arrays to be fabricated because the pixel circuits compensate for the pixel to pixel variations without requiring longer pixel addressing times. These pixel addressing times become a limiting factor when designing large displays. The invention is particularly suitable for displays in which the drive transistor comprises a LTPS transistor.

[0059] The invention can be applied to other transistor technologies, such as microcrystalline silicon.

[0060] Various other modifications will be apparent to those skilled in the art.

Claims

1. An active matrix device comprising an array of display pixels (1), each pixel comprising:

a current driven light emitting display element (2);

a drive transistor (T_D) for driving a current through the display element;

first and second capacitors (C_1, C_2) connected in series between the gate (G) and source (S) or drain (D) of the drive transistor (T_D), a data input to the pixel being provided to the junction (30) between the first and second capacitors thereby to charge the second capacitor (C_2) to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the first capacitor (C_1); and **characterised by** comprising a discharge transistor (A_4) connected between the junction (30) between the first and second capacitors and a common line (26) for all pixels of the display.

2. A device as claimed in claim 1, wherein the drive transistor (T_D) comprises a p-type thin film transistor.

3. A device as claimed in claim 1 or 2, wherein the drive transistor (T_D) comprises a polysilicon or microcrystalline silicon transistor.

4. A device as claimed in claim 3, wherein the drive transistor (T_D) comprises a low temperature polysilicon transistor.

5. A device as claimed in any preceding claim, wherein each pixel further comprises an input transistor (A_1) connected between an input data line (6) and the junction (30) between the first and second capacitors.

6. A device as claimed in any preceding claim, wherein each pixel is operable in two modes, a first mode in which the input transistor (A_1) is off and the voltage derived from the drive transistor threshold voltage is stored on the first capacitor (C_1), and a second mode in which the input transistor (A_1) is on and a data input to the pixel charges the second capacitor (C_2) to the voltage derived from the pixel data voltage.

7. A device as claimed in any preceding claim, wherein the drive transistor (T_D) is a p-type transistor and the source of the drive transistor is connected to a power supply line (26).

8. A device as claimed in claim 7, wherein the common line comprises the power supply line (26).

9. A device as claimed in any preceding claim, wherein each pixel further comprises a second transistor (A_2) connected between the gate (G) and drain (D) of the drive transistor (T_D).

10. A device as claimed in claim 9, wherein the second transistor (A_2) is controlled by a first gate control line which is shared between a row of pixels.

11. A device as claimed in any preceding claim, wherein the first and second capacitors (C_1,C_2) are connected in series between the gate (G) and source (S) of the drive transistor (T_D).

12. A device as claimed in any preceding claim, wherein each pixel further comprises a third transistor (A_3) connected between the drive transistor and the display element (2).

13. A device as claimed in any preceding claim, wherein the display element (2) comprises an electroluminescent display element.

14. A device as claimed in claim 13, wherein the electroluminescent (EL) display element (2) comprises an electrophosphorescent organic electroluminescent display element.

15. A method of driving an active matrix display device comprising an array of current driven light emitting display pixels (1), each pixel comprising an display element (2) and a drive transistor (T_D) for driving a current through the display element, the method comprising, for each pixel:

isolating a data line (6) from the pixel, and while the data line is isolated:

driving a current through the drive transistor, and charging a first capacitor (C_1) to a resulting gate-source voltage;
discharging the first capacitor (C_1) through a discharge transistor (A_4) connected between one terminal of the first capacitor and a common line, until the drive transistor turns off, the first capacitor (C_1) thereby storing a threshold voltage;

coupling a data line (6) to the pixel, and while the data line is coupled:

charging a second capacitor (C_2), in series with the first capacitor between the gate and source or drain of the drive transistor (T_D), to a data input voltage from the data line (6); and

using the drive transistor (T_D) to drive a current through the display element using a gate voltage that is derived from the voltages across the first and second capacitors (C_1,C_2).

16. A method as claimed in claim 15, wherein the isolating and coupling comprises switching an address transistor (A_1) connected between the data line (6) and an input (30) to the pixel.

17. A method as claimed in claim 16, wherein the address transistor (A_1) for each pixel in a row is switched on simultaneously by a common row address control line.

18. A method as claimed in claim 17, wherein the address transistors for one row of pixels are turned on substantially immediately after the address transistors for an adjacent row are turned off.

19. A method as claimed in any one of claims 15 to 18, wherein when the data line (6) is isolated from the pixel and the first capacitor is being charged, the data line is used to provide a data input voltage to another pixel associated with the data line.

20. A method as claimed in any one of claims 15 to 19, for driving a display device in which each pixel comprises a p-type drive transistor.

21. A method as claimed in any one of claims 15 to 20, for driving a display device in which the drive transistor comprises a polysilicon or microcrystalline silicon transistor.

22. A method as claimed in claim 21, for driving a display device in which the drive transistor of each pixel comprises a LTPS transistor.

Patentansprüche

1. Aktivmatrix-Vorrichtung umfassend ein Array von Display-Pixeln (1), wobei jedes Pixel aufweist:

ein stromgesteuertes Licht emittlerendes Anzeige-Element (2);
einen Treiber-Transistor (T_D) zum Treiben eines Stroms durch das Anzeige-Element;
erste und zweite Kondensatoren (C_1, C_2), die in Reihe zwischen Gate (G) und Source (S) oder Drain (D) des Treiber-Transistors (T_D) geschaltet sind, wobei ein Daten-Eingang zu dem Pixel, der an der Verbindungsstelle (30) zwischen dem ersten und zweiten Kondensator vorgesehen ist, um somit den zweiten Kondensator (C_2) auf eine Spannung zu laden, die von der Pixel-Daten-Spannung abgeleitet ist, und wobei eine Spannung, die von der Treiber-Transistor-Schwellwert-Spannung abgeleitet ist, auf dem ersten Kondensator (C_1) gespeichert ist; und
gekennzeichnet durch
einen Entlade-Transistor (A_4), der zwischen der Verbindungsstelle (30) zwischen dem ersten und zweiten Kondensator und einer gemeinsamen Leitung (26) für alle Pixel der Anzeige geschaltet ist.

2. Vorrichtung nach Anspruch 1, wobei der Treiber-Transistor (T_D) einen p-Typ Dünnfilm-Transistor aufweist.

3. Vorrichtung nach Anspruch 1 oder 2, wobei der Treiber-Transistor (T_D) einen Polysilizium- oder mikrokristallinen Silizium-Transistor aufweist.

4. Vorrichtung nach Anspruch 3, wobei der Treiber-Transistor (T_D) einen Niedrigtemparatur-Polysilizium-Transistor aufweist.

5. Vorrichtung nach einem der vorhergehenden Ansprüche, wobei jedes Pixel ferner einen Eingangs-Transistor (A_1) aufweist, der zwischen einer Eingangs-Datenleitung (6) und der Verbindungsstelle (30) zwischen dem ersten und zweiten Kondensator geschaltet ist.

6. Vorrichtung nach einem der vorhergehenden Ansprüche, wobei jedes Pixel in zwei Modi betreibbar ist, in einem ersten Modus, in dem der Eingangs-Transistor (A_1) ausgeschaltet ist und die Spannung, die von der Treiber-Transistor-Schwellwert-Spannung abgeleitet ist, auf dem ersten Kondensator (C_1) gespeichert ist, und in einem zweiten Modus, in dem der Eingangs-Transistor (A_1) eingeschaltet ist und ein Dateneingang zu dem Pixel den zweiten Kondensator (C_2) auf die Spannung kit, die von der Pixel-Daten-Spannung abgeleitet ist.

7. Vorrichtung nach einem der vorhergehenden Ansprüche, wobei der Treiber-Transistor (T_D) ein p-Typ-Transistor ist und die Source des Treiber-Transistors (T_D) mit einer Stromversorgungs-Leitung (26) verbunden ist.

8. Vorrichtung nach Anspruch 7, wobei die gemeinsame Leitung die Stromversorgungs-Leitung (26) umfasst.

9. Vorrichtung nach einem der vorhergehenden Ansprüche, wobei jedes Pixel ferner einen zweiten Transistor (A2) aufweist, der zwischen Gate (G) und Drain (D) des Treiber-Transistors (T_D) geschaltet ist.

10. Vorrichtung nach Anspruch 9, wobei der zweite Transistor (A_2) durch eine erste Gate-Steuerleitung gesteuert ist, die von einer Zeile von Pixeln gemeinsam genutzt wird.

11. Vorrichtung nach einem der vorhergehenden Ansprüche, wobei die ersten und zweiten Kondensatoren (C_1, C_2) in Serie zwischen Gate (G) und Source (S) des Treiber-Transistors (T_D) geschaltet sind.

12. Vorrichtung nach einem der vorhergehenden Ansprüche, wobei jedes Pixel ferner einen dritten Transistor (A_3) aufweist, der zwischen dem Treiber-Transistor (T_D) und dem Anzeige-Element (2) geschaltet ist.

13. Vorrichtung nach einem der vorhergehenden Ansprüche, wobei das Anzeige-Element (2) ein Elektrolumineszenz-Anzeige-Element aufweist.

14. Vorrichtung nach Anspruch 13, wobei das Elektrolumineszenz- (EL) Anzeige-Element (2) ein elektrophosphoreszierendes organisches Elektrolumineszenz-Anzeige-Element aufweist.

15. Verfahren zum Ansteuern bzw. Treiben einer Aktivmatrix-Anzelge-Vorrichtung mit einem Array von stromgesteuerten Licht emittierenden Anzeige-Pi-

xeln (1), wobei jedes Pixel ein Anzeige-Element (2) und einen Treiber-Transistor (T_D) für das Treiben von Strom durch das Display-Element aufweist, wobei das Verfahren für jedes Pixel umfasst:

Isolieren bzw. Trennen einer Datenleitung (6) von dem Pixel, und während die Datenleitung getrennt ist:

Treiben eines Stroms durch den Treiber-Transistor (T_D), und Aufladen eines ersten Kondensators (C_1) zu einer resultierenden Gate-Source-Spannung;
Entladung des ersten Kondensators (C_1) durch einen Entlade-Transistor (A_4), der zwischen einem Anschluss des ersten Kondensators und einer gemeinsamen Leitung geschaltet ist, bis der Antriebs-Transistor abschaltet, wodurch der erste Kondensator (C_1) eine Schwellwert-Spannung speichert;
Verbinden einer Datenleitung (6) zu dem Pixel, und während die Datenleitung verbunden ist:

Aufladen eines zweiten Kondensators (C_2), in Reihe mit dem ersten Kondensator zwischen Gate und Source oder Drain des Treiber-Transistors (T_D), mit einer Daten-Eingangs-Spannung aus der Datenleitung (6); und
Verwenden des Treiber-Transistors (T_D), um einen Strom durch das Anzeige-Element zu treiben, wobei eine Gate-Spannung verwendet wird, die aus den Spannungen über den ersten und zweiten Kondensatoren (C_1, C_2) abgeleitet wird.

16. Verfahren nach Anspruch 15, wobei das Trennen und Verbinden das Schalten eines Adress-Transistors (A_1) umfasst, der zwischen der Datenleitung (6) und einem Eingang (30) zu dem Pixel verbunden ist.

17. Verfahren nach Anspruch 16, wobei der Adress-Transistor (A_1) für jedes Pixel in einer Zeile gleichzeitig durch eine gemeinsame Zeilen-Adressen-Leitung eingeschaltet wird.

18. Verfahren nach Anspruch 17, wobei die Adress-Transistoren für eine Zeile von Pixeln im Wesentlichen unmittelbar nach den Adress-Transistoren für eine benachbarte Zeile eingeschaltet werden.

19. Verfahren nach einem der Ansprüche 15 bis 18, wobei, wenn die Datenleitung (6) von dem Pixel getrennt und der erste Kondensator aufgeladen wird, die Datenleitung verwendet wird, um eine Daten-Eingangs-Spannung zu einem anderen Pixel bereit zu stellen, das der Datenleitung zugeordnet ist.

20. Verfahren nach einem der Ansprüche 15 bis 19 zum Ansteuern einer Anzeige-Vorrichtung, bei der jedes Pixel einen p-Typ Treiber-Transistor (T_D) aufweist.

21. Verfahren nach einem der Ansprüche 15 bis 20, zum Ansteuern einer Anzeige-Vorrichtung, bei der der Treiber-Transistor (T_D) einen Polysilizium oder mikrokristallinen Silizium-Transistor aufweist.

22. Verfahren nach Anspruch 21 zum Antreiben einer Anzeige-Vorrichtung, bei der der Treiber-Transistor jedes Pixels einen LTPS-Transistor aufweist.

Revendications

1. Un dispositif à matrice active comportant une matrice de pixels d'affichage (1), chaque pixel comprenant:

un élément d'affichage d'émission de lumière commandé par un courant;
un transistor de commande (T_D) pour commander un courant au travers de l'élément d'affichage;
une première et seconde capacités (C_1, C_2) connectées en série entre la grille (G) et la source (S) ou le drain (D) du transistor de commande (T_D), une entrée de donnée du pixel étant disposée à la jonction (30) entre la première et la seconde capacités pour ainsi charger la seconde capacité (C_2) à un potentiel dérivé du potentiel de donnée de pixel, et un potentiel dérivé du potentiel de seuil du transistor de commande étant chargé sur la première capacité (C_1), **caractérisé en ce qu'**il comporte
un transistor de décharge (A_4) connecté entre la jonction (30) entre la première et la seconde capacité et un conducteur commun à tous les pixels de l'affichage.

2. Un dispositif tel que revendiqué dans la revendication 1, dans lequel le transistor de commande (T_D) comporte un transistor à film fin de type P.

3. Un dispositif tel que revendiqué dans la revendication 1 ou 2, dans lequel le transistor de commande (T_D) comporte un transistor silicium poly silicium ou micro-crystalin.

4. Un dispositif tel que revendiqué dans la revendication 3, dans lequel le transistor de commande (T_D) comporte un transistor poly silicium à faible température.

5. Un dispositif tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel chaque pixel comporte en outre un transistor d'entrée (A_1) connecté entre une ligne d'entrée de don-

nées (6) et la jonction (30) entre la première et la seconde capacité.

6. Un dispositif tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel chaque pixel peut fonctionner suivant deux modes, un premier mode dans lequel le transistor d'entrée (A_1) est éteint et le potentiel dérivé du potentiel de seuil du transistor de commande est chargé dans la première capacité (C_1), et un second mode dans lequel le transistor d'entrée (A_1) est allumé et une entrée de donnée pour le pixel charge la seconde capacité (C_2) au potentiel dérivé du potentiel de donnée de pixel.

7. Un dispositif tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel le transistor de commande (T_D) est un transistor de type P et la source du transistor de commande est connectée à un conducteur d'alimentation électrique (26).

8. Un dispositif tel que revendiqué dans la revendication 7, dans lequel le conducteur commun comporte le conducteur d'alimentation électrique (26).

9. Un dispositif tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel chaque pixel comporte en outre un second transistor (A_2) connecté entre la grille (G) et le drain (D) du transistor de commande (T_D).

10. Un dispositif tel que revendiqué dans la revendication 9, dans lequel le second transistor (A_2) est commandé par un premier conducteur de commande de grille qui est partagé entre une rangée de pixels.

11. Un dispositif tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel la première et la seconde capacités (C_1, C_2) sont connectées en série entre la grille (G) et la source (S) du transistor de commande (T_D).

12. Un dispositif tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel chaque pixel comporte en outre un troisième transistor (A_3) connecté entre le transistor de commande et l'élément d'affichage (2).

13. Un dispositif tel que revendiqué dans l'une quelconque des revendications précédentes, dans lequel l'élément d'affichage (2) comporte un élément d'affichage électroluminescent.

14. Un dispositif tel que revendiqué dans la revendication 13, dans lequel l'élément d'affichage (2) électroluminescent (EL) comporte un élément d'affichage électroluminescent organique électrophosphorescent.

15. Une méthode de commande d'un dispositif d'affichage à matrice active comportant une matrice de pixels d'affichage d'émission de lumière commandés par un courant (1), chaque pixel comprenant un élément d'affichage (2) et un transistor de commande (T_D) pour commander un courant au travers de l'élément d'affichage; la méthode comprenant, pour chacun des pixels:

- l'isolation d'un conducteur de données (6) du pixel, et pendant l'isolation du conducteur de données:

  la commande d'un courant au travers du transistor de commande, et la charge d'une première capacité (C_1) vers un potentiel grille-source résultant;
  la décharge de la première capacité (C_1) au travers un transistor de décharge (A_4) connecté entre une électrode de la première capacité et un conducteur commun, jusqu'à l'extinction du transistor de commande, la première capacité (C_1) stockant un potentiel de seuil;

le couplage du conducteur de données (6) au pixel, et pendant le couplage du conducteur de données:

  la charge de la seconde capacité (C_2) en série avec la première capacité entre la grille et la source ou le drain du transistor de commande (T_D), vers un potentiel d'entrée de donnée depuis le conducteur de données (6), et;

l'utilisation du transistor de commande (T_D) pour la commande d'un courant au travers l'élément d'affichage en utilisant un potentiel de grille qui est dérivé des potentiels au travers la première et la seconde capacité (C_1, C_2).

16. Une méthode telle que revendiquée dans la revendication 15, dans laquelle l'isolation et le couplage comportent la commutation d'un transistor d'adressage (A_1) connecté entre le conducteur de données (6) et une entrée (30) vers le pixel.

17. Une méthode telle que revendiquée dans la revendication 16, dans laquelle le transistor d'adressage (A_1) pour chacun des pixels au sein d'une rangée est commuté passant de manière simultanée au moyen d'un conducteur d'adressage de rangée commune.

18. Une méthode telle que revendiquée dans la revendication 17, dans laquelle les transistors d'adressage pour une rangée de pixels sont commandés pas-

sants immédiatement après l'extinction des transistors d'adressage d'une rangée adjacente.

19. Une méthode telle que revendiquée dans l'une des revendications 15 à 18, dans laquelle lorsque le conducteur de données (6) est isolé du pixel et que la première capacité est chargée, le conducteur de données est utilisé pour fournir un potentiel d'entrée de données à un autre pixel associé au conducteur de données.

20. Une méthode telle que revendiquée dans l'une des revendications 15 à 19, pour la commande d'un dispositif d'affichage dans lequel chacun des pixels comporte un transistor de commande de type P.

21. Une méthode telle que revendiquée dans l'une quelconque des revendications 15 à 20, pour la commande d'un dispositif d'affichage dans lequel le transistor de commande comporte un transistor silicium poly silicium ou micro-crystalin.

22. Une méthode telle que revendiquée dans la revendication 21, pour la commande d'un dispositif d'affichage dans lequel le transistor de commande de chaque pixel comporte un transistor LTPS.

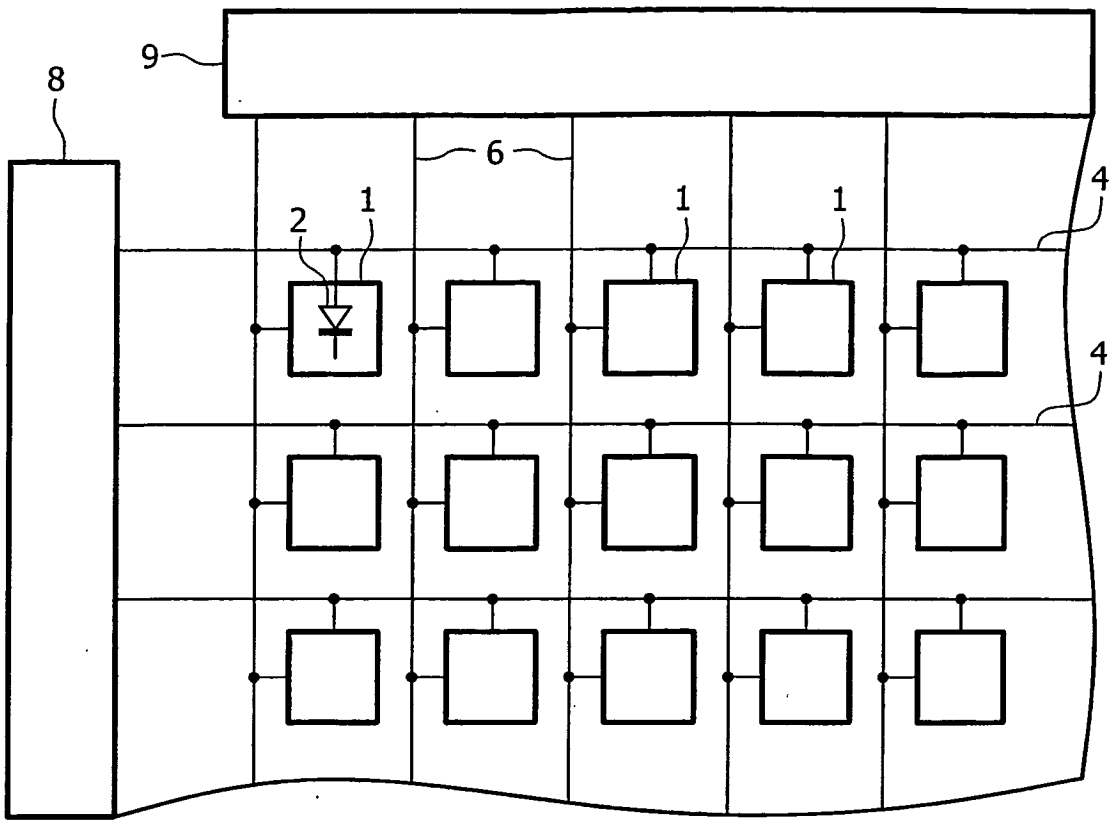

FIG. 1 PRIOR ART

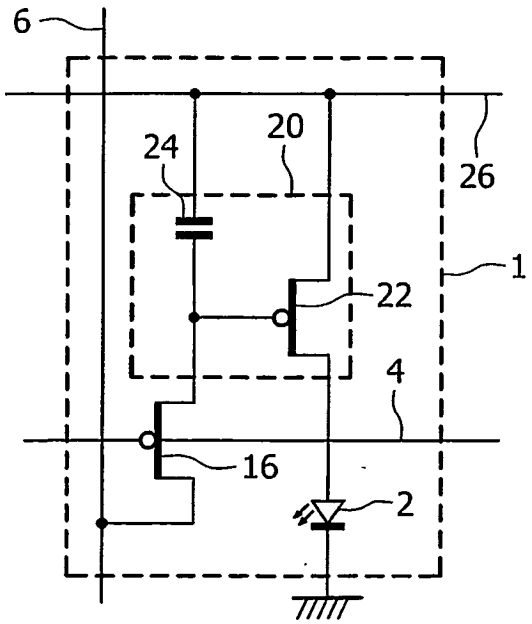

FIG. 2 PRIOR ART

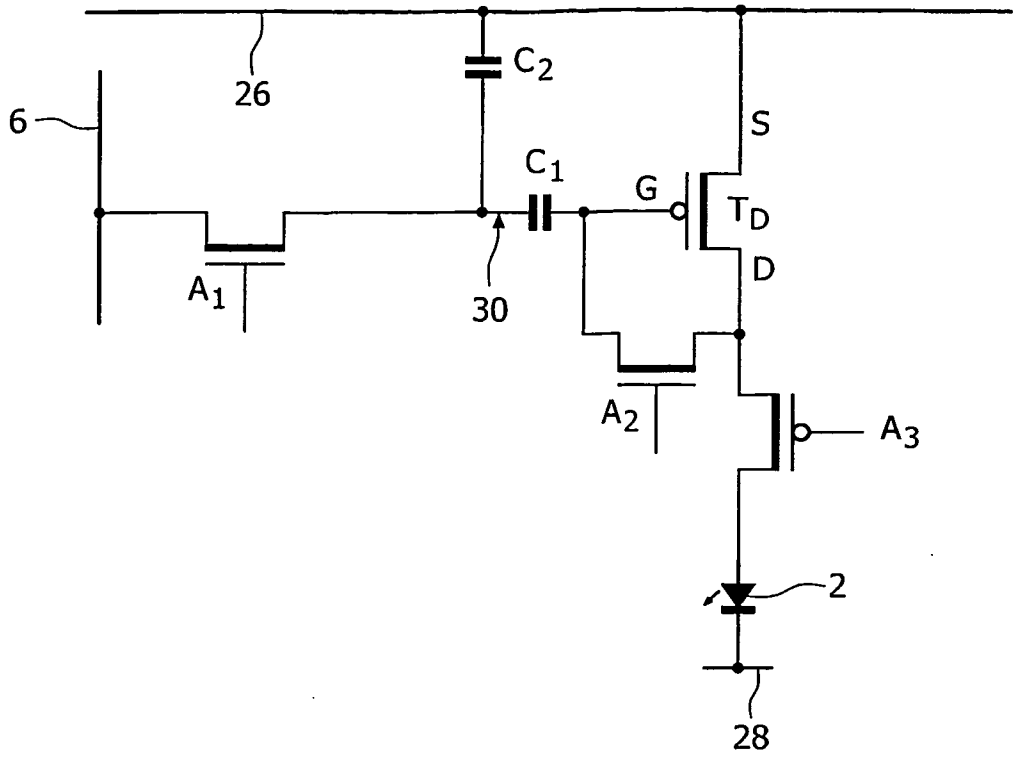

FIG. 3 PRIOR ART

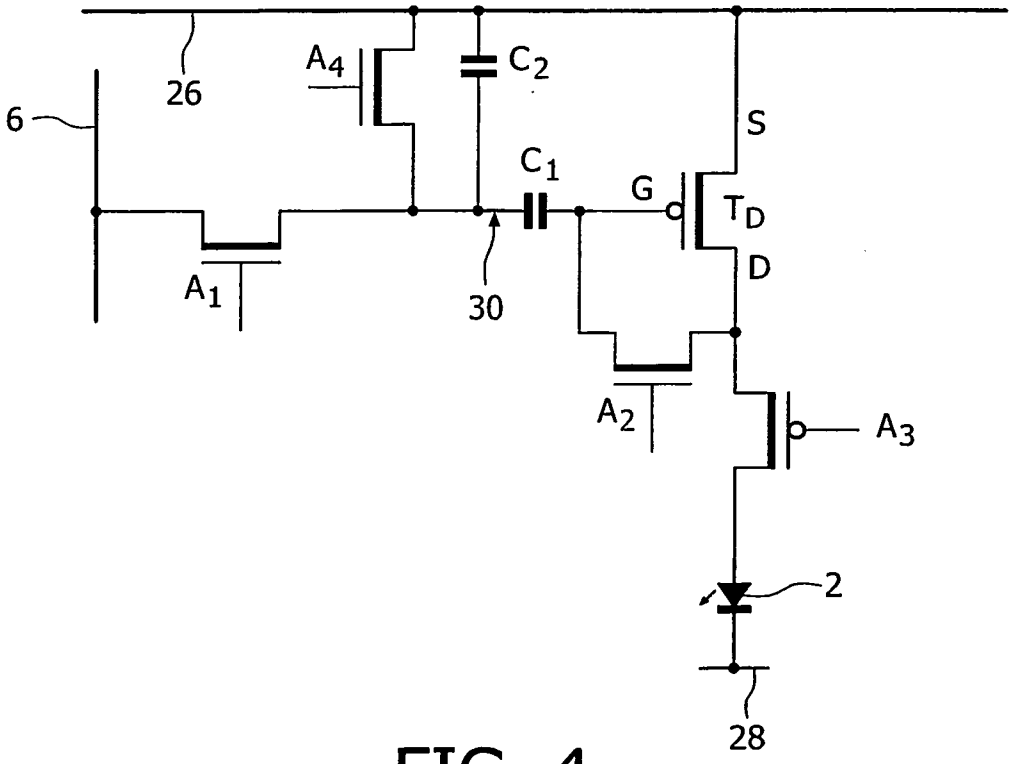

FIG. 4

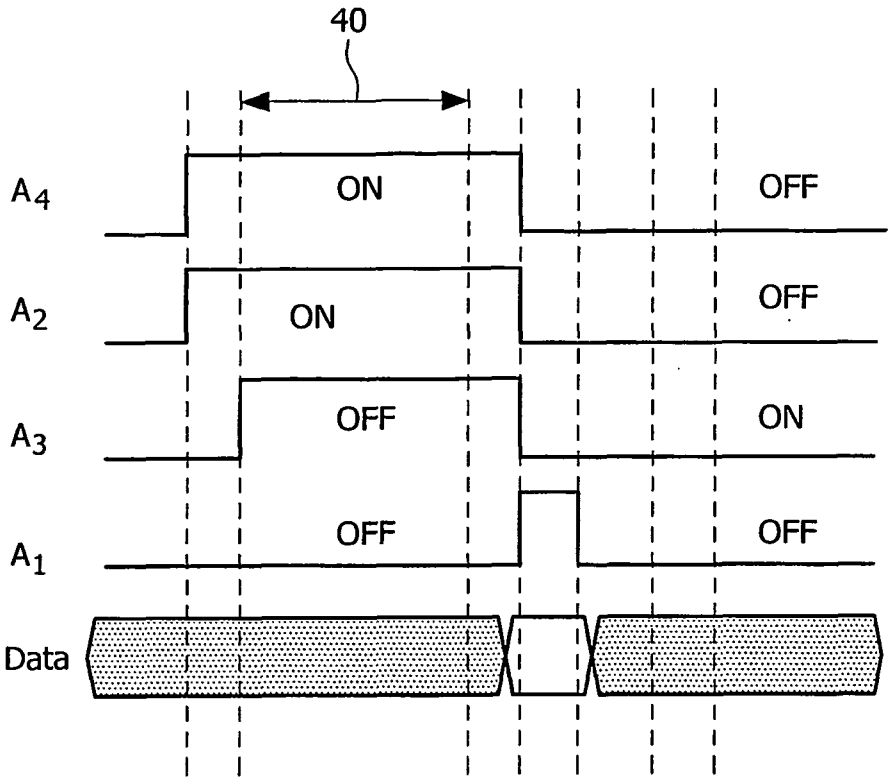

FIG. 5

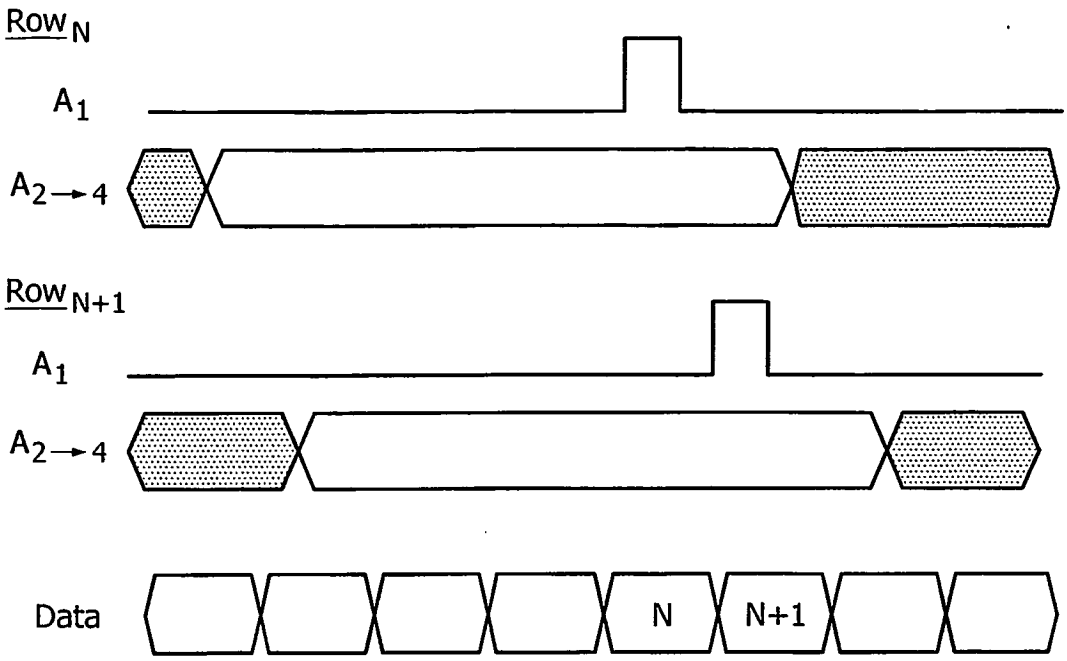

FIG. 6

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 0717446 A **[0006]**
- WO 9636959 A **[0006]**
- WO 0307729 A **[0012]**

专利名称(译)	具有有源矩阵的电致发光显示装置		
公开(公告)号	EP1704554B1	公开(公告)日	2012-05-02
申请号	EP2005702559	申请日	2005-01-04
[标]申请(专利权)人(译)	皇家飞利浦电子股份有限公司		
申请(专利权)人(译)	皇家飞利浦电子N.V.		
当前申请(专利权)人(译)	奇美群创光电		
发明人	FISH, DAVID A., C/O PHILIPS INTELLECTUAL P & S CHILDS, MARK J., C/O PHILIPS INTELLECTUAL P & S		
IPC分类号	G09G3/32 G09G3/20		
CPC分类号	G09G3/3233 G09G3/20 G09G2300/0417 G09G2300/0809 G09G2300/0819 G09G2300/0852 G09G2300/0861 G09G2310/061 G09G2320/043		
优先权	2004000213 2004-01-07 GB		
其他公开文献	EP1704554A1		
外部链接	Espacenet		

摘要(译)

有源矩阵EL显示器具有串联连接在像素驱动晶体管的栅极和源极或漏极之间的第一和第二电容器。输入到像素的数据被提供给第一和第二电容器之间的结，从而将第二电容器充电到从像素数据电压得到的电压，并且从驱动晶体管阈值电压得到的电压存储在第一电容器上。放电晶体管连接在第一和第二电容器之间的结和用于显示器的所有像素的公共线之间。该器件使用公共线作为阈值电压测量操作的放电吸收/源。通过避免为此目的使用数据线，当发生阈值测量时，像素可以处于非寻址状态。

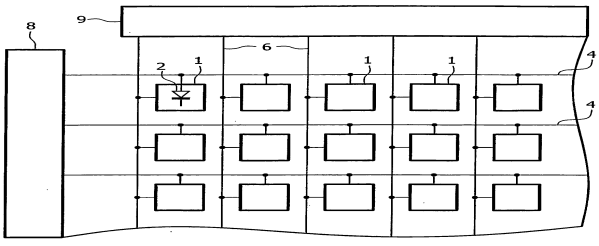

FIG. 1 PRIOR ART

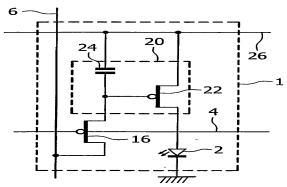

FIG. 2 PRIOR ART