(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 246 157 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
24.01.2007 Bulletin 2007/04

(51) Int Cl.:
G09G 3/32 *(2006.01)*

(21) Application number: **01120624.0**

(22) Date of filing: **29.08.2001**

(54) **Emissive display using organic electroluminescent devices**

Emitierende Anzeige mit organischen elektrolumineszenten Vorrichtungen

Dispositif d'affichage émissif utilisant des dispositifs organiques électroluminescents

(84) Designated Contracting States:
DE FR GB NL

(30) Priority: **30.03.2001 JP 2001098864**

(43) Date of publication of application:
02.10.2002 Bulletin 2002/40

(73) Proprietor: **Hitachi, Ltd.**
Tokyo 100-8280 (JP)

(72) Inventors:
- **Mikami, Yoshiro,**
  Hitachi, Ltd.,
  Int. Prop. Gp.
  Chiyoda-ku,
  Tokyo 100-8220 (JP)
- **Ouchi, Takayuki,**
  Hitachi, Ltd.,
  Int. Prop. Gp.
  Chiyoda-ku,
  Tokyo 100-8220 (JP)
- **Kaneko, Yoshiyuki,**
  Hitachi, Ltd.,
  Int. Prop. Gp.
  Chiyoda-ku,
  Tokyo 100-8220 (JP)
- **Sato, Toshihiro,**
  Hitachi, Ltd.,
  Int. Prop. Gp.
  Chiyoda-ku,
  Tokyo 100-8220 (JP)

(74) Representative: **Beetz & Partner**
Steinsdorfstrasse 10
80538 München (DE)

(56) References cited:
US-A- 4 039 890

- **PATENT ABSTRACTS OF JAPAN vol. 1998, no. 14, 31 December 1998 (1998-12-31) & JP 10 232649 A (CASIO COMPUT CO LTD), 2 September 1998 (1998-09-02)**

EP 1 246 157 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a display, in particular, to an emissive display using organic electroluminescent (EL) devices.

[0002] The application of the organic EL devices to a plane type display is promoted, and it is proposed to realize an active matrix display with high brightness. As regards the driving system using a low temperature polysilicon thin film transistor(TFT), it is described in SID 99 Technical Digest, pp. 372-375.

[0003] In the pixel structure, a scan line, a signal line, an EL power supply line, and a capacitance reference voltage line are arranged to intersect with one another, and in order to drive the EL device, a holding circuit of a signal voltage is formed by an n-type scan TFT and a storage capacitor. The held signal voltage is applied to a gate of a p-channel type driving TFT, and controls a conductance of a main circuit of the driving TFT. The main circuit of the driving TFT and the organic EL device are connected in series from the EL power supply line and connected to an EL common line.

[0004] In driving this pixel, a pixel selection pulse is applied from the scan line, and the signal voltage is written to the storage capacitor through the scan TFT, and is held. The held signal voltage is applied as the gate voltage of the driving TFT, and controls a drain current, according to a conductance of the driving TFT determined by a source voltage supplied from the power supply line, and a drain voltage, and a driving current of the EL device is controlled, thereby controlling the display brightness.

[0005] However, in this system, there is a property in which even when the same signal voltage is applied in order to control the current, when the threshold value, and the on-resistance are varied, the driving current of the EL device is changed, and thus TFTs with less unevenness and having uniform characteristics are required.

[0006] As a transistor suitable for realizing such a driving circuit, there is a low temperature polysilicon TFT having a high mobility, using a user annealing process, and applicable to a large-type substrate. However, it is known that it has unevenness in the device characteristics, and when it is used as the organic EL device driving circuit, due to the unevenness of the TFT characteristics, even when the same signal voltage is applied, the unevenness in the brightness occurs in each pixel, and it has not been sufficient to display the gray scale with high precision.

[0007] Also, in JP-A-10-232649, as a driving method, the pixel is made to digitally and binary display the on/off state. As a result, since it is not necessary to use as the operating point, the neighbor of the threshold value at which the unevenness of the TFT characteristics reflects on the display significantly, there is a merit of reducing the unevenness of the brightness of the pixel. In order to obtain the gray scale display, one-frame time is divided into 8-subframes of different display times, and the average brightness is controlled by changing the light emission time.

[0008] In document US 4 039 890 a composite semiconductor light-emitting display array is disclosed using a static binary pixel circuit constituted of two cross-coupled inverters to drive the drive transistor of an LED in a matrix of LEDs.

SUMMARY OF THE INVENTION

[0009] In the digital driving system mentioned above, it is necessary to provide within the pixel a memory circuit capable of holding data of frame time or longer, and for stable memory operation, about seven transistors are necessary. However, in a pixel whose area is limited, when many transistors are included, the aperture ratio will be decreased, and when intended to obtain high resolution, the area for arranging the circuit will need 3 times as large as the analog pixel, and the high resolution becomes impossible.

[0010] An object of the present invention is to overcome the problems in the conventional technique mentioned above, and simplify the memory circuit built-in the pixel, and to provide an emissive display which has an increased aperture ratio, and high resolution.

[0011] Another object of the present invention is to provide an emissive display providing reduced power consumption of the circuit of the display.

[0012] To achieve the above-mentioned object, as to two sets of inverter circuits constituting a memory circuit arranged in each pixel, a circuit connecting an organic EL device and a transistor in series is used as one set of inverter circuit, thereby omitting a transistor in the memory circuit, simplifying the circuit, and improving the aperture ratio.

[0013] Furthermore, in the mutual connection of the two sets of inverters, by connecting so that display data is input to a line connected to a gate of the transistor connected in series with the EL device, it is possible to reduce a write load, to enable to write at high speed, and to obtain high resolution.

[0014] Furthermore, by forming a circuit configuration connected so that no through current flows by using p-channel transistors for all the transistors in the pixel, it is possible to reduce the power consumption at the memory holding period. Also, since it is possible to reduce the leakage current at the memory period, the power consumption of the circuit can be reduced.

[0015] The operation of the present invention will be explained. In the memory circuit arranged within the pixel, since

the organic EL device operates as a diode, the driving transistor is connected in series, and it operates as a load device in the inverter. By this arrangement, an inverter circuit is formed, and by combining with another set of inverter circuit formed by only the CMOS transistors, it functions as a memory circuit.

[0016] In the writing of data to the pixel memory, by inputting the data so that the data is written to the gate of the driving transistor, since the gate capacitance is small, a driving load is reduced and high speed writing becomes possible.

[0017] Other objects, features and advantages of the present invention will become apparent from the following description of the embodiments of the invention taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018]

Fig. 1 is a configuration circuit diagram of a pixel circuit of an organic EL display according to one embodiment of the present invention.
Fig. 2 is a configuration circuit diagram of an EL inverter circuit.
Fig. 3 is an explanation diagram showing an inverter characteristic.
Fig. 4 is a configuration circuit diagram of a memory cell circuit of one embodiment.
Fig. 5 is a block diagram showing a configuration of the organic EL display.
Fig. 6 is an operation waveform diagram of a pixel circuit according to one embodiment.
Fig. 7 is a configuration circuit diagram of a pixel circuit by a PMOS inverter.
Fig. 8 is a configuration circuit diagram of a pixel circuit by n-channel transistors.
Fig. 9 is an operation waveform diagram of a shift register.
Fig. 10 is a schematic configuration diagram of a display.
Fig. 11 is a configuration circuit diagram of a pixel circuit by two EL inverter circuits.
Fig. 12 is a diagram showing a mask layout of a pixel circuit.
Fig. 13 is a macroscopic diagram of a display pixel light emission portion.
Fig. 14 is an explanation diagram showing a light emission intensity distribution.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0019] Hereinafter, a plurality of embodiments of the present invention will be explained in detail by using the accompanying drawings. Fig. 1 shows a pixel circuit configuration of a display which is a first embodiment. In the pixel, a scan line 4 and a data line 5 are arranged so that they intersect with each other, and a region enclosed by the lines is a pixel region. Furthermore, an EL power supply line 6, and an EL common line 7 are connected.

[0020] In the inside of the pixel, a memory circuit 10 including an EL inverter circuit 1 comprised of an EL device 8 and a driving transistor 9, and including a CMOS inverter circuit 2 formed by CMOS connection is arranged. The memory circuit 10 is connected to the data line 5 through a main circuit of a scan transistor 3, and a gate of the scan transistor 3 is connected to the scan line 4.

[0021] Fig. 2 shows the operation of the EL inverter circuit 1. The driving transistor 9 is a p-channel transistor, and its source terminal is connected to the EL power supply line 6 and its drain terminal is connected to an anode of the EL device 8, and a cathode of the EL device 8 is connected to the EL common line 7. The EL power supply line 6 and the common line 7 are connected to all the pixels in common. By applying a positive voltage to the EL power supply line 6, and a negative voltage to the EL common line 7, the input and output terminals of the inverter circuit 1 are formed in such that, the gate electrode of the driving transistor 9 functions as the input terminal 61, and a terminal connecting the driving transistor 9 to the EL device 8 functions as the output terminal 62.

[0022] Fig. 3 shows the input and output characteristic of the EL inverter circuit 1. Since the EL device 8 exhibits in its current-voltage characteristic an exponential function characteristic similar to a diode having a threshold value, when the input voltage is at a high level near the EL power supply line 6, since the driving transistor 9 is in an off state, the output terminal 62 exhibits a low voltage substantially the same as the EL common line 7. When the voltage of the input terminal 61 is gradually lowered, and upon exceeding the threshold value, the current of the main circuit of the driving transistor 9 starts to flow. As a result, corresponding to the current-voltage characteristic of the EL device 8, the output voltage rises. When the input voltage becomes further low, the current increases, the voltage of the output terminal further rises, and approaches the EL power supply voltage.

[0023] Since the EL inverter circuit 1 operates in this manner, the present circuit operates as a logical inversion circuit, that is, an inverter circuit including the EL device as a circuit device. Hereinafter, this circuit is referred to as an EL inverter circuit.

[0024] Fig. 4 shows a configuration of a memory circuit which is formed by combining the EL inverter circuit with a CMOS inverter circuit. In the basic configuration of the memory, input terminals of two inverters are connected mutually

to output terminals of the other. A logical state is input to this junction point from the outside as the input terminal of data, and the stable state of the circuit is controlled, and by reading out the data as the output terminal without changing the state of the circuit, this circuit is used as a memory circuit.

[0025] In Fig. 4, the input terminal 61 of the EL inverter 1 is connected to an output terminal 71 of the CMOS inverter 2. Also the input terminal 73 of the CMOS inverter 2 is connected to the output terminal 62 of the EL inverter 1, and by this connection, the combined circuit functions as a memory cell which assumes a bistable state.

[0026] When used as a memory cell, by using the input terminal 61 of the EL inverter 1 as the input terminal 71 of data, the memory cell suitable for light load and high speed operation is formed. Since this is a thin film structure formed on a wide area as far as possible within the pixel, so as to make the EL device 8 emit light, a capacitance 75 between the terminals is large. Accordingly, when the output terminal 62 of the EL inverter 1 is used as the data input terminal, a large capacitance will be obtained.

[0027] When comparing this value, the capacitance of the input terminal 61 of the EL inverter 1 is about 30 f F which can be regarded as the gate capacitance of one transistor, supposing that the size for all the transistors of the circuit; a gate length, gate width is 10 μm, gate capacitance is 0.3 fF/μm^2. On the other hand, when the output terminal of the other EL inverter is used as the data input terminal, the capacitance of the EL device becomes 1.9 pF, and the capacitance becomes large as large as 63 times, supposing that the pixel size is 100μm^2, the aperture ratio is 70 %, the thickness of the EL device is 0.1μm, and the average relative dielectric constant e of the EL device is 3.

[0028] For this reason, when the data is written through the matrix line, it takes a long time, and the driving of a high resolution panel having a short scan time, and a large-size panel having an increased line resistance becomes difficult. Therefore, it is an important point in order to achieve the high performance to use the junction point between the input terminal 61 of the EL inverter circuit 1 and the output terminal 71 of the CMOS inverter circuit 2 as an input terminal of the memory cell.

[0029] The operation of the pixel configuration using the memory cell mentioned above will be explained. In the memory circuit of Fig. 1, the input terminal 11 of the memory cell 10 is connected to the data line 5 through the main circuit of the scan transistor 3, and the conductivity of the scan transistor 3 is controlled by the voltage of the scan line 4.

[0030] Fig. 5 shows an embodiment of the present invention. A display region 22 is formed by arranging the pixels 21 each containing therein the memory cell explained in Fig. 1, and in order to drive the matrix, a shift register 24 is connected to the data line, and a scan driving circuit 23 is connected to the scan line. The control signal for controlling the circuit operation and the display data are supplied through an input line 25. Also the EL power supply line 6 of the pixels 21 and the EL common line 7 are together connected to a pixel power supply 26.

[0031] According to the present embodiment, the feature is that the driving circuit has a simple configuration because a high speed writable memory is contained within the pixel, and in the driving circuit around the display region, it is only necessary to provide a digital shift register.

[0032] Fig. 6 shows the display operation of the pixel. A scan pulse for sequentially scanning the matrix in one frame period is applied to the scan line. Binary data of high and low levels corresponding to on and off states of the pixels in the row of the matrix is supplied to the data line. At the timing at which the scan pulse is applied, a voltage state of the data line is fetched into the memory cell. At this time, when the data is at the L-level, the output of the EL inverter is inverted to become the H-level. On the other hand, the output of the CMOS inverter on the contrary becomes the L-level, and this level is held in the memory cell. At this time, since the transistor in the EL inverter is in a conduction state, the current flows in the EL device, and the organic EL device becomes the light emission state.

[0033] Furthermore, when the data line is at the H-level at the time when the scan pulse is applied, the output of the EL inverter is changed to L-level, and the output of the CMOS inverter is changed to H-level. In this state, since the current does not flow the EL device, it becomes light non-emission state. As mentioned above, the pixel can operate to fetch the voltage state of the data line into the memory cell in response to the scan pulse.

[0034] Next, a second embodiment shown in Fig. 7 will be explained. In the present embodiment, the transistors within the pixel are all formed by only p-channel type having the same threshold value characteristic. By this configuration, the feature is that the transistor fabrication process is simplified, and it is possible to manufacture at low cost.

[0035] In the circuit configuration, the EL device 8 and the driving transistor 9 have the same configuration as the first embodiment. The other set of inverter is not the CMOS inverter, but a PMOS inverter 47 in which all the transistors are formed by p-channel transistors. The operation of this circuit will be explained below.

[0036] The PMOS inverter 47 is formed by two p-channel transistors including a reset transistor 46 and a set transistor 43, and one MOS diode which is a bias diode 44, and a bias capacitance 45. The set transistor 43 is turned on when it changes the output of inverter 47 to a L-(logical low) level. In order to change the output of the set transistor 43 to the L-level, which is the p-channel type, the gate voltage of the set transistor 43 is made to be lower than the voltage of the EL common line 7 by the bias capacitance 45 and the bias diode 44. The reset transistor 46 is turned on when its output is made to change to H-(logical high) level.

[0037] When connected in this manner, the PMOS inverter 47 has its input terminal 49 connected to the input terminal 48 of the EL inverter, and the output terminal 50 is connected to the gate of the reset transistor 46. Also, the input terminal

49 is connected to the gate of the driving transistor 9. Since the gate terminal 49 of the set transistor 43 is always connected to the diode 44, it is normally at the voltage value of the EL common voltage, and the set transistor 43 is in the off state.

[0038] Here, as the input signal, when the data signal is changed from the H-level to L-level, since it is capacitance-coupled by the bias capacitance 45, the gate terminal 49 of the set transistor 43 is pulled down. As a result, the set transistor 43 conducts, and the output terminal 48 is changed to L-level. Consequently, since the EL inverter produces a logical inversion signal, the output terminal 50 becomes H-level and the EL device is turned on. The gate voltage of the reset transistor 46 is at H-level, and the reset transistor 46 becomes off state. Thus, the output 48 of the PMOS inverter 47 holds the L-level.

[0039] Next, in the case where the input 49 of the pixel changed to H-level, the gate of the set transistor 43 becomes off state due to the capacitance coupling. Since it is connected also to the gate of the driving transistor 9, the output 50 of the EL inverter is changed to L-level, and by this the reset transistor 46 becomes on state, and the output of the PMOS inverter 47 changes to H-level.

[0040] As mentioned above, this pixel circuit is a bistable circuit in which the output terminal of the EL inverter circuit is able to hold H- or L-level, and it possesses the function as a memory. Furthermore, in the PMOS inverter 47, since the current flows only when the state of the circuit is changed, regardless of the fact that it is a logical circuit formed by only the PMOS transistors, there is an advantage that the power consumption is very small. In this respect, the diode may be replaced by a resistor, and in the case of the resistor, an alternating current coupling circuit including a time constant circuit is connected to the input circuit of the set transistor 43. As the resistor, a high resistance layer such as i-Si (intrinsic silicon) etc. may be used, and which makes the device structure simple as compared with the diode. Also, since it is only necessary to control the time constant, the writing at high speed becomes possible.

[0041] Furthermore, as a circuit configuration for small power consumption, there is a third embodiment in which all the transistors are formed by n-channel type transistors. As shown in Fig. 8, all the transistors are formed by N-type. They are a scan transistor 143, set transistor 142, reset transistor 144, and bias diode 145.

[0042] The circuit operation is the same as the second embodiment. When it is intended to form this circuit with thin-film transistors, since it is possible to reduce the current during off state of the transistors to a great extent by employing the leakage current reducing structure such as a LDD structure with N-ch TFT, and a series connection configuration of transistors, the power consumption of circuit can be further reduced as compared with the second embodiment. As to the configuration for reducing the leakage current, a general method may be used.

[0043] In the second and third embodiments, when the on state of pixel is continued, both the set transistor and the reset transistor enter the off state. Then the voltage of the input terminal of the EL inverter gradually rises from the L-level due to the leakage current of the scan transistor, and becomes unstable and the current of the driving transistor gradually decreases. Therefore, this situation is avoided by applying a H level voltage each time the data signal is scanned.

[0044] Fig. 9 shows the operation of the shift register. Within a period during which a scan pulse 131 is applied to the scan line, shift clocks are applied during a period in which data is being shifted. In the period of the scan pulse 131, first, all the data line output terminals go to H-level together. During this period, PMOS inverter input terminals of all the pixels on one line go to H-level. This period must be held for at least the propagation delay time of the data line. Thereafter, the data is sequentially aligned for one line by the shift register. Thereafter, the state of each data output is held for the propagation delay time or longer of the data line, and the data is fetched to the pixel, and the scan pulse finishes.

[0045] In order to realize the operation mentioned above, initializing means is provided in a latch of each stage of the shift register so that the latch becomes H-level in the reset state, and the shift clock may be applied intermittently.

[0046] Fig. 10 shows a fourth embodiment. This is an example of configuration of a panel of a portable telephone and the like, and a video display region 92 by an organic EL device matrix driven by a TFT and a peripheral driving circuit, and organic EL device indicator 93 are formed on the same glass substrate 91, and a data control signal and a power supply are supplied through a flexible print substrate 95.

[0047] The pixel circuit 96 is connected to drive the organic EL device indicator 93, and the pixel circuit 96 is used not only for the matrix pixel having a feature of memory function and low power driving, but also as the display driving control circuit of individual organic EL device indicator. Thus, by turning off the video display, and turning on the indicator 94 only, and by rewriting by applying the data and the scan pulse and the control signal to the pixel circuit 96 only when the display condition is to be changed, it is possible to reduce the power at the time of stand-by.

[0048] Fig. 11 shows a fifth embodiment. In the present embodiment, the input and output terminals of two inverters including a logical EL inverter 81 and a display EL inverter 82 are mutually connected, and a pixel circuit is formed by only three transistors. In this case, since the EL devices are alternately turned on responsive to the memory state, by making the area of the load EL device 83 smaller than the EL device used for display, and by providing a covering layer 84 to cover the light emission portion so that the display is not disturbed, the number of the transistors can be decreased without degrading the display contrast.

[0049] Fig. 12 is a mask layout diagram of the pixel circuit shown in Fig. 1. The scan line 4, data line 5, EL power supply line 6, EL common line 7, CMOS inverter 2, driving transistor 3, and EL display electrode 115 are arranged.

Although not shown, an organic EL layer, and an EL cathode layer connected to the common line 7 with the same voltage are deposited on all over the surface of the pixel. As shown, the EL power supply line 6, and EL common line 7 are arranged in the vertical direction, so that they are aligned orthogonal to the scan line, and by virtue of this, an advantage is obtained in which at the time of line sequential driving, even when the loads for each column are varied simultaneously, since the current on the power supply line 6 is stable and not varied, the memory content is also stable and satisfactory display is provided.

[0050] Furthermore, when many lines are arranged in the vertical direction, the EL display electrode 115 will become small and narrow, however, the display in the case where the light emission region occupying the pixel is small, as shown in the pixel light emission condition diagram in Fig. 13, the light emission occurs at very small portion within the pixel arranged in matrix.

[0051] The brightness condition of this pixel is shown in Fig. 14. The place dependency of the light emission brightness in a narrow and small pixel light emission region 122 and a wide light emission region 121 is shown. In the case where an average brightness of the whole pixel is combined, in the narrow and small pixel brightness 124, a brightness higher than the brightness 125 of a wide pixel appears in a spot-like, as a result, even when the environment light 123 is high, since the brightness of the light emission portion is high, the interpretation of the display becomes easy. This enables to see the display in good condition even at the light place with limited power such as a portable telephone, and there is a feature that the display easily visible can be provided with low power.

[0052] The intensity of environment light, supposing in the outdoor, is 10000 lux, and considering that the light illuminates a complete diffusion surface, the brightness of reflected light is 3000 cd/m^2 or larger. At this time, the relationship between the average brightness and the brightness of light emission portion, the aperture ratio is expressed in the equation (1) below.

$$\text{average brightness} = \text{brightness of light emission portion} \times \text{aperture ratio} \qquad (1)$$

[0053] Here, when substituting > 3000 (cd/m^2) as the outdoor environment light for the brightness of light emission portion in equation (1), it becomes that aperture ratio < average brightness/3000. For example, since the average brightness in the notebook type personal computer is 100 (cd/m^2), the aperture ratio of the light emission portion may be 3%. In this manner, by determining the aperture ratio from equation (1), it is possible to visualize the display even in the light environment.

[0054] In this respect, since the aperture ratio of the pixel in Fig. 12 is 15%, supposing that the average brightness is 450 (cd/m^2), a desired display characteristic can be obtained. In particular, by combining with the pixel having the memory built-in according to the present invention, since it is possible to visualize a satisfactory display excellent in the uniformity of display characteristic under the outdoor environment light, it is suitable for the portable information equipment such as a portable telephone, portable TV set, etc.

[0055] According to the present invention, since it is possible to simplify the memory circuit built-in the pixel of the emissive display, an advantage is provided in which a high resolution image can be realized. Also, the power consumption of the circuit of the display is reduced. Furthermore, under the environment light, the display excellent in the uniformity of display characteristic can be provided.

Claims

1. An emissive display having one or more pixels enclosed by a plurality of scan lines (4) and a plurality of signal lines (5) intersecting with each other, each pixel comprises an electroluminescent device (8) formed by an organic multi-layer driven by a current and a memory circuit (10) having a first inverter circuit (1) and a second inverter circuit (2), wherein the first inverter circuit (1) comprises a display control circuit having at least one first transistor (9), said memory circuit stores display information of said pixel according to a conduction state or a non-conduction state of the source-drain circuit of the first transistor (9), and controls the on and off state of said electroluminescent device on a binary basis, **characterized in that** the first inverter circuit (1) comprises said electroluminescent device (8) as a load device, and **in that** the source-drain circuit of the transistor (9) is serially connected with the electroluminescent device (8).

2. An emissive display according to claim 1, wherein
said memory circuit (10) constitutes a bi-stable circuit in which an input terminal of one of said first and second

inverter circuits is mutually connected to an output terminal of the other of said first and second inverter circuits, and the gate terminal portion of the transistor (9) of said first inverter circuit (1) is connected to said signal line (5) through the source-drain circuit of a second transistor (3), and the gate of said second transistor (3) is connected to the scan line (4), thereby to provide an input circuit for inputting data to be stored in said memory circuit (10).

3. An emissive display according to claim 1 or 2, wherein said second inverter circuit comprises a CMOS inverter.

4. An emissive display according to claim 2, wherein a series-parallel conversion circuit using a shift register (24) is provided outside the display region (22) aligned with said pixel, wherein each output of each stage of said shift register (24) is connected to a corresponding signal line

5. An emissive display according to claim 1, wherein the first inverter circuit is connected between a power supply line (6) and a reference voltage line (7), the memory circuit comprising:

a sampling circuit connected to an input terminal of said first inverter circuit for controlling the connection with said signal line (5) in response to a scan pulse applied through said scan line; a set circuit for controlling the connection between said power supply line (6) and the input terminal of said first inverter circuit, by an output of said first inverter circuit; and
a reset circuit for controlling the connection between the reference voltage line (7) and the input terminal of said first inverter circuit, by a signal voltage sampled by said sampling circuit.

6. An emissive display according to claim 5, wherein said set circuit or said reset circuit is provided with an AC coupling circuit formed by using a capacitance (45) and a diode (44) or a resistor for applying an input signal exceeding a voltage of the power supply or the reference voltage to a gate terminal of the transistor, and all the transistors of said pixel are formed by P-type or N-type.

7. An emissive display according to claim 5, wherein
a signal shift register capable of outputting a binary signal is connected to said signal line, and a scan line driver circuit generating a scan pulse to select the pixel is connected to said scan line, and
an initialized period is provided in said signal shift register so that said signal line applies a logical signal to turn off said electroluminescent device within a scan pulse period.

8. An emissive display according to claim 1 or 2, wherein the second inverter circuit comprises a further electroluminescent device and covering means to cover the further electroluminescent device.

9. An emissive display according to claim 1 or 2, wherein in said pixel, a relationship of an aperture ratio < average brightness [cd/m^2] / 3000 [cd/m^2] is present between the aperture ratio and the average brightness, where the aperture ratio is the area ratio of the area of light emission area to the pixel area.

10. An emissive display according to claim 1 or 2, wherein a power supply and reference voltage line of said inverter circuit are arranged in a vertical direction of the pixel, and a relationship of an aperture ratio < an average brightness [cd/m^2] / 3000 [cd/m^2] is present between the aperture ratio and the average brightness, where the aperture ratio is the area ratio of the area of light emission area to the pixel area.

Patentansprüche

1. Emittierende Anzeige mit einem oder mehreren Bildpunkten, die von mehreren Abtastleitungen (4) und mehreren Signalleitungen (5), die einander schneiden, umschlossen sind, wobei jeder Bildpunkt eine elektrolumineszente Vorrichtung (8) umfasst, die von einer durch einen Strom betriebenen organischen Mehrschicht und einer Speicherschaltung (10), die eine erste Wechselrichterschaltung (1) und eine zweite Wechselrichterschaltung (2) aufweist, gebildet wird, wobei die erste Wechselrichterschaltung (1) eine Anzeigesteuerungsschaltung mit zumindest einem ersten Transistor (9) umfasst, die Speicherschaltung Anzeigeinformationen des Bildpunkts nach Maßgabe eines Leitungszustands oder eines Nicht-Leitungszustands der Quelle-Senke-Schaltung des ersten Transistors (9) speichert und den Ein- und Aus-Zustand der elektrolumineszenten Vorrichtung auf binärer Basis steuert, **dadurch gekennzeichnet, dass** die erste Wechselrichterschaltung (1) die elektrolumineszente Vorrichtung (8) als Lastvorrichtung umfasst und dass die Quelle-Senke-Schaltung des Transistors (9) mit der elektrolumineszenten Vorrichtung (8) seriell geschaltet ist.

2. Emittierende Anzeige nach Anspruch 1, wobei
die Speicherschaltung (10) eine bi-stabile Schaltung darstellt, in der ein Eingabeanschluss der einen von der ersten und zweiten Wechselrichterschaltung mit einem Ausgabeanschluss der anderen von der ersten und zweiten Wechselrichterschaltung wechselseitig verbunden ist, und
der Gate-Anschlussbereich des Transistors (9) der ersten Wechselrichterschaltung (1) durch die Quelle-Senke-Schaltung eines zweiten Transistors (3) mit der Signalleitung (5) verbunden ist und das Gate des zweiten Transistors (3) mit der Abtastleitung (4) verbunden ist, so dass dadurch eine Eingabeschaltung zur Eingabe von Daten, die in der Speicherschaltung (10) gespeichert werden sollen, bereitgestellt wird.

3. Emittierende Anzeige nach Anspruch 1 oder 2, wobei die zweite Wechselrichterschaltung einen CMOS-Wechselrichter umfasst.

4. Emittierende Anzeige nach Anspruch 2, wobei eine Serien-Parallel-Wandlungsschaltung, die ein Schieberegister (24) verwendet, außerhalb des mit dem Bildpunkt ausgerichteten Anzeigebereichs (22) vorgesehen ist, wobei jeder Ausgang jeder Stufe des Schieberegisters (24) mit einer entsprechenden Signalleitung verbunden ist.

5. Emittierende Anzeige nach Anspruch 1, wobei die erste Wechselrichterschaltung zwischen einer Leistungszufuhrleitung (6) und einer Bezugsspannungsleitung (7) geschaltet ist, wobei die Speicherschaltung Folgendes umfasst:

eine mit einem Eingabeanschluss der ersten Wechselrichterschaltung verbundene Abtastschaltung zum Steuern der Verbindung mit der Signalleitung (5) in Ansprechung auf einen durch die Abtastleitung angelegten Abtastimpuls;
eine eingestellte Schaltung zum Steuern der Verbindung zwischen der Leistungszufuhrleitung (6) und dem Eingabeanschluss der ersten Wechselrichterschaltung durch eine Ausgabe der ersten Wechselrichterschaltung; und
eine rückgestellte Schaltung zum Steuern der Verbindung zwischen der Bezugsspannungsleitung (7) und dem Eingabeanschluss der ersten Wechselrichterschaltung durch eine von der Abtastschaltung abgetastete Signalspannung.

6. Emittierende Anzeige nach Anspruch 5, wobei die eingestellte Schaltung oder die rückgestellte Schaltung mit einer Wechselstrom-Koppelschaltung versehen ist, die durch Verwendung einer Kapazität (45) und einer Diode (44) oder eines Registers zum Anlegen eines Eingabesignals gebildet wird, das eine Spannung der Leistungszufuhr oder die Bezugsspannung zu einem Gate-Anschluss des Transistors übersteigt, und alle Transistoren des Bildpunkts durch einen P-Typ oder N-Typ gebildet sind.

7. Emittierende Anzeige nach Anspruch 5, wobei
ein zur Ausgabe eines binären Signals fähiges Signalschieberegister mit der Signalleitung verbunden ist und eine Abtastleitung-Treiberschaltung, die zur Auswahl des Bildpunkts einen Abtastimpuls erzeugt, mit der Abtastleitung verbunden ist, und in dem Signalscheiberegister eine Initialisierungsperiode vorgesehen ist, so dass die Signalleitung zur Abschaltung der elektrolumineszenten Vorrichtung innerhalb einer Abtastimpulsperiode ein logisches Signal anlegt.

8. Emittierende Anzeige nach Anspruch 1 oder 2, wobei die zweite Wechselrichterschaltung eine weitere elektrolumineszente Vorrichtung und Abdeckmittel zum Abdecken der weiteren elektrolumineszenten Vorrichtung umfasst.

9. Emittierende Anzeige nach Anspruch 1 oder 2, wobei
in dem Bildpunkt eine Beziehung eines Öffnungsverhältnisses < Durchschnittshelligkeit [cd/m^2] / 3000 [cd/m^2] zwischen dem Öffnungsverhältnis und der Durchschnittshelligkeit vorhanden ist, wobei das Öffnungsverhältnis das Flächenverhältnis der Fläche der Lichtemissionsfläche zur Bildpunktfläche ist.

10. Emittierende Anzeige nach Anspruch 1 oder 2, wobei
eine Leistungszufuhr und eine Bezugsspannungsleitung der Wechselrichterschaltung in vertikaler Richtung des Bildpunkts angeordnet sind und eine Beziehung eines Öffnungsverhältnisses < einer Durchschnittshelligkeit [cd/m^2] / 3000 [cd/m^2] zwischen dem Öffnungsverhältnis und der Durchschnittshelligkeit vorhanden ist, wobei das Öffnungsverhältnis das Flächenverhältnis der Fläche der Lichtemissionsfläche zur Bildpunktfläche ist.

Revendications

1. Dispositif d'affichage émissif ayant un ou plusieurs pixel(s) entouré(s) par une pluralité de lignes de balayage (4) et une pluralité de lignes de signal (5) s'entrecoupant, chaque pixel comprenant un dispositif électroluminescent (8) formé par une multicouche organique entraînée par un courant et un circuit de mémoire (10) ayant un premier circuit inverseur (1) et un second circuit inverseur (2), dans lequel le premier circuit inverseur (1) comprend un circuit de commande d'affichage ayant au moins un premier transistor (9), ledit circuit de mémoire stocke des informations d'affichage dudit pixel selon un état de conduction ou un état de non conduction du circuit source-drain du premier transistor (9), et commande l'état marche et arrêt dudit dispositif électroluminescent sur une base binaire, **caractérisé en ce que** le premier circuit inverseur (1) comprend ledit dispositif électroluminescent (8) en tant que dispositif de charge, et **en ce que** le circuit source-drain du transistor (9) est connecté en série avec le dispositif électroluminescent (8).

2. Dispositif d'affichage émissif selon la revendication 1, dans lequel ledit circuit de mémoire (10) constitue un circuit bistable dans lequel une borne d'entrée d'un parmi lesdits premiers et second circuits inverseurs est connecté mutuellement à une borne de sortie de l'autre parmi lesdits premier second circuits inverseurs, et
la partie de borne de grille du transistor (9) dudit premier circuit inverseur (1) est connectée à ladite ligne de signal (5) à travers le circuit source-drain d'un second transistor (3), et la grille du second transistor (3) est connectée à la ligne de balayage (4), produisant ainsi un circuit d'entrée pour entrer des données à stocker dans ledit circuit de mémoire (10).

3. Dispositif d'affichage émissif selon la revendication 1 ou 2, dans lequel ledit second circuit inverseur comprend un inverseur CMOS.

4. Dispositif d'affichage émissif selon la revendication 2, dans lequel un circuit de conversion série-parallèle utilisant un registre à décalage (24) est prévu à l'extérieur de la région d'affichage (22) alignée avec ledit pixel, dans lequel chaque sortie de chaque étage dudit registre à décalage (24) est connectée à une ligne de signal correspondante.

5. Dispositif d'affichage émissif selon la revendication 1, dans lequel le premier circuit inverseur est connecté entre une ligne d'alimentation de puissance (6) et une ligne de tension de référence (7), le circuit de mémoire comprenant : un circuit d'échantillonnage connecté à une borne d'entrée dudit premier circuit inverseur pour commander la connexion à ladite ligne de signal (5) en réponse à une impulsion de balayage appliquée à travers ladite ligne de balayage ; un circuit d'initialisation pour commander la connexion entre ladite ligne d'alimentation de puissance (6) et la borne d'entrée dudit premier circuit inverseur, par une sortie dudit premier circuit inverseur ; et
un circuit de réinitialisation pour commander la connexion entre la ligne de tension de référence (7) et la borne d'entrée dudit premier circuit inverseur, par une tension de signal échantillonnée par ledit circuit d'échantillonnage.

6. Dispositif d'affichage émissif selon la revendication 5, dans lequel ledit circuit d'initialisation ou ledit circuit de réinitialisation est pourvu d'un circuit de couplage AC formé en utilisant une capacité (45) et une diode (44) ou une résistance pour appliquer un signal d'entrée excédant une tension de l'alimentation de puissance ou la tension de référence à la borne de grille du transistor, et tous les transistors dudit pixel sont formés en type P ou en type N.

7. Dispositif d'affichage émissif selon la revendication 5, dans lequel le registre à décalage de signal capable de délivrer un signal binaire est connecté à ladite ligne de signal, et un circuit d'attaque de ligne de balayage générant une impulsion de balayage pour sélectionner le pixel est connecté à ladite ligne de balayage, et
une période initialisée est prévue dans ledit registre à décalage de signal de sorte que ladite ligne de signal applique un signal logique pour éteindre ledit dispositif électroluminescent dans une période d'impulsion de balayage.

8. Dispositif d'affichage émissif selon la revendication 1 ou 2, dans lequel le second circuit inverseur comprend un autre dispositif électroluminescent et des moyens de recouvrement pour recouvrir ledit autre dispositif électroluminescent.

9. Dispositif d'affichage émissif selon la revendication 1 ou 2, dans lequel dans ledit pixel, une relation d'un rapport d'ouverture < brillance moyenne [cd/m^2] / 3 000 [cd/m^2] est présente entre le rapport d'ouverture et la brillance moyenne, où le rapport d'ouverture est le rapport de surface de la surface d'émission de lumière par rapport à la surface de pixel.

10. Dispositif d'affichage émissif selon la revendication 1 ou 2, dans lequel l'alimentation de puissance et une ligne de

tension de référence dudit circuit inverseur sont arrangées dans une direction verticale du pixel, et une relation d'un rapport d'ouverture < brillance moyenne [cd/m^2] / 3 000 [cd/m^2] est présente entre le rapport d'ouverture et la brillance moyenne, où le rapport d'ouverture est le rapport de surface de surface d'émission de lumière par rapport à la surface de pixel.

FIG. 1

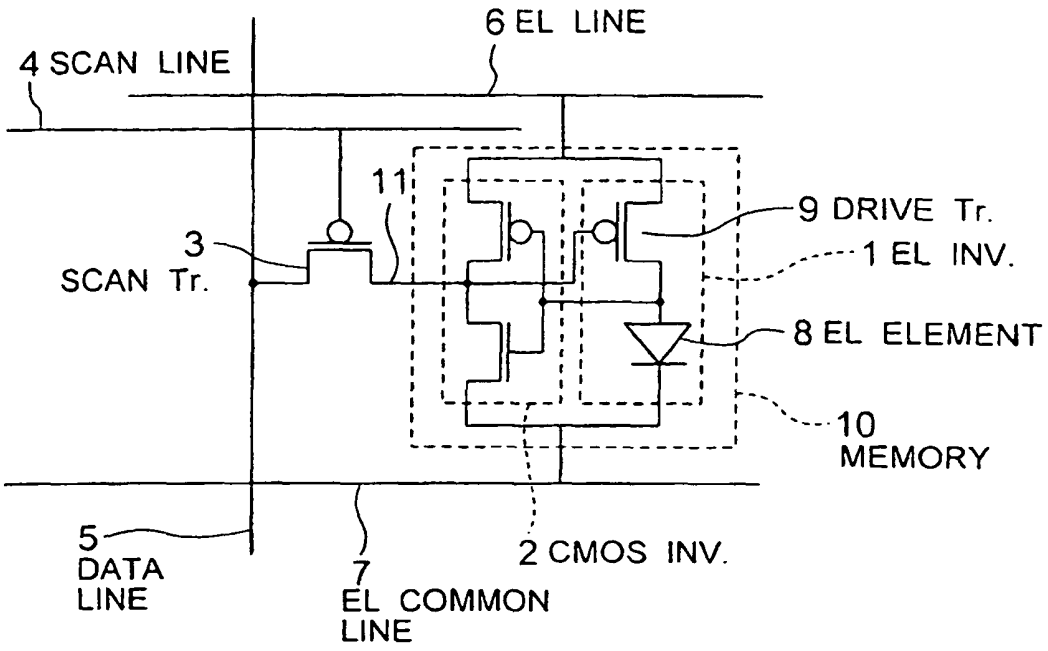

6 EL LINE
4 SCAN LINE
11
9 DRIVE Tr.
3
SCAN Tr.
1 EL INV.
8 EL ELEMENT
10
MEMORY
5
DATA
LINE
7
EL COMMON
LINE
2 CMOS INV.

FIG. 2

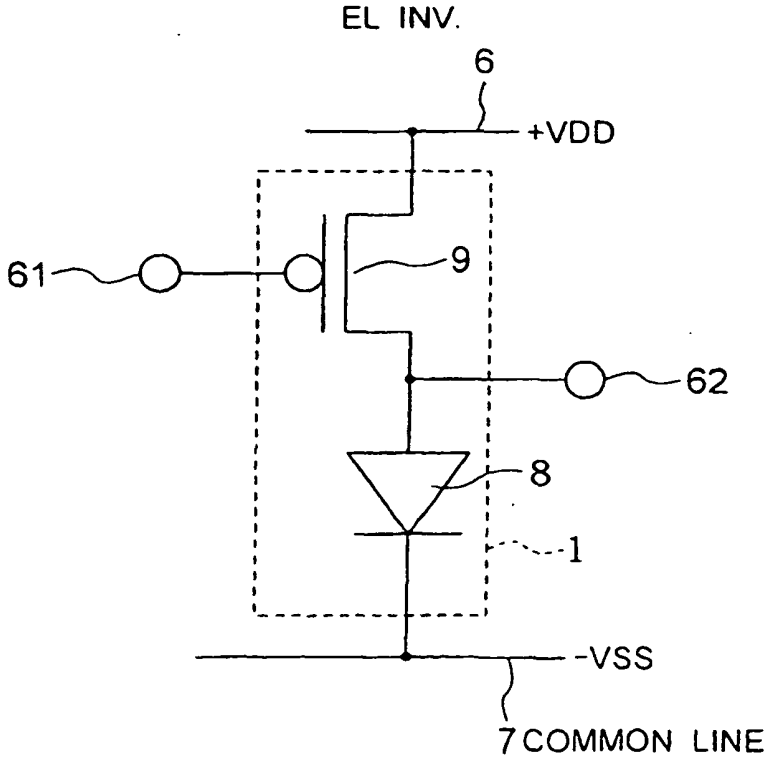

EL INV.
6
+VDD
61
9
62
8
1
-VSS
7 COMMON LINE

FIG. 3

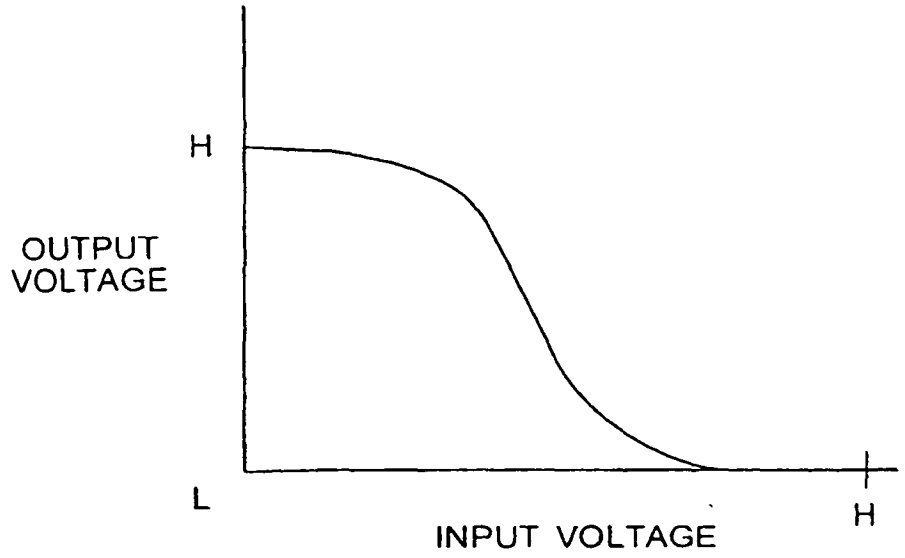


FIG. 4

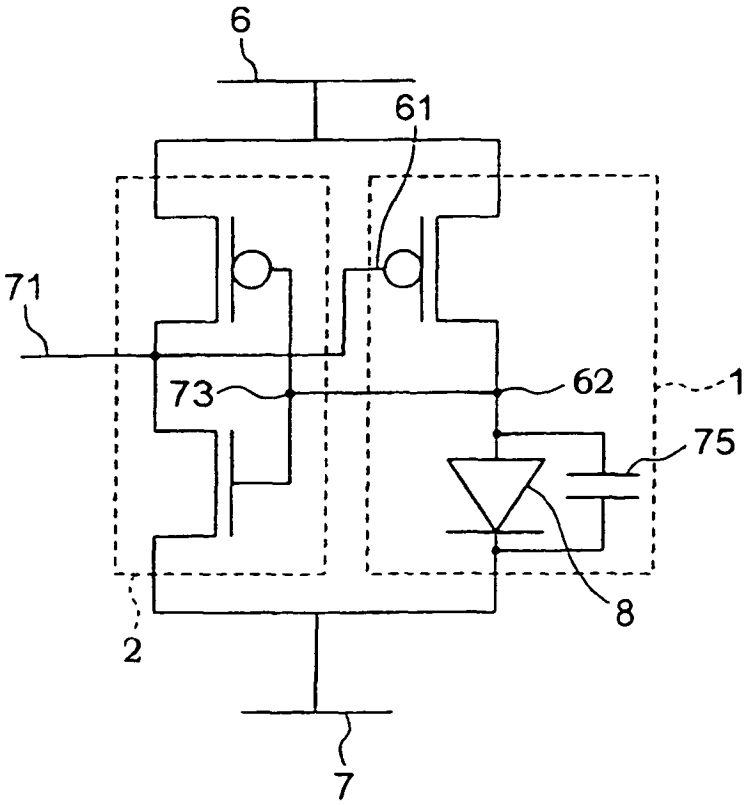


FIG. 5

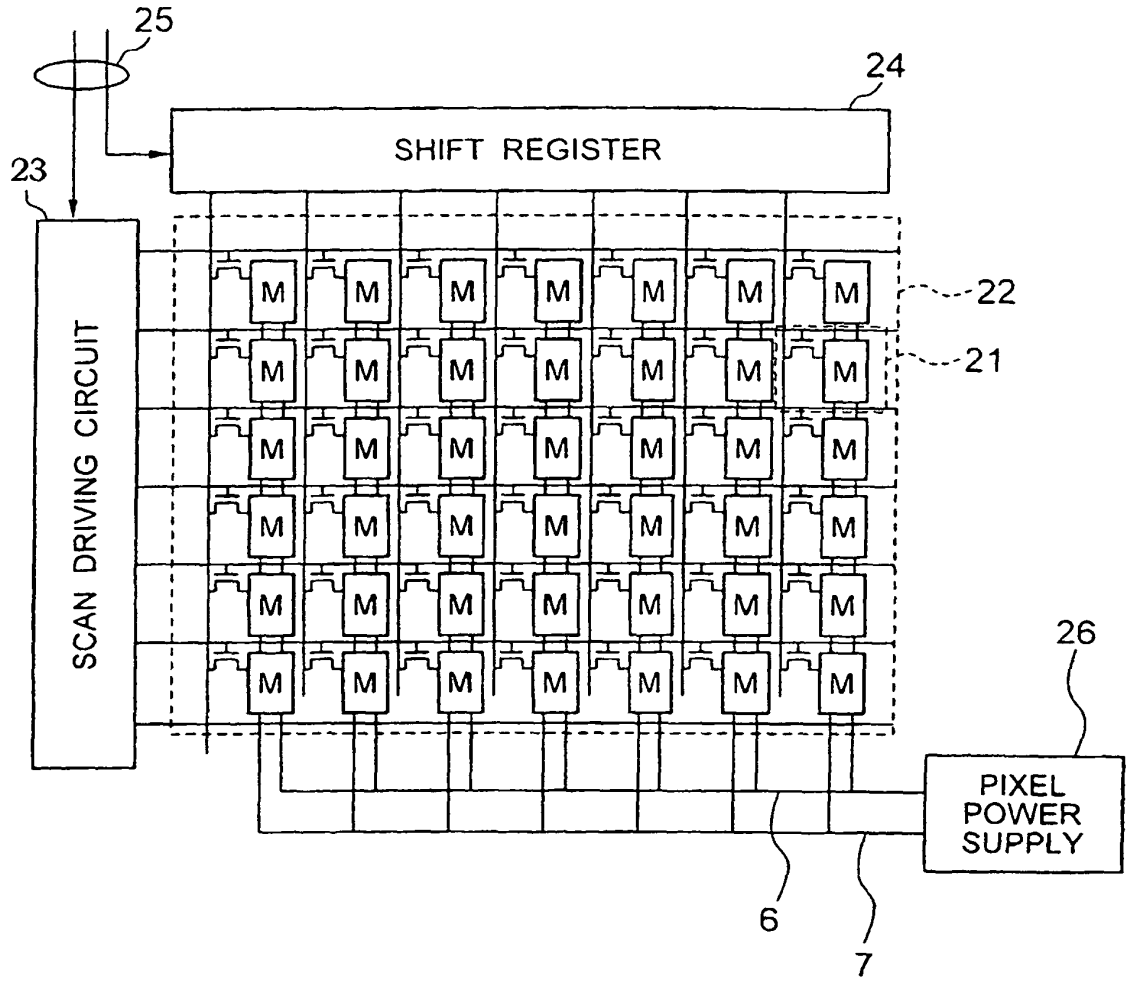

25
24
SHIFT REGISTER
23
SCAN DRIVING CIRCUIT
M
22
21
26
PIXEL POWER SUPPLY
6
7

FIG. 6

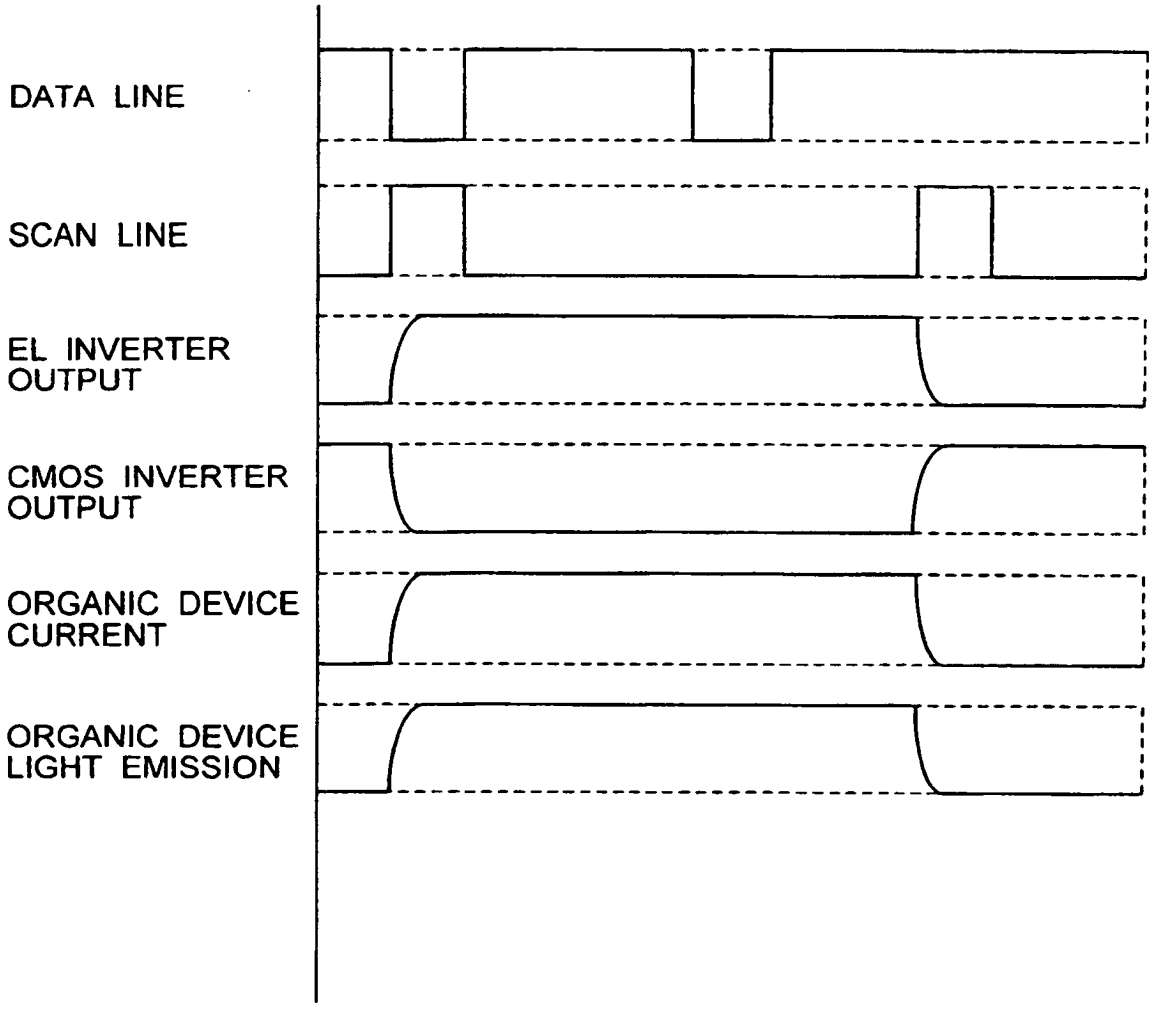

DATA LINE
SCAN LINE
EL INVERTER OUTPUT
CMOS INVERTER OUTPUT
ORGANIC DEVICE CURRENT
ORGANIC DEVICE LIGHT EMISSION

FIG. 7

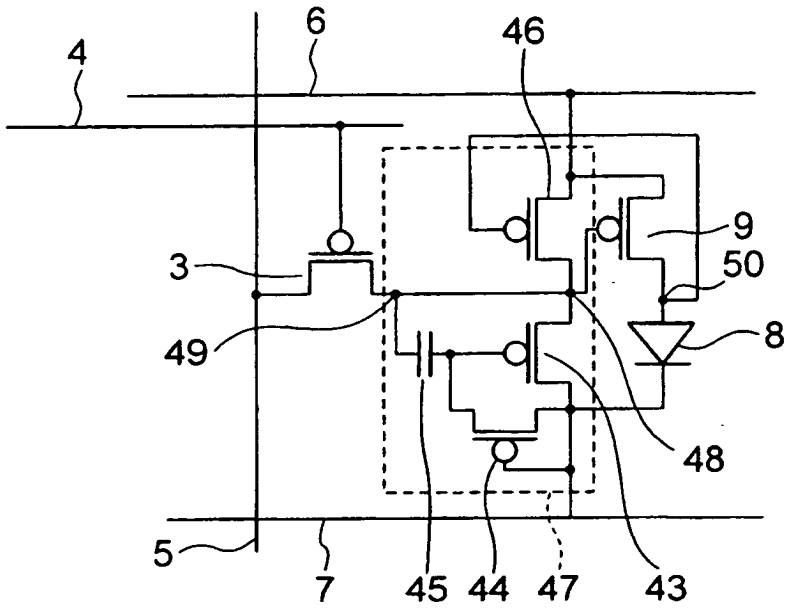


FIG. 8

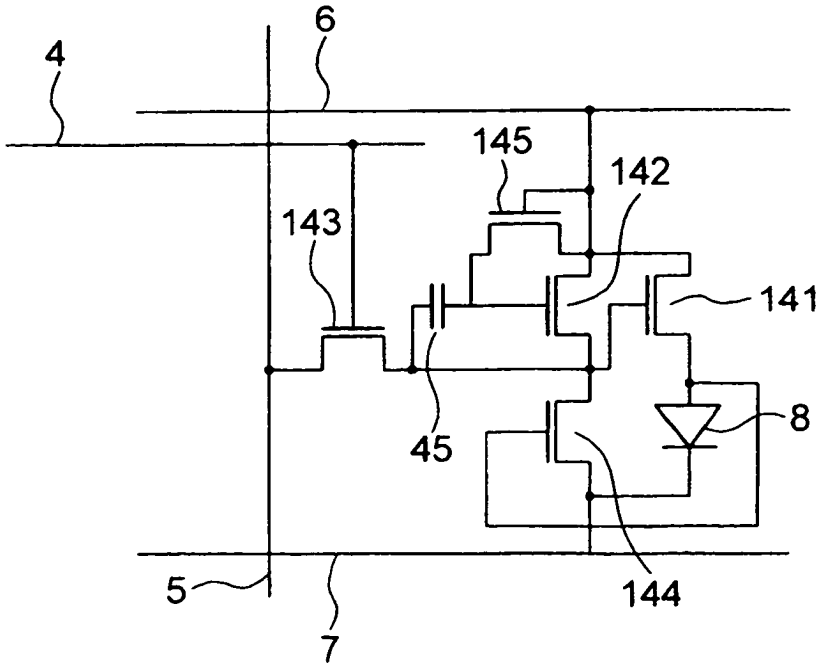


FIG. 9

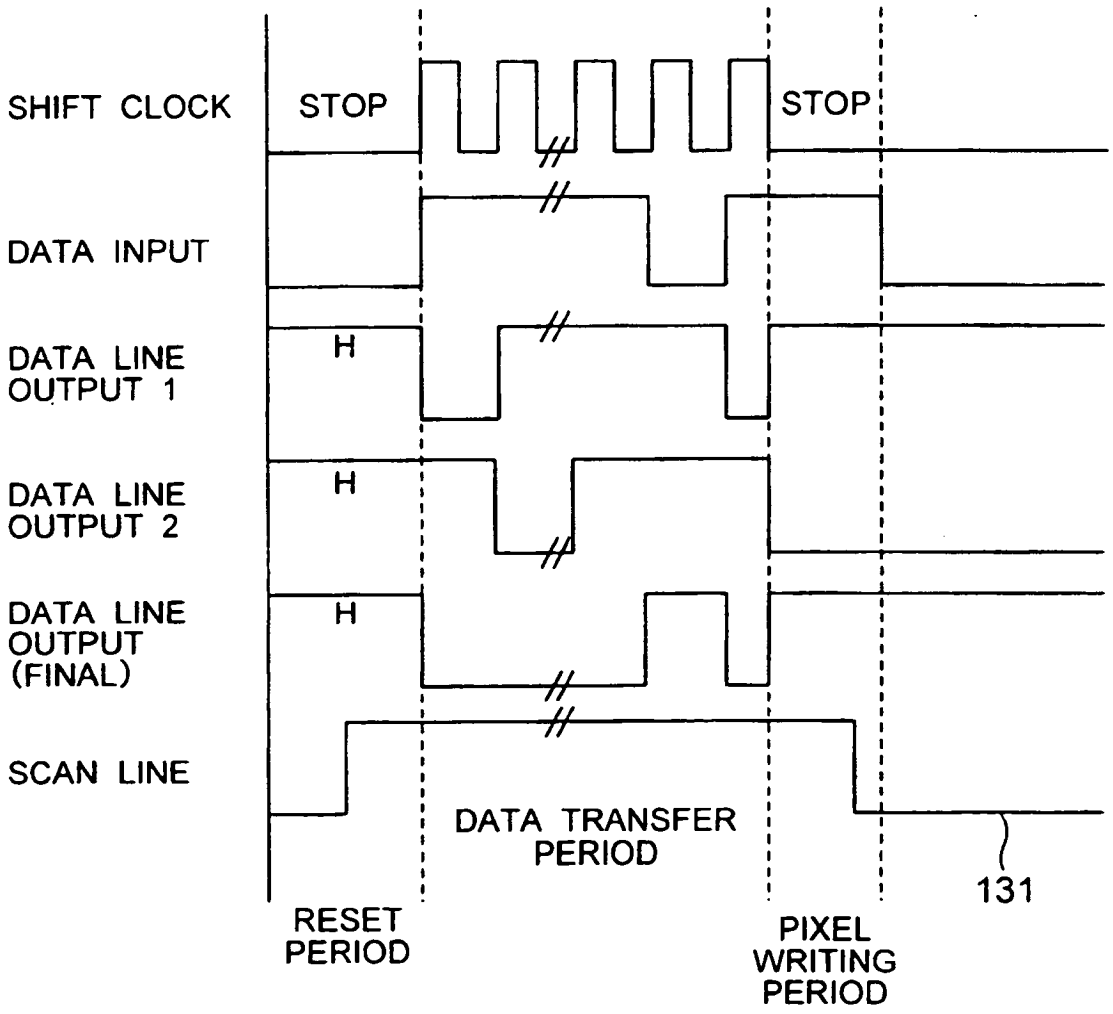

SHIFT CLOCK
STOP
STOP
DATA INPUT
DATA LINE OUTPUT 1
H
DATA LINE OUTPUT 2
H
DATA LINE OUTPUT (FINAL)
H
SCAN LINE
DATA TRANSFER PERIOD
131
RESET PERIOD
PIXEL WRITING PERIOD

FIG. 10

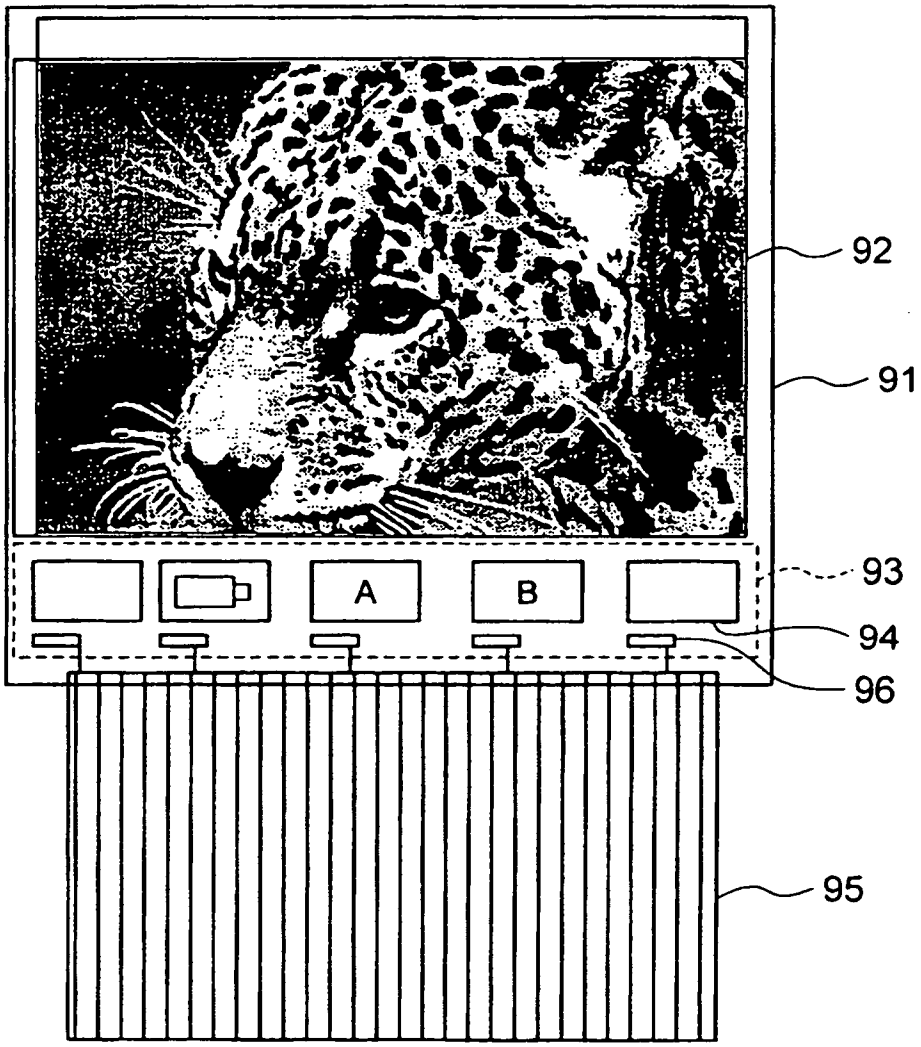


FIG. 11

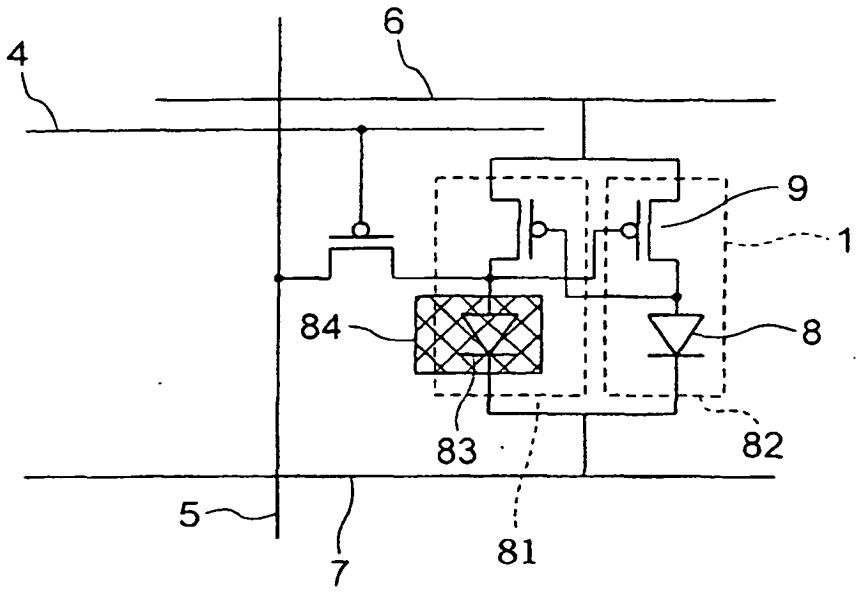


FIG. 12

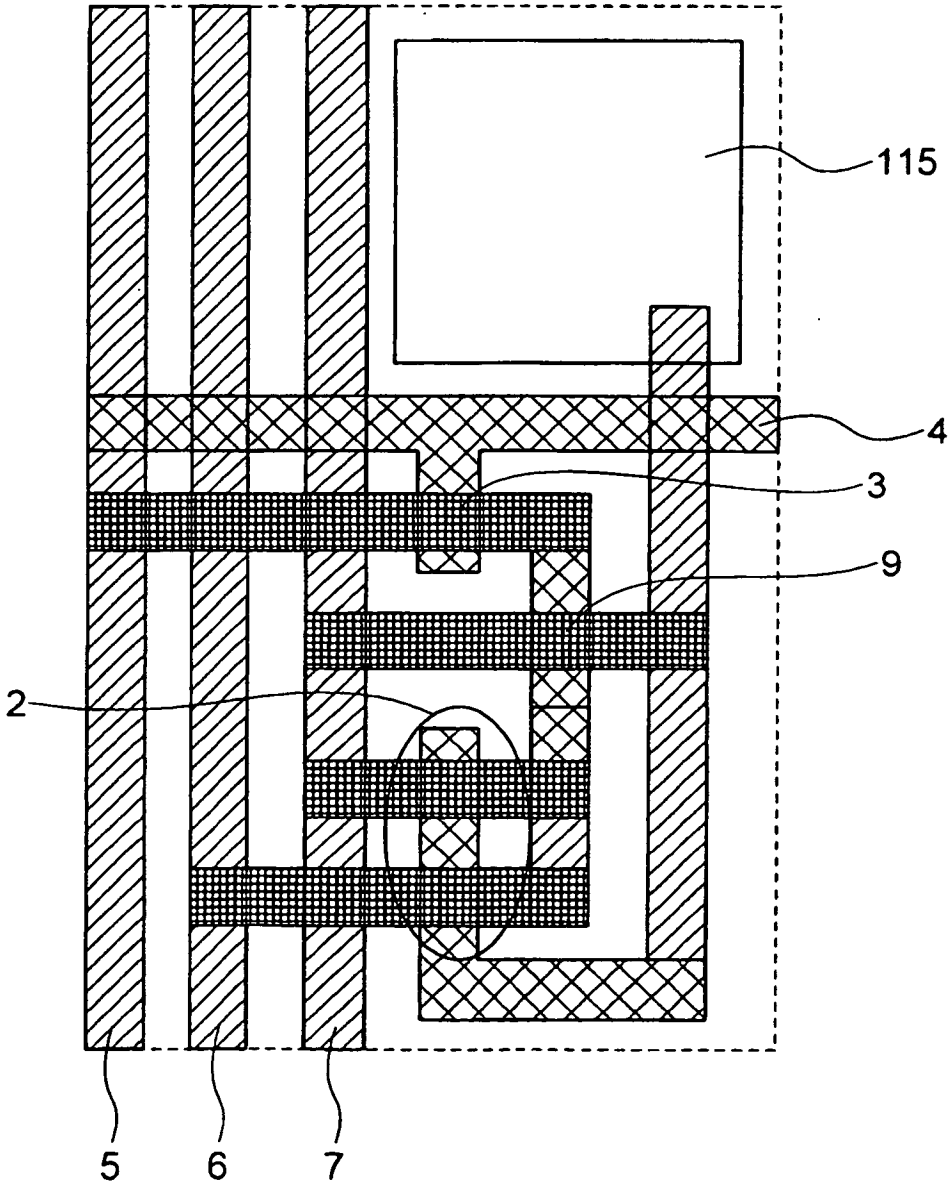


FIG. 13

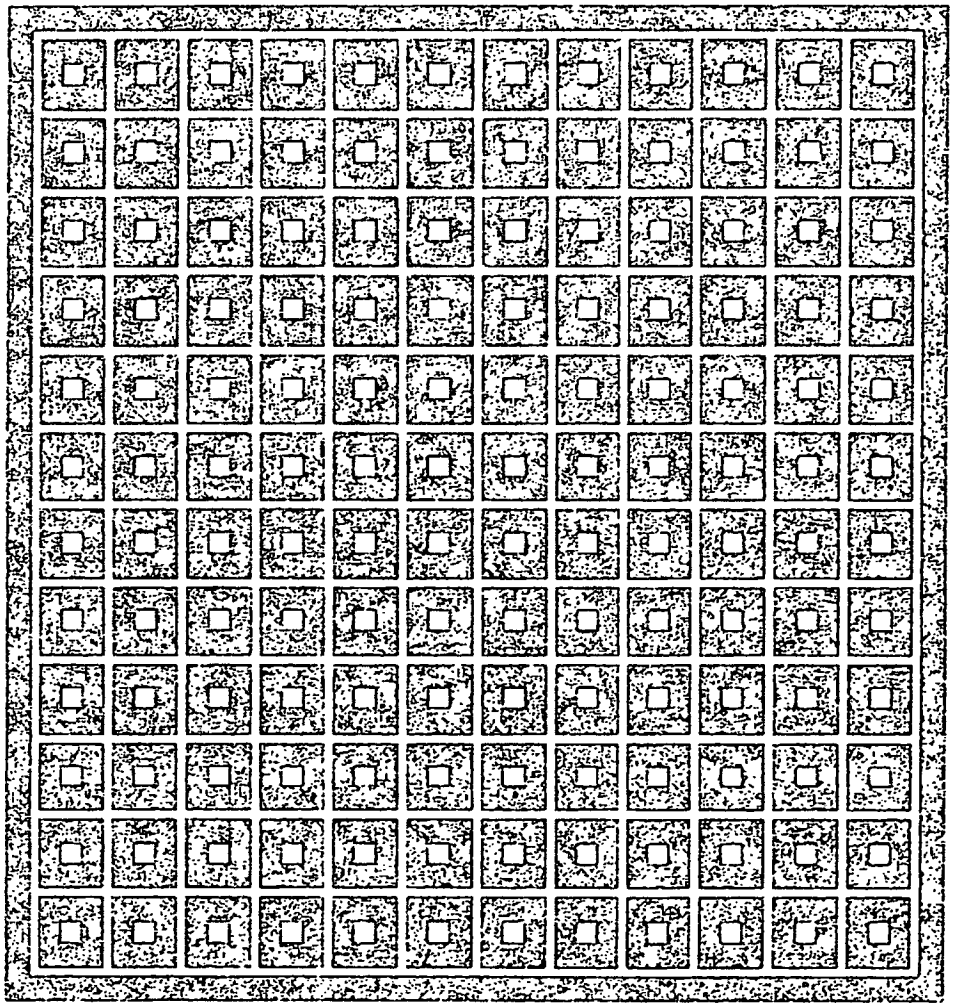
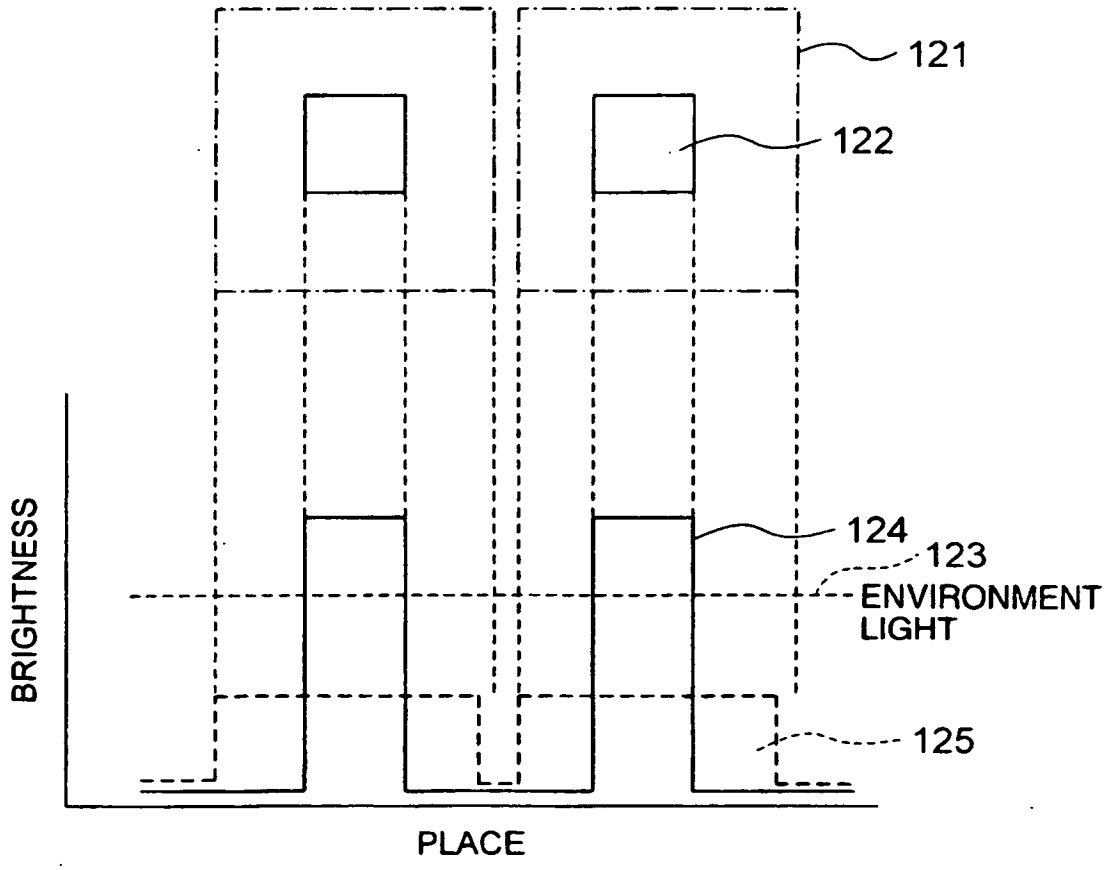


FIG. 14



专利名称(译)	使用有机电致发光器件的发光显示器		
公开(公告)号	EP1246157B1	公开(公告)日	2007-01-24
申请号	EP2001120624	申请日	2001-08-29
[标]申请(专利权)人(译)	株式会社日立制作所		
申请(专利权)人(译)	HITACHI，LTD.		
当前申请(专利权)人(译)	HITACHI，LTD.		
[标]发明人	MIKAMI YOSHIRO HITACHI LTD INT PROP GP OUCHI TAKAYUKI HITACHI LTD INT PROP GP KANEKO YOSHIYUKI HITACHI LTD INT PROP GP SATO TOSHIHIRO HITACHI LTD INT PROP GP		
发明人	MIKAMI, YOSHIRO, HITACHI, LTD., INT. PROP. GP. OUCHI, TAKAYUKI, HITACHI, LTD., INT. PROP. GP. KANEKO, YOSHIYUKI, HITACHI, LTD., INT. PROP. GP. SATO, TOSHIHIRO, HITACHI, LTD., INT. PROP. GP.		
IPC分类号	G09G3/32 H05B33/08 G09G3/20 G09G3/30 H01L51/50		
CPC分类号	G09G3/3258 G09G3/3291 G09G2300/0439 G09G2300/0465 G09G2300/0842 G09G2300/0857 G09G2300/0861 G09G2320/0252 G09G2330/021		
优先权	2001098864 2001-03-30 JP		
其他公开文献	EP1246157A2 EP1246157A3		
外部链接	Espacenet		

摘要(译)

提供一种使用有机电致发光器件（8）的发光显示器，其中简化了像素电路，增加了孔径比，实现了高分辨率，并且降低了功耗。在该配置中，在两组逆变器电路中，一组转换器电路由连接有机电致发光器件（8）和晶体管（9）的电路（1）串联形成，并且存储器电路的晶体管是省略。此外，在两组逆变器的相互连接中，显示数据被输入到与有机电致发光器件（8）串联连接的晶体管（9）的栅极连接的线，并且由于这种连接，写入减少了负载，并且通过能够高速写入来实现高分辨率。