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(54) **Pixel unit circuit, pixel array, display panel and display panel driving method**

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## Description

## BACKGROUND

5 **[0001]** Embodiments of the disclosed technology relate to a pixel unit circuit, a pixel array, a display panel and display panel driving method.

US2009/284511A1 discloses a method for driving an OLED panel, which comprises a preparation, a threshold detection, a writing, and an emission period during which different transistors of the pixel unit circuits are switched on and off. An object underlying this known method is to compensate changes of luminance of a light emitting element such as an OLED, which are caused due to changes of the characteristics of the light emitting element over the time. According to the method, the transistors of a pixel unit circuit are switched during a threshold detection period such that the electric charges stored in a storage capacitor Cs and an OLED capacitor COLED are discharged by a current flowing from a driving transistor Td to a power source line, which is set to zero, until the potential difference between the gate and source of transistor Td substantially reaches the threshold voltage Vth of the driving transistor. This can make the current Ids flowing from the drain to the source of the driving transistor Td independent from the threshold voltage Vth, and, thus, can compensate changes of the characteristics of the driving transistor Td.

**[0002]** As a light emitting device of current type, an organic light emitting diode (OLED) has been increasingly used in high-performance display apparatuses. A traditional passive matrix organic light emitting display (PMOLED) requires less driving time for a single pixel as the size of the display is gradually increased, thus it is necessary to increase transient current and increase power consumption. Meanwhile, application of a large current may cause the voltage drop on the ITO (indium tin oxide) line to an extremely large level and make the operation voltage for the OLED extremely high, and thereby the efficiency thereof is reduced. By contrast, an active matrix organic light emitting display (AMOLED) can input current for each pixel in a line by line scan manner with a switching element, and can solve these problems.

**[0003]** During the operation of the AMOLED pixel circuit, due to the uniformity of the threshold voltage of the TFTs as switching elements, the uniformity of the OLED itself or resistance voltage drop (IR Drop, a phenomenon in which, in a rear board, the voltage of a region that is close to the ARVDD power supply position is higher than that of a region that is far away from the power supply position) etc, circuit instability and unevenness of the OLED luminance may be incurred, thereby the pixel circuit array as a whole is affected. Therefore, the circuit being driven by the OLED needs to be improved in related arts, so that compensation is performed on the pixels with the OLED driving circuit.

30 **[0004]** According to driving type, the AMOLED can be divided into three categories, i.e., digital type, current type and voltage type. Similar to the traditional AMOLED driving method, the driving method of the voltage type is a method in which a voltage signal representing a gray scale is provided by an integrated driving chip, and the voltage signal will be converted to a current signal inside the pixel circuit so as to drive the OLED pixel. This method is advantageous in that the driving speed is fast and the implementation is easy, is suitable to driving display panels of a large size, and has been widely employed in industries.

**[0005]** Fig. 1 shows a first kind of driving circuit of the voltage type for driving the OLED in related arts. In each pixel, a voltage signal on the data line is transmitted by the T2 to the gate of the T1, and the received data voltage signal is converted by the T1 into a corresponding data current signal and supplied to the OLED. When normally operated, the T1 is in a saturation condition, and the current thereof can be represented as:

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$$I_{OLED} = \frac{1}{2} \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{data} - ARVDD - V_{thp})^2 \quad (1)$$

45 where  $\mu_p$  represents a mobility of carries,  $C_{ox}$  represents a gate oxide capacitance, W/L represents a ratio of width to length of a TFT channel, Vdata represents a data voltage, ARVDD represents a power supply of the rear board of the AMOLED and is shared by all of the pixel unit circuits, and Vthp represents the threshold voltage of the T1. As can be known from the above expression, if the Vthp of the driving TFT (T1 in Fig. 1) in different pixel unit circuits are different, there exists a difference in the currents delivered to the respective OLEDs even if the data voltages to be delivered are of the same; meanwhile, if the ARVDD practically applied to the respective pixels are different, there also exists a difference in the currents delivered to the OLEDs.

**[0006]** Fig. 2A is a schematic diagram showing a second kind of the driving circuit of the voltage type for driving the OLED in related arts, and Fig. 2B shows a timing control diagram for the driving circuit of the voltage type. In this circuit, the voltage applied to the gate of the T2 is a voltage of  $V_{DATA} + V_{thp}$ , which is independent of the power supply voltage VDD, thus this circuit can compensate for the IR Drop, but can not compensate for the uniformity of the TFTs.

55 **[0007]** Fig. 3A is a schematic diagram showing a third kind of the driving circuit of the voltage type for driving the OLED in related arts, and Fig. 3B shows a timing control diagram for the driving circuit of the voltage type. In this circuit structure, the voltage practically applied to the gate of the transistor T1 is independent of the threshold voltage Vth of the T1 and

the power supply voltage ELVDD, and the threshold voltage uniformity of the driving transistor T1 and the IR Drop can be compensated for. However, this circuit requires four TFTs and two capacitors, and the voltage practically applied to the gate of the transistor T1 is associated with a ratio of the two capacitors; whereas the magnitudes of the two capacitors in this circuit differ not much, and a dynamic range of the inputted voltage is relatively small.

5 **[0008]** Fig. 4A is a schematic diagram showing a fourth kind of the driving circuit of the voltage type for driving the OLED in related arts, and Fig. 4B shows a timing control diagram for the driving circuit of the voltage type. In this circuit, the current inputted to the OLED remains constant, and the uniformity of the OLED can be compensated for; however, the voltage applied to the gate of the transistor T1 is associated with both of the threshold voltage  $V_{th}$  of the T1 and the power supply voltage ELVDD, and the threshold voltage uniformity of the driving transistor T1 and the IR Drop can not  
10 be compensated for.

## SUMMARY

15 **[0009]** One embodiment according to the disclosed technology provides a pixel circuit array comprising: scanning lines; data lines; and pixel unit circuits defined by the scanning lines and the data lines intersected with each other. Each of the pixel unit circuits comprise a light emitting circuit for emitting light, a driving circuit for driving the light emitting circuit, a precharge circuit for normally operating the driving circuit, a compensation circuit for compensating for the threshold voltage of the driving circuit, a holding circuit for holding voltages of a control terminal and an input terminal of the driving circuit, a first power supply terminal for supplying voltage to the precharge circuit, a second power supply  
20 terminal for supplying voltage to the driving circuit, a third power supply terminal for supplying voltage to the light emitting circuit, a scanning control terminal for controlling the precharge circuit to be operated or switched off, a first control terminal for controlling the holding circuit to be operated or switched off; and a second control terminal for controlling the compensation circuit to be operated or switched off; wherein the input terminal of the precharge circuit is connected to the first power supply terminal, a first output terminal thereof is connected to the input terminal of the holding circuit,  
25 the second output terminal thereof is connected to the input terminal of the compensation circuit and the control terminal of the driving circuit, and the control terminal thereof is connected to the scanning control terminal; the output terminal of the compensation circuit is connected to the output terminal of the driving circuit and the input terminal of the light emitting circuit, and the control terminal thereof is connected to the second control terminal; wherein the output terminal of the holding circuit is connected to the input terminal of the driving circuit and the second power supply terminal, and  
30 the control terminal thereof is connected to the first control terminal.

**[0010]** Another embodiment according to the disclosed technology provides an OLED panel comprising the pixel circuit array as described above.

35 **[0011]** A further embodiment according to the disclosed technology provides an OLED panel driving method used for the above OLED panel, wherein, of the pixel driving circuit therein, the precharge circuit includes a fourth transistor and a first capacitor; the compensation circuit includes a second transistor; the holding circuit includes a third transistor; the driving circuit includes a first transistor; and the light emitting circuit includes an organic light emitting diode (OLED), the method comprising steps of: outputting, by the scanning line, an active signal through the scanning control terminal so as to turn on the fourth transistor, and outputting an inactive signal by the first control terminal and the second control  
40 terminal so as to turn off the second transistor and the third transistor; inputting the active signal to the gate of the first transistor so as to turn on the first transistor; and transmitting a first level signal outputted from the second power supply terminal to the anode of the OLED through the first transistor.

## BRIEF DESCRIPTION OF THE DRAWINGS

45 **[0012]**

Fig. 1 shows a first kind of a driving circuit of a voltage type for driving an OLED in related arts;

Fig. 2A is a schematic diagram showing a second kind of the driving circuit of the voltage type for driving the OLED in related arts;

50 Fig. 2B shows a timing control diagram for the driving circuit of the voltage type;

Fig. 3A is a schematic diagram showing a third kind of the driving circuit of the voltage type for driving the OLED in related arts;

Fig. 3B shows a timing control diagram for the driving circuit of the voltage type;

55 Fig. 4A is a schematic diagram showing a fourth kind of the driving circuit of the voltage type for driving the OLED in related arts;

Fig. 4B shows a timing control diagram for the driving circuit of the voltage type;

Fig. 5 is a diagram showing a main structure of an OLED panel according to an embodiment of the disclosed technology;

Fig. 6A is a diagram showing a main structure of a pixel unit circuit according to an embodiment of the disclosed technology; and

Fig. 6B a diagram showing a detailed structure of the pixel unit circuit according to an embodiment of the disclosed technology.

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## DETAILED DESCRIPTION

**[0013]** An OLED panel according to an embodiment of the disclosed technology includes a first power supply terminal, a second power supply terminal, a third power supply terminal and a pixel circuit array. The pixel circuit array comprises a plurality of pixel unit circuits, and the pixel circuit array further includes scanning lines and data lines. Each of the pixel unit circuits includes a first transistor, a second transistor, a third transistor, a fourth transistor, a first capacitor and an organic light emitting diode (OLED). The gate of the first transistor is connected to one terminal of the first capacitor and the source of the second transistor. The source of the first transistor is connected to the drain of the third transistor and the second power supply terminal. The drain of the first transistor is connected to the drain of the second transistor and the anode of the OLED. The source of the third transistor is connected to another terminal of the first capacitor and the drain of the fourth transistor. The gate of the fourth transistor is connected to the scanning line. The source of the fourth transistor is connected to the first power supply terminal. The adoption of the pixel unit circuits provided by the embodiment of the disclosed technology allows a current delivered to the OLED to be independent of the threshold voltage of TFTs and the power supply voltage, thus the uniformity of the threshold voltages of TFTs, the uniformity of the OLEDs and the IR Drop can be compensated for. Furthermore, the number of devices employed by disclosed technology is relative small, thus the aperture ratio can be effectively improved.

**[0014]** With reference to Fig. 5, the display panel according to the embodiment of the disclosed technology includes a pixel circuit array 501. The OLED panel further includes a control circuit 502 for supplying a control signal to the pixel circuit array 501.

**[0015]** In addition to scanning lines, data lines and pixel unit circuits, the pixel circuit array 501 comprises pixel unit circuits defined by the scanning lines and the data lines intersected with each other.

**[0016]** With reference to Fig. 6A, the pixel unit circuit according to the embodiment of the disclosed technology comprises a light emitting circuit 605 for emitting light, a driving circuit 604 for driving the light emitting circuit 605; a precharge circuit 601 for normally operating the driving circuit 604; a compensation circuit 602 for compensating for the threshold voltage of the driving circuit 604; a holding circuit 603 for holding voltages of a control terminal and an input terminal of the driving circuit; a first power supply terminal 606 for supplying a voltage to the precharge circuit 601; a second power supply terminal 607 for supplying a voltage to the driving circuit 604; a third power supply terminal 608 for supplying a voltage to the light emitting circuit 605; a scanning control terminal 609 for controlling the precharge circuit 601 to be operated or switched off; a first control terminal 610 for controlling the holding circuit 603 to be operated or switched off; and a second control terminal 611 for controlling the compensation circuit 602 to be operated or switched off. Of the precharge circuit 601, an input terminal is connected to the first power supply terminal 606, a first output terminal is connected to the input terminal of the holding circuit 603, a second output terminal is connected to the input terminal of the compensation circuit 602 and the control terminal of the driving circuit 604, and a control terminal is connected to the scanning control terminal 609. Of the compensation circuit 602, an output terminal is connected to an output terminal of the driving circuit 604 and an input terminal of the light emitting circuit 605, and a control terminal is connected to the second control terminal 611. Of the holding circuit 603, an output terminal is connected to an input terminal of the driving circuit 604 and the second power supply terminal 607, and a control terminal is connected to the first control terminal 610. An output terminal of the light emitting circuit 605 is connected to the third power supply terminal 608. Each of the first control terminal 610 and the second control terminal 611 is connected to the control circuit 502, and different control signals are outputted by the control circuit 502 through the first control terminal 610 and the second control terminal 611. The scanning control terminal 609 is connected to the scanning lines of the pixel circuit array, and control signals are provided to the precharge circuit 601 by the scanning lines through the scanning control terminal 609. The first power supply terminal 606 is connected to the data lines of the pixel circuit array 501. The second power supply terminal 607 and the third power supply terminal 608 are connected to different power supply voltage terminals respectively.

**[0017]** The first power supply terminal 606, the second power supply terminal 607 and the third power supply terminal 608 are connected to different power supply voltage terminals respectively for supplying the power supply voltages to the pixel circuit array 501.

**[0018]** With reference to 6B, the precharge circuit 601 includes a fourth transistor (simply referred to as T4 hereinafter) and a first capacitor (simply referred to as C1 hereinafter), and the first output terminal of the precharge circuit 601 is the node N1 of Fig. 6B, and the second output terminal thereof is the node N2 of Fig. 6B. The compensation circuit 602 comprises a second transistor (simply referred to as T2 hereinafter). The holding circuit 603 comprises a third transistor (simply referred to as T3 hereinafter). The driving circuit 604 comprises a first transistor (simply referred to as T1 hereinafter). The light emitting circuit 605 comprises an OLED. The input terminal of the precharge circuit 601 refers to

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the source terminal of the T4, and the output terminal of the precharge circuit 601 refers to the drain terminal of the T4. The input terminal of the compensation circuit 602 refers to the source terminal of the T2, the output terminal of the circuit 602 refers to the drain terminal of the T2. The input terminal of the holding circuit 603 refers to the source terminal of the T3, and the output terminal of the circuit 603 refers to the drain terminal of the T3. The input terminal of the driving circuit 604 refers to the source terminal of the T1, and the output terminal of the circuit 604 refers to the drain terminal of the T1. The input terminal of the light emitting circuit 605 refers to the anode terminal of the light emitting diode T5. If the T4 is turned on, then the precharge circuit 601 is operated, while the T4 is turned off, and then the precharge circuit 601 is switched off. If the T3 is turned on, then the holding circuit 603 is operated, while the T3 is turned off, and then the holding circuit 603 is switched off. If the T2 is turned on, then the compensation circuit 602 is operated, while the T2 is turned off, and then the compensation circuit 602 is switched off.

**[0019]** The gate of the T1 is connected to one terminal of the C1 and the source of the T2; the source of the T1 is connected to the drain of the T3 and the second power supply terminal 607, and the output terminal of the second power supply terminal 607 is the VP terminal of Fig. 6B. The drain of the T1 is connected to the drain of the T2 and the anode of the OLED. The source of the T3 is connected to another terminal of the C1 and the drain of the T4, and the gate of the T3 is connected to the first control terminal 610. The gate of the T4 is connected to the scanning control terminal 609, the source of the T4 is connected to the first power supply terminal 606, and the output terminal of the first power supply terminal 606 is the VD terminal of Fig. 6B. The gate of the T2 is connected to the second control terminal 611 which is the VC terminal of Fig. 6B; the second control terminal 611 provides a second control signal for the T2. The gate of the T3 is connected to the first control terminal 610 which is the EM terminal of Fig. 6B; the first control terminal 610 provides a first control signal for the T3. In the circuit, the OLED can be equivalent to a light emitting diode T5 and a capacitor  $C_{OLED}$  connected in parallel; the anode of the OLED is the anode of the light emitting diode T5, which is the node N3 of Fig. 6B, i.e., the input terminal of the light emitting circuit 608; the output terminal of the light emitting circuit 608 is the cathode terminal of the light emitting diode T5. The cathode terminal of the light emitting diode T5 is connected to the third power supply terminal 608. The first control signal and the second control signal are both provided by the control circuit 502 on the OLED panel; the control circuit 502 is used to control the first control signal and the second control signal, that is, the control circuit 502 controls the gate voltages of the T2 and the T3 through the second control terminal 611 and the first control terminal 610 respectively.

**[0020]** Each of the first transistor, the second transistor, the third transistor and the fourth transistor in the embodiment of the disclosed technology can be a TFT; in an example, all of the TFTs in the embodiment of the disclosed technology are P-type TFTs. Those skilled in the art can also make modifications or alternation to the embodiment of the disclosed technology. For example, the TFTs of the embodiments of the disclosed technology can be replaced with N-type TFTs, in which case the circuit structure and the control signal timings will be altered correspondingly; and since the operation principle thereof is similar to that of the pixel circuit constituted by the P-type TFTs, those skilled in the art will know how to realize the another embodiment of the disclosed technology with the N-type TFTs under the teachings of the embodiment of the disclosed technology.

**[0021]** In the embodiment of the disclosed technology, the driving of the OLED can be divided into three periods of an initialization period, a compensation period and a holding period.

#### Initialization Period

**[0022]** The first power supply terminal 606 (VD) and the second power supply terminal 607 (VP) output a low power supply level (ARVSS), while the third power supply terminal 608 outputs a high power supply level (ARVDD). The OLED can be equivalent to a light emitting diode T5 and a second capacitor (simply referred to as  $C_{OLED}$  hereinafter) that are connected in parallel in terms of electrics performance, thus the OLED is reversely turned off. The voltage stored in the node N1 of Fig. 6 at the previous one period is ARVDD, and the voltage stored in the node N2 at the previous one period is  $ARVDD - V_{DATA}(n-1) + V_{REF} + V_{thp}$ , and then it can be learned that the voltage drop on the C1 is  $-V_{DATA}(n-1) + V_{REF} + V_{thp}$ , where  $V_{DATA}(n-1)$  is the data voltage inputted in the previous one frame,  $V_{REF}$  is a direct-current reference voltage, and  $V_{thp}$  is the threshold voltage of the T1 ( $V_{thp} < 0$ ). At this moment, the scanning line outputs the low power supply level (VGL), and controls the EM and the VC to be the high power supply level (VGH). The T1 and the T4 are turned on, and the T2 and the T3 are turned off, thus the low power supply level ARVSS are transferred to the node N1 via the T4; due to bootstrap effect by the C1, the voltage of the node N2 is changed to  $ARVSS - V_{DATA}(n-1) + V_{REF} + V_{thp}$ , i.e., a voltage obtained by subtracting the voltage drop on the C1 from the voltage of the node N1. In the embodiment of the disclosed technology, with the  $V_{REF}$  being suitably selected so that  $-V_{DATA}(n-1) + V_{REF} < 0$ , i.e., the voltage at node N2 is a low level, the T1 is turned on, and the voltage of the node N3 is also equal to ARVSS.

**[0023]** Thereafter, the output voltage of the VD terminal is changed from the ARVSS to the data voltages  $V_{DATA}(n)$  of the current frame, the VP remains at the low power supply level (ARVSS), and the VN remains at the high power supply level (ARVDD). At this moment, the voltage of the node N2 is changed to  $V_{DATA}(n) - V_{DATA}(n-1) + V_{REF} + V_{thp}$ , i.e., a voltage obtained by subtracting the voltage drop on the C1 from the voltage of the node N1. The voltage of the node N3

remains at the ARVSS. The VC is controlled to be the low power supply level (VGL), and the T2 is turned on; the C1 is serially connected to the capacitor  $C_{OLED}$  of the equivalent circuit of the OLED. From the principle of charge conservation, the final voltages of the N2 (which is also referred to as node  $V_{INIT}$  after the T2 is turned on) and the N3 can be obtained as:

$$[-V_{DATA}(n-1)+VREF+Vthp] \cdot C_6 + (ARVSS-ARVDD) \cdot C_{OLED} = V_{INIT} \cdot (C_6 + C_{OLED}) \quad (1).$$

Thus,

$$V_{INIT} = \frac{[-V_{DATA}(n-1)+VREF+Vthp] \cdot C_6 + (ARVSS-ARVDD) \cdot C_{OLED}}{C_6 + C_{OLED}} \quad (2).$$

Since  $ARVSS-ARVDD < 0$  and  $C_{OLED} \gg C_6$  generally,

$$V_{INIT} \approx ARVSS-ARVDD \quad (3),$$

and the nodes of N2 and N3 are identical in voltage, which is  $V_{INIT}$ . That is, at this period, a precharge to the voltages of the nodes N2 and N3 are completed.

Compensation Period

**[0024]** Where the data voltage  $V_{DATA}(n)$  of the current frame is outputted at the VD terminal, the direct-current reference voltage (VREF) is outputted at the VP terminal, and the high power supply level signal (ARVDD) is outputted at the VN terminal, the OLED remains reversely turned off. The scanning line (SCAN terminal) and the VC are controlled to be the low power supply level (VGL), and the EM is controlled to be the high power supply level (VGH); at this period, since VREF is higher than zero, and the initialization voltage  $V_{INIT}$  of the nodes N2 and N3 is lower than zero, the T1 which is turned on now is equivalent to a diode at this moment, and the current is flowed from the VREF to the node N3 to charge the node N3; after the voltage of node N3 is increased to a voltage of  $VREF+Vthp$  (which is a voltage obtained by adding the VREF to the threshold voltage of the T1), the T1 is turned off. When the compensation period comes to an end, the charge stored on both terminals of the C1 is  $(VREF+Vthp-V_{DATA}(n)) \cdot C_6$ ; since the T4 is operated in the linear region, the threshold voltage is not consumed.

Holding Period

**[0025]** Where the high power supply level (ARVDD) is outputted at the VD terminal and the low power supply level (ARVSS) is outputted at the VN terminal, the OLED is forwardly turned on. The SCAN and the VC is controlled to be the high power supply level (VGH) and the EM is controlled to be the low power supply level (VGL), then the T1 and the T3 are turned on, and the T2 and the T4 are turned off; C1 is connected between the gate and the source of the T1 for holding the  $V_{GS}$  (that is, gate-source voltage) of the T1, and the charge stored therein remains unchanged. The node N1 is connected to the ARVDD through the T3, and due to bootstrap effect of the C1, the voltage of the node N2 is changed to  $ARVDD-V_{DATA}(n)+VREF+Vthp$ , i.e., a voltage obtained by subtracting the voltage drop on the C1 from the voltage of the node N1. The  $V_{GS}$  of the T1 remains  $VREF+Vthp-V_{DATA}(n)$  (that is, subtracting the voltage of the node N2 from the ARVDD). At this moment, the current flowed through the T1 is represented as:

$$I_{OLED} = \frac{1}{2} \cdot \mu_p \cdot C_{OX} \cdot \frac{W}{L} \cdot [VREF+Vthp-V_{DATA}(n)-Vthp]^2 \quad (4);$$

thus

$$I_{OLED} = \frac{1}{2} \cdot \mu_p \cdot C_{OX} \cdot \frac{W}{L} \cdot [VREF-V_{DATA}(n)]^2 \quad (5).$$

As can be learned from the equation (5), the current flowed to the T1 is independent of the threshold voltage of the T1

and the power supply voltage ARVDD; thus with the above three periods, the compensation for the uniformity of the threshold voltage of the T1 and the IR Drop is substantially realized. As long as the inputted direct-current reference voltage VREF and the data voltage  $V_{DATA}(n)$  are constant, the current flowed through the T1 is constant, and the uniformity of the OLED can be effectively compensated for.

5 [0026] Hereinafter, an OLED panel driving method according to an embodiment of the disclosed technology will be explained in details in the following. The method comprises steps as follows.

[0027] At step 701, an active signal is outputted from the scanning control terminal 609 so as to turn on the fourth transistor, and inactive signals are outputted from the first control terminal 610 and the second control terminal 611 so as to turn off the second transistor and the third transistor. The embodiment of the disclosed technology will be illustrated in connection with Fig. 6B.

10 [0028] At step 702, the active signal is outputted to the gate of the first transistor so that the first transistor is turned on.

[0029] At step 703, the first level signal outputted from the second power supply terminal 607 is transmitted to the anode of the OLED through the first transistor.

15 [0030] Both the first power supply terminal 606 and the second power supply terminal 607 output the first level signal, the scanning line outputs the active signal by the scanning control terminal 609, and the third power supply terminal 608 outputs the second level signal. In the embodiment of the disclosed technology, the first level signal may be the low power supply level signal (ARVSS), the second level signal may be the high power supply level signal (ARVDD), and the active signal may be the low level signal. The first control signal and the second control signal are made to be the inactive signal at the same time. The anode of the OLED in the pixel unit circuit is the node N3 of Fig. 6B.

20 [0031] Thereafter, the output voltage of the first power supply terminal 606 is changed to the data voltage of the current frame, and the active signal is outputted from the control circuit 502 through the second control terminal 611, so that the second transistor is turned on, and the voltages of the drain and the gate of the first transistor are of the same and equal to the output voltage of the second power supply terminal 607. In the embodiment of the disclosed technology, the active signal can be the low level signal. The second control terminal 611 is connected to the gate of the second transistor, and the control circuit 502 outputs the active signal to the gate of the second transistor through the second control terminal 611, thus the second transistor is turned on. The second power supply terminal 607 outputs the direct-current reference voltage.

25 [0032] The second power supply terminal 607 outputs the second level signal, and the third power supply terminal 608 outputs the first level signal. The active signal is outputted to the gate of the first transistor so that the first transistor is turned on, and the active signal is outputted from the first control terminal 610 so that the third transistor is turned on. The inactive signal is outputted from the second control terminal 611 and the scanning control terminal 609, so that the second transistor and the fourth transistor are turned off and the data current is delivered to the OLED through the drain of the first transistor.

30 [0033] An OLED panel according to an embodiment of the disclosed technology includes the first power supply terminal 606, the second power supply terminal 607, the third power supply terminal 608 and the pixel circuit array 501. The pixel circuit array 501 comprises the pixel unit circuits and further scanning lines. The pixel unit circuit each includes the first transistor, the second transistor, the third transistor, the fourth transistor, the first capacitor and the OLED. The gate of the first transistor is connected to one terminal of the first capacitor and the source of the second transistor. The source of the first transistor is connected to the drain of the third transistor and the second power supply terminal. The drain of the first transistor is connected to the drain of the second transistor and the anode of the OLED. The source of the third transistor is connected to another terminal of the first capacitor and the drain of the fourth transistor. The gate of the fourth transistor is connected to the scanning control terminal, and the source thereof is connected to the first power supply terminal 606.

35 [0034] With the pixel unit circuit provided by the embodiment of the disclosed technology, as long as the inputted direct-current reference voltage and the data voltage signal are not varied, the current delivered to the OLED remains constant, thus the uniformity of the OLED can be compensated for. Furthermore, the current delivered to the OLED is independent of the threshold voltage of the TFTs and the power supply voltage of the OLED panel, thus the uniformity of the threshold voltage of TFTs and the IR Drop can be compensated for. The control method is simple and easy to realize. The structure of the pixel unit circuit according to the embodiment of the disclosed technology is simple, and the required devices are of a small number, thus the aperture ratio can be effectively improved.

40 [0035] Apparently, those skilled in the art can make various alternations and modifications to the embodiments of the disclosed technology without departing from the spirit and scope of the disclosed technology. Thus, provided that the alternations and modifications to the disclosed technology are within the scope of the claims of the disclosed technology and the equivalents thereof, the disclosed technology is also intended to be inclusive of such alternations and modifications.

## Claims

1. An organic light-emitting diode (OLED) panel driving method adapted for an OLED panel including a pixel circuit array (501), the pixel circuit array comprising: scanning lines; data lines; and pixel unit circuits defined by the scanning lines and the data lines intersected with each other, each of the pixel unit circuits comprising: an OLED, a first transistor (T1), a second transistor (T2), a third transistor (T3), a fourth transistor (T4) and a first capacitor (C1), wherein

the gate of the first transistor (T1) is connected to one terminal of the first capacitor (C1) and the source of the second transistor (T2); the source of the first transistor (T1) is connected to the drain of the third transistor (T3) and a second power supply terminal (VP); the drain of the first transistor (T1) is connected to the drain of the second transistor (T2) and the anode of the OLED; the gate of the second transistor (T2) is connected to a second control terminal (VC); the source of the third transistor (T3) is connected to the other terminal of the first capacitor (C1) and the drain of the fourth transistor (T4), and the gate thereof is connected to a first control terminal (EM); and the gate of the fourth transistor (T4) is connected to a scanning control terminal (SCAN), and the source thereof is connected to the first power supply terminal (VD); and the cathode of the OLED is connected to a third power supply terminal (VN), wherein the scanning control terminal is connected to one of the scanning lines, and the first power supply terminal is connected to one of the data lines;

**characterized by** the method comprising steps of:

a first step: outputting a low level by the first power supply terminal (VD) and the second power supply terminal (VP), outputting a high level by the third power supply terminal (VN), outputting a low level by the scanning control terminal (SCAN), outputting a high level by the first control terminal (EM) and the second control terminal (VC), so as to turn on the first transistor (T1) and the fourth transistor (T4) and turn off the second transistor (T2) and the third transistor (T3);

a second step: outputting a data voltage by the first power supply terminal (VD) and outputting a low level by the second control terminal (VC) while maintaining the low level at the second power supply terminal (VP), maintaining the high level at the third power supply terminal (VN), maintaining the low level at the scanning control terminal (SCAN) and maintaining the high level at the first control terminal (EM), so as to maintain the first transistor (T1) and the fourth transistor (T4) ON, maintain the third transistor (T3) OFF, and turn on the second transistor (T2);

a third step: keeping outputting the data voltage by the first power supply terminal (VD) and outputting a direct-current reference voltage (VREF) by the second power supply terminal (VP) while maintaining the high level at the third power supply terminal (VN), maintaining the low level at the scanning control terminal (SCAN), maintaining the high level at the first control terminal (EM), and maintaining the low level at the second control terminal (VC), so as to maintain the first transistor (T1), the second transistor (T2) and the fourth transistor (T4) ON and maintain the third transistor (T3) OFF, and meanwhile to cause a current flowing from the second power supply terminal (VP) through the first transistor (T1) to charge the drain of the first transistor (T1) until the first transistor (T1) is turned off, wherein the direct-current reference voltage (VREF) is higher than 0; and

a fourth step: outputting a high level by the second power supply terminal (VP), outputting a low level by the third power supply terminal (VN), outputting a high level by the scanning control terminal (SCAN), outputting a low level by the first control terminal (EM) and outputting a high level by the second control terminal (VC), so as to maintain the first transistor (T1) ON, turn on the third transistor (T3) and turn off the second transistor (T2) and the fourth transistor (T4), wherein the high level outputted by the second power supply terminal is higher than the direct-current reference voltage (VREF) outputted by the second power supply terminal.

2. The method according to claim 1, wherein, the first transistor (T1), the second transistor (T2), the third transistor (T3) and the fourth transistor (T4) are P-type transistors.

3. The method according to claim 1, wherein, in the second step, after the second transistor (T2) is turned on, the voltage at the drain of the first transistor (T1) is equal to the voltage at the gate of the first transistor (T1).

4. The method according to claim 1, wherein, in the fourth step, the first capacitor (C1) is connected between the gate and source of the first transistor (T1) and is used for maintaining the gate-source voltage of the first transistor (T1), so that the current flowing through the first transistor (T1) and the OLED is independent of the threshold voltage of the first transistor (T1).

## Patentansprüche

1. Organische-Licht-emittierende-Diode (OLED)-Tafel-Ansteuerungs-verfahren, geeignet für eine OLED-Tafel, die ein Pixelschaltungs-Array (501) enthält, wobei das Pixelschaltungs-Array umfasst:

5 Scan-Leitungen; Datenleitungen; und Pixeleinheitschaltungen, definiert mittels der sich gegenseitig kreuzenden Scan-Leitungen und Datenleitungen, wobei jede der Pixeleinheitschaltungen umfasst: eine OLED, einen ersten Transistor (T1), einen zweiten Transistor (T2), einen dritten Transistor (T3), einen vierten Transistor (T4) und einen ersten Kondensator (C1), wobei

10 das Gate des ersten Transistors (T1) angeschlossen ist an einen Anschluss des ersten Kondensators (C1) und die Source des zweiten Transistors (T2); wobei die Source des ersten Transistors (T1) angeschlossen ist an den Drain des dritten Transistors (T3) und einen Energiezufuhranschluss (VP); wobei der Drain des ersten Transistors (T1) angeschlossen ist an den Drain des zweiten Transistors (T2) und die Anode der OLED; wobei das Gate des zweiten Transistors (T2) angeschlossen ist an ein zweites Steuerterminal (VC); wobei die Source des dritten Transistors (T3) angeschlossen ist an den anderen Anschluss des ersten Kondensators (C1) und den Drain des vierten Transistors (T4), und wobei das Gate davon angeschlossen ist an einen ersten Steueranschluss (EM);

15 und wobei das Gate des vierten Transistors (T4) angeschlossen ist an einen Scan-Steueranschluss (SCAN), und wobei die Source davon angeschlossen ist an den ersten Energiezufuhranschluss (VD); und wobei die Kathode des OLEDs angeschlossen ist an einen dritten Energiezufuhranschluss (VN), wobei der Scan-Steueranschluss angeschlossen ist an eine der Scan-Leitungen, und wobei der erste Energiezufuhranschluss angeschlossen ist an eine der Datenleitungen;

20 **gekennzeichnet dadurch, dass** das Verfahren die Schritte aufweist:

25 einen ersten Schritt: Ausgabe eines niedrigen Levels mittels des ersten Energiezufuhranschlusses (VD) und des zweiten Energiezufuhranschlusses (VP), Ausgabe eines hohen Levels mittels des dritten Energiezufuhranschlusses (VN), Ausgabe eines niedrigen Levels mittels des Scan-Steueranschlusses (SCAN), Ausgabe eines hohen Levels mittels des ersten Steueranschlusses (EM) und des zweiten Steueranschlusses (VC), um den ersten Transistor (T1) und den vierten Transistor (T4) einzuschalten und um den zweiten Transistor (T2) und den dritten Transistor (T3) auszuschalten;

30 einen zweiten Schritt: Ausgabe einer Datenspannung mittels des ersten Energiezufuhranschlusses (VD) und Ausgabe eines niedrigen Levels mittels des zweiten Steueranschlusses (VC), während Aufrechterhaltung des niedrigen Levels an dem zweiten Energiezufuhranschluss (VP), Aufrechterhaltung des hohen Levels an dem dritten Energiezufuhranschluss (VN), Aufrechterhaltung des niedrigen Levels an dem Scan-Steueranschluss (SCAN) und Aufrechterhaltung des hohen Levels an dem ersten Steueranschluss (EM), um den ersten Transistor (T1) und den vierten Transistor (T4) eingeschaltet zu halten, den dritten Transistor (T3) ausgeschaltet zu halten und den zweiten Transistor (T2) einzuschalten;

35 einen dritten Schritt: Beibehaltung der Ausgabe der Datenspannung mittels des ersten Energiezufuhranschlusses (VD) und Ausgabe einer Gleichspannungs-Referenzspannung (VERF) mittels des zweiten Energiezufuhranschlusses (VP) während der Aufrechterhaltung des hohen Levels an dem dritten Energiezufuhranschluss (VN), der Aufrechterhaltung des niedrigen Levels an dem Scan-Steueranschluss (SCAN), der Aufrechterhaltung des hohen Levels an dem ersten Steueranschluss (EM), und der Aufrechterhaltung des niedrigen Levels an dem zweiten Steueranschluss (VC), um den ersten Transistor (T1), den zweiten Transistor (T2) und den vierten Transistor (T4) eingeschaltet zu halten und um den dritten Transistor (T3) ausgeschaltet zu halten, und um währenddessen einen Stromfluss von dem zweiten Energiezufuhranschluss (VP) durch den ersten Transistor (T1) zu veranlassen, um den Drain des ersten Transistors (T1) zu laden, bis der erste Transistor (T1) ausgeschaltet wird, wobei die Gleichspannungs-Referenzspannung (VERF) höher ist als 0; und

40 einen vierten Schritt: Ausgabe eines hohen Levels mittels des zweiten Energiezufuhranschlusses (VP), Ausgabe eines hohen Levels mittels des dritten Energiezufuhranschlusses (VN), Ausgabe eines hohen Levels mittels des Scan-Steueranschlusses (SCAN), Ausgabe eines hohen Levels mittels des ersten Steueranschlusses (EM) und Ausgabe eines hohen Levels mittels des zweiten Steueranschlusses (VC), um den ersten Transistor (T1) eingeschaltet zu halten, den dritten Transistor (T3) einzuschalten und den zweiten Transistor (T2) und den vierten Transistor (T4) auszuschalten, wobei der hohe Level, der mittels des zweiten Energiezufuhranschlusses ausgegeben wird, höher ist als die Gleichspannungs-Referenzspannung (VERF), die mittels des zweiten Energiezufuhranschlusses .

2. Verfahren gemäß Anspruch 1, wobei der erste Transistor (T1), der zweite Transistor (T2), der dritte Transistor (T3)

und der vierte Transistor (T4) P-Typ-Transistoren sind.

3. Verfahren gemäß Anspruch 1, wobei in dem zweiten Schritt, nachdem der zweite Transistor (T2) eingeschaltet ist, die Spannung an dem Drain des ersten Transistors (T1) gleich der Spannung an dem Gate des ersten Transistors (T1) ist.
4. Verfahren gemäß Anspruch 1, wobei in dem vierten Schritt der erste Kondensator (C1) zwischen das Gate und die Source des ersten Transistors (T1) geschaltet wird und verwendet wird zur Aufrechterhaltung der Gate-Source-Spannung des ersten Transistors (T1), so dass der Stromfluss durch den ersten Transistor (T1) und die OLED unabhängig von der Schwellenspannung des ersten Transistors (T1) ist.

## Revendications

1. Un procédé de commande de panneau à diode électroluminescente organique (DELO) adapté pour un panneau à DELO comportant un réseau de circuits de pixels (501), le réseau de circuits de pixels comprenant : des lignes de balayage ; des lignes de données ; et des circuits d'unité de pixel définis par les lignes de balayage et les lignes de données qui se croisent les unes avec les autres, chacun des circuits d'unité de pixel comprenant : une DELO, un premier transistor (T1), un deuxième transistor (T2), un troisième transistor (T3), un quatrième transistor (T4) et un premier condensateur (C1), dans lequel
- la grille du premier transistor (T1) est connectée à une borne du premier condensateur (C1) et à la source du deuxième transistor (T2) ; la source du premier transistor (T1) est connectée au drain du troisième transistor (T3) et à une deuxième borne d'alimentation (VP) ; le drain du premier transistor (T1) est connecté au drain du deuxième transistor (T2) et à l'anode de la DELO ; la grille du deuxième transistor (T2) est connectée à une deuxième borne de commande (VC) ; la source du troisième transistor (T3) est connectée à l'autre borne du premier condensateur (C1) et au drain du quatrième transistor (T4), et sa grille est connectée à une première borne de commande (EM) ; et la grille du quatrième transistor (T4) est connectée à une borne de commande de balayage (SCAN), et sa source est connectée à la première borne d'alimentation (VD) ; et la cathode de la DELO est connectée à une troisième borne d'alimentation (VN), dans lequel la borne de commande de balayage est connectée à l'une des lignes de balayage, et la première borne d'alimentation est connectée à l'une des lignes de données ;
- caractérisé en ce que** le procédé comprend les étapes de :

une première étape : délivrer un niveau bas par la première borne d'alimentation (VD) et par la deuxième borne d'alimentation (VP), délivrer un niveau haut par la troisième borne d'alimentation (VN), délivrer un niveau bas par la borne de commande de balayage (SCAN), délivrer un niveau haut par la première borne de commande (EM) et par la deuxième borne de commande (VC), de manière à activer le premier transistor (T1) et le quatrième transistor (T4) et inactiver le deuxième transistor (T2) et le troisième transistor (T3) ;

une deuxième étape : délivrer une tension de données par la première borne d'alimentation (VD) et délivrer un niveau bas par la deuxième borne de commande (VC) tout en maintenant le niveau bas à la deuxième borne d'alimentation (VP), maintenir le niveau haut à la troisième borne d'alimentation (VN), maintenir le niveau bas à la borne de commande de balayage (SCAN) et maintenir le niveau haut à la première borne de commande (EM), de manière à maintenir actifs le premier transistor (T1) et le quatrième transistor (T4), à maintenir inactif le troisième transistor (T3) et à activer le deuxième transistor (T2) ;

une troisième étape: continuer à délivrer la tension de données par la première borne d'alimentation (VD) et délivrer une tension continue de référence (VREF) par la deuxième borne d'alimentation (VP) tout en maintenant le niveau haut à la troisième borne d'alimentation (VN), en maintenant le niveau bas à la borne de commande de balayage (SCAN), en maintenant le niveau haut à la première borne de commande (EM), et en maintenant le niveau bas à la deuxième borne de commande (VC), de manière à maintenir actifs le premier transistor (T1), le deuxième transistor (T2) et le quatrième transistor (T4) et maintenir inactif le troisième transistor (T3), et à provoquer pendant ce temps la circulation d'un courant depuis la deuxième borne d'alimentation (VP) à travers le premier transistor (T1) pour charger le drain du premier transistor (T1) jusqu'à ce que le premier Transistor (T1) soit rendu inactif, dans lequel la tension continue de référence est supérieure à 0 ; et

une quatrième étape: délivrer un niveau haut par la deuxième borne d'alimentation (VP), délivrer un niveau bas par la troisième borne d'alimentation (VN), délivrer un niveau haut par la borne de commande de balayage (SCAN), délivrer un niveau bas par la première borne de commande (EM) et délivrer un niveau haut par la deuxième borne de commande (VC), de manière à maintenir actif le premier transistor (T1), à activer le troisième transistor (T3) et à rendre inactifs le deuxième transistor (T2) et le quatrième transistor (T4), dans lequel le niveau haut délivré par la deuxième borne d'alimentation est supérieur à la tension continue de référence

délivrée par la deuxième borne d'alimentation.

2. Le procédé selon la revendication 1, dans lequel le premier transistor (T1), le deuxième transistor (T2), le troisième transistor (T3) et le quatrième transistor (T4) sont des transistors de type P.

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3. Le procédé selon la revendication 1, dans lequel, dans la deuxième étape, après que le deuxième transistor (T2) ait été activé, la tension au drain du premier transistor (T1) est égale à la tension à la grille du premier transistor (T1).

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4. Le procédé selon la revendication 1, dans lequel, dans la quatrième étape, le premier condensateur (C1) est connecté entre la grille et la source du premier transistor (T1) et est utilisé pour maintenir la tension grille-source du premier transistor (T1), de manière que le courant circulant à travers le premier transistor (T1) et la DELO soit indépendant de la tension de seuil du premier transistor (T1).

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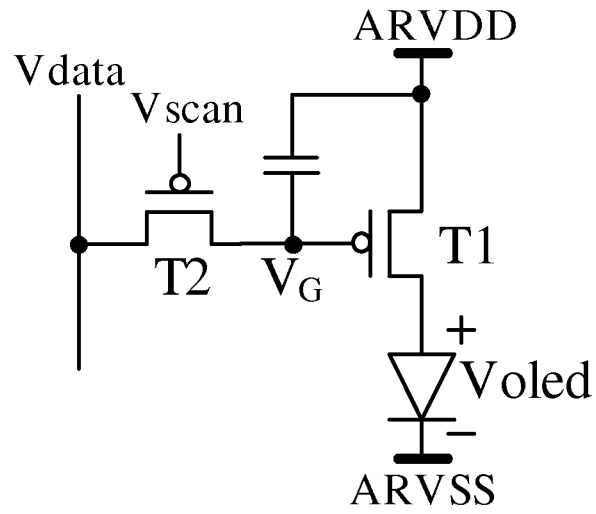


FIG.1 (PRIOR ART)

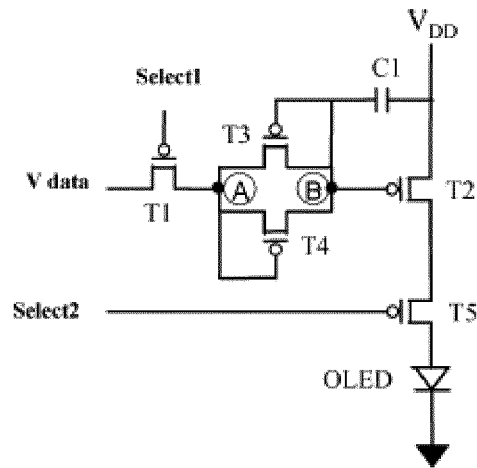


FIG.2A (PRIOR ART)

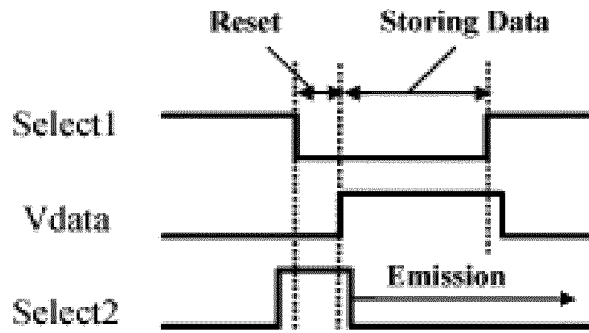


FIG.2B (PRIOR ART)

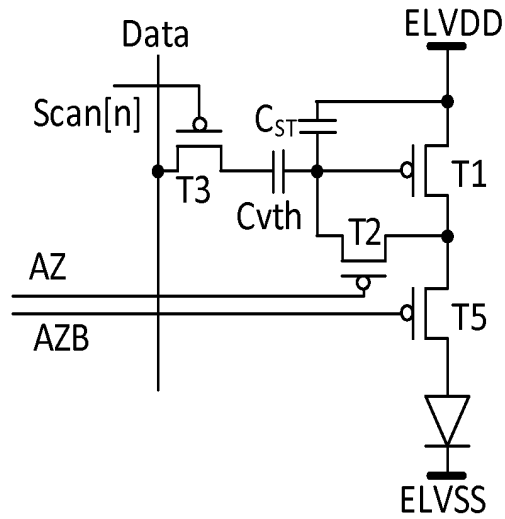


FIG.3A (PRIOR ART)

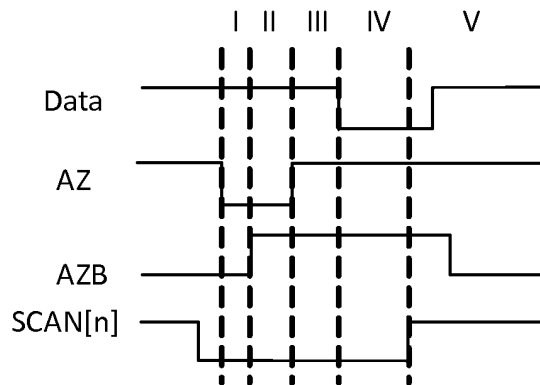


FIG.3B (PRIOR ART)

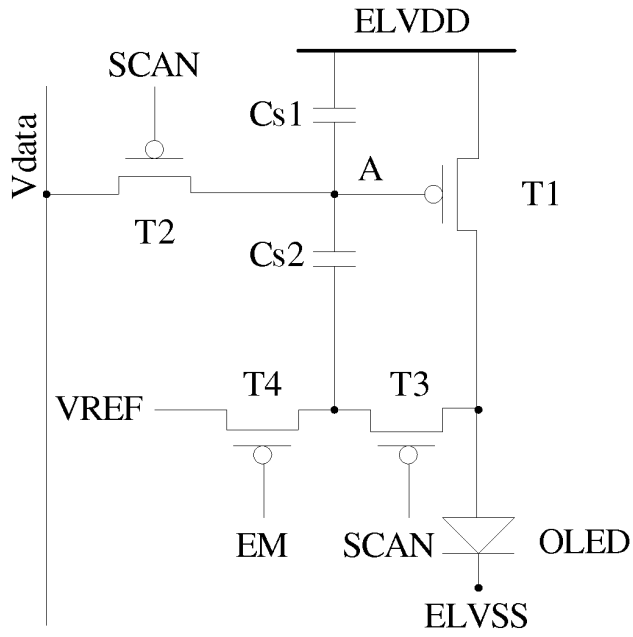


FIG.4A (PRIOR ART)

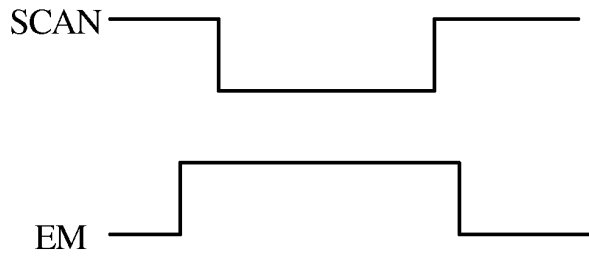


FIG.4B (PRIOR ART)

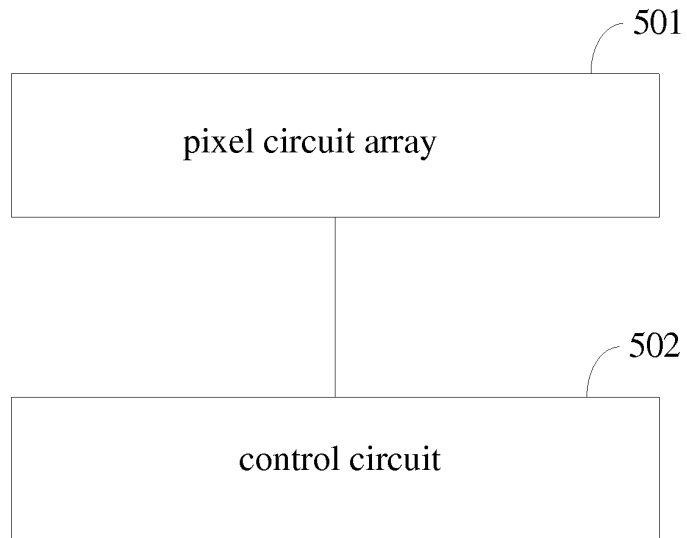


FIG.5

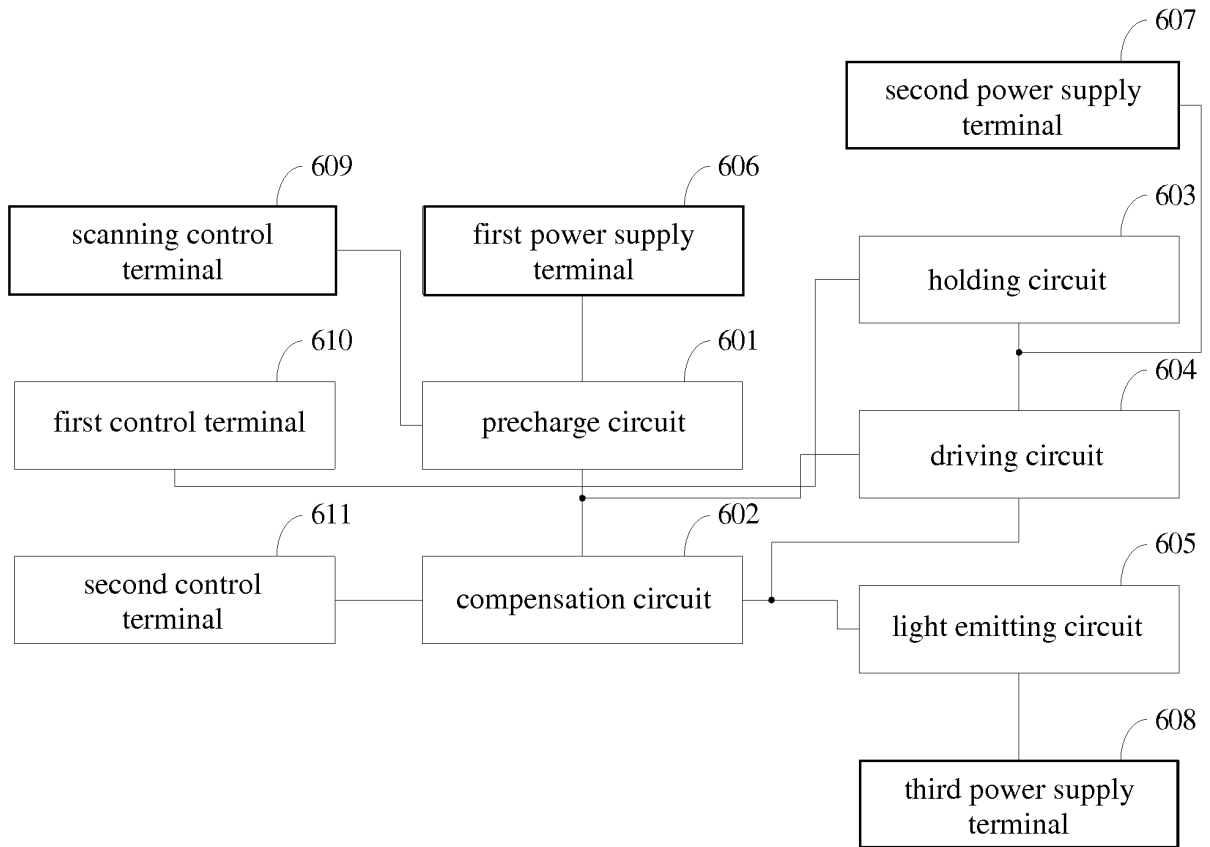


FIG.6A

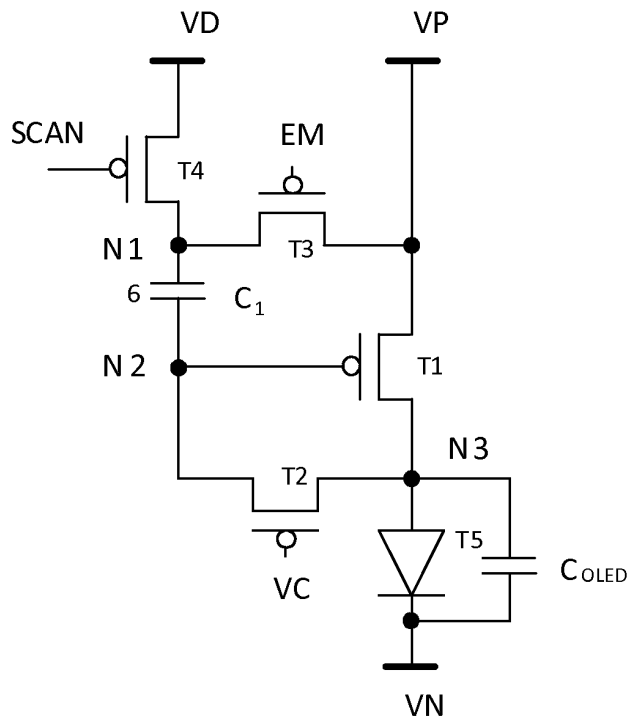


FIG.6B

**REFERENCES CITED IN THE DESCRIPTION**

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**Patent documents cited in the description**

- US 2009284511 A1 [0001]

专利名称(译)	像素单元电路，像素阵列，显示面板和显示面板的驱动方法		
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优先权	201110124714.X 2011-05-13 CN		
其他公开文献	EP2523182A1		
外部链接	<a href="#">Espacenet</a>		

摘要(译)

所公开的技术涉及像素单元电路，像素阵列，显示面板和显示面板驱动方法。像素电路阵列包括像素单元电路，每个像素单元电路包括预充电电路，补偿电路，保持电路，驱动电路，发光电路，第一电源端子，第二电源端子，第三电源端子，扫描控制端子，第一控制端子和第二控制端子。利用像素单元电路，只要输入的直流参考电压和数据电压信号不变，输送到OLED的电流保持恒定，因此可以补偿OLED的均匀性。

$$I_{OLED} = \frac{1}{2} \cdot \mu_p \cdot C_{ox} \cdot \frac{W}{L} \cdot (V_{data} - V_{TDD} - V_{thp})^2 \quad (1)$$