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(54) **OLED DISPLAY PANEL WITH PWM CONTROL**

OLED-ANZEIGETAFEL MIT PWM-STEUERUNG

ÉCRAN D'AFFICHAGE OLED À COMMANDE EN PWM

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## Description

### FIELD OF THE INVENTION

**[0001]** The present invention relates to a display panel having pixels arranged in a matrix.

### BACKGROUND OF THE INVENTION

**[0002]** As organic EL displays are self-emissive, they exhibit high contrast and quick response, making them suitable for video applications such as televisions which display natural images and the like. In general, an organic EL element is driven by way of control elements such as transistors, in which multiple tones are realized by driving transistors with a constant current according to data, or by driving transistors with a constant voltage so as to change the emission period.

**[0003]** In the case of driving transistors with a constant current, as they are used in a saturated region, variation in the characteristics of the transistors such as thresholds and mobility causes variation in the current flowing through an organic EL element, which results in non-uniformity in display. As such, JP 2007-79599A discloses a method of reducing non-uniformity in display by digitally driving transistors in a linear region with a constant voltage.

**[0004]** However, according to the example disclosed in JP 2007-79599 A, in the drive transistor connected in series to the organic EL element, the gate terminal and the drain terminal thereof are diode-connected by a reset transistor, and even when the reset transistor is turned off, the gate potential of the drive transistor varies due to leakage current from the reset transistor. JP 2007-79599A discloses examples for addressing the problem of leakage current, including use of an n-channel transistor as the reset transistor and introduction of LLD (Lightly Doped Drain) structure only to the reset transistor. However, these measures make the manufacturing process of transistors complicated, which makes cost reduction difficult.

**[0005]** Document WO 01/54107 A1 concerns a circuit for driving an OLED in a graphic display. The circuit employs a current source operating in a switched mode. The output of the current source is connected to a terminal of the OLED. The current source is responsive to a combination of a selectively set cyclical voltage signal and a cyclical variable amplitude voltage signal. The current source when switched on is designed and optimized to supply the OLED with the amount of current necessary for the OLED to achieve maximum luminance.

**[0006]** Document US 2006/0022305 A1 concerns an active matrix-driven display device that operates with reduced variation of brightness attributable to time-related or temperature-related variation with no increase in power consumption. The device has pixels arranged in a matrix, each pixel comprising: an EL element; a coupling capacitor; a writing transistor having a gate connected to a scan voltage line; a driving transistor which drives the EL element in accordance with a gate voltage; a threshold value compensation transistor having one end connected to a connecting point of the driving transistor and EL element, another end connected to a connection point of the coupling capacitor and the writing transistor, and a gate connected to a control signal line; and a storage capacitor having one end connected to a gate of the driving transistor and another end connected to a ramp voltage line. In operation, the threshold value compensation transistor and writing transistor are turned on so that current flows through the driving transistor and a corresponding voltage is written into the coupling capacitor. Then, the threshold value compensation transistor is turned off while the writing transistor is kept on, and a data voltage is written into the storage capacitor. A triangular wave is applied to the ramp voltage line to control an on period of the driving transistor to thereby control light emission.

### SUMMARY OF THE INVENTION

**[0007]** A display panel according to an aspect of the present invention comprises the features of claim 1.

**[0008]** Further, preferably a light-emission control transistor is arranged between the connecting point of the drain of the drive transistor and the reset transistor, and the light-emitting element, and when the reset transistor is turned on, the light-emission control transistor is turned off. According to the present invention, an emission period can be controlled, and also current can be controlled effectively according to image data. Further, as the drain of the reset transistor is connected to the gate of the drive transistor via the selection transistor, effects of leakage current from the reset transistor on the gate voltage of the drive transistor can be controlled.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0009]**

FIG 1 is a diagram showing the configuration of a pixel circuit;
FIG 2 is a diagram showing states of respective lines when data are written;
FIG 3 is a diagram illustrating sweeping;
FIG 4 is a diagram showing circuits for applying a sweep pulse;
FIG 5A is a diagram showing an example of timing to apply a sweep pulse;
FIG 5B is a diagram showing another example of timing to apply a sweep pulse;
FIG 6 is a diagram showing another example of circuits for applying a sweep pulse; and
FIG 7 is a diagram showing the configuration of a display panel.

## DETAILED DESCRIPTION OF THE INVENTION

**[0010]** Hereinafter, an embodiment of the present invention will be described with reference to the drawings.

**[0011]** FIG 1 shows an exemplary configuration of a pixel 15 in a display according to an embodiment. The pixel 15 includes an organic EL element 1, a drive transistor 2, a selection transistor 3, a reset transistor 4, a light-emission control transistor 5, a storage capacitor 6, and a coupling capacitor 7. It should be noted that a P-type thin film transistor is adopted for every transistor.

**[0012]** The drive transistor 2 is configured such that its source terminal is connected to a power source line 13 shared by all pixels, its drain terminal is connected to the source terminal of the light-emission control transistor 5 and to the source terminal of the reset transistor 4, and its gate terminal is connected to one end of the storage capacitor 6 and the source terminal of the selection transistor 3, the other end of the storage capacitor 6 being connected to a sweep line 12. The gate terminal of the selection transistor 3 is connected to a selection line 9, and the drain terminal thereof is connected to one end of the coupling capacitor 7 and the drain terminal of the reset transistor 4, the other end of the coupling capacitor 7 being connected to a data line 8. The gate terminal of the reset transistor 4 is connected to a.reset line 10. The gate terminal of the light-emission control transistor 5 is connected to light-emission control line 11, and the drain terminal thereof is connected to the anode of the organic EL element 1. The cathode of the organic EL element 1 is connected to a cathode electrode 14 shared by all pixels.

**[0013]** FIG 2 shows signal waveforms to be input to the data line 8, the selection line 9, the reset line 10, and the light-emission control line 11, for driving the pixel 15. First, when a black level potential Vb is supplied to the data line 8, the selection line 9 and the reset line 4 are turned into low levels, and the selection transistor 3 and the reset transistor 4 are turned on. Thereby, the gate terminal and the drain terminal of the drive transistor 2 are connected (diode-connected), so that a current flows through the organic EL element 1 via the light-emission control transistor 5. Then, when the light-emission control line 11 is turned to a high level, the light-emission control transistor 5 is turned off. Thereby, the current flowing through the organic EL element flows into the coupling capacitor 7 via the reset transistor 4, and further into the storage capacitor 6 via the selection transistor 3 to thereby shift the gate potential of the drive transistor 2 to a direction in which the current does not flow (direction in which the voltage increases). Thereby, the gate potential of the drive transistor 2 converges near a potential Vdd-Vth which is lower than the power supply potential Vdd of the power source line 13 by a threshold potential Vth.

**[0014]** Then, when the reset line 10 is turned to a high level, the gate potential of the drive transistor 2 is maintained at Vdd-Vth by the storage capacitor 6 and the coupling capacitor 7. In this state, when a white level potential Vw (<Vb) is supplied to the data line 8, the gate potential Vg of the drive transistor 2 becomes Vg=Vdd-Vth-Cc/(Cc+Cs)*(Vb-Vw), where Cc represents the capacitance of the coupling capacitor 7 and Cs represents the capacitance of the storage capacitor 6. Under assumption that Cc is sufficiently larger than Cs, Vg=Vdd-Vth-(Vb=Vw). Consequently, to the gate potential of the drive transistor 2, Vth is automatically applied to offset the difference between the white level and the black level.

**[0015]** When writing of data ends, the selection line 9 is turned to a high level, and the gate potential is stored in the storage capacitor 6 until being selected next time.

**[0016]** Although the selection transistor 3 and the reset transistor 4 are off during the non-selected period, leakage current is likely to be caused in the reset transistor 4. This is because if a black level Vb is written as image data into the pixel 15, the gate potential Vg becomes Vdd-Vth, whereby almost no current flows through the organic EL element 1, so that, although the potential of the source terminal of the reset transistor 4 drops to a potential near the cathode potential VSS, its drain potential remains Vdd-Vth. As such, the potential difference between the source and the drain of the reset transistor 4 is large.

**[0017]** In the pixel 15, as the selection transistor 3 is arranged between the gate terminal of the drive transistor 2 and the drain terminal of the reset transistor 4, even if the drain potential drops due to leakage current of the reset transistor 4, the drop does not affect the gate potential of the drive transistor 2, so that the written gate potential is maintained.

**[0018]** FIG 3 shows a sweep pulse to be applied to the sweep line after image data are written. After the data are written, a triangular wave is input to the sweep line 12 as shown in FIG 3. Thereby, the gate potential of the drive transistor 2 varies in the same manner as the sweep line 12 via the storage capacitor 6. If the power supply potential Vdd was supplied to the sweep line 12 when the data were written, a potential difference of Vth+(Vb-Vw) would be written into the storage capacitor 6. Under the assumption that the potential (sweep potential) of the sweep line 12 is Vsw, the gate potential Vg of the drive transistor 2 varies according to Vg=Vsw-Vth-(Vb-Vw). When the sweep potential Vsw is Vdd+(Vb-Vw), the gate potential of the drive transistor 2 becomes Vdd-Vth so that the light goes out. As such, as the difference (Vb-Vw) is larger, the blackout period becomes shorter (emission period becomes longer), and as the difference is smaller, the blackout period becomes longer (emission period becomes shorter). In other words, the emission period can be controlled by the data difference (Vb-Vw) between the white level and the black level input.

**[0019]** Accordingly, by supplying a data voltage corresponding to the brightness of the pixel as a white level Vw, the pixel emits light for a period corresponding to the data. As such, a PMW control for controlling the emission period is performed by the brightness data, and Vth of the drive transistor 2 is also compensated at the same

time. Further, in the case of digital drive, both the black level Vb and the white level Vw are supplied as data voltage. Although the white level Vw is constant, it is also possible to compensate for Vth of each drive transistor 2 even in this case.

**[0020]** FIG 4 shows examples of peripheral circuits for supplying a control signal to the data line 8, the selection line 9, the reset line 10, and the light-emission control line 11 of the pixel 15. In general, at least one shift register 16 is provided for the respective lines, and selected data are sequentially shifted from the highest line to lower lines. The output terminal of the shift resister 16 is connected to an input terminal of each of a selection enable circuit 17, a reset enable circuit 18, and a light-emission enable circuit 19. Another input terminal of the selection enable circuit 17 is connected to a selection enable line SE, another input terminal of the reset enable circuit 18 is connected to a reset enable line RE, and another input terminal of the light emission enable circuit 19 is connected to a light-emission enable line LE.

**[0021]** If the selection enable line SE is turned to a high level when selected data of a high level are stored in the shift register 16, the selection line 9 becomes low and is selected. At that time, if the reset enable line RE is turned to a high level, the reset line 10 becomes low, so that the gate terminal and the drain terminal of the drive transistor 2 are connected, whereby current flows into the organic EL element 1.

**[0022]** Then, when the black level potential Vb is supplied from a data driver 25 to the data line 8 so that the light-emission enable line LE is turned to a high level, the light-emission control line 11 becomes high, whereby the current flowing into the organic EL element 1 is interrupted and the threshold potential Vth is written into the storage capacitor 6 and the coupling capacitor 7. When the reset enable line RE is turned to a low level, the reset line 10 becomes high, and the threshold potential Vth is stored in the storage capacitor 6 and the coupling capacitor 7. Then, when image data Vw are supplied from the data driver 25 to the data line 8, data in which Vth is corrected are written into the gate terminal of the drive transistor 2.

**[0023]** Then, when the selected data of a high level, stored in the shift register 16, are shifted to the next stage and data of a low level are stored therein, the selection line 9 is turned to high level, the reset line 10 is turned to a high level, and the light-emission control line 11 is turned to a low level by the selection enable circuit 17, the reset enable circuit 18, and the light-emission enable circuit 19, respectively, regardless of the states of the selection enable line SE, the reset enable liner RE, and the light-emission enable line LE, whereby the data written in the pixel 15 are stored.

**[0024]** In this writing operation, when the selection line 9 is selected and turned to a low level, the sweep line 12 is connected to a reference potential line 23 to which Vref (Vdd) is supplied, by way of a switch 22. At the same time, as the low potential of the selection line 9 is inverted by an inverter 20 so as to turn a switch 21 off, the sweep line 12 is cut off from a sweep potential line 24 to which the sweep potential Vsw is supplied.

**[0025]** When the writing operation ends, the selection line 9 becomes high, and as the switch 22 is turned off, the sweep line 12 is cut off from the reference potential line 23, and the switch 21 is turned on by a signal inverted by the inverter 20, whereby the sweep line 12 is connected to the sweep potential line 24. Thus, the sweep line 12 is fixed only at the time of writing, and when the writing ends, operation to restart sweeping will be repeated.

**[0026]** In the present embodiment, the emission period is controlled by a sweep pulse. If the drive transistor 2 is in a saturated region, the amount of current flowing in the drive transistor 2 is controlled by the analog data voltage and the emission period controlled by the sweep pulse. However, if the drive transistor 2 is in a linear region, as the emission period is digitally controlled, effects exerted by the characteristics of the transistor are reduced. As such, non-uniformity in display can be reduced even with this aspect.

**[0027]** As shown in FIG 5A, emission control by sweeping may be performed for one frame period by use of the peripheral circuits shown in FIG 4, or may be divided into two periods as shown in FIG 5B such that the writing period and the emission period controlled by sweeping are separated. In the example of FIG 5B, the sweep pulse is maintained at a high level in the writing period during which data are written, in order not to emit light in the pixel during the writing period, and the level of the sweep pulse falls when the writing period ends. In the writing period, if the amplitude $\Delta$Vsw of the sweep pulse is added to the white level Vw as an offset so that the data potential Vw' to be supplied to the data line 8 becomes Vw+$\Delta$Vsw, the gate potential Vg of the drive transistor 2 becomes Vg=Vdd-Vth-(Vb-Vw)+$\Delta$Vsw. If $\Delta$Vsw is larger than (Vb-Vw), the pixel does not emit light during the writing period. As the level of the sweep pulse falls in the emission period, light emission begins, and the emission period is controlled in proportion to (Vb-Vw). In the case where the writing period and the sweep period are separated as shown in FIG 5B, the switches 21 and 22, the inverter 20, and the reference potential line 23 shown in FIG 4 may be omitted as shown in FIG 6. Thus, the only requirement is to produce a triangular wave in the emission period while keeping the sweep potential constant at Vref (Vdd) in the writing period.

**[0028]** Further, the light-emission control transistor 5 may be omitted as in the pixel 15 of FIG 6. In that case, the light-emission control line 11, the light-emission enable circuit 19, and the light-emission enable line LE can also be omitted, so the pixel circuit and the peripheral circuits are simplified. However, if the light-emission control transistor 5 is omitted, when the selection transistor 3 and the reset transistor 4 are turned on, the potential to be written into the storage capacitor 6 and to the coupling capacitor 7 is not the threshold potential Vth of the drive transistor 2 but a reset potential which is divided by

the diode-connected drive transistor 2 and the organic EL element 1. The reset potential is also a potential corresponding to the characteristics of the drive transistor 2, providing the almost same advantages as those described above.

**[0029]** The procedures to write image data after writing the reset potential and sweep the sweep line 12 to emit light are also the same. Further, light emission may be performed by controlling a sweep pulse in one frame period as shown in FIG. 5A by switching potentials to which the sweep line 12 is connected between the time of selecting a line and the time of emitting light, by way of the switches 21 and 22 and the inverter 20.

**[0030]** The sweep pulse is not necessarily a perfect triangular wave, so long as an up phase and a down phase are alternately repeated. The slopes of the up phase and the down phase are not necessarily constant, and may be different between the up phase and the down phase. Further, a period of a constant voltage may exist near the peak. Furthermore, with a waveform which is convex downward, the emission period and the blackout period can be reversed.

**[0031]** FIG 7 shows the overall configuration of a display panel. A data signal and a timing signal are supplied to the data driver 25, and are then appropriately supplied to data lines 8 in a row direction, each of which is arranged corresponding to an individual pixel. A vertical driver 26, incorporating the shift register 16, timely controls the voltage of the selection line 9 and the reset line 10. Each of the selection lines 9 and each of the reset lines 10 is provided corresponding to an individual pixel line. Further, a sweep pulse is generated in a sweep pulse generation circuit 27, and is supplied to each pixel. An area in which pixels are arranged in a matrix is a display area 28.

**[0032]** Although in the above example an organic EL element is adopted as a light-emitting element, other light-emitting elements of current drive type can also be used.

**PARTS LIST**

**[0033]**

| | |
|---|---|
| 1 | element |
| 2 | drive transistor |
| 3 | selection transistor |
| 4 | reset transistor |
| 5 | light-emission control transistor |
| 6 | storage capacitor |
| 7 | coupling capacitor |
| 8 | data line |
| 10 | reset line |
| 11 | light-emission control line |
| 12 | sweep line |
| 13 | power source line |
| 14 | cathode electrode |
| 15 | pixel |
| 16 | shift register |
| 17 | selection enable circuit |
| 18 | reset enable circuit |
| 19 | light-emission enable circuit |
| 20 | inverter |
| 21 | switch |
| 22 | switch |
| 23 | reference potential line |
| 24 | sweep potential line |
| 25 | data driver |
| 26 | vertical driver |
| 27 | sweep pulse generation circuit |
| 28 | display area |

**Claims**

**1.** A display panel comprising a data line (8), a selection line (9), a reset line (10), and a sweep line (12), and having pixels arranged in a matrix, each pixel comprising:

a coupling capacitor (7) having one end connected to the data line (8);
a selection transistor (3) having one end connected to another end of the coupling capacitor (7) and a gate connected to the selection line (9);
a drive transistor (2), having a gate connected to another end of the selection transistor (3), which supplies current in accordance with a gate voltage;
a light-emitting element (1) which is connected

to a drain of the drive transistor (2) and emits light by the current supplied from the drive transistor (2);
a reset transistor (4) having one end connected to a connecting point of the drive transistor (2) and the light-emitting element (1), another end connected to a connecting point of the coupling capacitor (7) and the selection transistor (3), and a gate connected to the reset line (10);
a storage capacitor (6) having one end connected to a gate of the drive transistor (2) and another end connected to the sweep line (12); and
the display panel further comprising a vertical driver (26) adapted to control the selection line and the reset line, a data driver (25) adapted to control the data line, and a sweep pulse generation circuit (27) adapted to generate a sweep pulse applied to the sweep line, said sweep pulse having a triangular wave which alternately repeats an up phase and a down phase, the display panel being adapted to perform a method comprising the following steps:

in a first step, turning on the reset transistor (4) and the selection transistor (3), rendering the drive transistor (2) diode-connected and supplying a potential on the data line (8) so that current flows through the drive transistor (2) and the light-emitting element (1), then
in a second step, maintaining the control performed in the first step such that a voltage corresponding to a characteristic of the drive transistor is written into the coupling capacitor (7), then
in a third step, turning off the reset transistor (4), then
in a fourth step, applying a voltage corresponding to the image data to the data line (8), said voltage being written into the storage capacitor (6) via the coupling capacitor (7), and then
in a fifth step turning off the selection transistor and then applying the sweep pulse to the sweep line (12) to control an on period of the drive transistor (2) in accordance with the gate voltage to thereby control light emission.

**2.** The display panel according to Claim 1 further comprising a light-emission control line (11) controlled by the vertical driver (26), wherein
each pixel further comprises a light emission control transistor (5) having a gate connected to the light-emission control line (11), said light emission control transistor (5) being arranged between the connecting point of the drains of the drive transistor (2) and the reset transistor (4), and the light-emitting element (1), and
wherein the display panel is further adapted to turn off the light-emission control transistor (5) at the beginning of the second step.

**Patentansprüche**

**1.** Anzeigetafel mit einer Datenleitung (8), einer Auswahlleitung (9), einer Rücksetzleitung (10) und einer Abtastleitung (12) und mit Pixeln, die in einer Matrix angeordnet sind, wobei jedes Pixel aufweist:

einen Kopplungskondensator (7), der ein Ende aufweist, das mit der Datenleitung (8) verbunden ist;
einen Auswahltransistor (3), der ein Ende aufweist, das mit einem weiteren Ende des Kopplungskondensators (7) verbunden ist, und ein Gate aufweist, das mit der Auswahlleitung (9) verbunden ist;
einen Treibertransistor (2), der ein Gate aufweist, das mit einem anderen Ende des Auswahltransistors (3) verbunden ist, und der Strom gemäß einer Gate-Spannung zuführt;
ein lichtemittierendes Element (1), das mit einem Drain des Treibertransistors (2) verbunden ist und Licht durch den Strom emittiert, der von dem Treibertransistor (2) zugeführt wird;
einen Rücksetztransistor (4), der ein Ende aufweist, das mit einem Verbindungspunkt des Treibertransistors (2) und des lichtemittierenden Elements (1) verbunden ist, ein anderes Ende aufweist, das mit einem Verbindungspunkt des Kopplungskondensators (7) und des Auswahltransistors (3) verbunden ist, und ein Gate aufweist, das mit der Rücksetzleitung (10) verbunden ist;
einen Speicherkondensator (6), der ein Ende aufweist, das mit einem Gate des Treibertransistors (2) verbunden ist, und ein anderes Ende aufweist, das mit der Abtastleitung (12) verbunden ist; und
wobei die Anzeigetafel ferner einen vertikalen Treiber (26), der dazu ausgebildet ist, die Auswahlleitung und die Rücksetzleitung zu steuern, einen Datentreiber (25), der dazu ausgebildet ist, die Datenleitung zu steuern, und eine Abtastimpuls-Erzeugungsschaltung (27) aufweist, die dazu ausgebildet ist, einen Abtastimpuls zu erzeugen, der an die Abtastleitung angelegt wird, wobei der Abtastimpuls eine Dreieckswelle aufweist, die abwechselnd eine Aufwärtsphase und eine Abwärtsphase wiederholt, wobei die Anzeigetafel dazu ausgebildet ist, ein Verfahren mit den folgenden Schritten durchzuführen:

in einem ersten Schritt, Einschalten des

Rücksetztransistors (4) und des Auswahltransistors (3), wobei der Treibertransistor (2) diodenverbunden wird und ein Potenzial auf der Datenleitung (8) zugeführt wird, so dass Strom durch den Treibertransistor (2) und das lichtemittierende Element (1) fließt, dann,
in einem zweiten Schritt, Aufrechterhalten der in dem ersten Schritt durchgeführten Steuerung, so dass eine Spannung, die einer Charakteristik des Treibertransistors entspricht, in den Kopplungskondensator (7) geschrieben wird, dann,
in einem dritten Schritt, Ausschalten des Rücksetztransistors (4), dann,
in einem vierten Schritt, Anlegen einer Spannung, die den Bilddaten entspricht, an die Datenleitung (8), wobei die Spannung über den Kopplungskondensator (7) in den Speicherkondensator (6) geschrieben wird, und dann,
in einem fünften Schritt, Ausschalten des Auswahltransistors und dann Anlegen des Abtastimpulses an die Abtastleitung (12) zum Steuern einer Einschaltdauer des Treibertransistors (2) nach Maßgabe der Gate-Spannung, um dadurch die Lichtemission zu steuern.

**2.** Anzeigetafel nach Anspruch 1, ferner mit einer Lichtemissionssteuerleitung (11), die von dem vertikalen Treiber (26) gesteuert wird, wobei
jedes Pixel ferner einen Lichtemissionssteuertransistor (5) aufweist, der ein Gate hat, das an die Lichtemissionssteuerleitung (11) angeschlossen ist, wobei der Lichtemissionssteuertransistor (5) zwischen dem Anschlusspunkt der Drains des Treibertransistors (2) und des Rücksetztransistors (4) und dem lichtemittierenden Element (1) angeordnet ist, und
wobei die Anzeigetafel ferner dazu ausgebildet ist, den Lichtemissionssteuertransistor (5) zu Beginn des zweiten Schritts abzuschalten.

## Revendications

**1.** Panneau d'affichage comprenant une ligne de données (8), une ligne de sélection (9), une ligne de réinitialisation (10), et une ligne de balayage (12), et ayant des pixels agencés en une matrice, chaque pixel comprenant :

un condensateur de couplage (7) ayant une extrémité connectée à la ligne de données (8) ;
un transistor de sélection (3) ayant une extrémité connectée à une autre extrémité du condensateur de couplage (7) et une grille connectée à la ligne de sélection (9) ;
un transistor d'attaque (2), ayant une grille connectée à une autre extrémité du transistor de sélection (3), qui délivre un courant en fonction d'une tension de grille ;
un élément électroluminescent (1) qui est connecté à un drain du transistor d'attaque (2) et émet une lumière par le courant délivré du transistor d'attaque (2);
un transistor de réinitialisation (4) ayant une extrémité connectée à un point de connexion du transistor d'attaque (2) et de l'élément électroluminescent (1), une autre extrémité connectée à un point de connexion du condensateur de couplage (7) et du transistor de sélection (3), et une grille connectée à la ligne de réinitialisation (10) ;
un condensateur de stockage (6) ayant une extrémité connectée à une grille du transistor d'attaque (2) et une autre extrémité connectée à la ligne de balayage (12) ; et
le panneau d'affichage comprenant en outre un circuit d'attaque vertical (26) adapté à commander la ligne de sélection et la ligne de réinitialisation, un circuit d'attaque de données (25) adapté à commander la ligne de données, et un circuit de génération d'impulsion de balayage (27) adapté à générer une impulsion de balayage appliquée à la ligne de balayage, ladite impulsion de balayage ayant une onde triangulaire qui répète de façon alternée une phase montante et une phase descendante, le panneau d'affichage étant adapté à mettre en oeuvre un procédé comprenant les étapes suivantes :

dans une première étape, l'activation du transistor de réinitialisation (4) et du transistor de sélection (3), la connexion du transistor d'attaque (2) à une diode et la délivrance d'un potentiel sur la ligne de données (8) de façon à ce qu'un courant traverse le transistor d'attaque (2) et l'élément électroluminescent (1), ensuite
dans une deuxième étape, le maintien de la commande exécutée à la première étape de façon à ce qu'une tension correspondant à une caractéristique du transistor d'attaque soit écrite dans le condensateur de couplage (7), ensuite
dans une troisième étape, la désactivation du transistor de réinitialisation (4), ensuite
dans une quatrième étape, l'application d'une tension correspondant aux données d'image à la ligne de données (8), ladite tension étant écrite dans le condensateur de stockage (6) par l'intermédiaire du condensateur de couplage (7), et ensuite
dans une cinquième étape, la désactivation du transistor de sélection et ensuite l'appli-

cation de l'impulsion de balayage à la ligne de balayage (12) pour commander une période d'activation du transistor d'attaque (2) en fonction de la tension de grille pour ainsi commander une émission de lumière.

**2.** Panneau d'affichage selon la revendication 1 comprenant en outre une ligne de commande d'émission de lumière (11) commandée par le circuit d'attaque vertical (26), dans lequel
chaque pixel comprend en outre un transistor de commande d'émission de lumière (5) ayant une grille connectée à la ligne de commande d'émission de lumière (11), ledit transistor de commande d'émission de lumière (5) étant agencé entre le point de connexion des drains du transistor d'attaque (2) et du transistor de réinitialisation (4), et l'élément électroluminescent (1), et
dans lequel le panneau d'affichage est en outre adapté à désactiver le transistor de commande d'émission de lumière (5) au début de la deuxième étape.

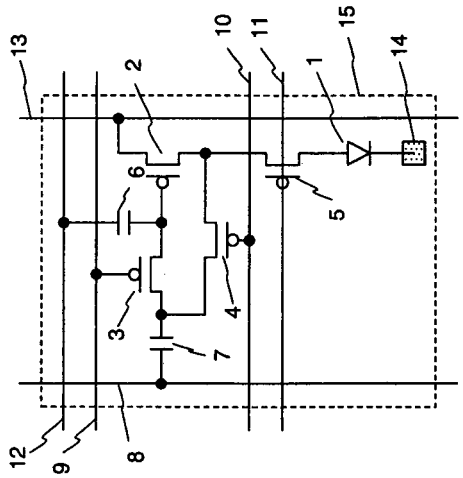


FIG. 1

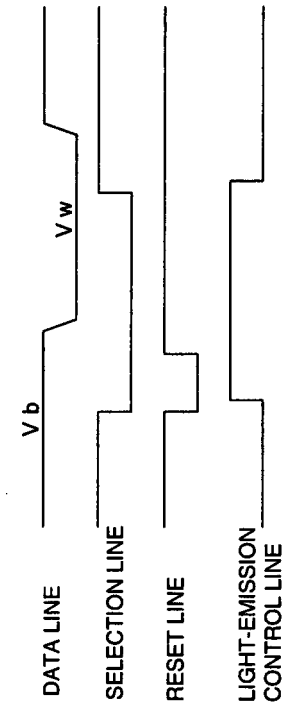
V b
V w
DATA LINE
SELECTION LINE
RESET LINE
LIGHT-EMISSION CONTROL LINE

FIG. 2

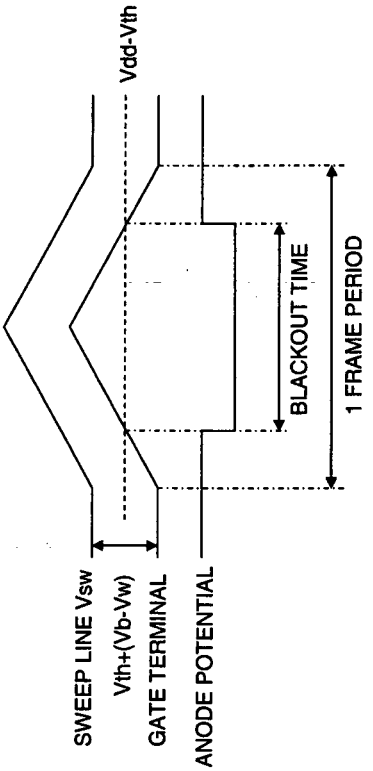
Vdd-Vth
BLACKOUT TIME
1 FRAME PERIOD
SWEEP LINE Vsw
Vth+(Vb-Vw)
GATE TERMINAL
ANODE POTENTIAL

FIG. 3

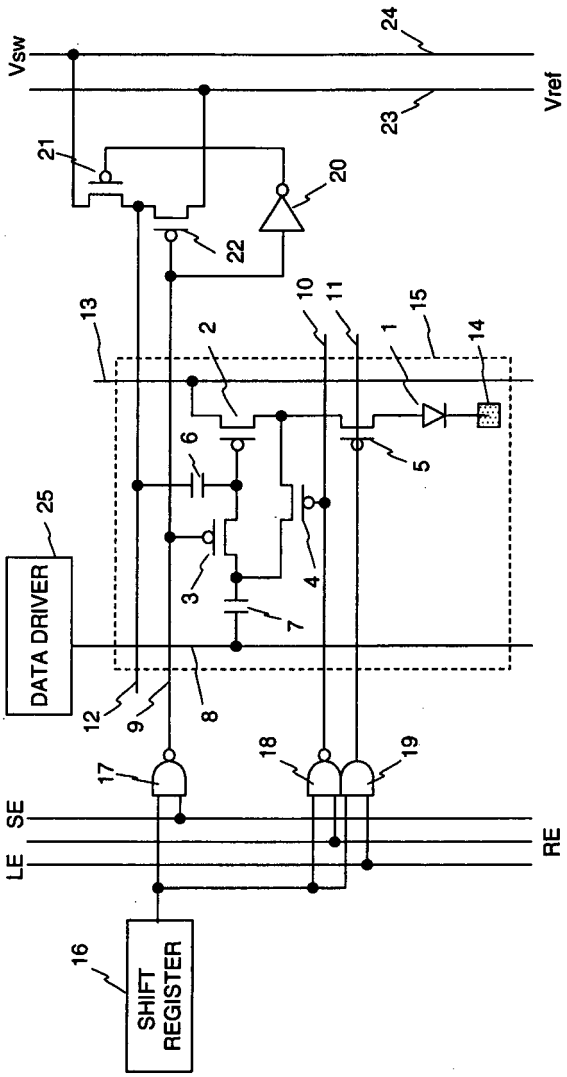
Vsw
Vref
24
23
21
20
22
13
2
10
11
1
15
14
6
5
25
DATA DRIVER
3
4
7
12
9
8
18
19
17
SE
LE
RE
16
SHIFT REGISTER

FIG. 4

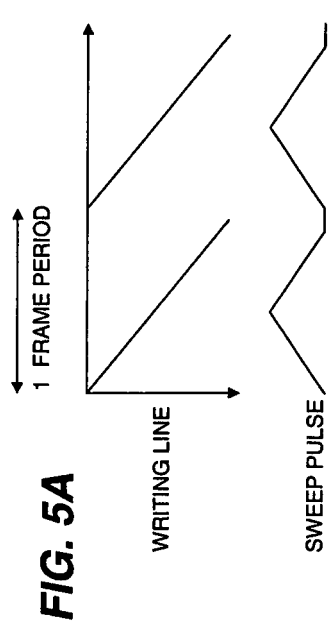
1 FRAME PERIOD
WRITING LINE
SWEEP PULSE

FIG. 5A

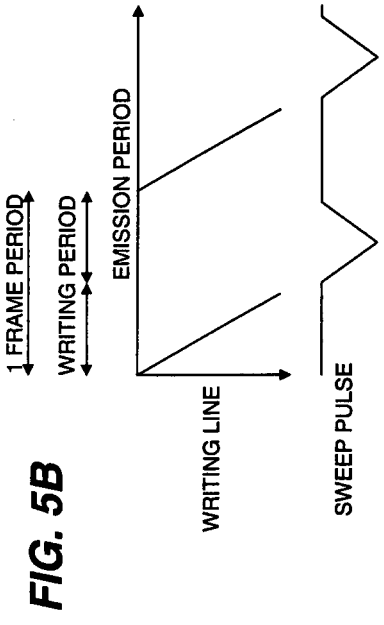
1 FRAME PERIOD
WRITING PERIOD
EMISSION PERIOD
WRITING LINE
SWEEP PULSE

FIG. 5B

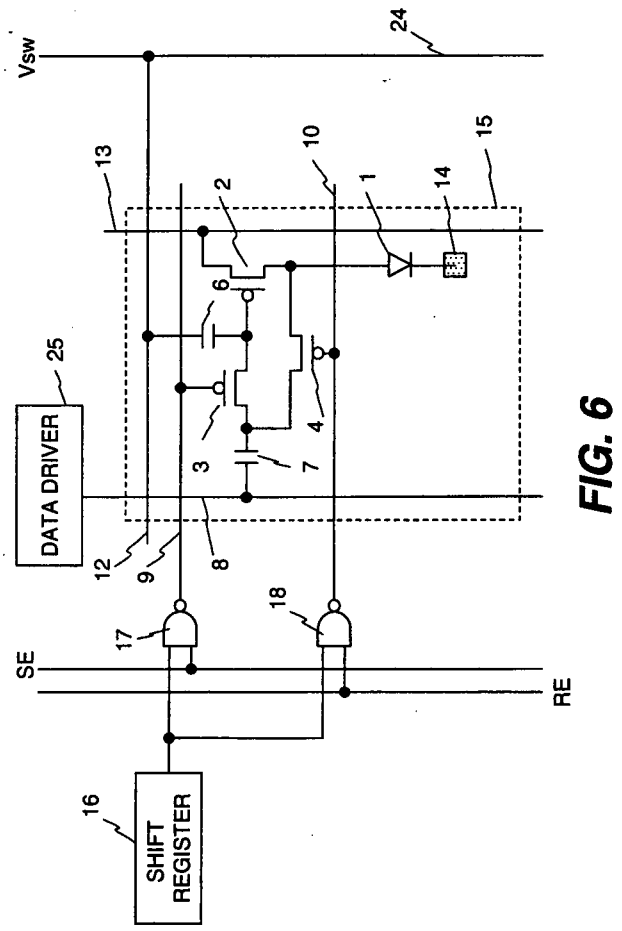
Vsw
24
13
10
15
2
1
14
6
25
DATA DRIVER
3
4
7
12
9
8
18
17
SE
RE
16
SHIFT REGISTER

FIG. 6

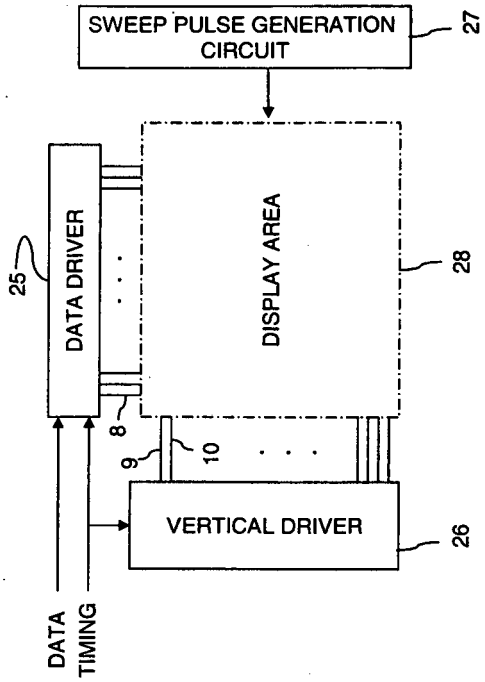
SWEEP PULSE GENERATION CIRCUIT
27
DATA DRIVER
25
DISPLAY AREA
28
8
9
10
VERTICAL DRIVER
26
DATA
TIMING

FIG. 7

## REFERENCES CITED IN THE DESCRIPTION

*This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.*

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- WO 0154107 A1 **[0005]**
- US 20060022305 A1 **[0006]**

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|---|---|---|---|
| 专利名称(译) | OLED显示面板，带PWM控制 | | |
| 公开(公告)号 | EP2255354B1 | 公开(公告)日 | 2013-04-24 |
| 申请号 | EP2009721992 | 申请日 | 2009-03-17 |
| [标]申请(专利权)人(译) | 全球OLED TECH | | |
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| 发明人 | KAWABE, KAZUYOSHI | | |
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| 优先权 | 2008070550 2008-03-19 JP | | |
| 其他公开文献 | EP2255354A1 | | |
| 外部链接 | Espacenet | | |


摘要(译)

提供一种将PWM驱动施加到驱动晶体管（2）的显示面板。驱动晶体管根据其栅极电压提供电流，并且电流被提供给发光元件（1）以照射发光元件。存储电容器（6）的一端连接到驱动晶体管的栅极，而其另一端连接到扫描线（12）。将交替重复上相和下相的三角波提供给扫描线，以便根据栅极电压控制驱动晶体管的导通时段，从而控制发光元件的发光。


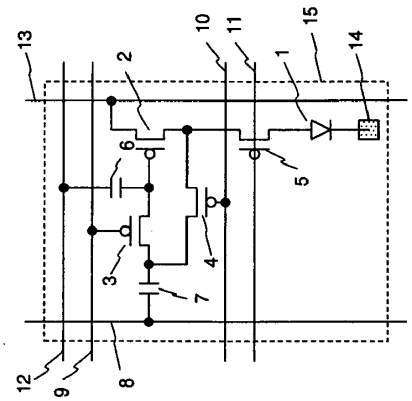


FIG. 1