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(54) **Method of fabricating an organic light emitting diode display device**

Verfahren zur Herstellung einer OLED-Anzeigevorrichtung

Procédé de fabrication d'un dispositif d'affichage à diodes électroluminescentes organiques

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Description

[0001] The present invention relates to 2. a method of fabricating an organic light emitting diode (OLED) display device and more particularly, to an OLED display device including a capacitor whose capacitance is increased using a method of fabricating a polysilicon layer using a metal catalyst. In general, polysilicon is widely used as a semiconductor layer of a thin film transistor due to its high field effect mobility and applicability to high-speed operating circuits and complementary metal-oxide-semiconductor (CMOS) circuits. The thin film transistors having a polysilicon layer are generally used as active elements of active matrix liquid crystal displays (AMLCDs), and switching elements and driving elements of organic light emitting diodes (OLEDs).

[0002] Here, methods of crystallizing an amorphous silicon layer into the polysilicon layer used for a thin film transistor include a solid phase crystallization (SPC) method, an excimer laser crystallization (ELC) method, a metal induced crystallization (MIC) method, and a metal induced lateral crystallization (MILC) method. In the SPC method, an amorphous silicon layer is annealed at a temperature of about 700°C or less, i.e., a transition temperature of a glass substrate of a display device for several hours to several tens of hours. In the ELC method, an excimer laser is irradiated on an amorphous silicon layer to locally heat the irradiated portion to a high temperature for a very short time period, so that the amorphous silicon layer is crystallized. In the MIC method, metals such as nickel, palladium, gold, aluminum, etc., are placed in contact with or injected into an amorphous silicon layer, so that the amorphous silicon layer is changed into a polysilicon layer, i.e., a phase change of the amorphous silicon is induced by the metal. In the MILC method, silicide, which is produced by reacting metal with silicon, is laterally and continuously diffused to sequentially induce crystallization of the amorphous silicon layer.

[0003] However, the SPC method requires a long time, and the annealing process is performed at a high temperature for a long time, which may deform a substrate. Also, in the ELC method, a high-priced laser device is required, and protrusions may be formed on the polycrystalline surface such that interfacial characteristics between a semiconductor layer and a gate insulating layer may deteriorate. Currently, research into methods of crystallizing an amorphous silicon layer using a metal is actively progressing because crystallization can be achieved at a lower temperature and with less time than the SPC method. The methods of crystallizing an amorphous silicon layer using a metal include the MIC method, the MILC method, and a super grain silicon crystallization method.

[0004] Meanwhile, in an OLED, capacitors are formed, and a capacitor having a high capacitance may be advantageous to the operation of the OLED. Thus, research into increasing the capacitance of the capacitor is required.

[0005] KR20040035409, JP H07 13196, US2004/004597, JP H06 67203 and JP2001337348 relate to TFT display panels with increased capacitance caused by shaping a capacitor around protrusions.

[0006] Aspects of the present invention provide a method of fabricating an organic light emitting diode (OLED) display device in which capacitance of a capacitor is increased by increasing a surface area of the capacitor in a simple manner. According to an aspect of the present invention, there is provided a method of fabricating an OLED display device according to claim 1. Optional features are set out in the dependent claims.

[0007] According to an exemplary embodiment, a method of fabricating an organic light emitting diode (OLED) display device includes the steps of claim 1. Additional aspects and/or advantages of the invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the invention.

[0008] These and/or other aspects and advantages of the invention will become apparent and more readily appreciated from the following description of the embodiments, taken in conjunction with the accompanying drawings of which:

FIGS. 1A to 1G illustrate manufacture of an organic light emitting diode (OLED) display device according to an exemplary embodiment of the present invention; and

FIG. 2 is a photograph showing a surface of a buffer layer from which a polysilicon layer is removed according to an exemplary embodiment of the present invention.

[0009] Reference will now be made in detail to the present embodiments of the present invention, examples of which are illustrated in the accompanying drawings, wherein like reference numerals refer to the like elements throughout. The embodiments are described below in order to explain the present invention by referring to the figures. In the drawings, the sizes and proportions of layers/regions may be exaggerated, and like reference numerals refer to like elements. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "formed on" or "disposed on" another element, it can be disposed directly on the other element, or intervening elements may also be present. In contrast, when an element is referred to as being "formed directly on" or "disposed directly on" another element, there are no intervening elements present

[0010] FIGS. 1A to 1G illustrate the manufacture of an organic light emitting diode (OLED) display device according to an exemplary embodiment of the present invention. Referring to FIG. 1A, a substrate 100 including a thin film transistor region a and a capacitor region b is prepared, and a buffer layer 110 is formed on the substrate 100. The substrate 100 may be formed of glass or plastic, and the buffer layer 110 may be formed of a single

insulating layer, such as one of a silicon oxide layer and a silicon nitride layer, or a stacked layer thereof, using a chemical vapor deposition (CVD) method or a physical vapor deposition (PVD) method.

[0011] Here, the buffer layer 110 may function to prevent the diffusion of moisture or impurities from the substrate 100 or to adjust a heat transfer rate in crystallization to facilitate crystallization of a later-formed amorphous silicon layer.

[0012] Next, referring to FIG. 1B, an amorphous silicon layer 120a is formed on the buffer layer 110. Then, a diffusion layer 123 and a metal catalyst layer 125 are formed on the amorphous silicon layer 120a. Here, the amorphous silicon layer 120a may be formed by a CVD or PVD method. Further, when the amorphous silicon layer 120a is formed or after the amorphous silicon layer 120a is formed, a dehydrogenation process may be performed to lower the concentration of hydrogen. The diffusion layer 123 may be formed of a silicon nitride layer through which a metal catalyst to be formed in the following process can be diffused in an annealing process, and may be formed of a stacked layer of a silicon nitride layer and a silicon oxide layer. The diffusion layer 123 may be formed by a CVD or PVD method. Here, the diffusion layer 123 may be formed to a thickness of 0.1nm (1Å) to 200nm (2000Å). When the diffusion layer 123 is formed to a thickness less than 0.1nm (1Å), the diffusion layer 123 may not sufficiently control the amount of metal catalyst diffused therethrough. When the thickness of the diffusion layer 123 exceeds 200nm (2000Å), the amount of metal catalyst that diffuses to the amorphous silicon layer 120a is small, and thus it may be difficult to crystallize the amorphous silicon layer into a polysilicon layer.

[0013] A metal catalyst is deposited on the diffusion layer 123 to form the metal catalyst layer 125. Here, one selected from the group consisting of Ni, Pd, Ag, Au, Al, Sn, Sb, Cu, Tb, and Cd. For example, nickel (Ni) may be used as the metal catalyst. Here, the metal catalyst layer 125 may be formed with an areal density of 1011 atoms/cm^2 to 1015 atoms/cm^2 on the diffusion layer 123. When the metal catalyst is formed with an areal density less than 1011 atoms/cm^2, the amount of seeds that are crystallization nuclei is small, and thus the amorphous silicon layer may not be crystallized into a polysilicon layer using a super grain silicon (SGS) method. Alternatively, when the metal catalyst is formed with an areal density greater than 1015 atoms/cm^2, the amount of metal catalyst diffused into the amorphous silicon layer is great, and thus grains of a resultant polysilicon layer are small. Furthermore, as the amount of remaining metal catalyst increases in the resultant polysilicon layer, characteristics of a semiconductor layer formed by patterning the polysilicon layer deteriorate.

[0014] As described above, an annealing process is performed on the substrate 100 on which the buffer layer 110, the amorphous silicon layer 120a, the diffusion layer 123, and the metal catalyst layer 125 are formed to move at least a portion of the metal catalyst of the metal catalyst layer 125 to a surface of the amorphous silicon layer 120a. That is, only a small amount of metal catalyst diffuses through the diffusion layer 123 to the surface of the amorphous silicon layer 120a, and most of the metal catalyst does not reach the amorphous silicon layer 120a or pass through the diffusion layer 123.

[0015] Therefore, the amount of metal catalyst reaching the surface of the amorphous silicon layer 120a is determined depending on a diffusion blocking ability of the diffusion layer 123, and the diffusion blocking ability of the diffusion layer 123 is closely related to the thickness of the diffusion layer 123. For example, as the diffusion layer 123 becomes thicker, the amount of metal catalyst to be diffused is reduced, and thus the grain size is increased. Moreover, as the diffusion layer becomes thinner, the amount of metal catalyst to be diffused is increased, and thus the grain size is reduced.

[0016] Here, the annealing process may be performed at a temperature of 200°C to 900°C, for example, 350°C to 500°C for several seconds to several hours to diffuse the metal catalyst of the metal catalyst layer 125 to the amorphous silicon layer 120a. When the annealing process is performed at such a temperature for such a time period, deformation of a substrate caused by an excessive annealing process can be prevented to increase manufacturing yield and to reduce manufacturing costs. The annealing process may be performed using one of a furnace process, a rapid thermal annealing (RTA) process, an UV process, and a laser process (i.e., any of these processes).

[0017] After the amorphous silicon layer 120a is crystallized into the polysilicon layer, the diffusion layer 123 and the metal catalyst layer 125 are removed. Referring to FIG. 1C, the amorphous silicon layer 120a crystallized into the polysilicon layer is patterned to form a semiconductor layer 120. Here, the semiconductor layer may be patterned using dry etching.

[0018] When the polysilicon layer is patterned into the semiconductor layer 120 using dry etching, grain boundaries on which metal silicides of the polysilicon layer crystallized by the metal catalyst gather and a seed region are not completely removed from the surface of the etched buffer layer and remain as a protrusion A. Therefore, the protrusion A remaining on the buffer layer 110 is formed in the same shape as a grain boundary that is formed by crystallizing the amorphous silicon layer into the polysilicon layer. In addition, when the grain size of the semiconductor layer 120 formed of the polysilicon layer is great, the frequency of the protrusions A on the buffer layer is reduced, and when the grain size is small, the frequency of the protrusions A is increased.

[0019] FIG. 2 is a photograph showing a surface of a buffer layer after a polysilicon layer crystallized by a metal catalyst is removed by dry etching. Referring to FIG. 2, a protrusion formed to a thickness of up to 68nm (680Å) is observed on the buffer layer 110, and a step difference of the protrusion may vary depending on crystallization condition and thickness of the removed polysilicon layer.

[0020] Referring to FIG. ID, a gate insulating layer 130 is formed on the surface of the substrate 100 on which the semiconductor layer 120 is formed. The gate insulating layer 130 is formed to cover at least a portion of the semiconductor layer 120 to insulate the semiconductor layer 120 from a later formed gate electrode or may be formed on the entire surface of the substrate 100 to cover the semiconductor layer 120. The gate insulating layer 130 may be formed of a silicon oxide layer, a silicon nitride layer or a combination thereof, and the protrusions A of the buffer layer causes the gate insulating layer 130 and the lower capacitor electrode 145 to have protrusions A in the same shape.

[0021] Afterwards, a single layer of aluminum (Al) or an aluminum alloy, such as aluminum-neodymium (Al-Nd), or a multilayer in which an aluminum alloy is stacked on a chromium (Cr) or molybdenum (Mo) alloy is used to form a metal layer for a gate electrode (not shown). Then, the metal layer for a gate electrode is etched using photolithography and etching to form a gate electrode 140 facing the semiconductor layer 120 in the thin film transistor region a at a predetermined region of the semiconductor layer 120, i.e., a channel region thereof, and a lower capacitor electrode 145 in the capacitor region b.

[0022] Therefore, the protrusions are formed on the lower capacitor electrode 145, and thus a surface area of the electrode is increased. As a result, the increased surface area causes a capacitance of the capacitor to be increased when the capacitor is completely formed.

[0023] Referring to FIG. IE, an interlayer insulating layer 150 is formed on the surface of the substrate 100 on which the gate electrode 140 and the lower capacitor electrode 145 are formed. The interlayer insulating layer 150 may be formed to cover the entire surface of the substrate 100, including the gate electrode 140 and the lower capacitor electrode 145, or may be formed to cover at least a portion of each of the gate electrode 140 and the lower capacitor electrode 145. Afterwards, a metal layer for source and drain electrodes (not shown) is formed on the surface of the interlayer insulating layer and then patterned, so that source and drain electrodes 160a and 160b disposed in the thin film transistor region a and electrically connected to the semiconductor layer 120, and an upper capacitor electrode 163 disposed on the capacitor region b and facing the lower electrode 145 are formed. The source and drain electrodes 160a and 160b are electrically connected to source and drain regions of the semiconductor layer 120 via through holes formed in the interlayer insulating layer 150 and the gate insulating layer 130. Further, because the lower capacitor electrode 145 and the upper capacitor electrode 163 follow the shape of the protrusions A of the buffer layer 110 and have an increased area, the capacitance of the resultant capacitor is increased.

[0024] The interlayer insulating layer 150 may be formed of a silicon nitride layer, a silicon oxide layer, or a combination thereof. Also, the source and drain electrodes 160a and 160b and the upper capacitor electrode 163 may be formed of one selected from the group consisting of molybdenum (Mo), chromium (Cr), tungsten (W), molybdenum-tungsten (MoW), aluminum (Al), aluminum-neodymium (Al-Nd), titanium (Ti), titanium nitride (TiN), copper (Cu), a Mo alloy, an Al alloy, and a Cu alloy.

[0025] Afterwards, referring to FIG. IF, after a protection layer 170 is formed on the entire surface of the substrate, a first electrode 180 connected to one of the source and drain electrodes 160a and 160b of the thin film transistor region a is formed on the protection layer 170. The first electrode 180 is connected to the one of the source and drain electrodes 160a and 160b via a through hole formed in the protective layer 170.

[0026] The first electrode 180 may be formed as an anode or a cathode. When the first electrode 180 is formed as an anode, the anode may be formed of a transparent conductive layer made of ITO, IZO or ITZO; and when the first electrode 180 is formed as a cathode, the cathode may be formed of Mg, Ca, Al, Ag, Ba, or alloys thereof.

[0027] Referring to FIG. 1G, a pixel defining layer 185 having an opening to at least partially expose the first electrode 180 is formed on the protective layer 170. The pixel defining layer 185 may also be formed to cover at least a portion of the first electrode 180. An organic layer 190, including a light emitting layer, is formed on the exposed first electrode 180. The organic layer 190 may comprise a hole injection layer, a hole transport layer, a hole blocking layer, an electron blocking layer, an electron injection layer, and an electron transport layer. A second electrode 195 is formed on the organic layer 190. As a result, the OLED display device according to an example embodiment of the present invention is completed.

[0028] While a polysilicon layer crystallized using a SGS method is described, MILC and MIC methods in which crystallization is performed using a metal catalyst can be used as the method of crystallizing the amorphous silicon layer, and the methods may be used alone or in combination.

[0029] According to aspects of the present invention, an amorphous silicon layer is crystallized using a metal catalyst to form a semiconductor layer formed of a polysilicon layer. Further, protrusions that are formed by residual metals remaining in the silicon layer upon crystallization on a buffer layer in the form of metal silicides cause a surface area of the buffer layer to be increased. As a result, an OLED display device may have a capacitor formed on the buffer layer whose capacitance is increased.

[0030] Although a few embodiments of the present invention have been shown and described, it would be appreciated by those skilled in the art that changes may be made in these embodiments without departing from the invention, the scope of which is defined in the claims.

Claims

1. A method of fabricating an organic light emitting diode (OLED) display device, the method comprising:

   forming a substrate (100) having a thin film transistor region (a) and a capacitor region (b);
   forming a buffer layer (110) on the substrate (100);
   forming protrusions (A) in the buffer layer (110);
   forming a capacitor (145,150,163) on the buffer layer (110) in the capacitor region (b), wherein the capacitor (145,150,163) follows the shape of the protrusions (A) of the buffer layer (110); and
   characterised in that the step of forming protrusions (A) in the buffer layer (110) comprises:

   forming an amorphous silicon layer (120a) on the buffer layer (110);
   forming a metal catalyst layer (125) on the amorphous silicon layer (120a) ;
   annealing the substrate (100) to crystallize the amorphous silicon layer (120a) into a polysilicon layer;
   removing the metal catalyst layer (125); and
   patterning the polysilicon layer to form a semiconductor layer (120) disposed on the buffer layer (110) in the thin film transistor region (a); and
   forming the protrusions (A) in the buffer layer (110) except for the portion of the buffer layer (110) on which the semiconductor layer (120) is formed,
   wherein when the polysilicon layer is patterned to form the semiconductor layer (120),
   grain boundaries on which metal silicides of the polysilicon layer crystallized by the metal catalyst gather and a seed region are not completely removed from the surface of the etched buffer layer and remain as said protrusions (A).

2. The method of claim further comprising:

   forming a gate insulating layer (130) on the substrate (100) to cover the semiconductor layer (120);
   forming a gate electrode (140) on the gate insulating layer (130) to face a predetermined region of the semiconductor layer (120);
   forming a first capacitor electrode (145) on the gate insulating layer (130) in the capacitor region (b);
   forming an interlayer insulating layer (150) on the substrate (100) to cover the gate electrode (140) and the first capacitor electrode (145);
   forming source and drain electrodes (160a,160b) on the interlayer insulating layer (150) which are electrically connected to the semiconductor layer (120);
   forming a second capacitor electrode (163) on the interlayer insulating layer (150) to face the first capacitor electrode (145);
   forming a first electrode (180) on the interlayer insulating layer (150), the first electrode (180) being electrically connected to one of the source and drain regions of the semiconductor layer (120);
   forming an organic layer (190) on the first electrode (180), the organic layer (190) including a light emitting layer; and
   forming a second electrode (195) on the organic layer (190).

3. The method of claim 1 or 2, further comprising:

   forming a diffusion layer (123) to control the diffusion of a metal catalyst on the amorphous silicon layer (120a) and forming the metal catalyst layer (125) on the diffusion layer (123),

   wherein the annealing is performed after the forming of the metal catalyst layer (125).

4. The method of claim 3, wherein the first capacitor electrode (145) and the gate electrode (140) are formed by simultaneous patterning.

5. The method of claim 3, wherein the second capacitor electrode (163) and the source and drain electrodes (160a,160b) are formed by simultaneous patterning.

Patentansprüche

1. Verfahren zur Herstellung einer Anzeigevorrichtung mit organischer lichtemittierender Diode (OLED), wobei das Verfahren Folgendes umfasst:

   Ausbilden eines Substrats (100), das einen Dünnschichttransistorbereich (a) und einen Kondensatorbereich (b) aufweist;
   Ausbilden einer Pufferschicht (110) auf dem Substrat (100);
   Ausbilden von Ausbuchtungen (A) in der Pufferschicht (110);
   Ausbilden eines Kondensators (145, 150, 163) auf der Pufferschicht (110) in dem Kondensatorbereich (b), wobei der Kondensator (145, 150, 163) der Form der Ausbuchtungen (A) der Pufferschicht (110) folgt; und
   dadurch gekennzeichnet, dass der Schritt des Ausbildens von Ausbuchtungen (A) in der Pufferschicht (110) Folgendes umfasst:

Ausbilden einer amorphen Siliciumschicht (120a) auf der Pufferschicht (110); Ausbilden einer Metallkatalysatorschicht (125) auf der amorphen Siliciumschicht (120a);
Ausglühen des Substrats (100), um die amorphe Siliciumschicht (120a) zu einer Polysiliciumschicht zu kristallisieren;
Entfernen der Metallkatalysatorschicht (125); und
Strukturieren der Polysiliciumschicht, um eine Halbleiterschicht (120) auszubilden, die auf der Pufferschicht (110) in dem Dünnschichttransistorbereich (a) angeordnet ist; und Ausbilden der Ausbuchtungen (A) in der Pufferschicht (110) mit Ausnahme des Abschnitts der Pufferschicht (110), auf dem die Halbleiterschicht (120) ausgebildet ist, wobei, wenn die
Polysiliciumschicht strukturiert wird, um die Halbleiterschicht (120) auszubilden, Korngrenzen, auf denen sich Metallsilicide der Polysiliciumschicht, kristallisiert durch den Metallkatalysator, ansammeln, und ein Keimlingsbereich nicht vollständig von der Oberfläche der
geätzten Pufferschicht entfernt werden und als die Ausbuchtungen (A) verbleiben.

2. Verfahren nach Anspruch 1, das ferner Folgendes umfasst:

Ausbilden einer Gateisolierschicht (130) auf dem Substrat (100), um die Halbleiterschicht (120) abzudecken;
Ausbilden einer Gateelektrode (140) auf der Gateisolierschicht (130), die einem vorbestimmten Bereich der Halbleiterschicht (120) zugewandt ist;
Ausbilden einer ersten Kondensatorelektrode (145) auf der Gateisolierschicht (130) in dem Kondensatorbereich (b);
Ausbilden einer Zwischenschicht-Isolierschicht (150) auf dem Substrat (100), um die Gateelektrode (140) und die erste Kondensatorelektrode (145) abzudecken;
Ausbilden von Source- und Drainelektroden (160a, 160b) auf der Zwischenschicht-Isolierschicht (150), die mit der Halbleiterschicht (120) elektrisch verbunden sind;
Ausbilden einer zweiten Kondensatorelektrode (163) auf der Zwischenschicht-Isolierschicht (150), die der ersten Kondensatorelektrode zugewandt ist (145);
Ausbilden einer ersten Elektrode (180) auf der Zwischenschicht-Isolierschicht (150), wobei die erste Elektrode (180) mit einem des Source- und Drainbereichs der Halbleiterschicht (120) elektrisch verbunden ist;
Ausbilden einer organischen Schicht (190) auf der ersten Elektrode (180), wobei die organische Schicht (190) eine lichtemittierende Schicht umfasst; und
Ausbilden einer zweiten Elektrode (195) auf der organischen Schicht (190).

3. Verfahren nach Anspruch 1 oder 2, das ferner Folgendes umfasst:

Ausbilden einer Diffusionsschicht (123), um die Diffusion eines Metallkatalysators auf der amorphen Siliciumschicht (120a) zu steuern und die Metallkatalysatorschicht (125) auf der Diffusionsschicht (123) auszubilden,
wobei das Ausglühen nach dem Ausbilden der Metallkatalysatorschicht (125) durchgeführt wird.

4. Verfahren nach Anspruch 3, wobei die erste Kondensatorelektrode (145) und die Gateelektrode (140) durch gleichzeitiges Strukturieren ausgebildet werden.

5. Verfahren nach Anspruch 3, wobei die zweite Kondensatorelektrode (163) und die Source- und Drainelektroden (160a, 160b) durch gleichzeitiges Strukturieren ausgebildet werden.

Revendications

1. Procédé de fabrication d'un dispositif d'affichage à diodes électroluminescentes organiques (OLED), le procédé comprenant :

la formation d'un substrat (100) ayant une région de transistor à couches minces (a) et une région de condensateur (b) ;
la formation d'une couche tampon (110) sur le substrat (100) ;
la formation de protubérances (A) dans la couche tampon (110) ;
la formation d'un condensateur (145, 150, 163) sur la couche tampon (110) dans la région de condensateur (b), où le condensateur (145, 150, 163) suit la forme des protubérances (A) de la couche tampon (110) ; et
caractérisé en ce que l'étape de formation de protubérances (A) dans la couche tampon (110) comprend :

la formation d'une couche de silicium amorphe (120a) sur la couche tampon (110) ;
la formation d'une couche de catalyseur métallique (125) sur la couche de silicium amorphe (120a) ;
le recuit du substrat (100) pour cristalliser

la couche de silicium amorphe (120a) en une couche de polysilicium ;
le retrait de la couche de catalyseur métallique (125) ; et
le modélisation de la couche de polysilicium pour former une couche semi-conductrice (120) disposée sur la couche tampon (110) dans la région de transistor à couches minces (a) ; et
la formation des protubérances (A) dans la couche tampon (110) à l'exception de la partie de la couche tampon (110) sur laquelle est formée la couche semi-conductrice (120),
dans lequel, lorsque la couche de polysilicium est modelisée pour former la couche semi-conductrice (120), des joints de grain sur lesquels des siliciures métalliques de la couche de polysilicium cristallisée par le catalyseur métallique se rassemblent et une région de germe ne sont pas complètement retirés de la surface de la couche tampon gravée et restent sous la forme desdites protubérances (A).

2. Procédé de la revendication 1, comprenant en outre :

la formation d'une couche d'isolation de grille (130) sur le substrat (100) pour couvrir la couche semi-conductrice (120) ;
la formation d'une électrode de grille (140) sur la couche d'isolation de grille (130) pour faire face à une région prédéterminée de la couche semi-conductrice (120) ;
la formation d'une première électrode de condensateur (145) sur la couche d'isolation de grille (130) dans la région de condensateur (b) ;
la formation d'une couche isolante intermédiaire (150) sur le substrat (100) pour couvrir l'électrode de grille (140) et la première électrode de condensateur (145) ;
la formation d'électrodes de source et de drain (160a, 160b) sur la couche isolante intermédiaire (150) qui sont électriquement reliées à la couche semi-conductrice (120) ;
la formation d'une deuxième électrode de condensateur (163) sur la couche isolante intermédiaire (150) pour faire face à la première électrode de condensateur (145) ;
la formation d'une première électrode (180) sur la couche isolante intermédiaire (150), la première électrode (180) étant électriquement reliée à l'une des régions de source et de drain de la couche semi-conductrice (120) ;
la formation d'une couche organique (190) sur la première électrode (180), la couche organique (190) comportant une couche électroluminescente ; et
la formation d'une deuxième électrode (195) sur la couche organique (190).

3. Procédé de la revendication 1 ou 2, comprenant en outre :

la formation d'une couche de diffusion (123) pour commander la diffusion d'un catalyseur métallique sur la couche de silicium amorphe (120a) et la formation de la couche de catalyseur métallique (125) sur la couche de diffusion (123),
où le recuit est effectué après la formation de la couche de catalyseur métallique (125).

4. Procédé de la revendication 3, dans lequel la première électrode de condensateur (145) et l'électrode de grille (140) sont formées par une modélisation simultanée.

5. Procédé de la revendication 3, dans lequel la deuxième électrode de condensateur (163) et les électrodes de source et de drain (160a, 160b) sont formées par une modélisation simultanée.

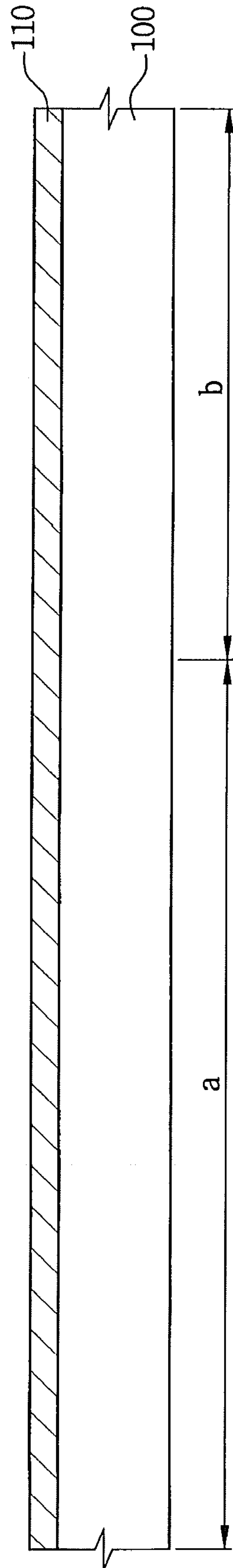


FIG. 1A

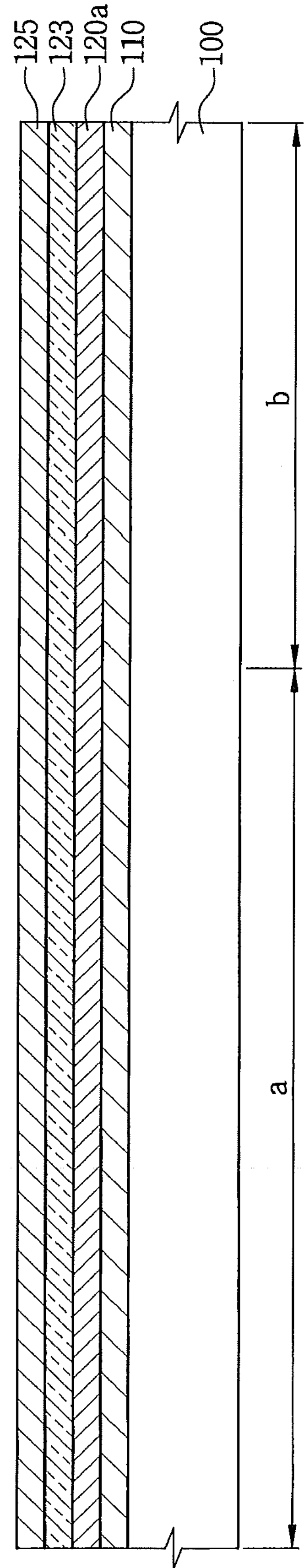


FIG. 1B

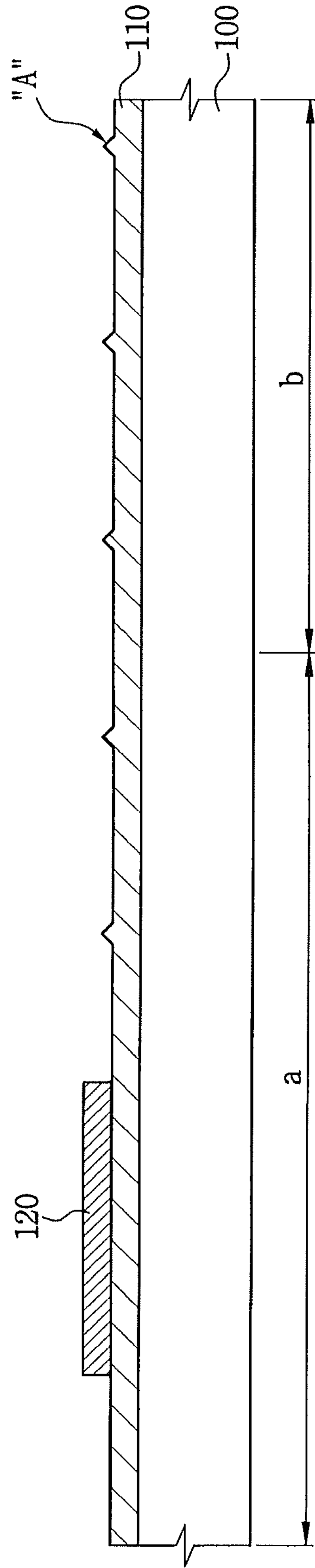


FIG. 1C
"A"
110
100
120
a
b

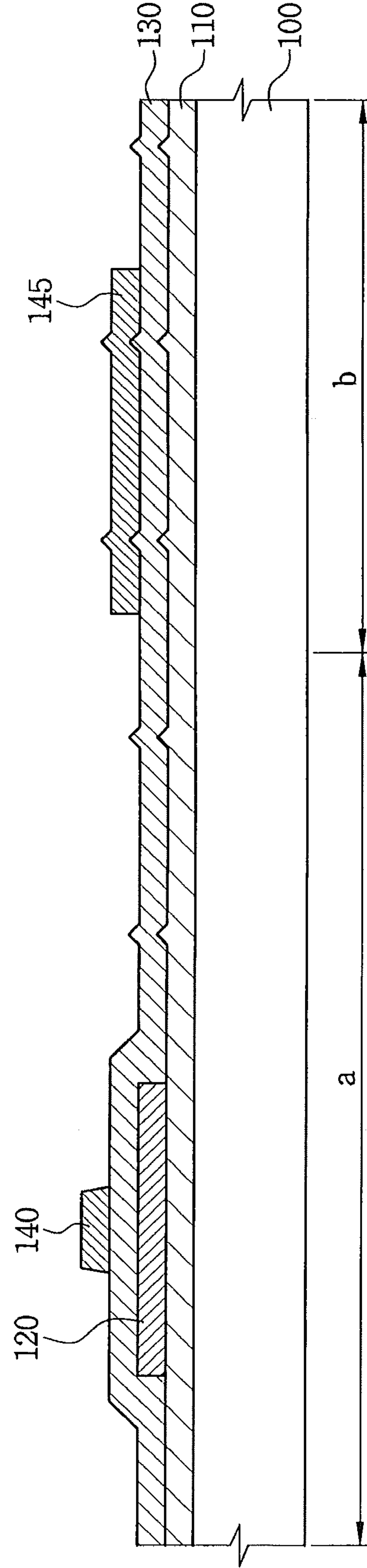
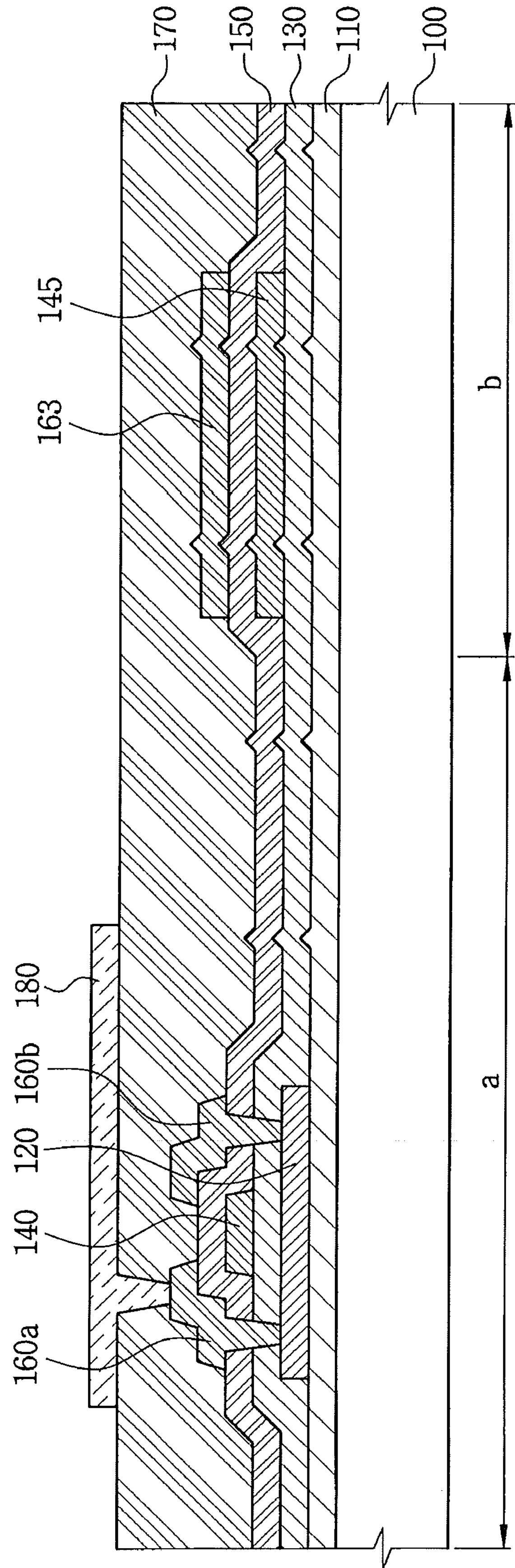


FIG. 1D
130
110
100
145
140
120
a
b

FIG. 1E

FIG. 1F



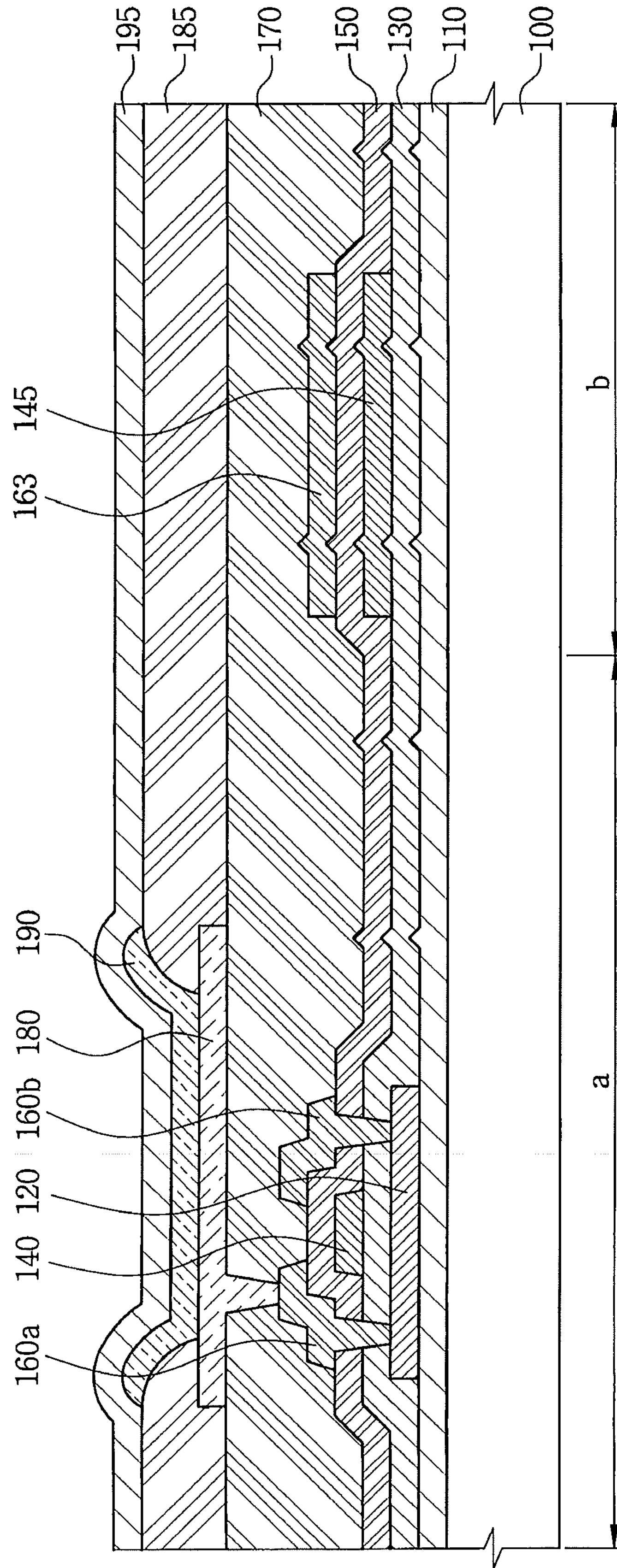
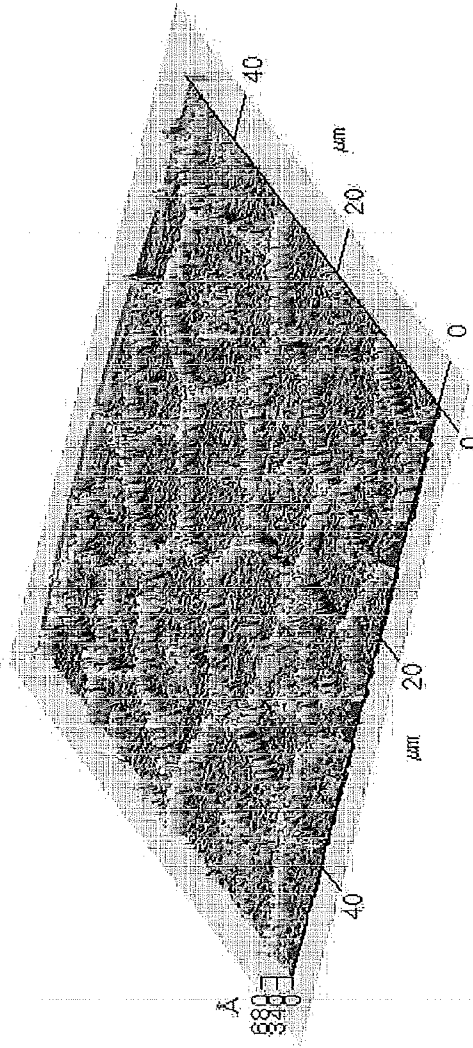


FIG. 1G

FIG.2



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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patsnap

专利名称(译)	制造有机发光二极管显示装置的方法		
公开(公告)号	EP2226845B1	公开(公告)日	2018-04-11
申请号	EP2010154502	申请日	2010-02-24
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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发明人	PARK, BYOUNG-KEON YANG, TAE-HOON SEO, JIN-WOOK JO, SOO-BEOM LEE, DONG-HYUN LEE, KIL-WON LISACHENKO, MAXIM CHUNG, YUN-MO CHOI, BO-KYUNG PARK, JONG-RYUK LEE, KI-YONG		
IPC分类号	H01L27/32		
CPC分类号	H01L27/3265 H01L2227/323 H01L51/52		
优先权	1020090018200 2009-03-03 KR		
其他公开文献	EP2226845A2 EP2226845A3		
外部链接	Espacenet		

摘要(译)

提供了一种有机发光二极管（OLED）显示装置及其制造方法。OLED显示装置包括具有薄膜晶体管区域和电容器区域的衬底，设置在衬底上的缓冲层，设置在衬底上的栅极绝缘层，设置在电容器区域中的栅极绝缘层上的下电容器电极，设置在所述基板上的层间绝缘层以及设置在所述层间绝缘层上并且面向所述下电容器电极的上电容器电极，其中，所述缓冲层，所述栅绝缘层，所述层间绝缘层，所述下电容器电极以及上部电容器电极具有其中形成具有与半导体层的晶界相同的形状的突起的表面。所得到的电容器具有增加的表面积，并且因此增加了电容。

FIG.1A

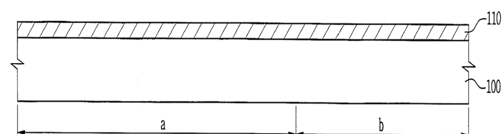

FIG.1B