

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
17 August 2006 (17.08.2006)

PCT

(10) International Publication Number
WO 2006/084360 A1

(51) International Patent Classification:
H05B 33/08 (2006.01) **G09G 3/32** (2006.01)
H01L 51/50 (2006.01)

(74) Agents: **HARRIS, John, D.** et al.; Gowling Lafleur Henderson LLP, 160 Elgin Street, Suite 2600, Ottawa, Ontario K1P 1C3 (CA).

(21) International Application Number:
PCT/CA2006/000177

(22) International Filing Date: 9 February 2006 (09.02.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2,496,642 10 February 2005 (10.02.2005) CA

(71) Applicant (for all designated States except US): **IGNIS INNOVATION INC.** [CA/CA]; 55 Culpepper Drive, Waterloo, Ontario N2L 5K8 (CA).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **NATHAN, Arokia** [CA/CA]; c/o Ignis Innovation Inc., 55 Culpepper Drive, Waterloo, Ontario N2L 5K8 (CA). **CHAJI, Reza, G.** [CA/CA]; 507-196 Westmount Rd. N., Waterloo, Ontario N2L 3G5 (CA).

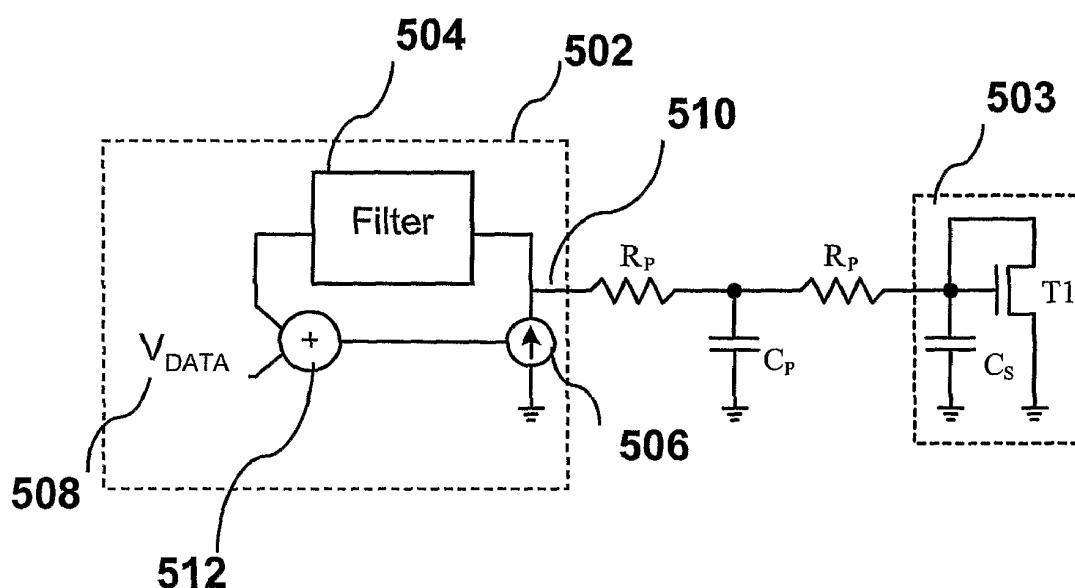
(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— with international search report

[Continued on next page]

(54) Title: DRIVING CIRCUIT FOR CURRENT PROGRAMMED ORGANIC LIGHT-EMITTING DIODE DISPLAYS



(57) Abstract: A load driving circuit for a load having a parasitic capacitance associated therewith is provided. The load being current programmed. The driving circuit has a data line having a voltage controlling the load, a feedback loop having a lowpass filter for monitoring the voltage of the data line; and a current source for providing a current to the data line; the current source being controlled by a signal line and an output from the lowpass filter.

WO 2006/084360 A1



For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Driving Circuit for Current Programmed Organic Light-Emitting Diode Displays

FIELD OF INVENTION

[0001] The present invention relates to methods and apparatus for driving a current line with a parasitic capacitance. In particular, the present invention relates to methods and apparatus for driving organic light-emitting diode (OLED) displays that are current programmed.

BACKGROUND OF THE INVENTION

[0002] Maturing of Flat Panel Display (FPD) technologies has provided larger and lower cost laptop monitors, small area/low power panels for cell phones and other portable devices, HDTV and widescreen formats for home television, and high reliability daylight readable displays for "glass cockpits" for aircraft.

[0003] Emerging technologies such as organic LEDs (OLED) promise to deliver higher quality emissive flat displays, allowing the removal of the backlight. When compared to LCDs, a thinner form-factor with almost perfect viewing angle and much faster response speed would be provided by OLEDs. Thus the intrinsic characteristics of OLEDs give visual and form factor advantages over LCDs.

[0004] A typical array structure of an active matrix organic light-emitting diode (AMOLED) is shown in Figure 1. The display 100 includes an array of pixels 102 that are arranged in rows and columns. The pixels 102 are connected to the data line 106 via a select transistor 104. The transistor 104 is a thin film transistor (TFT). The data line 106 is driven by a current source 108. The overlap capacitance of the transistors 104 connected to data line 106 and the line capacitance of the data line 106 itself leads to a high parasitic capacitance.

[0005] The basic OLED structure for a given pixel 102 consists of a stack of thin organic layers between a transparent anode and a metallic cathode. The organic layers include a hole-injection layer, a hole-transport layer, an emissive layer, and an electron transport layer. When an appropriate voltage is applied to the structure the injected positive and negative charges combine in the emissive layer to product light. OLEDs are therefore self-emissive displays and thus do not

require a backlight as is required by LCDs. Also the charge combination process causes very little time delay providing for a fast response time.

[0006] OLED displays are current-controlled display devices. LCDs, on the other hand, are voltage-controlled. Current programming provides the OLED with a current that is independent of the characteristics of any other components such as thin film transistors (TFT) or the OLED itself, and compensates for V_t shift, spatial mismatch, and OLED degradation. However, the parasitic capacitance contributed from the line and select transistors connected to the line results in a large settling time. The settling time is a function of the initial line voltage and threshold voltage of the drive TFT. Although, the settling time can be improved partially by pre-charging, the improvement is not sufficient for medium and large area displays.

[0007] The parasitic capacitance of the drive transistor and the data line to which it is connected is schematically shown in Figure 2. In particular Figure 2 schematically shows the equivalent circuit for a current programmed pixel 202, having a current source 203 and a transistor 204, during a programming cycle. Capacitance C_p 210 and resistance R_p 208 are the parasitic components while capacitance C_s 206 is the capacitance of the storage capacitor. If C_s 206 \ll C_p 210 and R_p 208 is small, the timing constant, or settling time, of the circuit shown in Figure 2 is:

$$[0008] \tau \propto 2 \frac{C_p}{\sqrt{I} * \beta} \quad (1)$$

[0009] where β is the coefficient in current-voltage (I-V) characteristics of the transistor 204 given by $I_{ds} = \beta (V_{gs} - V_{th})^2$. Here, I_{ds} is the drain-source current, V_{gs} the gate-source voltage, and V_{th} the threshold voltage.

[0010] If the capacitance C_p 210 is a large capacitance, around 40pf, and β is small for the transistor 204, which is fabricated with amorphous silicon (a-Si), τ is of the order of millisecond. However, the timing budget of the programming cycle is less than 100 μ s for large area displays. Since the efficiency of the OLED has been increased, the amount of current required to

achieve the maximum brightness is very small; therefore, τ , which is also a function of current, increases dramatically.

[0011] This parasitic capacitance thus contributes to a high settling time for current programmed pixels, limiting the timing budget of the programming cycle. This can cause considerable error due to imperfect settling. In order to remove this error, a simple and fast solution for driving the current programmed pixels that is suitable for applications in OLED displays is needed.

[0012] United States patent application No. 20040095297A1 to Libsch et al. describes a programming method in which the programming current is controlled by a current sensor. A schematic diagram of the circuit of Figure 1 of Libsch et al. is shown in Figure 3. During the programming cycle a current sensor 302 monitors the voltage across resistor R 304 through the feedback 308. The current sensor 302 controls the programming current. After the pixel settles, the current flowing through the resistor R 304 and the OLED 306 is the same as wanted current. Because of the use of feedback 308, this driving method has a fast settling time. However, the drawback of this circuit is that it has a high power consumption resulting from resistor R 304. The resistor R 304 should quite large such that the circuit is able to sense a low current level accurately. Therefore, the power dissipated in resistor R 304 is considerable. The other drawback of this circuit is that it suffers from mismatch. The spatial mismatch changes the value of resistor R 304 causing non-uniformity in the display. It also has the addition feedback 308.

[0013] United States Patent 6,433,488 to Bu discloses an OLED driver circuit that implements a current comparator in a feedback loop. The circuit presented in Figure 2 of Bu is schematically presented in Figure 4. In a programming cycle, SCAN is high so the transistor T2 402 is off and the transistor T4 404 is on. Therefore, the current flows through the transistor T3 406, the OLED 408, and the transistor T1 410. A current comparator 412 defines the reference voltage 414 based on comparison result of the pixel current, via feedback line 416, and reference current 418. After the pixel settles, the pixel current 416 is the same as reference current 418. This circuit provides a fast settling time for the pixel because of the use of feedback. However, the circuit has a high

power compensation because of the two transistors (T1 410 and T2 402) in the path of current during the driving cycle, further this method uses four transistors and extra feedback line 416.

[0014] Therefore there is a need for a circuit that improves the settling time of the current driven circuit that does not encounter the high power consumption of the known circuits.

SUMMARY OF THE INVENTION

[0015] The present invention relates to a circuit for driving an OLED pixel. The invention further relates to a circuit that enables the use of current programmed pixel circuits in large area displays by improving the settling time.

[0016] It is an object of the invention to obviate or mitigate at least one shortcoming of circuits for improving time sensitivity of the prior art.

[0017] In accordance with one aspect of the invention a load driving circuit for a load having a parasitic capacitance associated therewith and being current programmed is provided. The driving circuit having a data line having a voltage controlling the load, a feedback loop having a lowpass filter for monitoring the voltage of the data line, and a current source for providing a current to the data line; the current source being controlled by a signal line and an output from the lowpass filter.

[0018] In accordance with another aspect of the invention a driving circuit for a light emitting diode that is current programmed and having a parasitic capacitance is provided. The driving circuit having a data line controlling the light emitting diode, a low pass filter monitoring the voltage of the data line, and a current source for providing a current to the data line; the current source being controlled by a signal line and an output from the lowpass filter.

[0019] In accordance with another aspect of the invention a driving circuit for a light emitting diode that is current programmed and having a parasitic capacitance is provided. The driving circuit comprising a data line controlling the light emitting diode, a feedback loop comprising, an analogue to digital

converter, and a controller running an algorithm that provides low pass filter functionality to the feedback loop, and a current source for providing a current to the data line; the current source receiving input from a digital to analogue converter that receives input from the controller.

5 [0020] In accordance with another aspect of the invention a method of driving a light emitting diode in a display, the light emitting diode having a parasitic capacitance and being current programmed is provided. The method comprising the steps of providing a current to the light emitting diode, the current being provided by a current source, monitoring a voltage of a data line
10 providing the current to the light emitting diode with a low pass filter, and mixing the voltage and a data line signal to form an input, providing the input to the current source.

[0021] This summary of the invention does not necessarily describe all features of the invention.

15 BRIEF DESCRIPTION OF THE DRAWINGS

[0022] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

20 [0023] FIGURE 1 presents a schematic diagram of a pixel array according of the prior art;

[0024] FIGURE 2 presents a schematic diagram of parasitics associated with a pixel of an OLED based display of the prior art;

[0025] FIGURE 3 presents a schematic diagram of pixel programming circuit of the prior art;

25 [0026] FIGURE 4 presents a schematic diagram of another pixel programming circuit of the prior art;

[0027] FIGURE 5 presents a schematic diagram of a display drive circuit having a feedback circuit in accordance with an embodiment of the invention;

[0028] FIGURE 6 presents a schematic diagram of a display drive circuit having a feedback circuit in accordance with another embodiment of the invention;

[0029] FIGURE 7 presents a schematic diagram of a display drive circuit having a bandpass filter in accordance with another embodiment of the invention;

[0030] FIGURE 8a presents a schematic diagram of a bandpass filter in accordance with another embodiment of the invention;

[0031] FIGURE 8b presents a schematic diagram of a bandpass filter in accordance with another embodiment of the invention;

[0032] FIGURE 9 presents curves of settling time in accordance with another embodiment of the invention.

[0033] FIGURE 10a presents calculated noise when a high-pass filter is used in accordance with an embodiment of the invention; and

[0034] FIGURE 10b presents calculated noise when a low-pass filter is used in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

[0035] As outlined in the discussion of Figure 2, the settling of the time of the current can be larger than that allowed because of the parasitic capacitance. Embodiments of the invention consider the use of a feedback circuit to provide positive feedback to a current source. This feedback allows for an improvement in the settling time of the current allowing current driven displays to have the necessary response times.

[0036] A basic feedback circuit according to one embodiment of the invention is shown in Figure 5. A display drive circuit 502 is used to drive a light-emitting pixel 503. The drive circuit 502 includes a voltage controlled current source (VCCS) 506 and a feedback loop. Within this feedback loop is a filter 504 and a voltage adder 512. The current source 506 is controlled by V_{DATA} 508 and the output of the filter 504, which monitors the voltage of data line

510. The current source 506, filter 504, and voltage adder 512 are part of the display driver 502 that can be implemented as a separate chip using CMOS technology or as part of a display using on-display TFT technology.

[0037] In another embodiment of the invention, shown in Figure 6, the filter is implemented as a differentiator 602. If the parasitic resistances R_p 604 are small enough and the VCCS 606 is a linear current source, the timing constant for the circuit shown in FIG. 6 is:

$$[0038] \tau \propto 2 \frac{(C_p - K)}{\sqrt{i^* \beta}} \quad (3)$$

[0039] Here 'i' is the current related to V_{DATA} 608. K is the coefficient of the differentiator 602 and should be selected close to the parasitic capacitance C_p 610 in order to achieve the desirable results. However, a reasonable difference between K and C_p has no significant effect on the settling time.

[0040] The circuit of Figure 6 can remove the effect of parasitic capacitance 610 and as a result can be used for fast programming of current programmed pixel 612, which is a general schematic that represent functionality of current programmed pixels. It will be apparent to one of skill in the art that the circuit of Figure 6 can be used with any current-programmed pixel circuits.

[0041] A filter circuit according to the currently preferred embodiment is shown in Figure 7. In this embodiment the display drive circuit 702 uses a bandpass (BP) filter 704 for the feedback function. The drive circuit 702 drives the pixel 703 and manages the effect of parasitic capacitance C_p 706 through the use of positive feedback. At the beginning of the programming cycle, the voltage of the line 708 changes rapidly, and so the VCCS 710 pumps more current into current line 708. As the voltage of the current line 708 settles, the current supplied by the current source 710 goes to a programming current. Also, the band-pass filter 704 mitigates high-frequency noise of the current line 708, which would otherwise influence the output current of the current source 710.

[0042] Figure 8a presents further detail of the bandpass filter used in display drive circuit 702. A simple filter circuit has been used such that the circuit fits

within the pixel pitch of approximately 100 μm . The bandpass filter of Figure 8A is generally indicated as 803 is implemented as a one-pole lowpass Butterworth filter and a differentiator. In the circuit of Figure 8a a current conveyer type II (CCII) is used for realization of the driver. The Z terminal 808 is connected directly to the Y terminal 806. Therefore, the voltage of node X 804 follows the voltage of the Z terminal 808 due to a feedback between the Y terminal 806 and the X terminal 804. Also, the capacitor C_{PL} 810 acts as a low pass filter and mitigates any high frequency noise. The capacitor C_F 812, on the other hand, differentiates the voltage at the X terminal 804, which is equal to the voltage of the line and converts it to a current. The current mirror duplicates this current and adds it to the programming current.

[0043] Another implementation of the lowpass filter that uses a digital implementation is presented in Figure 8b. In this Figure the drive circuit 819 is used to drive pixel 825. The voltage of the line 820 is read back by an ADC 822. The controller 824 block runs an algorithm and changes the current of the current source 826 using the DAC 828. An important aspect of the algorithm run by the controller 824 is the calculation of the difference between the current sample $V[n]$ and the previous sample $V[n-1]$. With a consideration to this difference the algorithm adjusts the current provided by the current source 826 to speed up the programming.

[0044] An analysis of the settling time associated with the circuit of Figure 8a is shown in Figure 9. A MATLABTM model was used to investigate the characteristics of the new current source. To simplify the analysis, the cut-off frequency of the LP filter is considered to be high. Thus, the overdrive voltage of T1 can be written as:

$$[0045] I_P \doteq (C_P - C_F) \frac{d}{dt} V - V^2 \quad (3)$$

[0046] where, V is the overdrive voltage of T1, and C_F the gain of differentiator. It is evident that C_F can compensate for the parasitic capacitance.

[0047] In Figure 9 the settling time of the current source 702 that implements a LP filter is less than 40 μ s whereas it is 400 μ s for the conventional case i.e. the current is provided by the current source with no feedback. It is also evident that increasing the cut-off frequency of the low pass filter makes the driver more sensitive to the noise of the current line. There is however an increase in the speed as the cut-off frequency increases.

[0048] Figure 10a presents a graph of pixel current over time during the programming cycle when a differentiator or high-pass filter is used. The noise of the line is fed back to the current through the differentiator. This causes the noise to be amplified. Moreover, it can make the driver unstable since the differentiator is highly sensitive to high frequency signals. As is apparent from this graph the noise of the line is amplified and destroys the signal. Figure 10b presents a graph of pixel current over time during the programming cycle when a low-pass filter is used. The reduced noise is readily apparent when Figure 10b is compared to Figure 10a.

[0049] The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

WHAT IS CLAIMED IS:

1. A load driving circuit for a load having a parasitic capacitance associated therewith and being current programmed, the driving circuit comprising:

a data line having a voltage controlling the load;

5 a feedback loop having a lowpass filter for monitoring the voltage of the data line; and

a current source for providing a current to the data line; the current source being controlled by a signal line and an output from the lowpass filter.

10 2. The load driving circuit according with claim 1 wherein the lowpass filter comprises a so-called Butterworth filter and a differentiator.

3. The load driving circuit according to claim 1 wherein the current source is a voltage controlled current source (VCCS).

4. A driving circuit for a light emitting diode that is current programmed and having a parasitic capacitance, the driving circuit comprising:

15 a data line controlling the light emitting diode;

a low pass filter monitoring the voltage of the data line; and

a current source for providing a current to the data line; the current source being controlled by a signal line and an output from the lowpass filter.

20 5. The driving circuit according with claim 4 wherein the lowpass filter comprises a so called Butterworth filter and a differentiator.

6. The driving circuit according to claim 4 wherein the current source is a voltage controlled current source (VCCS).

7. The driving circuit according to claim 4 wherein the light emitting diode is an organic light emitting diode.

8. The driving circuit according to claim 4, wherein an illumination of the light emitting diode is responsive to the current provided by the data line.

9. The driving circuit according to claim 4, wherein the light emitting diode is controlled by a thin film transistor.

5 10. A driving circuit for a light emitting diode that is current programmed and having a parasitic capacitance, the driving circuit comprising:

a data line controlling the light emitting diode;

a feedback loop comprising:

an analogue to digital converter; and

10 a controller running an algorithm that provides low pass filter functionality to the feedback loop; and

a current source for providing a current to the data line; the current source receiving input from a digital to analogue converter that receives input from the controller.

15 11. The driving circuit according to claim 10 wherein the current source is a voltage controlled current source (VCCS).

12. The driving circuit according to claim 10 wherein the light emitting diode is an organic light emitting diode.

20 13. A display having an array of pixels each including an organic light emitting diode wherein the diode is driven by a driving circuit according to claim 4.

~~14. A display having an array of pixels each including an organic light emitting diode wherein the diode is driven by a driving circuit according to claim 10.~~

25 15. A method of driving a light emitting diode in a display, the light emitting diode having a parasitic capacitance and being current programmed, the method comprising the steps of:

providing a current to the light emitting diode, the current being provided by a current source;

monitoring a voltage of a data line providing the current to the light emitting diode with a low pass filter; and

5 mixing the voltage and a data line signal to form an input;

providing the input to the current source.

16. The method according to claim 15, wherein the current source is a voltage controlled current source (VCCS).

10 17. The method according to claim 15, wherein the light emitting diode is an organic light emitting diode.

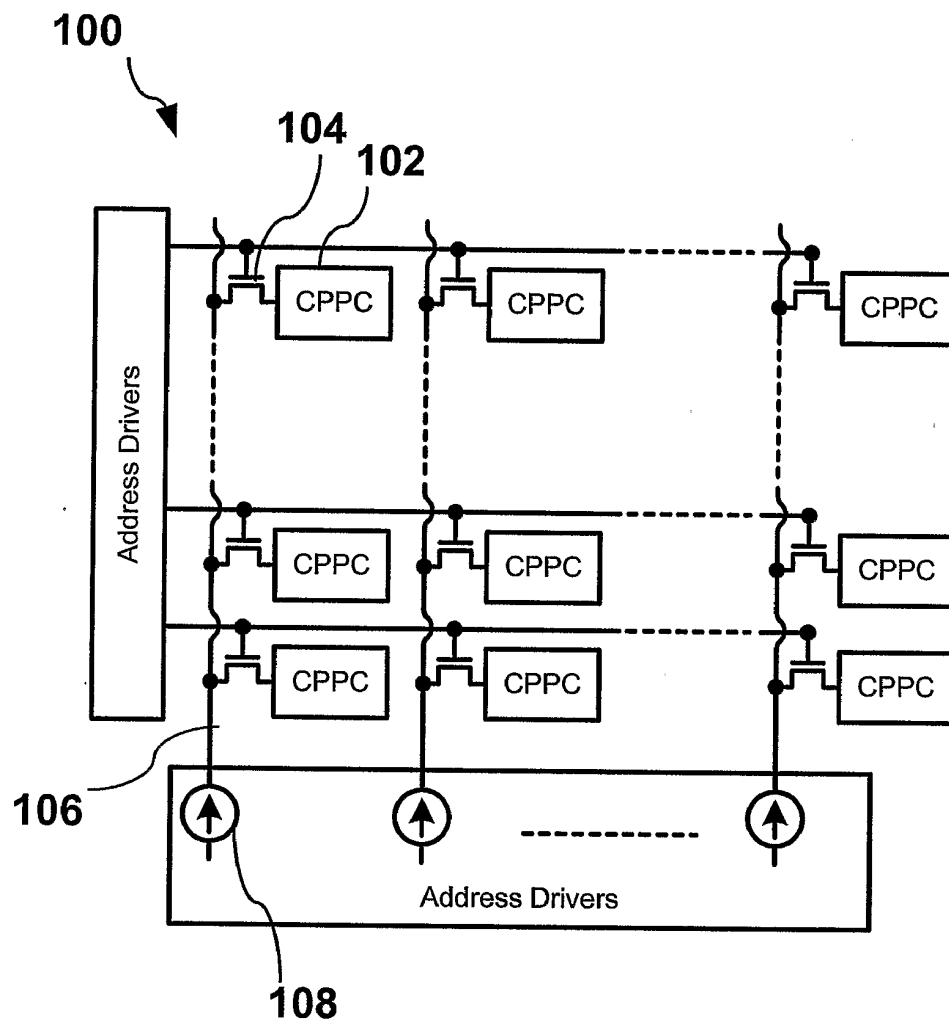


Figure 1

Prior Art

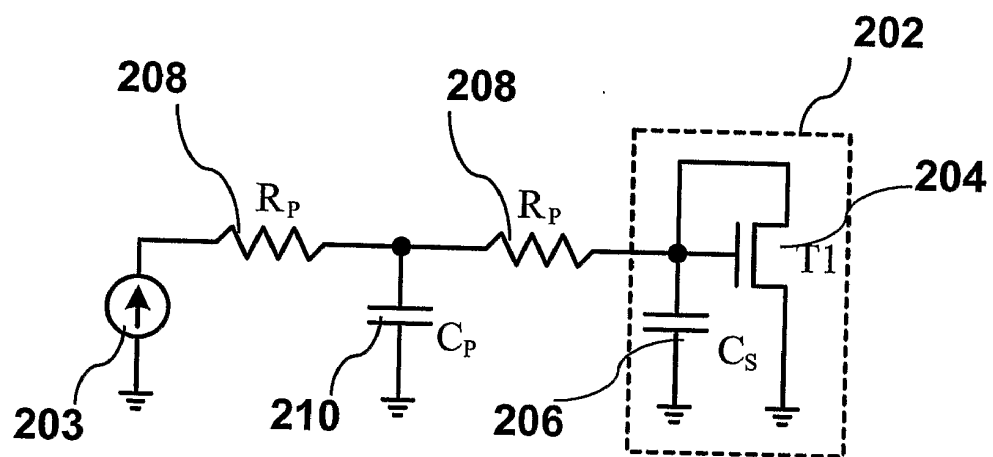


Figure 2
Prior Art
2/10

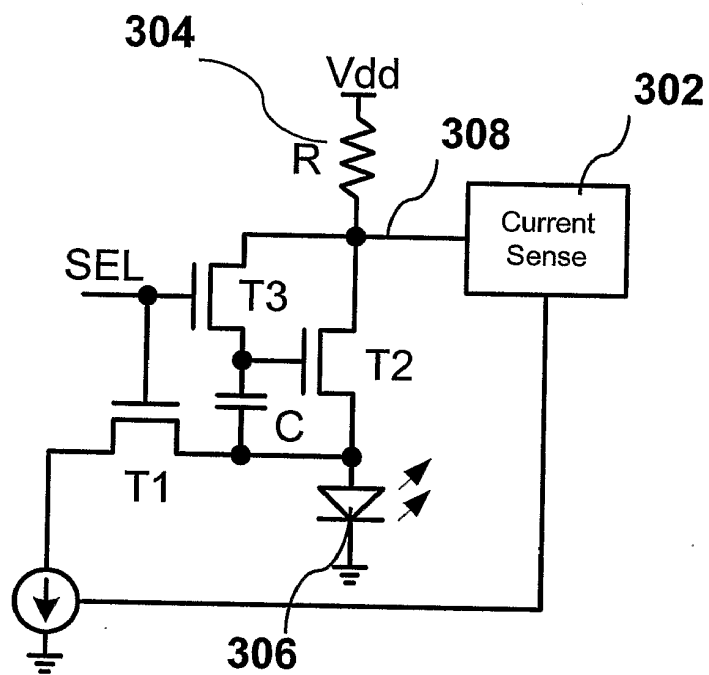


Figure 3

Prior Art

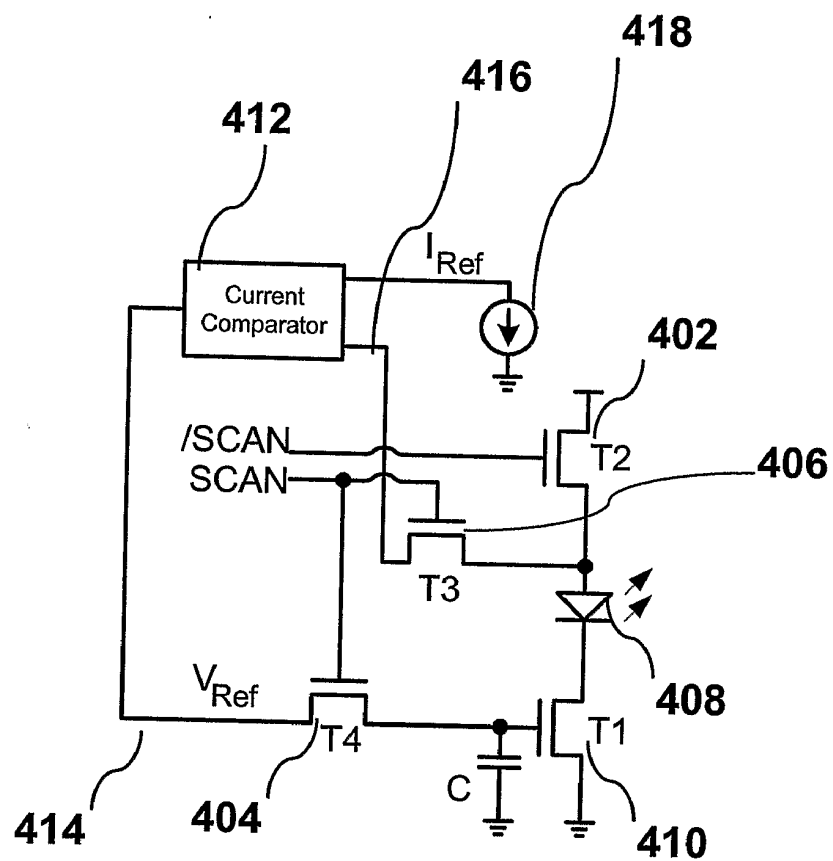


Figure 4

Prior Art

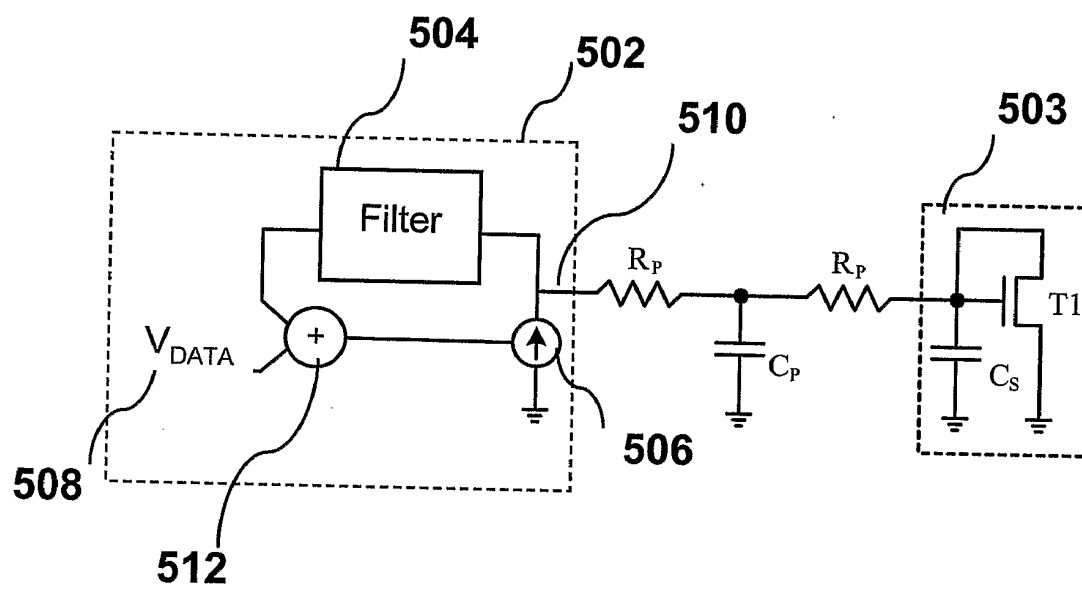


Figure 5

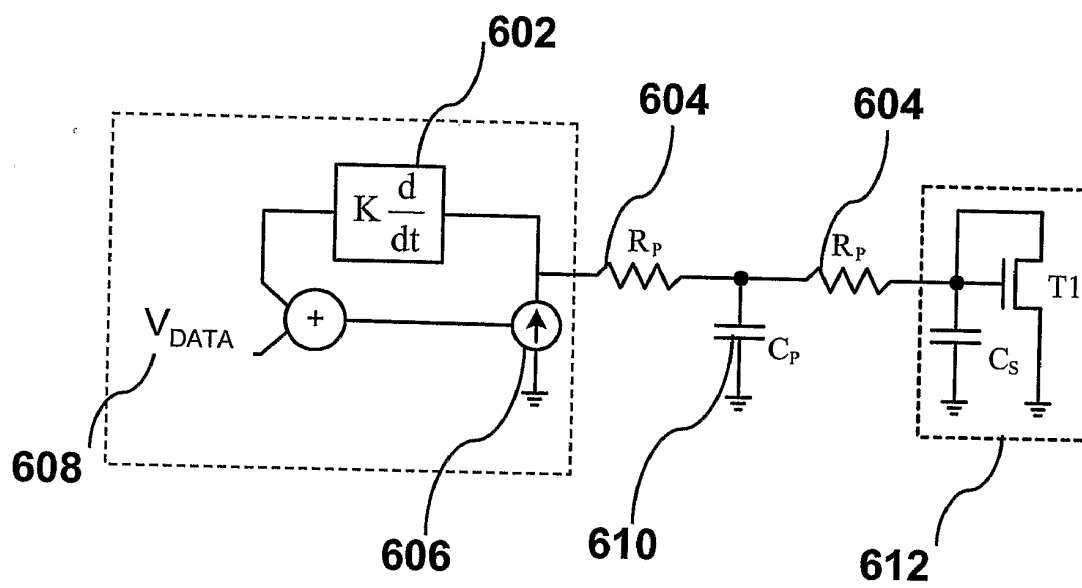


Figure 6

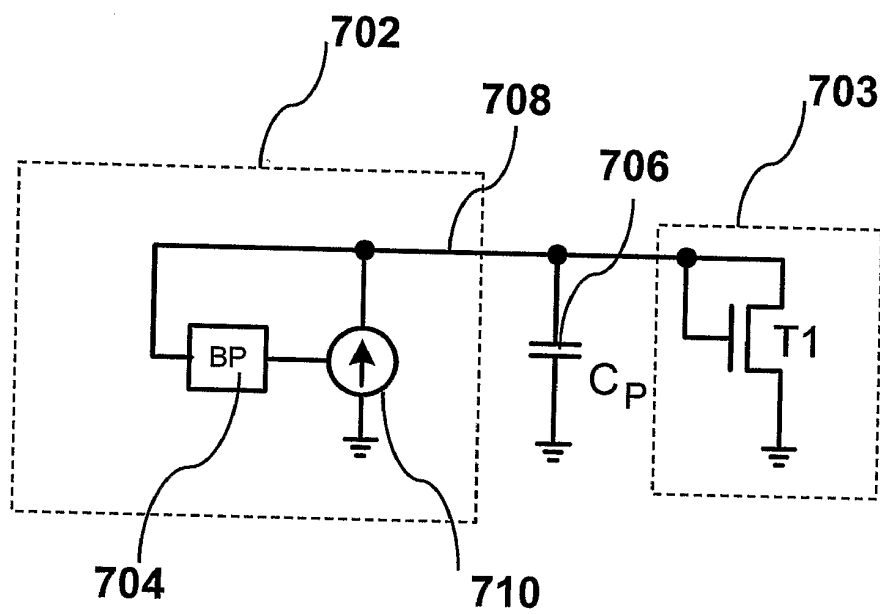


Figure 7

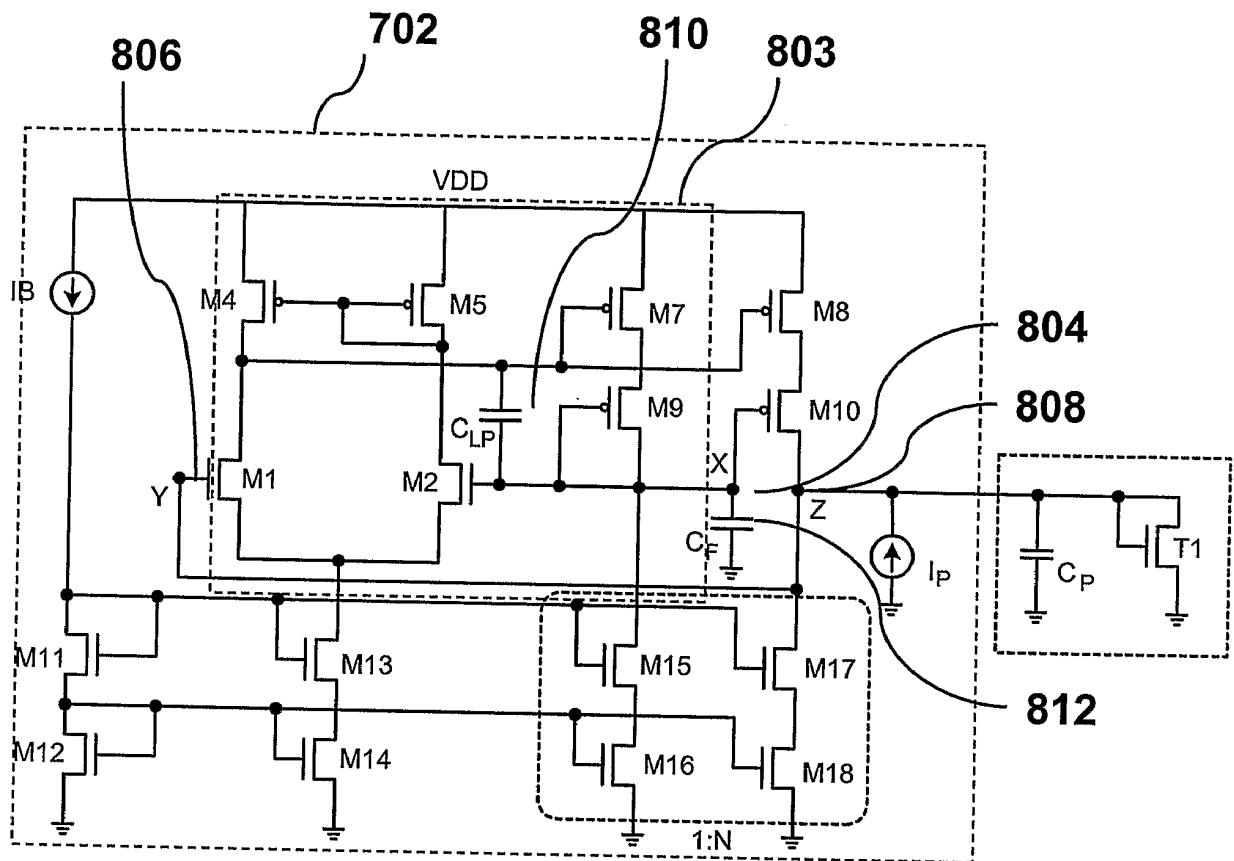


Figure 8a

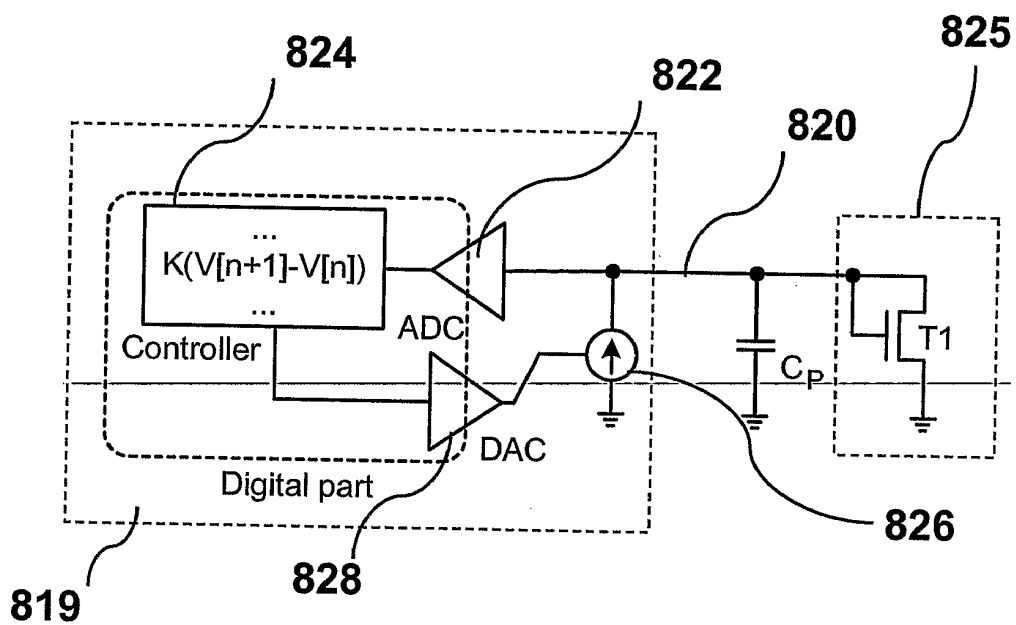


Figure 8b

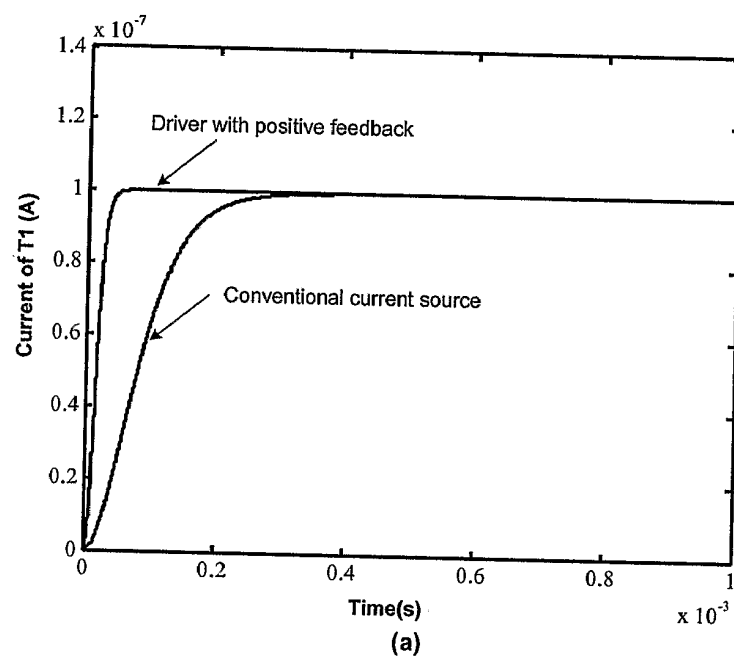


Figure 9

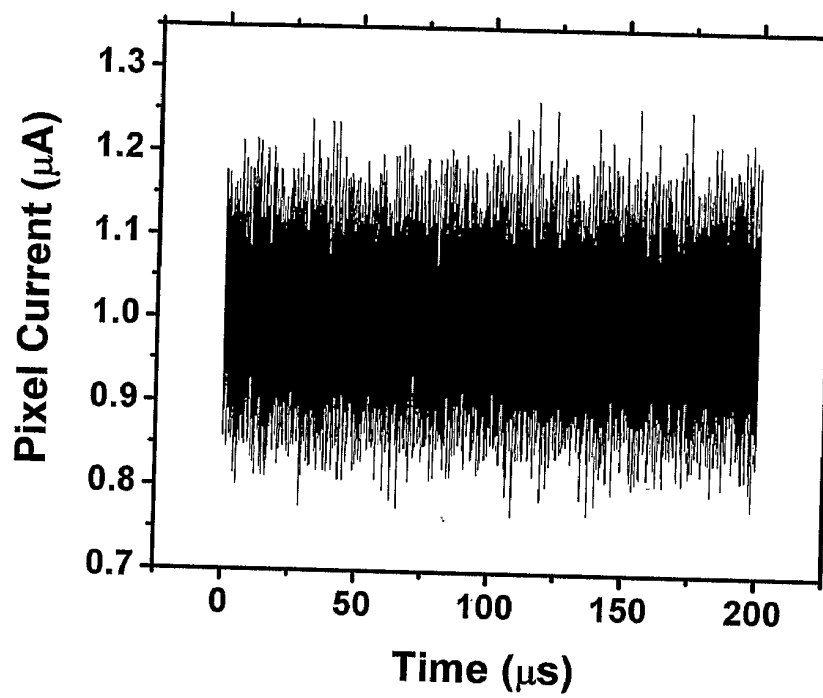


Figure 10a

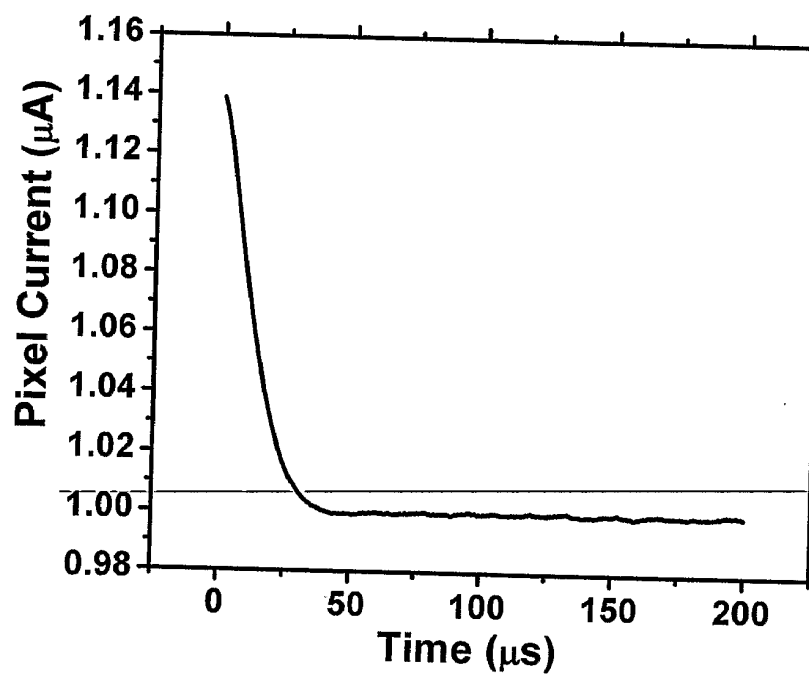


Figure 10b
10/10

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CA2006/000177

A. CLASSIFICATION OF SUBJECT MATTER

IPC: **H05B 33/08** (2006.01) , **H01L 51/50** (2006.01) , **G09G 3/32** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H05B33, H01L51, G09G3, H01L27

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic database(s) consulted during the international search (name of database(s) and, where practicable, search terms used)

Epodoc, Delphion, Canadian Patent Database. Terms used: led, oled, light emitting, organic, current program*, display, matrix, grid, array, settling time, timing constant, parasitic, capacitance, filter, feedback.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,X	US 2005/0068275 (Kane) 31 March 2005 (31-03-2005) whole document	1, 4, 10, 15
A	US 5,198,803 (Shie et al.) 30 March 1993 (30-03-1998) column 3, line 61 to column 4, line 26; figures 1A and 1B	1, 4, 10, 15
A	US 2003/0030603 (Shimoda) 13 February 2003 (13-02-2003) paragraphs 0037 to 0038; figure 4	1, 4, 10, 15

[] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E" earlier application or patent but published on or after the international filing date	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&" document member of the same patent family
"O" document referring to an oral disclosure, use, exhibition or other means	
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

31 May 2006 (31-05-2006)

Date of mailing of the international search report

2 June 2006 (02-06-2006)

Name and mailing address of the ISA/CA
Canadian Intellectual Property Office
Place du Portage I, C114 - 1st Floor, Box PCT
50 Victoria Street
Gatineau, Quebec K1A 0C9
Facsimile No.: 001(819)953-2476

Authorized officer

Andrew O'Malley (819) 953-5481

INTERNATIONAL SEARCH REPORT

Information on patent family members

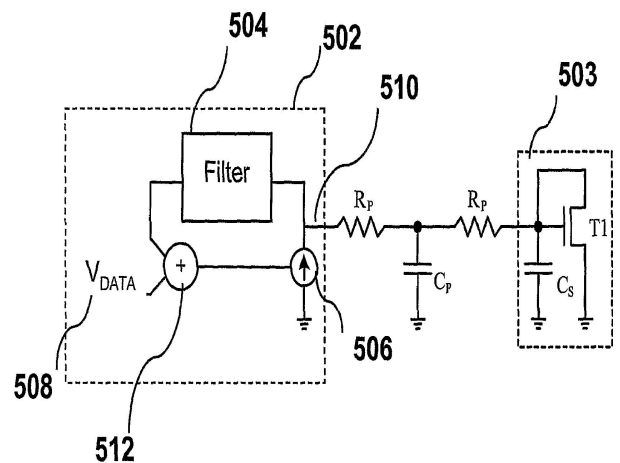
International application No.
PCT/CA2006/000177

Patent Document Cited in Search Report	Publication Date	Patent Family Member(s)	Publication Date
US2005068275	31-03-2005	US2005067971 A1	31-03-2005
US5198803	30-03-1993	NONE	
US2003030603	13-02-2003	JP2003058106 A	28-02-2003
		US6809706 B2	26-10-2004

专利名称(译)	用于电流编程的有机发光二极管显示器的驱动电路		
公开(公告)号	EP1854338A4	公开(公告)日	2008-08-27
申请号	EP2006705133	申请日	2006-02-09
[标]申请(专利权)人(译)	伊格尼斯创新公司		
申请(专利权)人(译)	IGNIS创新INC.		
当前申请(专利权)人(译)	IGNIS创新INC.		
[标]发明人	NATHAN AROKIA CHAJI REZA G		
发明人	NATHAN, AROKIA, CHAJI, REZA, G.		
IPC分类号	H05B33/08 G09G3/32 G09G3/3208		
CPC分类号	G09G3/3283 G09G3/3241 G09G2310/0248 G09G2320/0252 G09G2320/0295 G09G2330/06 H05B33/08		
优先权	2496642 2005-02-10 CA		
其他公开文献	EP1854338A1 EP1854338B1		
外部链接	Espacenet		

摘要(译)

提供了一种用于具有与之相关的寄生电容的负载的负载驱动电路。正在编程的负载。该驱动电路具有：具有控制负载的电压的数据线；以及具有用于监视数据线的电压的低通滤波器的反馈回路；以及电流源，用于向数据线提供电流；电流源由信号线和低通滤波器的输出控制。



Abstract: A load driving circuit for a load having a parasitic capacitance associated therewith is provided. The l