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(71) Applicant: **Samsung Display Co., Ltd.**
Yongin-si
Gyeonggi-do 17113 (KR)

(72) Inventor: Kim, Moojong
1005-2006 Suwon-si, Gyeonggi-do (KR)

(74) Representative: **Dr. Weitzel & Partner**
Patent- und Rechtsanwälte mbB
Friedenstrasse 10
89522 Heidenheim (DE)

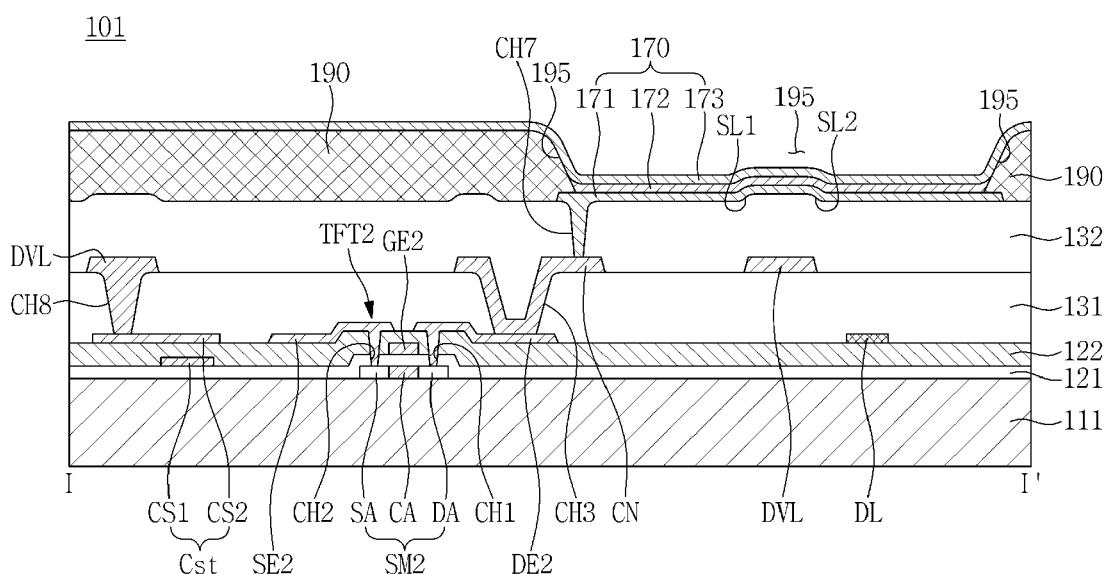
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(54) **ORGANIC LIGHT EMITTING DIODE DISPLAY DEVICE AND MANUFACTURING METHOD THEREOF**

(57) An organic light emitting diode display device includes a substrate. A first protective layer is disposed on the substrate. A conductive line is disposed on the first protective layer. A second protective layer is disposed on the conductive line. A first electrode is disposed

on the second protective layer. An organic light emitting layer is disposed on the first electrode. A second electrode is disposed on the light emitting layer. The first electrode is symmetric with respect to a center of the conductive line.

FIG. 3



Description

1. TECHNICAL FIELD

[0001] The present disclosure relates to an organic light emitting diode ("OLED") display device and a method of manufacturing the OLED display device.

2. DISCUSSION OF RELATED ART

[0002] Organic light emitting diode ("OLED") display devices are a type of self-luminous display device that displays an image using OLEDs that emit light. OLED display devices have characteristics such as low power consumption, high luminance, and high respond speed. OLED display devices generally have a multilayer structure including an OLED. Due to the multilayer structure, as an OLED display device emits light from the OLEDs, a viewing angle-dependent color shift may occur. Particularly, when a lower portion of a pixel electrode is not symmetric or uniform, the recognized color may change according to the viewing direction.

SUMMARY

[0003] According to one embodiment of the invention, an organic light emitting diode display device includes a substrate. A first protective layer is disposed on the substrate. A conductive line is disposed on the first protective layer. A second protective layer is disposed on the conductive line. A first electrode is disposed on the second protective layer. An organic light emitting layer is disposed on the first electrode. A second electrode is disposed on the light emitting layer. The first electrode is symmetric on a plane with respect to a center of the conductive line. In other words, the first electrode is symmetric in a plan view onto the substrate with respect to a center or center line of the conductive line.

[0004] According to one embodiment of the invention, which can be combined with the before or other embodiments of the invention, an organic light emitting diode display device includes a substrate. A first protective layer is disposed on the substrate. The first protective layer has a recess disposed therein. A conductive line is disposed within the recess of the first protective layer. A second protective layer is disposed on the conductive line. A first electrode is disposed on the second protective layer. An organic light emitting layer is disposed on the first electrode. A second electrode is disposed on the light emitting layer. The first electrode overlaps the recess of the first protective layer.

[0005] According to one embodiment of the invention, a method of manufacturing an organic light emitting diode display device includes forming a photosensitive material layer on a substrate by applying a photosensitive material onto the substrate. A first protective layer is formed on the substrate by patterning the photosensitive material layer. The first protective layer has a recess and a contact

hole therein. A conductive line is formed within the recess of the first protective layer. A second protective layer is formed on the conductive line. A first electrode is formed on the second protective layer. A light emitting layer is formed on the first electrode. A second electrode is formed on the light emitting layer. The first electrode overlaps the recess of the first protective layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] A more complete appreciation of the present disclosure and many of the attendant aspects thereof will become more apparent by describing in detail exemplary embodiments thereof with reference to the accompanying drawings, wherein:

FIG. 1 is a plan view illustrating a pixel of an organic light emitting diode ("OLED") display device according to an exemplary embodiment of the present disclosure;

FIG. 2 is a circuit diagram illustrating one pixel illustrated in FIG. 1;

FIG. 3 is a cross-sectional view taken along line I-I' of FIG. 1;

FIG. 4 is a cross-sectional view illustrating white angular dependency (WAD);

FIG. 5A is a cross-sectional view illustrating resonance at a slope;

FIG. 5B is a diagram illustrating a spherical coordinate system for determining coordinates by a distance r , a tilt angle θ and an azimuth angle ϕ , in accordance with exemplary embodiments of the present disclosure;

FIG. 6 is a plan view illustrating a pixel of an OLED display device according to an exemplary embodiment of the present disclosure;

FIG. 7 is a cross-sectional view illustrating an OLED display device according to an exemplary embodiment of the present disclosure;

FIG. 8 is a cross-sectional view illustrating an OLED display device according to an exemplary embodiment of the present disclosure;

FIG. 9 is a cross-sectional view illustrating an OLED display device according to an exemplary embodiment of the present disclosure; and

FIGS. 10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H and 10I are cross-sectional views illustrating a process of manufacturing an OLED display device according to an exemplary embodiment of the present disclosure.

DETAILED DESCRIPTION

[0007] Exemplary embodiments of the present disclosure will now be described more fully hereinafter with reference to the accompanying drawings. Although the invention can be modified in various manners and have several exemplary embodiments, exemplary embodi-

ments of the present disclosure are illustrated in the accompanying drawings and will be mainly described in the specification. However, the scope of the invention is not limited to the exemplary embodiments and should be construed as including all the changes, equivalents, and substitutions included in the scope of the invention.

[0008] In the drawings, thicknesses of a plurality of layers and areas may be illustrated in an enlarged manner for clarity and ease of description thereof. When a layer, area, or plate is referred to as being "on" another layer, area, or plate, it may be directly on the other layer, area, or plate, or intervening layers, areas, or plates may be present therebetween. Further when a layer, area, or plate is referred to as being "below" another layer, area, or plate, it may be directly below the other layer, area, or plate, or intervening layers, areas, or plates may be present therebetween.

[0009] The spatially relative terms "below", "beneath", "less", "above", "upper", and the like, may be used herein for ease of description to describe the relations between one element or component and another element or component as illustrated in the drawings. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation, in addition to the orientation depicted in the drawings. For example, in the case where a device illustrated in the drawing is turned over, the device positioned "below" or "beneath" another device may be placed "above" another device. Accordingly, the illustrative term "below" may include both the lower and upper positions. The device may also be oriented in the other direction, and thus the spatially relative terms may be interpreted differently depending on the orientations.

[0010] Throughout the specification, when an element is referred to as being "connected" to another element, the element is "directly connected" to the other element, or "electrically connected" to the other element with one or more intervening elements interposed therebetween. It will be further understood that the terms "comprises," "comprising," "includes" and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0011] It will be understood that, although the terms "first," "second," "third," and the like may be used herein to describe various elements, these elements should not be limited by these terms. These terms are only used to distinguish one element from another element. Thus, "a first element" discussed below could be termed "a second element" or "a third element," and "a second element" and "a third element" can be termed likewise without departing from the teachings herein.

[0012] Hereinafter, an exemplary embodiment of the present disclosure will be described with reference to FIGS. 1, 2 and 3.

[0013] FIG. 1 is a plan view illustrating a pixel of an

organic light emitting diode ("OLED") display device 101 according to an exemplary embodiment of the present disclosure, FIG. 2 is a circuit diagram illustrating one pixel PX illustrated in FIG. 1, and FIG. 3 is a cross-sectional view taken along line I-I' of FIG. 1.

[0014] The OLED display device 101, according to an exemplary embodiment of the present disclosure, includes a plurality of pixels. The term "pixel" refers to a smallest unit for displaying an image. Referring to FIGS. 1, 2 and 3, the pixel PX includes a switching thin film transistor TFT1, a driving thin film transistor TFT2, an OLED 170 and a capacitor Cst.

[0015] The pixel PX may generate light having a predetermined color, for example, one of red, green or blue. However, the color of the light generated in the pixel PX is not limited thereto, and light having a color such as cyan, magenta or yellow may be generated in the pixel PX.

[0016] The pixel PX is connected to a gate line GL, a data line DL and a driving voltage line DVL. The gate line GL extends in one direction. The data line DL extends in another direction intersecting the gate line GL. Referring to FIG. 1, the driving voltage line DVL extends in a substantially same direction as a direction in which the data line DL extends. The gate line GL transmits a scan signal, the data line DL transmits a data signal, and the driving voltage line DVL provides a driving voltage.

[0017] The thin film transistors TFT1 and TFT2 may include a driving thin film transistor TFT2 for controlling the OLED 170 and a switching thin film transistor TFT1 for switching the driving thin film transistor TFT2. Although each pixel PX is described as including two thin film transistors TFT1 and TFT2, the invention may have fewer or more thin film transistors in each pixel. For example, each pixel PX may include one thin film transistor and a capacitor, or may include three or more thin film transistors and two or more capacitors.

[0018] A portion at which the thin film transistors TFT1 and TFT2, the gate line GL, the data line DL, the driving voltage line DVL and the capacitor Cst are disposed is referred to as a wiring unit and each of the gate line GL, the data line DL, the driving voltage line DVL and the capacitor Cst is referred to as a wiring. The thin film transistors TFT1 and TFT2 may also be one of the wirings or a part of the wiring. In addition, since the gate line GL, the data line DL and the driving voltage line DVL are electrically conductive, they may also be referred to as "a conductive line."

[0019] The switching thin film transistor TFT1 includes a first gate electrode GE1, a first source electrode SE1, a first drain electrode DE1 and a first semiconductor layer SM1. The first gate electrode GE1 is connected to the gate line GL and the first source electrode SE1 is connected to the data line DL.

[0020] The first drain electrode DE1 is connected to a first capacitor plate CS1 through a fifth contact hole CH5 and a sixth contact hole CH6. The switching thin film transistor TFT1 transmits a data signal applied to the data

line DL to the driving thin film transistor TFT2 according to a scan signal applied to the gate line GL.

[0021] The driving thin film transistor TFT2 includes a second gate electrode GE2, a second source electrode SE2, a second drain electrode DE2 and a second semiconductor layer SM2. The second gate electrode GE2 is connected to the first capacitor plate CS1. The second source electrode SE2 is connected to the driving voltage line DVL through a tenth contact hole CH10. The second drain electrode DE2 is connected to a connection electrode CN through a third contact hole CH3 and the connection electrode CN is connected to a first electrode 171 through a seventh contact hole CH7.

[0022] An organic light emitting layer 172 is disposed on the first electrode 171 and a second electrode 173 is disposed on the organic light emitting layer 172. A common voltage is applied to the second electrode 173, and the organic light emitting layer 172 generates light according to an output signal of the driving thin film transistor TFT2.

[0023] The capacitor Cst is connected between the second gate electrode GE2 and the second source electrode SE2 of the driving thin film transistor TFT2. The capacitor Cst charges and maintains a signal input to the second gate electrode GE2 of the driving thin film transistor TFT2. The capacitor Cst includes the first capacitor plate CS1 that is connected to the first drain electrode DE1 through the sixth contact hole CH6. The capacitor Cst further includes a second capacitor plate CS2 that is connected to the driving voltage line DVL through an eighth contact hole CH8 and a ninth contact hole CH9.

[0024] Referring to FIG. 3, thin film transistors TFT1 and TFT2 and the OLED 170 are disposed on a substrate 111.

[0025] The type of the substrate 111 is not particularly limited. For example, the substrate 111 may include an insulating material such as glass, plastic, quartz, or the like. The material for the substrate 111 may have excellent mechanical strength, thermal stability, transparency, surface smoothness, ease of handling and water resistance.

[0026] A buffer layer may be disposed on the substrate 111. The buffer layer may substantially prevent diffusion of impurities into the switching thin film transistor TFT1 and the driving thin film transistor TFT2.

[0027] The first semiconductor layer SM1 and the second semiconductor layer SM2 are each disposed on a substrate 111. The first semiconductor layer SM1 and the second semiconductor layer SM2 each include a semiconductor material and act as active layers of the switching thin film transistor TFT1 and the driving thin film transistor TFT2, respectively. Each of the first semiconductor layer SM1 and the second semiconductor layer SM2 includes a source area SA, a drain area DA and a channel area CA that is disposed between the source area SA and the drain area DA.

[0028] The first semiconductor layer SM1 and the second semiconductor layer SM2 may each include amor-

phous silicon, polycrystalline silicon, or the like, or may include an oxide semiconductor. For example, each of the first semiconductor layer SM1 and the second semiconductor layer SM2 may include an inorganic semiconductor material or an organic semiconductor material. The source area SA and the drain area DA may be doped with an n-type impurity or a p-type impurity.

[0029] A gate insulating layer 121 is disposed on both the first semiconductor layer SM1 and the second semiconductor layer SM2. The gate insulating layer 121 protects the first semiconductor layer SM1 and the second semiconductor layer SM2. The gate insulating layer 121 may include an organic insulating material or an inorganic insulating material.

[0030] The first gate electrode GE1 and the second gate electrode GE2 are disposed on the gate insulating layer 121. The first gate electrode GE1 and the second gate electrode GE2 are disposed so as to overlap the channel areas CA of the first semiconductor layer SM1 and the second semiconductor layer SM2, respectively. In addition, the first capacitor plate CS1 is disposed on the gate insulating layer 121. The second gate electrode GE2 may be formed integrally with the first capacitor plate CS1.

[0031] An insulating interlayer 122 is disposed on the first gate electrode GE1, the second gate electrode GE2 and the first capacitor plate CS1. The insulating interlayer 122 may include an organic insulating material or an inorganic insulating material.

[0032] The first source electrode SE1, the first drain electrode DE1, the second source electrode SE2 and the second drain electrode DE2 are each disposed on the insulating interlayer 122. The second drain electrode DE2 contacts the drain area DA of the second semiconductor layer SM2 through a first contact hole CH1 defined in the gate insulating layer 121 and the insulating interlayer 122. The second source electrode SE2 contacts the source area SA of the second semiconductor layer SM2 through a second contact hole CH2 defined in the gate insulating layer 121 and the insulating interlayer 122. The first source electrode SE1 contacts the first semiconductor layer SM1 through a fourth contact hole CH4 defined in the gate insulating layer 121 and the insulating interlayer 122, and the first drain electrode DE1 contacts the first semiconductor layer SM1 through the fifth contact hole CH5 defined in the gate insulating layer 121 and the insulating interlayer 122.

[0033] In addition, the data line DL and the second capacitor plate CS2 are disposed on the insulating interlayer 122.

[0034] A first protective layer 131 is disposed on the first source electrode SE1, the first drain electrode DE1, the second source electrode SE2, the second drain electrode DE2, the data line DL, and the second capacitor plate CS2. The first protective layer 131 serves to protect the switching thin film transistor TFT1 and the driving thin film transistor TFT2 and also serves to planarize upper surfaces thereof.

[0035] According to an exemplary embodiment of the present disclosure, the first protective layer 131 may include a photosensitive material. For example, the first protective layer 131 may include a photosensitive polymer resin.

[0036] The driving voltage line DVL and the connection electrode CN are disposed on the first protective layer 131.

[0037] The driving voltage line DVL and the connection electrode CN may be formed in a same process using a same material.

[0038] For example, the driving voltage line DVL includes a conductive material. For example, the driving voltage line DVL may include or be formed of aluminum (Al) or alloys thereof, silver (Ag) or alloys thereof, copper (Cu) or alloys thereof, molybdenum (Mo) or alloys thereof, chromium (Cr), tantalum (Ta) and/or titanium (Ti). In addition, the driving voltage line DVL may have a multi-layer structure including a refractory metal layer and a low resistance conductive layer. As such, the driving voltage line DVL is a conductive line including a conductive material.

[0039] The driving voltage line DVL is connected to the second capacitor plate CS2 through the eighth contact hole CH8 and the ninth contact hole CH9 defined in the first protective layer 131. In addition, the driving voltage line DVL is connected to the second source electrode SE2 through the tenth contact hole CH10 defined in the first protective layer 131.

[0040] The connection electrode CN is connected to the second drain electrode DE2 through the third contact hole CH3 defined in the first protective layer 131.

[0041] A second protective layer 132 is disposed on the driving voltage line DVL and the connection electrode CN. According to an exemplary embodiment of the present disclosure, the second protective layer 132 may include a photosensitive material. For example, the second protective layer 132 may include a photosensitive polymer resin.

[0042] The second protective layer 132 serves to protect the driving voltage line DVL and the connection electrode CN and also serves to planarize upper surfaces thereof. However, in the case where the driving voltage line DVL and the connection electrode CN are relatively thick as compared to the second protective layer 132, the upper portion of the driving voltage line DVL and the connection electrode CN might not be completely planarized by the second protective layer 132. Due to the high level of integration of the wiring, a large amount of current or data may need to be transmitted within a wiring of a relatively small area. Accordingly, the wiring may be relatively thick. In the case where thick wiring is used, although the second protective layer 132 is disposed above these wirings, for example, the driving voltage line DVL and the connection electrode CN, the upper portion thereof might not be completely planarized. Referring to FIG. 3, the second protective layer 132 includes slopes SL1 and SL2 above the driving voltage line DVL.

[0043] The first electrode 171 is disposed on the second protective layer 132. The first electrode 171 is also disposed on the slopes SL1 and SL2 formed at the second protective layer 132. The first electrode 171 may be, for example, an anode. According to an exemplary embodiment of the present disclosure, the first electrode 171 is a pixel electrode.

[0044] The first electrode 171 is connected to the connection electrode CN through the seventh contact hole CH7 defined in the second protective layer 132. As the connection electrode CN is connected to the second drain electrode DE2 through the third contact hole CH3 defined in the first protective layer 131, the first electrode 171 may be electrically connected to the second drain electrode DE2 of the driving thin film transistor TFT2.

[0045] Referring to FIG. 3, the driving voltage line DVL is disposed below the first electrode 171. The first electrode 171 overlaps the driving voltage line DVL.

[0046] The driving voltage line DVL is one of the conductive lines, and the first electrode 171 is symmetric with respect to the driving voltage line DVL which is one of the conductive lines. For example, the first electrodes 171 is arranged symmetrically on a plane respectively in a plan view onto the substrate 111 with respect to the driving voltage line DVL respectively with respect to a center or center line of the driving voltage line DVL.

[0047] Referring to FIG. 1, the driving voltage line DVL may be relatively straight, and the first electrode 171 is bilaterally symmetric with respect to the driving voltage line DVL or a center line thereof. This may refer to a symmetry in a horizontal direction, for example the extending direction of the gate lines GL or in general with respect to a first direction. However, exemplary embodiments of the present disclosure are not limited thereto. The driving voltage line DVL may have a curved shape or a broken line shape, and/or the first electrode 171 may be arranged vertically symmetrically with respect to the driving voltage line DVL or a center line thereof. When used herein, the reference to a vertical symmetry especially refers to a bilaterally symmetric extension of the first electrode 171 in a vertical direction, for example the extending direction of the data lines DL or in general in a second direction which is perpendicular to the first direction.

[0048] A pixel defining layer 190 partitioning a light emission area is disposed on the second protective layer 132.

[0049] The pixel defining layer 190 may include a polymer organic material. The pixel defining layer 190 may include a polyimide (PI) resin, a polyacrylic resin, a polyethylene terephthalate (PET) resin and/or a polyethylene naphthalate (PEN) resin. According to an exemplary embodiment of the present disclosure, the pixel defining layer 190 includes a PI resin.

[0050] The pixel defining layer 190 defines an opening 195 and the first electrode 171 is exposed from the pixel defining layer 190 through the opening 195. In addition, the light emission area of the OLED 170 is defined by

the opening 195.

[0051] Referring to FIGS. 1 and 3, the first electrode 171 overlaps at least a portion of the pixel defining layer 190 and does not overlap the pixel defining layer 190 at the opening 195.

[0052] According to an exemplary embodiment of the present disclosure, the opening 195 is symmetric on a plane respectively a plan view onto the substrate 111 with respect to the drive voltage line DVL or a center line of the drive voltage line DVL, which is one of the conductive lines.

[0053] The first electrode 171 is electrically conductive, and may be a transmissive electrode, a transfective electrode or a reflective electrode. In the case where the first electrode 171 is a transmissive electrode, the first electrode 171 includes a transparent conductive oxide. For example, the transparent conductive oxide may include indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), and/or indium tin zinc oxide (ITZO). In the case where the first electrode 171 is a transfective electrode or a reflective electrode, the first electrode 171 may include Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, and/or Cu.

[0054] The organic light emitting layer 172 is disposed on the first electrode 171. For example, the organic light emitting layer 172 is disposed at the opening 195 on the first electrode 171. The organic light emitting layer 172 may be disposed on a sidewall of the opening 195 defined by the pixel defining layer 190 and on the pixel defining layer 190.

[0055] The organic light emitting layer 172 includes a light emitting material. In addition, the organic light emitting layer 172 may include a host and a light emitting dopant. The organic light emitting layer 172 may be manufactured in accordance with a known method using a known material. For example, the organic light emitting layer 172 may be formed using various methods such as a vacuum deposition method, a spin coating method, a cast method, a Langmuir-Blodgett (LB) method, an inkjet printing method, a laser printing method, a laser induced thermal imaging (LITI) method, and the like.

[0056] A hole injection layer (HIL) and/or a hole transport layer (HTL) may be disposed between the first electrode 171 and the organic light emitting layer 172.

[0057] The second electrode 173 is disposed on the organic light emitting layer 172.

[0058] The second electrode 173 may be a common electrode and may be a cathode. The second electrode 173 may be a transmissive electrode, a transfective electrode or a reflective electrode.

[0059] In the case where the second electrode 173 is a transmissive electrode, the second electrode 173 may include Li, Ca, LiF/Ca, LiF/Al, Al, Mg, BaF, Ba, Ag and/or Cu. For example, the second electrode 173 may include a mixture of Ag and Mg.

[0060] In the case where the second electrode 173 is a transfective electrode or a reflective electrode, the second electrode 173 may include Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, LiF/Ca, LiF/Al, Mo, Ti and/or Cu. In

addition, the second electrode 173 may further include a transparent conductive layer including indium tin oxide (ITO), indium zinc oxide (IZO), zinc oxide (ZnO), indium-zinc-tin oxide (IZTO), and the like, in addition to the transfective electrode or the reflective electrode.

[0061] At least one of an electron transport layer (ETL) and an electron injection layer (EIL) may be disposed between the organic light emitting layer 172 and the second electrode 173.

[0062] In the case where the OLED 170 is a top emission type, the first electrode 171 may be a reflective electrode and the second electrode 173 may be a transmissive electrode or a transfective electrode. When the OLED 170 is a bottom emission type, the first electrode 171 may be a transmissive electrode or a transfective electrode, and the second electrode 173 may be a reflective electrode.

[0063] According to an exemplary embodiment of the present disclosure, the OLED 170 is a top emission type, the first electrode 171 is a reflective electrode, and the second electrode 173 is a transfective electrode.

[0064] FIG. 4 is a cross-sectional view illustrating white angular dependency (WAD).

[0065] The OLED display device 101 has a multilayer stack structure (see FIG. 3), and light emitted from the organic light emitting layer 172 is emitted outwardly, passing through the multilayer structure. According to an exemplary embodiment of the present disclosure, the light generated in the organic light emitting layer 172 passes through the second electrode 173 to be emitted outwardly.

[0066] When optical resonance occurs in the course of light repeating being reflected between two reflective surfaces, energy of the light increases and the light having the increased energy may pass through the multilayer stacked structure to be emitted outwardly. Such a structure to allow light to resonate between two reflective layers is called a resonance structure, and a distance between the two reflective layers at which resonance occurs is called a resonance distance. The resonance distance depends on the wavelength of the light.

[0067] Since the first electrode 171 is a reflective electrode and the second electrode 173 is a transfective electrode in the OLED display device 101, according to an exemplary embodiment of the present disclosure, light may be reflected between the first electrode 171 and the second electrode 173 and light resonance may occur. When a wavelength of the light emitted from the organic light emitting layer 172 is denoted as λ_1 and a distance between the first electrode 171 and the second electrode 173 is t_1 , light resonance may occur when the following Formula 1 is satisfied:

$$[Formula\ 1] \quad 2 \cdot n_1 \cdot t_1 = m_1 \cdot \lambda_1$$

[0068] In Formula 1, n_1 denotes an average refractive

index between the first electrode 171 and the second electrode 173, and m_1 is an integer. In addition, the distance t_1 between the first electrode 171 and the second electrode 173 is a distance between an upper surface of the first electrode 171 and a lower surface of the second electrode 173, which opposes the first electrode 171. As used herein, λ_1 denotes a wavelength of light L1 emitted toward the front side.

[0069] In an exemplary embodiment of the present disclosure, although a same color is displayed in the OLED display device 101, different colors may be visually recognized depending on the viewing angle of the observer. For example, when a display surface of the display device that emits white light is viewed from the front, white is recognized, but when viewed from the side, a bluish or yellowish color may be recognized. This phenomenon is called the white angular dependency (WAD), and the WAD is known to be caused by a path difference of light depending on the viewing angle.

[0070] Referring to FIG. 4, the light L1 viewed from the front may resonate according to Formula 1.

[0071] Light L2 emitted toward the lateral side is incident to an interface Sb at an angle θ_i in a medium having a thickness t_1 and a refractive index n_1 and is emitted at an angle θ_o . In such an exemplary embodiment of the present disclosure, when a wavelength of the light L2 emitted toward the lateral side is denoted as λ_2 , the relation of the following Formula 2 is satisfied in order for the light to resonate.

[Formula 2]

$$2 \cdot n_1 \cdot t_1 \cdot \cos(\theta_i) = m_2 \cdot \lambda_2$$

[0072] In Formula 2, m_2 is an integer.

[0073] In such an exemplary embodiment of the present disclosure, when the incident angle θ_i at the interface Sb increases, a value of $\cos(\theta_i)$ becomes smaller, and accordingly, the resonance condition may change and the resonance wavelength may change. As a result, the wavelength λ_2 of the light L2 emitted toward the lateral side differs from the wavelength of the light L1 emitted toward the front side.

[0074] For example, when the incident angle θ_i increases, the value of $\cos(\theta_i)$ becomes small, and accordingly, the wavelength λ_2 that satisfies the resonance condition becomes small. Accordingly, the light L2 having a shorter wavelength than a wavelength of the light L1 emitted toward the front side is emitted toward the lateral side, and thus the WAD occurs.

[0075] FIG. 5A is a cross-sectional view illustrating resonance at a slope, and FIG. 5B is a diagram illustrating a spherical coordinate system for determining coordinates by a distance r , a tilt angle θ and an azimuth angle ϕ , in accordance with exemplary embodiments of the present disclosure.

[0076] As described above, light is reflected between

the first electrode 171 and the second electrode 173 of the OLED display device 101, according to an exemplary embodiment of the present invention, and light resonance occurs.

[0077] Referring to FIGS. 3 and 5A, due to a thickness of the driving voltage line DVL, slopes SL1 and SL2 are formed at the second protective layer 132 above the driving voltage line DVL. In addition, resonance also occurs between the first electrode 171 and the second electrode 173 disposed on the slopes SL1 and SL2. Light L21 and light L22 resonate in the direction perpendicular to surfaces of the first electrode 171 and the second electrode 173 at the slopes SL1 and SL2. Even though light L21 and light L22 have a substantially same or similar wavelength, they are to be emitted in different directions.

[0078] For example, referring to FIG. 5A, light L21 and light L22 resonating between the first electrode 171 and the second electrode 173 at different points R1 and R2 of the slopes SL1 and SL2 are also emitted in the lateral direction.

[0079] In such an example, when a left slope SL1 and a right slope SL2 illustrated in FIG. 5A are symmetric to each other, the light L21 and light L22 respectively viewed from the left and right sides will have a substantially identical wavelength. However, when the left slope SL1 and the right slope SL2 are not symmetric to each other, the resonance conditions in the left slope SL1 and the right slope SL2 become different, and accordingly the wavelength of the observed light will be different depending on the viewing angle of the user.

[0080] FIG. 5B shows a spherical coordinate system for determining coordinates by a distance r , a tilt angle θ and an azimuth angle ϕ . In the case where the left slope SL1 and the right slope SL2 are asymmetric to each other, light of a different wavelength will be visually recognized according to the azimuth angle ϕ of the spherical coordinate system. For example, a WAD deviation occurs according to the azimuth angle ϕ . Such a WAD deviation degrades the display characteristics of the OLED display device 101.

[0081] According to an exemplary embodiment of the present disclosure, in order to substantially prevent degradation of the display characteristics of the OLED display device 101, the slopes SL1 and SL2 are formed symmetrically below the first electrode 171. To this end, the first electrode 171 is disposed symmetrically with respect to the driving voltage line DVL. Accordingly, the display characteristics of the OLED display device 101 may be increased.

[0082] FIG. 6 is a plan view illustrating a pixel of an OLED display device 102 according to an exemplary embodiment of the present disclosure.

[0083] According to an exemplary embodiment of the present disclosure, a driving voltage line DVL, on a first protective layer 131, which is a conductive line, is formed in a radial direction on a plane with respect to a center C of a first electrode 171. In other words, the driving voltage line DVL extends in at least three directions, for ex-

ample extends in four directions in a plan view onto the substrate 111 from the center C of the first electrode 171. For example, referring to FIG. 6, the driving voltage line DVL is disposed in a cruciform (+) shape with respect to the center C of the first electrode 171. Accordingly, the first electrode 171 is horizontally symmetric and vertically symmetric with respect to the driving voltage line DVL.

[0084] Referring to FIG. 6, the driving voltage line DVL includes a horizontal line HL and a vertical line VL. According to an exemplary embodiment of the present disclosure, the driving voltage line DVL has a mesh shape in which a plurality of horizontal lines HL and a plurality of vertical lines VL are arranged in an intersecting manner.

[0085] FIG. 7 is a cross-sectional view illustrating an OLED display device 103 according to an exemplary embodiment of the present disclosure. This exemplary embodiment of the present disclosure may be combined with one, several or all of the other embodiments of the present disclosure.

[0086] Referring to FIG. 7, a first protective layer 131 includes a recess 135, and a driving voltage line DVL, which is a conductive line, is disposed at the recess 135. In such an exemplary embodiment, the recess 135 overlaps the first electrode 171. For example, the driving voltage line DVL is disposed at the recess 135 below the first electrode 171.

[0087] A depth d1 of the recess 135 is substantially equal to a thickness h1 of the driving voltage line DVL which is a conductive line. For example, the depth d1 of the recess 135 and the thickness h1 of the driving voltage line DVL may have a size difference of about 0.01 μm . The thickness h1 and the depth d1 may refer to a direction perpendicular on the main surface of the substrate 111.

[0088] In the case where the depth d1 of the recess 135 and the thickness h1 of the driving voltage line DVL are substantially equal to each other, a second protective layer 132 is flat above the driving voltage line DVL, and the first electrode 171 may be formed on a planar surface. Accordingly, the azimuth angle-dependent WAD deviation may be substantially prevented.

[0089] However, the present invention is not limited thereto, and the depth d1 of the recess 135 may be different from the thickness h1 of the driving voltage line DVL. For example, the depth d1 of the recess 135 may be greater than or less than the thickness h1 of the driving voltage line DVL. In the case where the second protective layer 132 includes an organic material, when a difference between the depth d1 of the recess 135 and the thickness h1 of the driving voltage line DVL is not relatively large, the second protective layer 132 may have a planar surface above the driving voltage line DVL by virtue of a planarizing effect of an organic material.

[0090] FIG. 8 is a cross-sectional view illustrating an OLED display device 104 according to an exemplary embodiment of the present disclosure.

[0091] The OLED display device 104 illustrated in FIG. 8 includes a thin film encapsulation layer 140 on a second

electrode 173 to protect an OLED 170. The thin film encapsulation layer 140 substantially prevents moisture or oxygen from permeating into the OLED 170.

[0092] The thin film encapsulation layer 140 includes at least one inorganic layer 141 and 143 and at least one organic layer 142 that are alternately disposed. The thin film encapsulation layer 140 illustrated in FIG. 8 includes two inorganic layers 141 and 143 and one organic layer 142. However, the structure of the thin film encapsulating layer 140 is not limited to the structure illustrated in FIG. 8.

[0093] The inorganic layers 141 and 143 may include metal oxide, metal oxynitride, silicon oxide, silicon nitride, and/or silicon oxynitride. The inorganic layers 141 and 143 are formed by a chemical vapor deposition (CVD) method or an atomic layer deposition (ALD) method. However, the present invention is not limited thereto, and the inorganic layers 141 and 143 may be formed through various methods known to those skilled in the art.

[0094] The organic layer 142 may include, for example, a polymer material. The organic layer 142 may be formed through a thermal deposition process. The thermal deposition process for forming the organic layer 142 is performed within a temperature range that does not damage the OLED 170. However, the present invention is not limited thereto, and the organic layer 142 may be formed through various other methods known to those skilled in the art.

[0095] The inorganic layers 141 and 143, which have a high density of thin film, mainly suppress the permeation of moisture or oxygen. Most of moisture and oxygen are blocked by the inorganic layers 141 and 143 from penetrating into the OLED 170.

[0096] The moisture and oxygen that have passed through the inorganic layers 141 and 143 are blocked again by the organic layer 142. The organic layer 142 also functions as a buffer layer to reduce the stress between the inorganic layers 141 and 143 and the organic layer 142 in addition to the moisture permeation restraint. In addition, since the organic layer 142 has planarizing characteristics, an uppermost surface of the thin film encapsulation layer 140 may be planarized by the organic layer 142.

[0097] Since the thin film encapsulation layer 140 may be relatively thin, the organic light emitting display 104 may be thin as well. Such an OLED display device 104 may have excellent flexible characteristics.

[0098] FIG. 9 is a cross-sectional view illustrating an OLED display device 105 according to an exemplary embodiment of the present disclosure.

[0099] The OLED display device 105 illustrated in FIG. 9 includes a sealing member 150 disposed on a second electrode 173 to protect an OLED 170.

[0100] The sealing member 150 may include a light transmissive insulating material such as glass, quartz, ceramic and plastic. The sealing member 150 has a plate shape and is attached to the substrate 111 to protect the OLED 170.

[0101] A filler 160 may be disposed between the OLED

170 and the sealing member 150. The filler 160 may include an organic material, for example, a polymer. In addition, a protective layer including a metal or an inorganic material may be disposed on the OLED 170 to protect the OLED 170.

[0102] Hereinafter, a method of manufacturing the OLED display device 103 according to an exemplary embodiment of the present disclosure will be described with reference to FIGS. 10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H and 10I. FIGS. 10A, 10B, 10C, 10D, 10E, 10F, 10G, 10H and 10I are views illustrating a process of manufacturing the OLED display device 103 according to an exemplary embodiment of the present disclosure.

[0103] Referring to FIG. 10A, a driving thin film transistor TFT2, a capacitor Cst, and a data line DL are formed on a substrate 111. Wirings such as a switching thin film transistor TFT1 and a gate line GL may also be formed on the substrate 111.

[0104] Referring to FIG. 10B, a photosensitive material is applied over an entire surface of the substrate 111 including the driving thin film transistor TFT2 such that a photosensitive material layer 130 is formed. The photosensitive material may use, for example, a photodegradable polymer resin. The photodegradable polymer resin may include polyimide (PI).

[0105] In addition, a pattern mask 301 is disposed above the photosensitive material layer 130, spaced apart from the photosensitive material layer 130. The pattern mask 301 includes a mask substrate 310 and a light blocking pattern 320 disposed on the mask substrate 310. The light blocking pattern 320 includes at least three areas, each having different light transmittances. Such a pattern mask 301 may also be referred to as a half tone mask.

[0106] The mask substrate 310 may use a transparent glass or plastic substrate. However, the invention is not limited thereto, and the mask substrate 310 may include another material having light transmittance and mechanical strength.

[0107] The light blocking pattern 320 may be formed by selectively applying a light blocking material to the mask substrate 310. The blocking pattern 320 includes a transmissive portion 321, a light blocking portion 322, and a semi-light transmissive portion 323.

[0108] The transmissive portion 321 is an area through which light is transmitted, and is located above an area to be defined with a third contact hole CH3 and above an area where an eighth contact hole CH8 is to be formed.

[0109] The light blocking portion 322 is a portion at which light transmission is blocked, and the light blocking portion 322 may be formed by applying a light blocking material to the mask substrate 310.

[0110] The semi-transmissive portion 323 is a portion through which a part of an incident light is transmitted, and it is located above an area to be defined with a recess 135. The semi-light transmissive portion 323 may have a structure in which a light transmissive area 323a and a light blocking slit 323b are alternately disposed. In such

an exemplary embodiment, the light transmittance of the semi-light transmissive portion 323 may be adjusted by adjusting an interval between the light transmissive area 323a and the light blocking slit 323b. In an exemplary embodiment of the present disclosure, the light transmittance of the semi-light transmissive portion 323 may be adjusted by adjusting a concentration of the light blocking material.

[0111] Referring to FIG. 10C, the photosensitive material layer 130 is patterned through exposure and development using the pattern mask 301, such that a first protective layer 131 including the recess 135, the third contact hole CH3 and the eighth contact hole CH8 is formed. For example, the photosensitive material layer 130 is exposed, developed, and then heat cured such that the first protective layer 131 may be formed.

[0112] Referring to FIG. 10D, a connection electrode CN and a driving voltage line DVL are formed on the first protective layer 131.

[0113] The connection electrode CN is connected to a second drain electrode DE2 through the third contact hole CH3.

[0114] The driving voltage line DVL is disposed at the recess 135 defined in the first protective layer 131. In addition, the driving voltage line DVL is connected to a second capacitor plate CS2 through the eighth contact hole CH8. Although not illustrated, the first protective layer 131 has a ninth contact hole CH9, and the driving voltage line DVL is connected to the second capacitor plate CS2 also through the ninth contact hole CH9. Although not illustrated, the driving voltage line DVL is connected to the second source electrode SE2 through a tenth contact hole CH10.

[0115] Referring to FIG. 10E, a second protective layer 132 is formed on the connection electrode CN and the driving voltage line DVL. The second protective layer 132 has a seventh contact hole CH7 exposing a part of the connection electrode CN.

[0116] The second protective layer 132 may be formed by exposure, development and curing of a photosensitive material.

[0117] Referring to FIG. 10F, a first electrode 171 is formed on the second protective layer 132.

[0118] The first electrode 171 overlaps the recess 135 and the driving voltage line DVL. In addition, the first electrode 171 is connected to the connection electrode CN through the seventh contact hole CH7. The first electrode 171 is connected to the second drain electrode DE2 of the driving thin film transistor TFT2 through the connection electrode CN.

[0119] Referring to FIG. 10G, a pixel defining layer 190 is formed above the substrate 111 including the first electrode 171 and the second protective layer 132.

[0120] The pixel defining layer 190 may include a photosensitive material, for example, a photodegradable polymer resin. Examples of the photodegradable polymer resin may include a polyimide (PI) resin, a polyacrylic resin, a polyethylene terephthalate (PET) resin, a poly-

ethylene naphthalate (PEN) resin, and the like.

[0121] An opening 195 is defined by the pixel defining layer 190. The first electrode 171 is exposed from the pixel defining layer 190 by the opening 195. For example, the pixel defining layer 190 exposes an upper surface of the first electrode 171, and protrudes along the periphery of the first electrode 171. The pixel defining layer 190 overlaps an end portion of the first electrode 171 and the opening 195 is located above the first electrode 171. According to an exemplary embodiment of the present disclosure, the opening 195 is symmetric on a plane with respect to the driving voltage line DVL, which is a conductive line. In other words, the opening 195 is symmetric in a plan view onto the substrate 111 with respect to the driving voltage line DVL or a center line or a center thereof.

[0122] Referring to FIG. 10H, an organic light emitting layer 172 is formed on the first electrode 171 that is exposed by the opening 195 of the pixel defining layer 190. The organic light emitting layer 172 may be formed, for example, by deposition.

[0123] Referring to FIG. 10I, a second electrode 173 is formed on the organic light emitting layer 172. The second electrode 173 is also formed on the pixel defining layer 190. The second electrode 173 may be formed by deposition. In such a manner, the OLED display device 103 illustrated in FIG. 7 may be manufactured.

[0124] As set forth hereinabove, in one or more exemplary embodiments of the present disclosure, since the first electrode is disposed symmetrically with respect to the conductive line therebelow, the azimuth angle-dependent color deviation of the OLED display device may be reduced. In addition, in one or more exemplary embodiments of the present disclosure, since the first electrode is disposed on a planar surface, the azimuth angle-dependent color deviation of the OLED display device may be substantially prevented.

[0125] While the present invention has been illustrated and described with reference to the exemplary embodiments thereof, it will be apparent to those of ordinary skill in the art that various changes in form and detail may be made thereto without departing from the scope of the present invention.

Claims

1. An organic light emitting diode display device (101, 102, 104, 105) comprising:

a substrate (111);
a first protective layer (131) disposed on the substrate (111);
a conductive line disposed on the first protective layer (131);
a second protective layer (132) disposed on the conductive line;
a first electrode (171) disposed on the second

protective layer (132);

an organic light emitting layer (172) disposed on the first electrode (171); and
a second electrode (173) disposed on the organic light emitting layer (172),
wherein the first electrode (171) is symmetric in a plan view onto the substrate (111) with respect to a center (C) or a center line of the conductive line.

2. An organic light emitting diode display device (103) comprising:

a substrate (111);
a first protective layer (131) disposed on the substrate (111), the first protective layer (131) having a recess (135) disposed therein;
a conductive line disposed within the recess (135) of the first protective layer (131);
a second protective layer (132) disposed on the conductive line;
a first electrode (171) disposed on the second protective layer (132);
an organic light emitting layer (172) disposed on the first electrode (171); and
a second electrode (173) disposed on the organic light emitting layer (172),
wherein the first electrode (171) overlaps the recess (135) of the first protective layer (131).

3. The organic light emitting diode display device (103) as claimed in claim 2, wherein a depth (d1) of the recess (135) of the first protective layer (131) is substantially equal to a thickness (h1) of the conductive line.

4. The organic light emitting diode display device (103) as claimed in claim 2, wherein a depth (d1) of the recess of the first protective layer (131) is different from a thickness (h1) of the conductive line.

5. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in at least one of claims 1 to 4, wherein the conductive line is a driving voltage line (DVL).

6. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in at least one of claims 1 to 5, wherein the conductive line is substantially straight.

7. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in at least one of claims 1 to 5, wherein the conductive line extends in at least three directions or in four directions in the plan view from a center (C) of the first electrode (171).

8. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in claim 7, wherein the conductive line has a lattice shape.
9. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in at least one of claims 1 to 8, further comprising a thin film transistor (TFT2) disposed between the substrate (111) and the first protective layer (131). 5
10. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in claim 9, wherein the thin film transistor (TFT2) is connected to the first electrode (171). 10
11. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in claim 9 or 10, wherein the thin film transistor (TFT2) is connected to the conductive line. 15
12. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in at least one of claims 1 to 11, further comprising a pixel defining layer (190) disposed on the second protective layer (132), the pixel defining layer (190) having an opening (195) that exposes at least a portion of the first electrode (171). 20
13. The organic light emitting diode display device (101, 102, 103, 104, 105) as claimed in claim 12, wherein the opening (195) is symmetric, on a plane, with respect to a center (C) of the conductive line. 25
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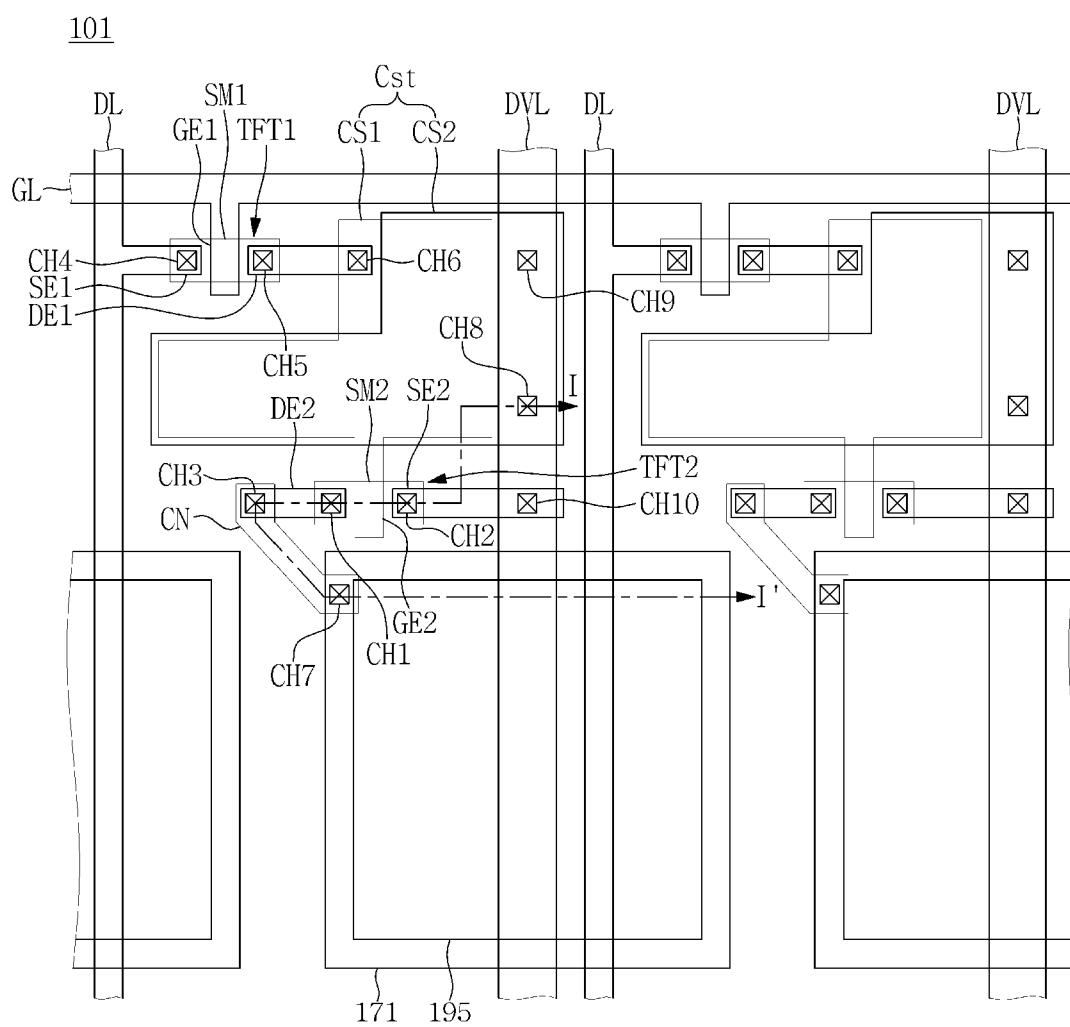
FIG. 1

FIG. 2

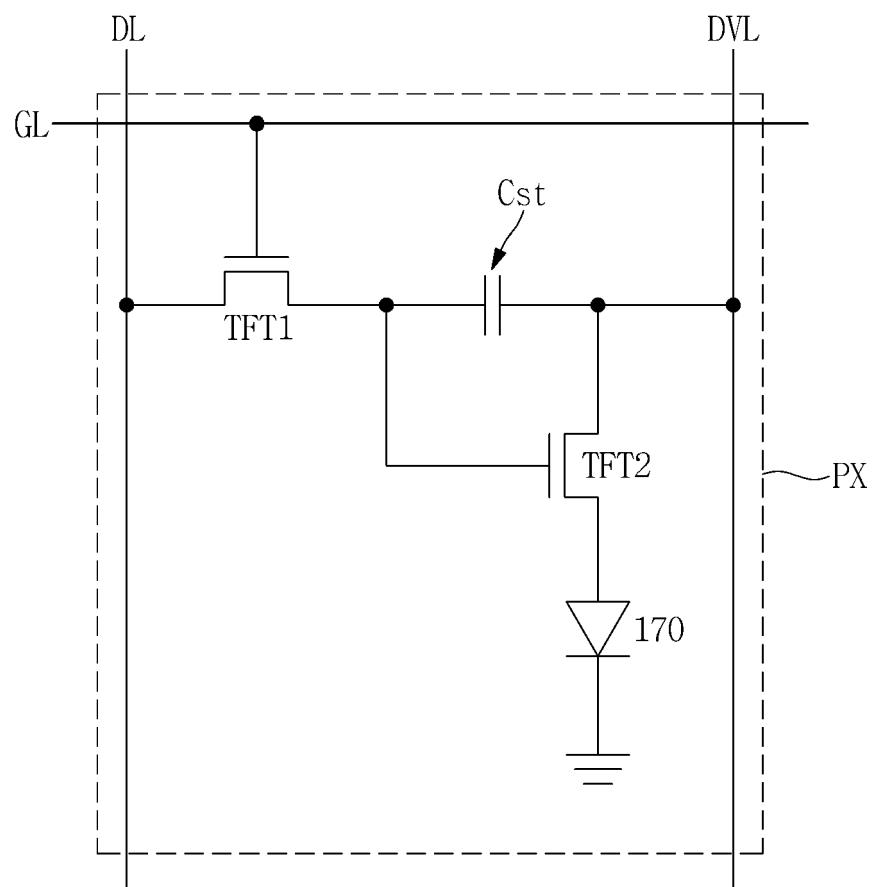


FIG. 3

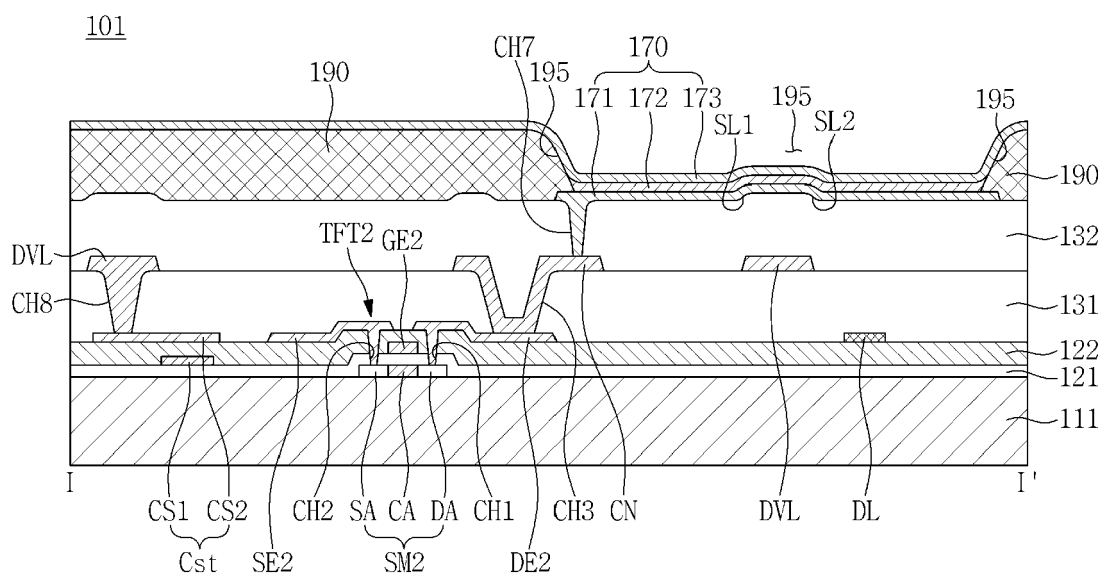


FIG. 4

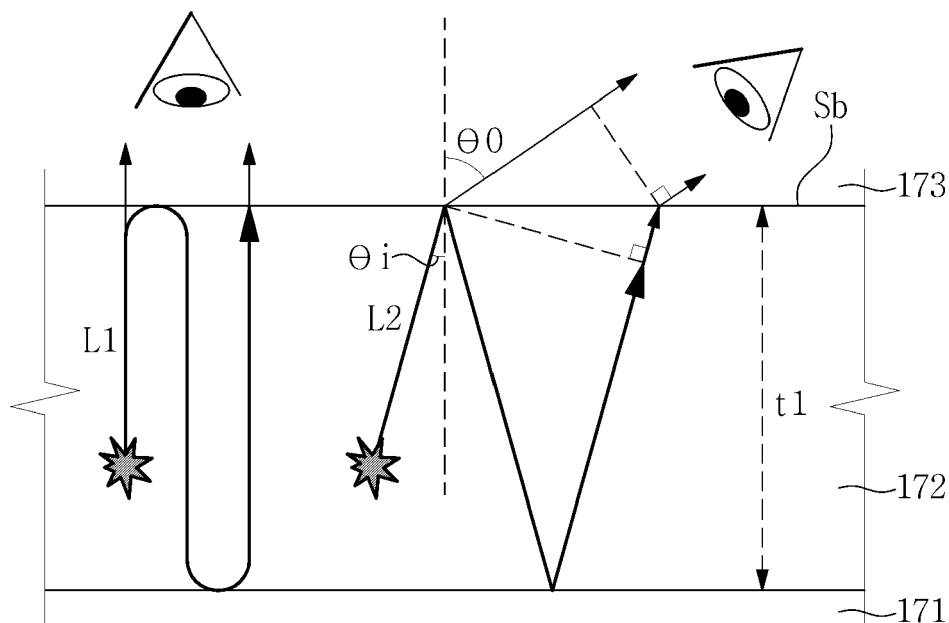


FIG. 5A

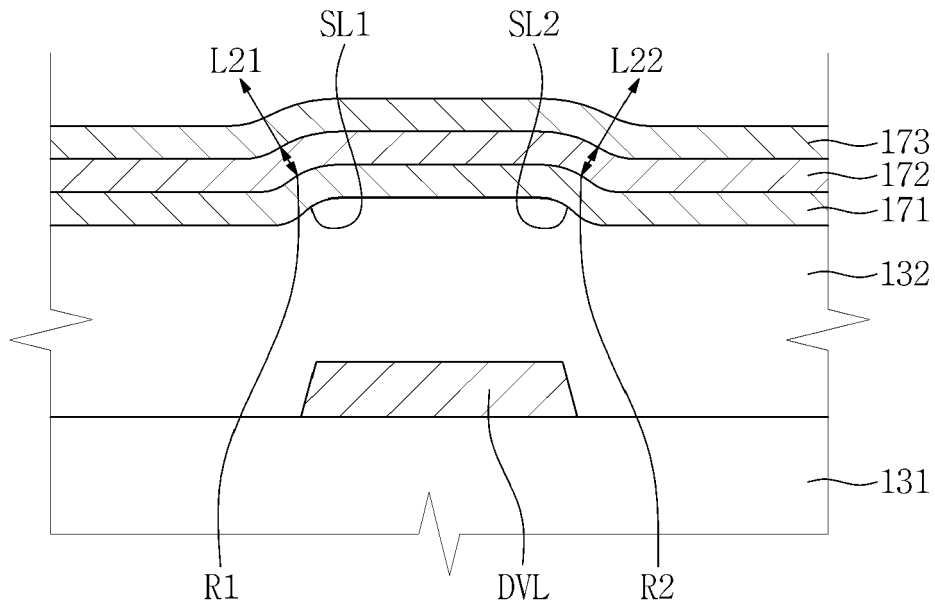


FIG. 5B

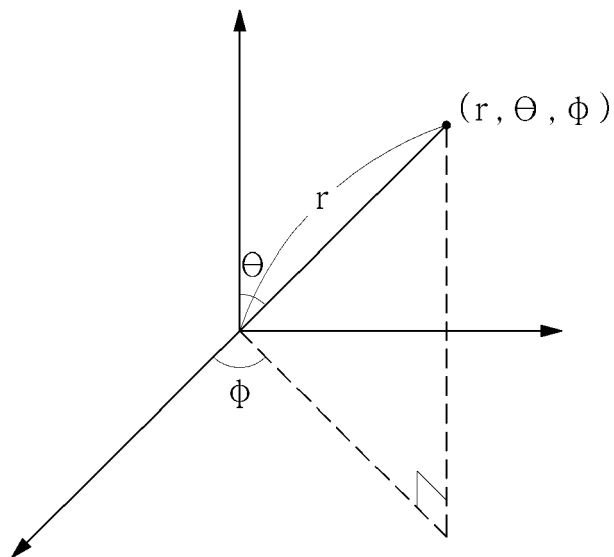


FIG. 6

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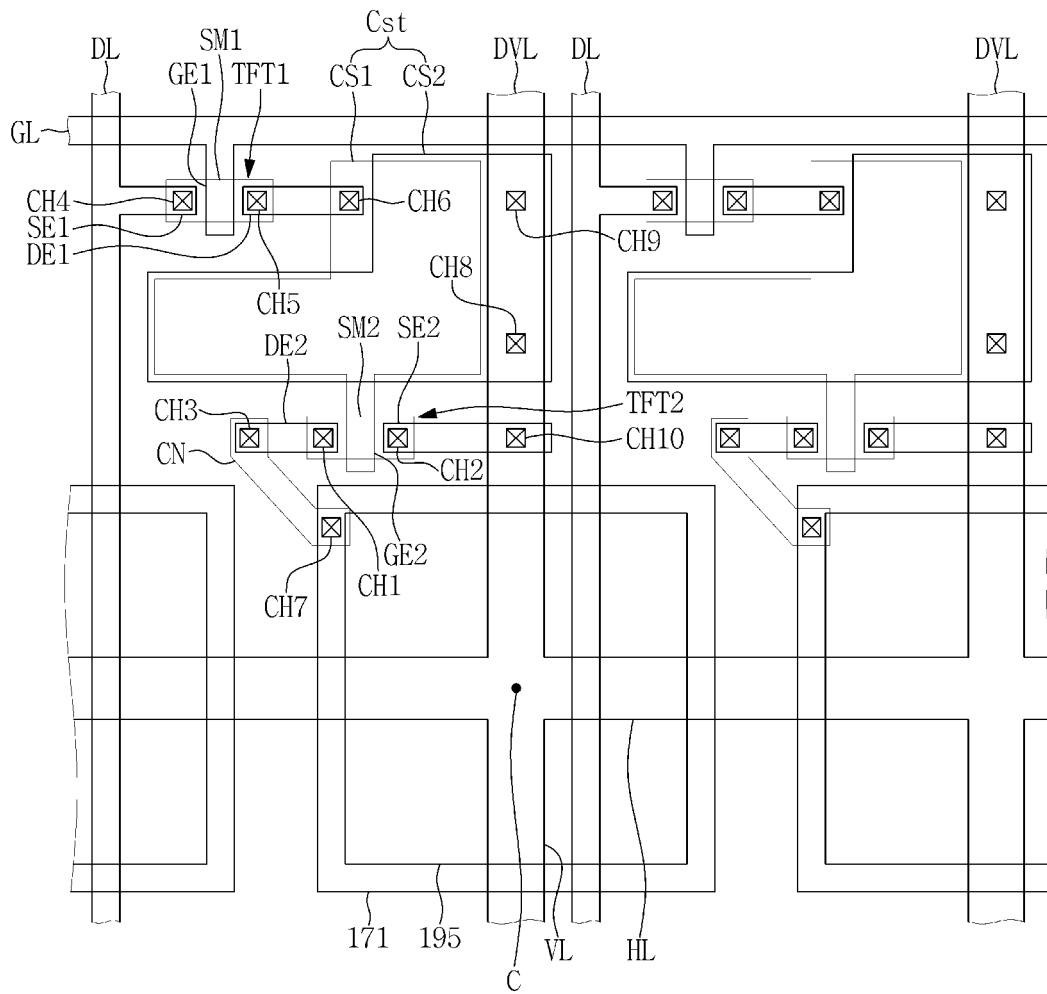


FIG. 7

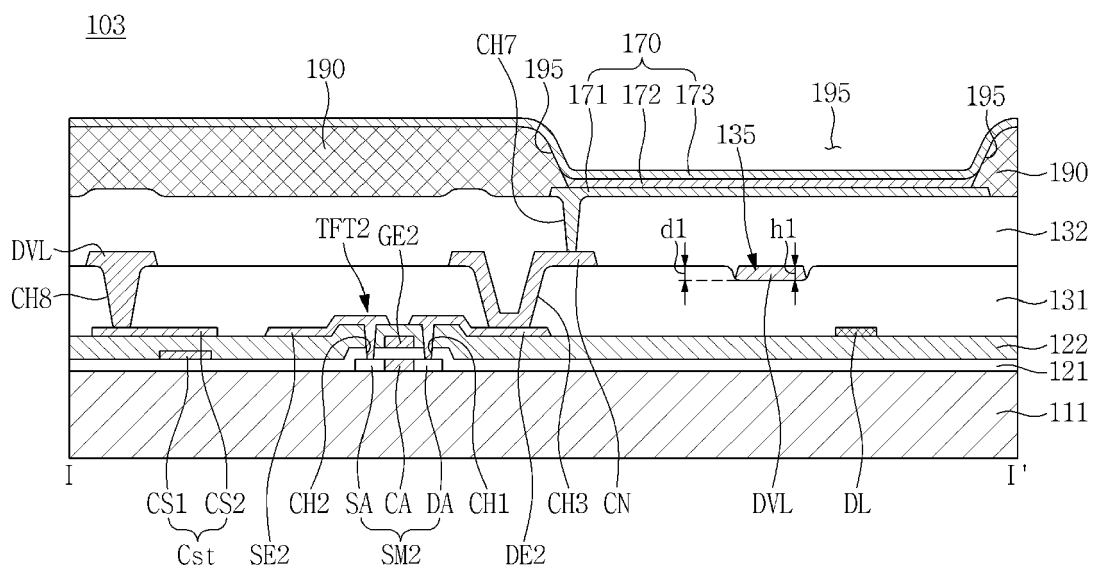


FIG. 8

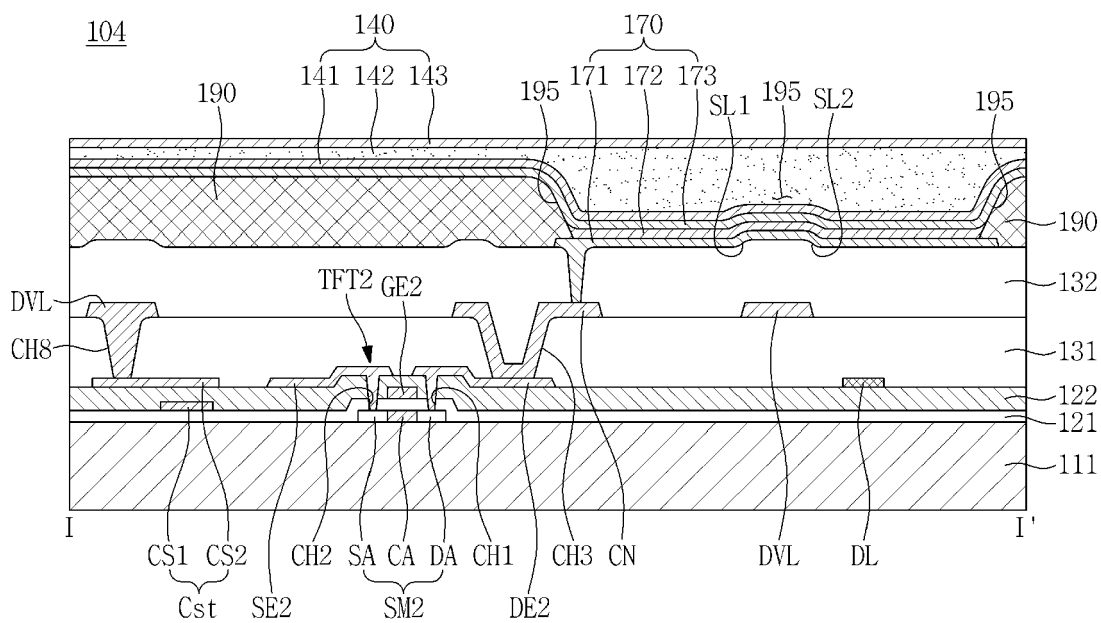


FIG. 9

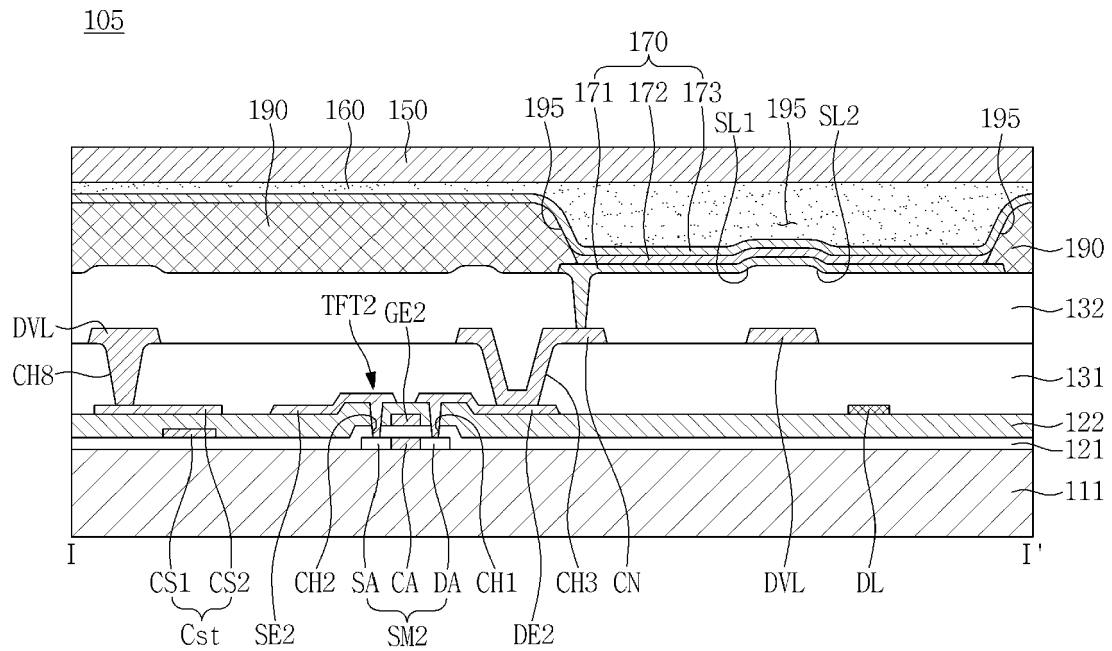


FIG. 10A

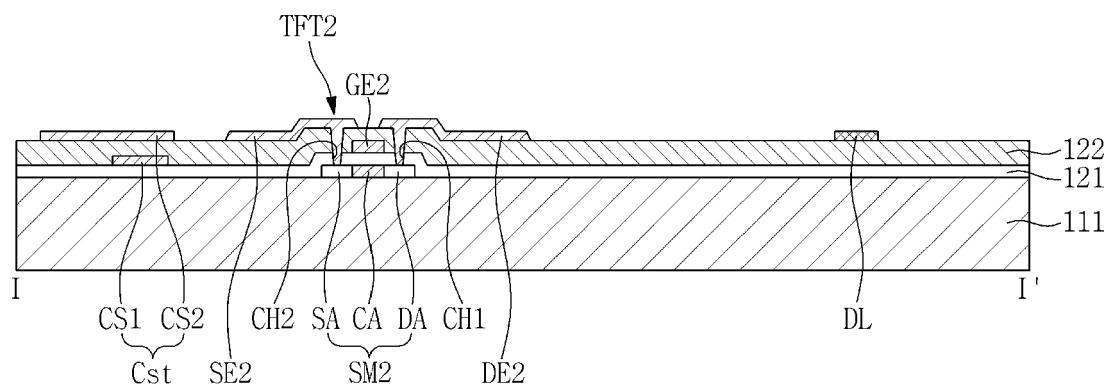


FIG. 10B

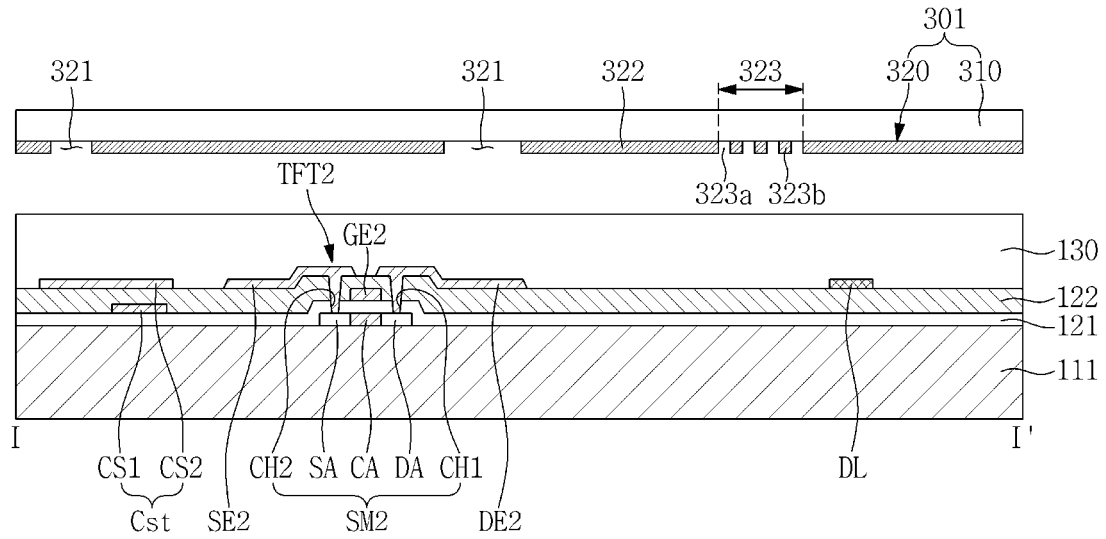


FIG. 10C

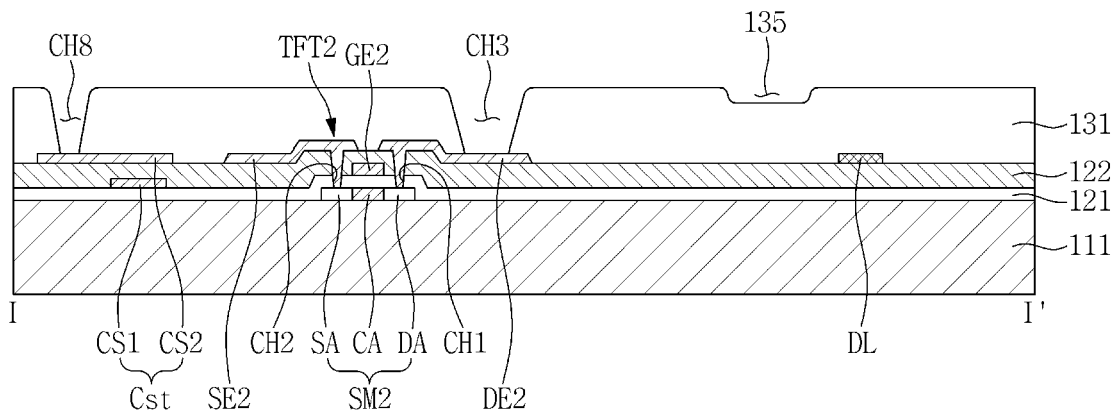


FIG. 10D

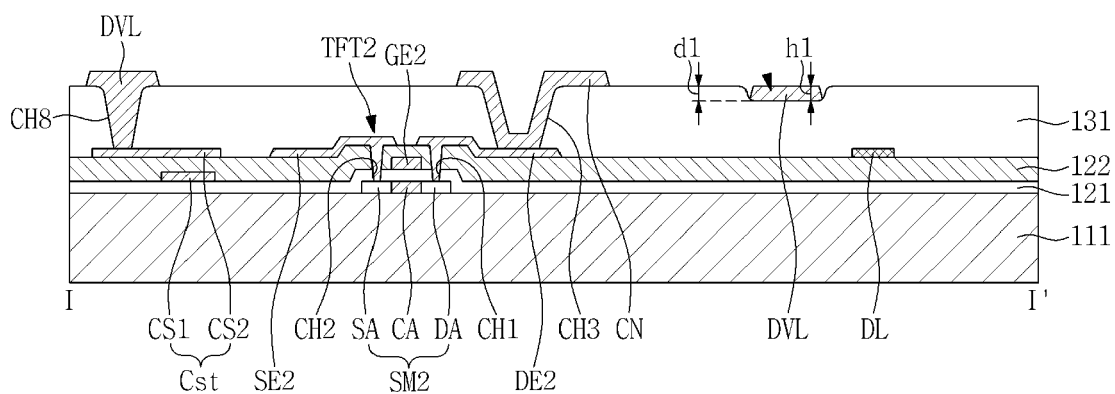


FIG. 10E

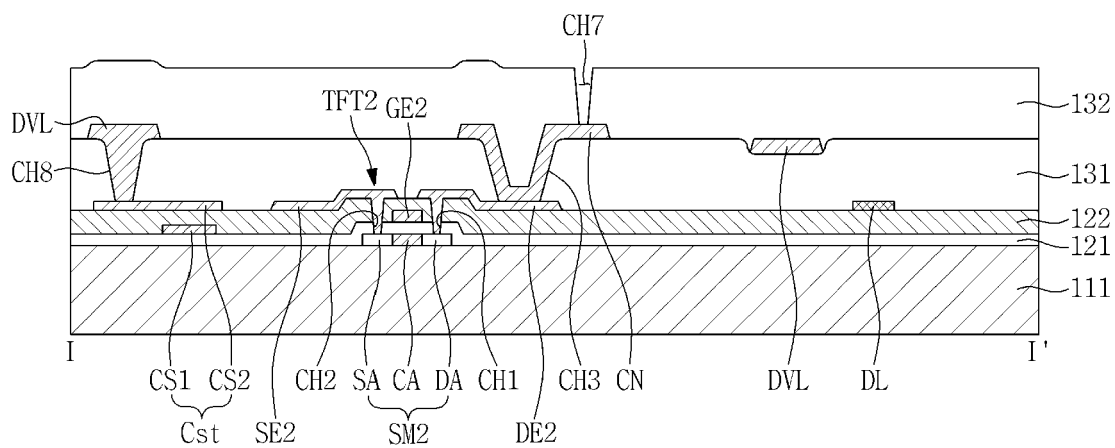


FIG. 10F

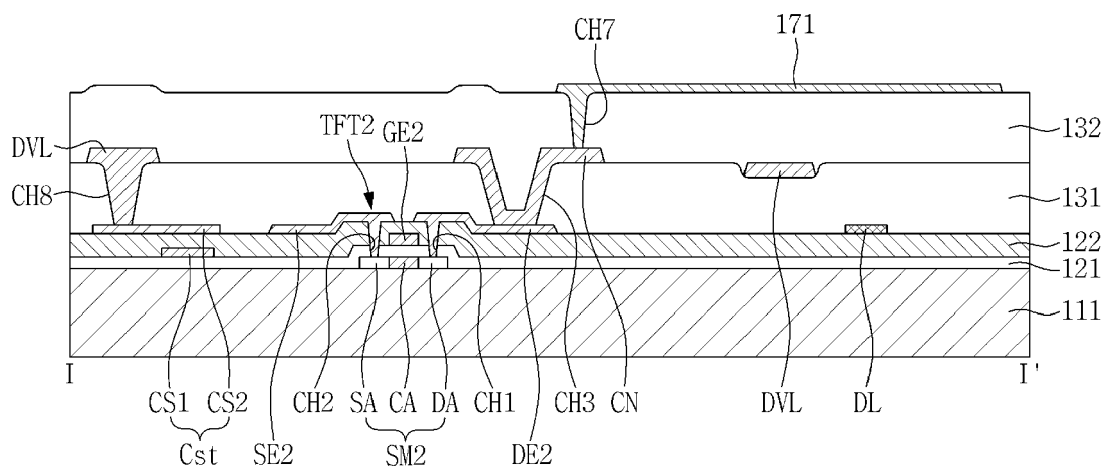


FIG. 10G

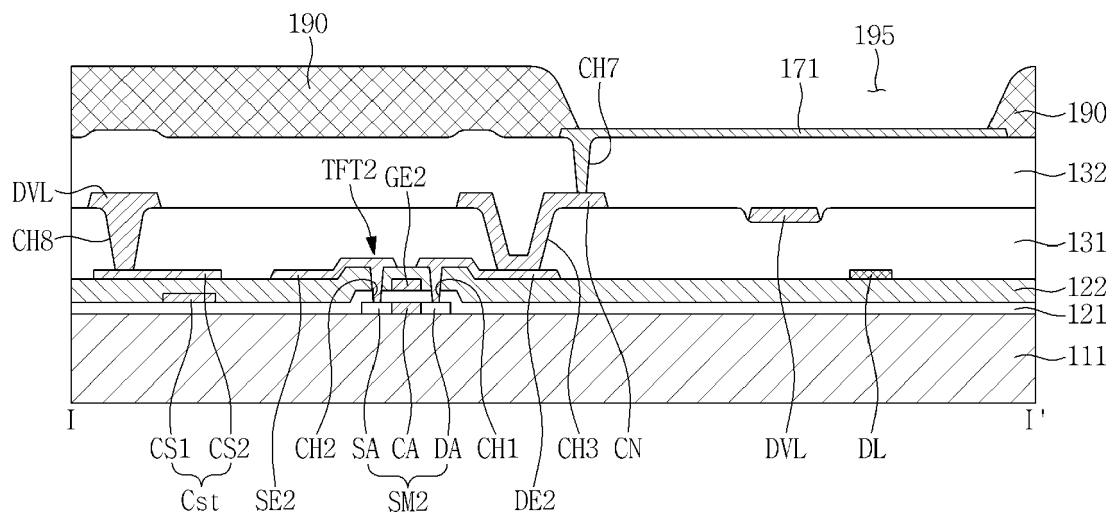


FIG. 10H

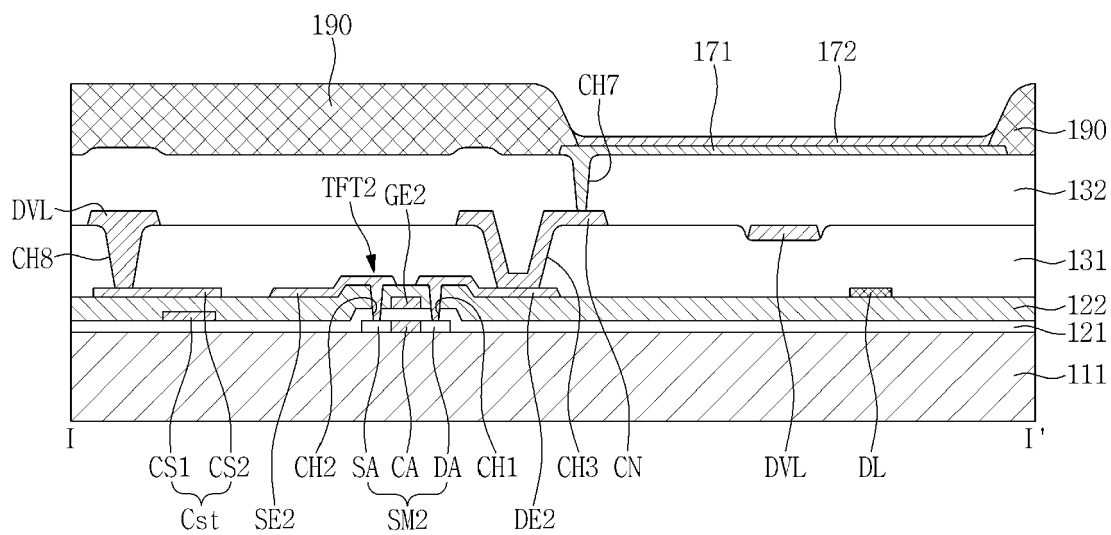
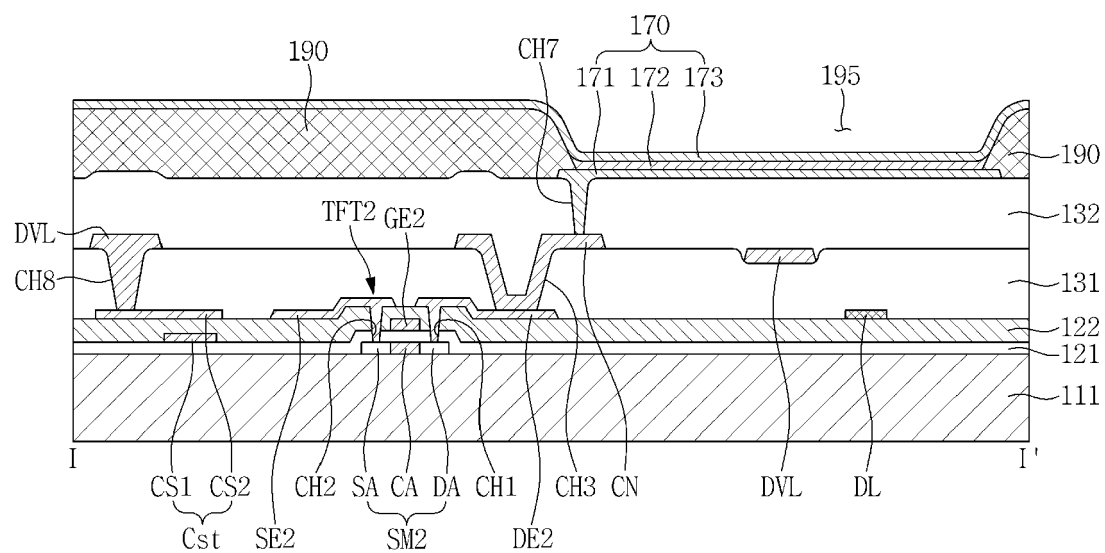


FIG. 10I





EUROPEAN SEARCH REPORT

Application Number
EP 17 20 4548

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DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	US 2016/210896 A1 (GIL ELLY [KR]) 21 July 2016 (2016-07-21)	1,5,6, 9-12	INV. H01L27/32
A	* paragraphs [0096], [0102] - [0104], [0130]; figures 2,4 *	7,8,13	

X	US 2015/179680 A1 (TSUNO HITOSHI [JP] ET AL) 25 June 2015 (2015-06-25)	2-4,6, 9-12	
A	* figure 3B *	5,7,8	

A	US 2014/332768 A1 (KWON DO-HYUN [KR] ET AL) 13 November 2014 (2014-11-13)	1-13	
	* paragraphs [0008] - [0019]; figure 2 *		

			TECHNICAL FIELDS SEARCHED (IPC)
			H01L
The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 20 April 2018	Examiner Welter, Steve
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

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EPO FORM 1503 03/02 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.**

EP 17 20 4548

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This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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20-04-2018

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专利名称(译)	有机发光二极管显示装置及其制造方法		
公开(公告)号	EP3331021A1	公开(公告)日	2018-06-06
申请号	EP2017204548	申请日	2017-11-30
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	KIM MOOJONG		
发明人	KIM, MOOJONG		
IPC分类号	H01L27/32		
CPC分类号	H01L27/3276 H01L51/5203 H01L27/3258 H01L27/326 H01L27/3206 H01L27/3248 H01L51/5253 H01L2227/323		
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审查员(译)	韦尔特，史蒂夫		
优先权	1020160162811 2016-12-01 KR		
外部链接	Espacenet		

摘要(译)

有机发光二极管显示装置包括基板。第一保护层设置在基板上。导电线设置在第一保护层上。第二保护层设置在导线上。第一电极设置在第二保护层上。有机发光层设置在第一电极上。第二电极设置在发光层上。第一电极相对于导电线的中心对称。

FIG. 3

