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(54) DISPLAY APPARATUS AND METHOD OF DRIVING THE SAME

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Description

BACKGROUND

1. Field

[0001] Embodiments of the inventive concept relate to a display apparatus and a method of driving the display apparatus. More particularly, example embodiments of the inventive concept relate to a display apparatus having a simple pixel structure and a method of driving the display apparatus.

2. Description of the Related Art

[0002] Recently, various flat panel display devices that reduce weight and volume have been developed. The flat panel display devices include a liquid crystal display (LCD) device, a field emission display (FED) device, a plasma display panel (PDP) device, an organic light emitting display (OLED) device, etc.

[0003] The OLED device has advantages such as rapid response speed and low power consumption because the OLED device among the flat panel display devices displays an image using an organic light emitting diode that emits a light during recombination of electrons and holes.

Whilst different to the subject-matter of the present disclosure, background art includes US2008136795 and US2006044244.

US2008136795 describes a pixel circuit including a driver, a switching transistor, and an OLED connected in series between a power supply line and a common cathode. A capacitor is connected between the gate of the driver transistor and the voltage line. The switching transistor is connected between the gate and drain of the driver transistor. A capacitor is connected between the drain of the driver transistor and a source line.

US2006044244 describes a pixel circuit where a potential wire is set to a potential, a voltage of a gate wire becomes Low, a voltage of a control wire becomes High, and a voltage of a control wire becomes High, so that a gate terminal of a driving transistor has a potential of a data wire. Moreover, a voltage of the gate wire becomes High so as to compensate a threshold voltage of the driving transistor. Thereafter, a voltage of the control wire becomes Low, and the potential wire is set to a potential, so that a voltage of a capacitor, i.e., a gate-source voltage of the driving transistor is changed. This causes a voltage of the control wire to be Low, so that a driving current flows into an organic light emitting device.

BRIEF SUMMARY

[0004] Embodiments of the inventive concept set out to provide a display apparatus having improved display quality in a standby mode that is a low-power mode.

[0005] Embodiments of the inventive concept also seek to provide a method of driving such a display apparatus.

[0006] The invention is defined by the independent claims. According to an embodiment of the inventive concept, there is provided a display apparatus as claimed in claim 1.

[0007] In an embodiment of the invention, each of the first, second and third transistors may be an N-type transistor.

[0008] In an embodiment of the invention, during a first period of a frame period, the first voltage line may receive a low voltage of a first driving signal, the second voltage line may receive a high voltage of the first power source signal, the third voltage line may receive a high voltage of the second driving signal and the n-th scan line may receive a high voltage of a scan signal.

[0009] In an embodiment of the invention, during a second period of the frame period, the first voltage line may receive a low voltage of the first driving signal, the second voltage line may receive a low voltage of the first power source signal lower than the low voltage of the first driving signal, the third voltage line may receive a low voltage of the second driving signal, and the n-th scan line may receive a high voltage of the scan signal.

[0010] In an embodiment of the invention, during a third period of the frame period, the first voltage line may receive a low voltage of the first driving signal, the second voltage line may receive a high voltage of the first power source signal, the third voltage line may receive a low voltage of the second driving signal, the n-th scan line may receive a high voltage of the scan signal during an n-th horizontal period in the third period, and the m-th data line may receive a data voltage corresponding to a plurality of horizontal lines.

[0011] In an embodiment of the invention, during the n-th horizontal period, a data voltage corresponding to an n-th horizontal line may be divided by a voltage division ratio of the first and second capacitors which are connected in series and divided voltage may be applied to the first node.

[0012] In an embodiment of the invention, the m-th data line may receive s a reference voltage before the m-th data line receives a data voltage corresponding to a first horizontal line of a plurality of horizontal lines, and the m-th data line may receive a reference voltage after the m-th data line receives a data voltage corresponding to a last horizontal line of a plurality of horizontal lines.

[0013] In an embodiment of the invention, the m-th data line may receive a reference voltage before the first voltage line receives a high voltage of the first driving signal and, the reference voltage may be equal to or lower than a lowest voltage in a voltage range of the data voltage.

[0014] In an embodiment of the invention, during a fourth period of the frame period, the first voltage line may receive a high voltage of the first driving signal, the second voltage line may receive a high voltage of the first power source signal, the third voltage line may receive a low voltage of the second driving signal, and the

n-th scan line may receive a low voltage of the scan signal.

[0015] In an embodiment of the invention, when a difference voltage between the high voltage and the low voltage of the first driving signal is applied to the first node, the first transistor may be turned on and a driving current corresponding to the data voltage applied to the first node may flow through the organic light emitting diode.

[0016] In an embodiment of the invention, each of the first, second and third transistors may be a P-type transistor.

[0017] In an embodiment of the invention, during a first period, the first voltage line may receive a low voltage of the first driving signal, the second voltage line may receive a low voltage of the first power source signal, the third voltage line may receive a low voltage of the second driving signal, and the n-th scan line receives a low voltage of the scan signal.

[0018] In an embodiment of the invention, the low voltage of the first power source signal may be higher than the low voltage of the first driving signal.

[0019] In an embodiment of the invention, during a second period of the frame period, the first voltage line may receive a low voltage of the first driving signal, the second voltage line may receive a low voltage of the first power source signal, the third voltage line may receive a high voltage of the second driving signal and the n-th scan line may receive a low voltage of the scan signal.

[0020] In an embodiment of the invention, during a third period of the fame period, the first voltage line may receive a low voltage of the first driving signal, the second voltage line may receive a low voltage of the first power source signal, the third voltage line may receive a high voltage of the second driving signal, the n-th scan line may receive a low voltage of the scan signal during an n-th horizontal period in the third period, and the m-th data line may receive a data voltage corresponding to a plurality of horizontal lines.

[0021] In an embodiment of the invention, during the n-th horizontal period, a data voltage corresponding to an n-th horizontal line may be divided by a voltage division ratio of the first and second capacitors which are connected in series and divided voltage may be applied to the first node.

[0022] In an embodiment of the invention, the m-th data line may receive a reference voltage before the m-th data line receives a data voltage corresponding to a first horizontal line of a plurality of horizontal lines, and the m-th data line may receive a reference voltage after the m-th data line receives a data voltage corresponding to a last horizontal line of a plurality of horizontal lines.

[0023] In an embodiment of the invention, the m-th data line may receive a reference voltage before the first voltage line receives a high voltage of the first driving signal, and the reference voltage mat be equal to or lower than a lowest voltage in a voltage range of the data voltage.

[0024] In an embodiment of the invention, during a fourth period of the frame period, the first voltage line may receive a high voltage of the first driving signal, the second voltage line may receive a high voltage of the first power source signal, the third voltage line may receive a high voltage of the second driving signal, and the n-th scan line may receive a high voltage of the scan signal.

[0025] In an embodiment of the invention, when a difference voltage between the high voltage and the low voltage of the first driving signal may be applied to the first node, the first transistor is turned on and a driving current corresponding to the data voltage applied to the first node may flow through the organic light emitting diode.

[0026] In an embodiment of the invention, at least one of the second and third transistors may have a dual gate structure.

[0027] According to an embodiment of the inventive concept, there is provided a method as claimed in claim 22.

[0028] In an embodiment of the invention, when the first transistor may be an N-type transistor, the low voltage of the first power source signal may be lower than the low voltage of the first driving signal, and the low voltages of the first power source signal and the first driving signal may be lower than a voltage of second power source signal applied to a cathode electrode of the organic light emitting diode.

[0029] In an embodiment of the invention, when the first transistor may be a P-type transistor, the low voltage of the first power source signal may be higher than the low voltage of the first driving signal, and the low voltages of the first power source signal and the first driving signal may be lower than a voltage of second power source signal applied to a cathode electrode of the organic light emitting diode.

[0030] In an embodiment of the invention, a difference between the high and low voltages of the first driving signal may be applied to a control electrode of the first transistor, a high voltage of the first driving signal being preset based on a turn-on voltage of the first transistor.

[0031] In an embodiment of the invention, the method may further include applying a reference voltage to a data line before the data line receives a data voltage corresponding to a first horizontal line of a plurality of horizontal lines, and applying the reference voltage to the data line after the data line receives a data voltage corresponding to a last horizontal line of a plurality of horizontal lines.

[0032] In an embodiment of the invention, the data line may receive the reference voltage before a control electrode of the first transistor receives the high voltage of the first driving signal.

[0033] In an embodiment of the invention, each of initializing the anode electrode, diode-coupling the first transistor and emitting the light from the organic light emitting diode may be simultaneously performed in all pixels.

[0034] According to an embodiment of the inventive concept, there is provided a display device. The display

device includes a plurality of pixels. A pixel of the plurality of pixels includes a first transistor comprising a control electrode connected to a first node, a first electrode connected to a second voltage line receiving a first power source signal and a second electrode connected to a second node, a first capacitor connected between a first voltage line receiving a first driving signal and the first node, an organic light emitting diode comprising an anode electrode connected to the second node and a cathode electrode receiving a second power source signal, and a second capacitor connected between an m-th data line and the second node (wherein, 'm' is a natural number.

[0035] In an embodiment of the invention, the pixel may further include a second transistor comprising a control electrode connected to an n-th scan line (wherein, 'n' is a natural number), a first electrode connected to the first node and a second electrode connected to the second node

In an embodiment of the invention, the pixel may further include a third transistor comprising a control electrode connected to a third voltage line receiving a second driving signal, a first electrode connected to the first voltage line and a second electrode connected to the second node.

[0036] In an embodiment of the invention, each of the first, second and third transistors may be an N-type transistor, and a low voltage of the first driving signal is greater than a sum of a low voltage of the first power source and a threshold voltage of the first transistor and less than a sum of the second power source signal and a turn on voltage of the organic light emitting diode.

[0037] In an embodiment of the invention, each of the first, second and third transistors is a P-type transistor, and a low voltage of the first power source signal is greater than a low voltage of the first driving signal and less than the second power source signal.

[0038] According to the inventive concept, the pixel circuit may include only three transistors and two capacitors and thus, an ultra high definition display may be easily designed using the pixel circuit. In addition, the compensating period in the frame period may be freely controlled and thus, sufficiently obtained. In addition, whether the organic light emitting diode emits or not the light may be controlled by adjusting a level of the first power source signal.

[0039] At least some of the above and other features of the invention are set out in the claims.

BRIEF DESRCIPTION OF THE DRAWINGS

[0040] The above and other features and advantages of the inventive concept will be made more apparent by describing in detail embodiments thereof with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram illustrating a display apparatus according to an embodiment of the invention;

FIG. 2 is a circuit diagram illustrating a pixel circuit according to an embodiment of the invention;

FIG. 3 is a timing chart illustrating a plurality of input signals of a display apparatus according to an embodiment of the invention;

FIGS. 4A and 4B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention;

FIGS. 5A and 5B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention;

FIGS. 6A and 6B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention;

FIGS. 7A and 7B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention;

FIG. 8 is a circuit diagram illustrating a pixel circuit according to an embodiment of the invention;

FIG. 9 is a timing chart illustrating a plurality of input signals of a display apparatus according to an embodiment of the invention;

FIGS. 10 to 12 are circuit diagrams illustrating pixel circuits according to embodiments of the invention;

FIG. 13 is a plan view illustrating a display part of a display apparatus according to an embodiment of the invention;

FIG. 14 is a cross-sectional view taken along a line I-I' of FIG. 13; and

FIGS. 15 to 19 are plan views illustrating a method of manufacturing of the display part according to an embodiment of the invention.

DETAILED DESRCIPTION

[0041] Hereinafter, embodiments of the inventive concept will be explained in detail with reference to the accompanying drawings.

[0042] FIG. 1 is a block diagram illustrating a display apparatus according to an embodiment of the invention.

[0043] Referring to FIG. 1, the display apparatus may include a controller 100, a display part 110, a data driver 130, a scan driver 150 and a voltage generator 170.

[0044] The controller 100 may be configured to generally control the display apparatus to display an image on the display part 110. The controller 100 is configured to receive a control signal 101c and image data 101d. The controller 100 is configured to provide the data driver 130 with a data control signal 103c and the image data 103d in order to drive the data driver 130. The controller 100 is configured to provide the scan driver 150 with a scan control signal 105c in order to drive the scan driver 150. The controller 100 is configured to provide the voltage generator 170 with a voltage control signal 107c in order to drive the voltage generator 170.

[0045] The controller 100 is configured to drive the display part 110 during a frame period which may include an initializing period, a compensating period, a data-pro-

gramming period and a light-emitting period.

[0046] The display part 110 may include a plurality of pixels P, a plurality of data lines DL1,.., DLm,..., DLM, a plurality of scan lines SL1,..., SLn,..., SLN, a first voltage line VL1, a second voltage line VL2 and a third voltage line VL3.

[0047] Each of the plurality of pixels P may include an organic light emitting diode and three transistors and two capacitors, which drive the organic light emitting diode.

[0048] The data lines DL1, ..., DLm, ..., DLM may respectively extend in a first direction D1 and be arranged in a second direction D2 crossing the first direction D1. Each data line DLm is configured to transfer a data voltage to pixels P in a same pixel-column which are arranged in the first direction D1.

[0049] The scan lines SL1,..., SLn,..., SLN may extend in the second direction D2 and be arranged in the first direction D1. Each scan line SLn is configured to transfer a scan signal to pixels P in a same pixel-row which are arranged in the second direction D2.

[0050] The first voltage line VL1 may transfer a first driving signal Vinit to the plurality of pixels P and the plurality of pixels P may commonly use the first voltage line VL1.

[0051] The second voltage line VL2 may transfer a first power source signal ELVDD to the plurality of pixels P and the plurality of pixels P may commonly use the second voltage line VL2.

[0052] The third voltage line VL3 may transfer a second driving signal Vcomp to the plurality of pixels P and the plurality of pixels P may commonly use the third voltage line VL3.

[0053] The data driver 130 is configured to provide the data lines DL1,.., DLm,..., DLM with the data voltage corresponding to the image data during the data-programming period of the frame period.

[0054] In addition, the data driver 130 is configured to provide the data lines DL1,.., DLm,..., DLM with a reference voltage before or after the data-programming period. The reference voltage may be equal to or lower than a black voltage corresponding to a black grayscale.

[0055] The scan driver 150 is configured to sequentially provide the scan lines SL1,..., SLn,..., SLN with the scan signals. The scan signal may have a high voltage and a low voltage.

[0056] The voltage generator 170 is configured to generate the first driving signal Vinit, the second driving signal Vcomp, the first power source signal ELVDD and a second power source signal ELVSS.

[0057] The first driving signal Vinit is applied to the first voltage line VL1 and has a high voltage and a low voltage. The high voltage and the low voltage of the first driving signal Vinit may have predetermined high and low voltages for driving the pixel P, respectively.

[0058] The second driving signal Vcomp is applied to the third voltage line VL3 and has a high voltage and a low voltage. The high voltage and the low voltage of the second driving signal Vcomp may respectively correspond to the high voltage and the low voltage of the scan signal.

[0059] The first power source signal ELVDD is applied to the second voltage line VL2 and has a high voltage and a low voltage. The high voltage of the first power source signal ELVDD may have a high voltage of a normal positive power source signal and the low voltage of the first power source signal ELVDD may have a predetermined low voltage for driving the pixel P.

[0060] The second power source signal ELVSS is applied to a common electrode of the pixels P, that is a cathode electrode of an organic light emitting diode and may have a low voltage of a normal negative power source signal.

[0061] FIG. 2 is a circuit diagram illustrating a pixel circuit according to an embodiment of the invention.

[0062] Referring to FIGS. 1 and 2, the pixel circuit PC1 may be included in the pixel P of the display part 110. The pixel circuit PC1 is an equivalent circuit of the pixel P.

[0063] The pixel circuit PC1 may include a first transistor T1, a second transistor T2, a third transistor T3, a first capacitor Cst, a second capacitor Cpr and an organic light emitting diode OLED.

[0064] According to this embodiment, each of the first, second and third transistors T1, T2 and T3 may be an N-type transistor. The N-type transistor may be turned on when a high voltage is applied to a control electrode, and turned off when a low voltage is applied to the control electrode. According to the embodiment, the high voltage may be a turn-on voltage of the N-type transistor and the low voltage may be a turn-off voltage of the N-type transistor.

[0065] The first transistor T1 may include a control electrode CE1 connected to a first node N1, a first electrode E11 connected to a second voltage line VL2 and a second electrode E12 connected to a second node N2. The second voltage line VL2 is configured to receive the first power source signal ELVDD.

[0066] The first power source signal ELVDD may have a high voltage which is a voltage of a normal positive power source signal and a low voltage which is a predetermined low voltage for driving the pixel circuit PC1. The first power source signal ELVDD may have the low voltage during the compensating period in which a threshold voltage of the first transistor T1 is compensated, and the high voltage during a remaining period of the frame period except for the compensating period.

[0067] The second transistor T2 may include a control electrode CE2 connected to the n-th scan line SLn, a first electrode E21 connected to the first node N1 and a second electrode E22 connected to the second node N2. The n-th scan line SLn is configured to receive an n-th scan signal S(n). The n-th scan signal S(n) may have a high voltage which turns on the second transistor T2 and a low voltage which turns off the second transistor T2. The second transistor T2 may diode-couple the first transistor T1 during the compensating period. That is, the second transistor T2 may connect the control electrode

CE1 and the second node N2 of the first transistor T1 during the compensating period.

[0068] The third transistor T3 may include a control electrode CE3 connected to the third voltage line VL3, a first electrode E31 connected to the first voltage line VL1 and a second electrode E32 connected to the second node N2. The first voltage line VL1 is configured to receive a first driving signal Vinit.

[0069] The first driving signal Vinit may have high and low voltages which are predetermined high and low voltages driving the pixel circuit PC1. The first driving signal Vinit has the high voltage during the light-emitting period during which the organic light emitting diode OLED emits the light, and the low voltage during a remaining period of the frame period except for the light-emitting period.

[0070] The third voltage line VL3 is configured to receive the second driving signal Vcomp. The second driving signal Vcomp may have a high voltage which turns on the third transistor T3 and a low voltage which turns off the third transistor T3.

[0071] The first capacitor Cst may be connected between the first voltage line VL1 and the first node N1. The first capacitor Cst may store a node voltage applied to the first node N1.

[0072] The second capacitor Cpr may be connected between the second node N2 and m-th data line DLm. The second capacitor Cpr may store the data voltage applied to the m-th data line DLm.

[0073] The first and second capacitors Cst and Cpr may be serially connected between the m-th data line DLm and the first voltage line VL1 through the second transistor T2. The data voltage applied to the m-th data line DLm may be divided by a voltage division ratio of the first and second capacitors Cst and Cpr and divided data voltage may be applied to the first node N1.

[0074] The organic light emitting diode OLED may include an anode electrode connected to the second node N2 and a cathode electrode which receives the second power source signal ELVSS.

[0075] When the transistor T1 is turned on, a driving current corresponding to the data voltage applied to the first node N1 may flow through the organic light emitting diode OLED and thus, the organic light emitting diode OLED may emit the light.

[0076] FIG. 3 is a timing chart illustrating a plurality of input signals of a display apparatus according to an embodiment of the invention.

[0077] Referring to FIGS. 1, 2 and 3, the display part may receive a plurality of input signals. The plurality of input signal may include the first power source signal ELVDD applied to the second voltage line VL2, the first driving signal Vinit applied to the first voltage line VL1, the second driving signal Vcomp applied to the third voltage line VL3, a plurality of scan signals S(1),.., S(n),.. S(N) applied to the plurality of scan lines, a data voltage DATA applied to the plurality of data lines and the second power source signal ELVSS applied to the cathode electrode of the organic light emitting diode OLED. The data voltage DATA may be referred to as a data voltage applied to the m-th data line DLm of the plurality of data lines.

[0078] The frame period may include a first period 'a' during which the anode electrode of the organic light emitting diode OLED is initialized, a second period 'b' during which the threshold voltage of the first transistor T1 is compensated, a third period 'c' during which the data voltage is applied to the pixel and a fourth period 'd' during which the organic light emitting diode OLED emit the light.

[0079] Referring to the first period 'a', the first voltage line VL1 receives a low voltage initL of the first driving signal Vinit. The low voltage initL of the first driving signal Vinit may be defined as the following Equation 1.

Equation 1

$$ELVDD_L + V_{th,T1} < Init_L < ELVSS + V_{on,OLED}$$

In Equation 1, $Vth_{,T1}$ represents a threshold voltage of the first transistor T1, $Von_{,OLED}$ represents a minimum voltage of the organic light emitting diode OLED while the organic light emitting diode OLED emits the light ('a turn on voltage of the organic light emitting diode OLED').

[0080] The third voltage line VL3 may receive a high voltage VGH of the second driving signal Vcomp. The high voltage VGH of the second driving signal Vcomp may have a turn-on voltage of the third transistor T3. For example, the high voltage VGH of the second driving signal Vcomp may be about 10 V.

[0081] The second voltage line VL2 may receive a high voltage ELVDDH of the first power source signal ELVDD. The high voltage ELVDDH of the first power source signal ELVDD may have a voltage of a normal positive power source signal.

[0082] For example, the low voltage initL of the first driving signal Vinit may be about -2.2 V, the high voltage $ELVDD_H$ of the first power source signal ELVDD may be about 7 V, the low voltage ELVDDL of the first power source signal ELVDD may be about -7 V, and the second power source signal ELVSS may be about 0 V.

[0083] The plurality of scan lines SL1,.., SLn,..., SLN may simultaneously receive the high voltages VGH of the plurality of scan signals S(1),.., S(n),.. S(N). The high voltage VGH of the scan signal may have a turn-on voltage of the second transistor T2. For example, the high voltage VGH of the scan signal may be about 10 V.

[0084] The plurality of data lines DL1,.., DLm,..., DLM may receive a reference voltage Vref. The reference voltage Vref may be equal to or lower than a lowest voltage in a voltage range of the data voltage. For example, when the voltage range of the data voltage is about 0.5V to about 7.5 V, the reference voltage Vref may be equal to or lower than about 0.5 V.

[0085] During the first period 'a', the anode electrodes of the organic light emitting diodes OLED which is connected to the second node N2 and the first node N1 in all pixels may be initialized by the low voltage initL of the

first driving signal Vinit, simultaneously.

[0086] Referring to the second period 'b', the first voltage line VL1 is configured to receive the low voltage initL of the first driving signal Vinit.

[0087] The third voltage line VL3 is configured to receive a low voltage VGL of second driving signal Vcomp. The low voltage VGL of the second driving signal Vcomp may have a turn-off voltage of the third transistor T3. For example, the low voltage VGL of the second driving signal Vcomp may be about -10 V.

[0088] The second voltage line VL2 is configured to receive a low voltage ELVDDL of the first power source signal ELVDD. For example, the low voltage ELVDDL of the first power source signal ELVDD may be about -7 V.

[0089] The plurality of scan lines SL1,.., SLn,..., SLN is configured to simultaneously receive high voltages VGH of the plurality of scan signals S(1),.., S(n),.. S(N) as the first period 'a'.

[0090] The plurality of data lines DL1,.., DLm,..., DLM is configured to receive the reference voltage Vref as the first period 'a'.

[0091] During the second period 'b', the threshold voltages of the first transistors T1 in all pixels may be simultaneously compensated using the sum voltage of the low voltage ELVDDL of the first power source signal ELVDD and the threshold voltage $Vth_{,T1}$ of corresponding first transistor T1.

[0092] Referring to the third period 'c', the second voltage line VL2 is configured to receive a high voltage ELVDDH of the first power source signal ELVDD.

[0093] The first voltage line VL1 is configured to receive the low voltage initL of the first driving signal Vinit.

[0094] The third voltage line VL3 is configured to receive the low voltage VGL of the second driving signal Vcomp.

[0095] The plurality of scan lines SL1,.., SLn,.., SLN is configured to sequentially receive high voltages VGH of the plurality of scan signals S(1),.., S(n),.. S(N).

[0096] The plurality of data lines DL1,.., DLm,..., DLM is configured to receive the data voltage DATA respectively corresponding to the plurality of horizontal lines in synchronization with the high voltages VGH of the plurality of scan signals S(1),.., S(n),.. S(N).

[0097] The first node N1 is configured to receive divided data voltage by a voltage division ratio of the first and second capacitors Cst and Cpr during a corresponding horizontal period of the pixel.

[0098] In addition, the third period 'c' may include at least one holding period during which the plurality of data lines DL1,.., DLm,..., DLM is configured to receive a reference voltage Vref. The holding period may be disposed before a first horizontal period in which a data voltage of a first horizontal line is applied to the plurality of data lines DL1,.., DLm,..., DLM and after a last horizontal period in which a data voltage of a last horizontal line is applied to the plurality of data lines DL1,.., DLm,..., DLM. Therefore, the plurality of data lines DL1,.., DLm,..., DLM may be maintained into the reference voltage Vref during the holding period.

[0099] Referring to the fourth period 'd', the second voltage line VL2 is configured to receive the high voltage ELVDDH of the first power source signal ELVDD.

[0100] The first voltage line VL1 is configured to receive a high voltage initH of the first driving signal Vinit. The high voltage initH of the first driving signal Vinit may be determined based on a turn-on voltage of the first transistor T1. For example, the high voltage initH of the first driving signal Vinit may be about 6.5 V.

[0101] The third voltage line VL3 is configured to receive the low voltage VGL of the second driving signal Vcomp.

[0102] The plurality of scan lines SL1,.., SLn,..., SLN is configured to simultaneously receive the low voltages VGL of the plurality of scan signals S(1),.., S(n),.. S(N).

[0103] The plurality of data lines DL1,.., DLm,..., DLM is configured to simultaneously receive the reference voltage Vref.

[0104] During the fourth period 'd', driving current corresponding to the data voltage applied to the first node N1 may be provided to the organic light emitting diode OLED and the organic light emitting diode OLED may emit the light. Thus, the organic light emitting diodes OLED in all pixels may simultaneously emit the light.

[0105] FIGS. 4A and 4B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention.

[0106] Referring to FIGS. 4A and 4B, the first period 'a' may correspond to an initializing period of the organic light emitting diode OLED.

[0107] In the first period 'a', the low voltage initL of first driving signal Vinit is applied to the first voltage line VL1, the high voltage VGH of the second driving signal Vcomp is applied to the third voltage line VL3, and the high voltage ELVDDH of the first power source signal ELVDD is applied to the second voltage line VL2. The n-th scan line SLn receives the high voltage VGH of the n-th scan signal S(n). The m-th data line DLm receives the reference voltage Vref.

[0108] Referring to a method of driving the pixel circuit PC1, the low voltage initL of the first driving signal Vinit is applied to the first node N1. The second transistor T2 is turned on in response to the high voltage VGH of the n-th scan signal S(n).

[0109] The third transistor T3 is turned on in response to the high voltage VGH of the second driving signal Vcomp, and then the low voltage initL of the first driving signal Vinit is provided to the second node N2. The anode electrode of the organic light emitting diode OLED connected to the second node N2 may be initialized by the low voltage initL of the first driving signal Vinit.

[0110] Therefore, during the first period 'a', the organic light emitting diode OLED may be initialized.

[0111] FIGS. 5A and 5B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention.

[0112] Referring to FIGS. 5A and 5B, the second pe-

riod 'b' may correspond to a compensating period during which the threshold voltage of the first transistor T1 is compensated.

[0113] In the second period 'b', the low voltage initL of the first driving signal Vinit is applied to the first voltage line VL1, the low voltage VGL of the second driving signal Vcomp is applied to the third voltage line VL3, the low voltage ELVDDL of the first power source signal ELVDD is applied to the second voltage line VL2. The n-th scan line SLn receives the high voltage VGH of the n-th scan signal S(n). The m-th data line receives the reference voltage Vref.

[0114] The second transistor T2 is turned on in response to the high voltage VGH of the n-th scan signal S(n). The third transistor T3 is turned off in response to the low voltage VGL of the second driving signal Vcomp.

[0115] When the second transistor T2 is turned on, the control electrode CE1 and the second electrode E12 of the first transistor T1 are connected to each other and the low voltage $ELVDD_L$ of the first power source signal ELVDD is applied to the first electrode E11 of the first transistor T1.

[0116] Because a drain electrode E12 which has a higher voltage than a source electrode E11 is connected to the gate, the transistor is diode-connected..

[0117] A voltage applied to the first electrode E11 of the first transistor T1 is determined to be lower than the low voltage initL of the first driving signal Vinit applied to the second electrode E12 and thus, the first electrode E11 may drive as the source and the second electrode E12 may drive as the drain.

[0118] Therefore, when the second transistor T2 is turned on, the gate and drain of the first transistor T1 are connected to each other and the first transistor T1 is diode-connected.

[0119] When the first transistor T1 is diode-connected, the first node N1 connected to the control electrode CE1 of the first transistor T1 receives a voltage corresponding to a sum voltage of the low voltage $ELVDD_L$ of the first power source signal and the threshold voltage Vth,T1 of the first transistor T1.

[0120] Therefore, the threshold voltage of the first transistor T1 may be compensated.

[0121] According to the embodiment of the invention, a length of the second period 'b' may be freely adjusted in the frame period and thus a sufficient compensating period may be obtained.

[0122] FIGS. 6A and 6B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention.

[0123] Referring to FIGS. 6A and 6B, the third period 'c' may correspond to a data-programming period during which the data voltage is applied to the plurality of pixels.

[0124] In the third period 'c', the low voltage initL of the first driving signal Vinit is applied to the first voltage line VL1, the low voltage VGL of the second driving signal Vcomp is applied to the third voltage line VL3, and the high voltage $ELVDD_H$ of the first power source signal ELVDD is applied to the second voltage line VL2. The n-th scan line SLn receives a high voltage VGH of an n-th scan signal S(n) during an n-th horizontal period Hn of the third period 'c'. The m-th data line DLm receives an n-th data voltage Vdata(n) of an n-th horizontal line corresponding to the n-th horizontal period Hn during the n-th horizontal period Hn.

[0125] Referring to the method of driving the pixel circuit PC1, the first transistor T1 which has the control electrode CE1 connected to the first node N1 is turned off because V_{GS} of the first transistor T1 is less than the threshold voltage Vth,T1. The first node N1 receives a voltage ($ELVDD_L$ + Vth,T1+$\alpha\Delta$Vdata) corresponding to a sum voltage of the low voltage $ELVDD_L$ of the first power source signal ELVDD, the threshold voltage Vth,T1 of the first transistor T1 and a divided voltage $\alpha\Delta$Vdata. The third transistor T3 is turned off in response to the low voltage VGL of the second driving signal Vcomp.

[0126] The second transistor T2 is turned on in response to the high voltage VGH of the n-th scan signal S(n), and then the first node N1 is connected to the second node N2. The first capacitor Cst and the second capacitor Cpr are connected to the first node N1 in series by the turned-on second transistor T2.

[0127] The n-th data voltage Vdata(n) corresponding to the pixel circuit PC1 is applied to the m-th data line DLm. The m-th data line DLm receives a difference voltage ΔVdata between the n-th data voltage Vdata(n) and the reference voltage Vref.

[0128] The first and second capacitors Cst and Cpr which are connected to the first node N1 in series has a voltage division ratio α corresponding to the first node N1. The voltage division ratio α and the difference voltage ΔVdata may be defined as the following Equation 2.

Equation 2

$$\alpha = \frac{C_{pr}}{C_{st}+C_{pr}}$$

$$\Delta V_{data} = V_{data(n)} - V_{ref}$$

[0129] Therefore, the difference voltage ΔVdata is divided by the voltage division ratio α of the first and second capacitors Cst and Cpr and divided voltage $\alpha\Delta$Vdata corresponding to the n-th data voltage Vdata(n) is applied to the first node N1.

[0130] Therefore, a voltage defined as the following Equation 3 may be applied to the first node N1 during the n-th horizontal period Hn.

Equation 3

$$ELVDD_L + V_{th,T1} + \alpha \cdot \Delta V_{data}$$

[0131] According to the exemplary embodiment, the third period 'c' may include a first holding period h1 corresponding to an early period of the third period 'c' and a second holding period h2 corresponding to a late period of the third period 'c'.

[0132] The first holding period h1 may correspond to a period which is before a first horizontal period in which a data voltage Vdata(1) of a first horizontal line is applied to the plurality of data lines DL1,.., DLm,..., DLM. During the first holding period h1, the reference voltage Vref is applied to the plurality of data lines DL1,.., DLm,..., DLM and thus, the plurality of data lines DL1,.., DLm,..., DLM may hold the reference voltage Vref before the first horizontal period.

[0133] The second holding period h2 may correspond to a period which is after an N-th horizontal period in which the data voltage Vdata(N) of an N-th horizontal line, that is a last horizontal line, is applied to the plurality of data lines DL1,.., DLm,..., DLM. During the second holding period h2, the reference voltage Vref is applied to the plurality of data lines DL1,.., DLm,..., DLM and thus, the plurality of data lines DL1,.., DLm,..., DLM may hold the reference voltage Vref after the N-th horizontal period.

[0134] FIGS. 7A and 7B are conceptual diagrams illustrating a method of driving the pixel circuit according to an embodiment of the invention.

[0135] Referring to FIGS. 7A and 7B, the fourth period 'd' may correspond to a light-emitting period during which the organic light emitting diode OLED emits the light.

[0136] Referring to the fourth period 'd', the high voltage initH of the first driving signal Vinit is applied to the first voltage line VL1, the low voltage VGL of the second driving signal Vcomp is applied to the third voltage line VL3, and the high voltage $ELVDD_H$ of the first power source signal ELVDD is applied to the second voltage line VL2. The n-th scan line SLn receives the low voltage VGL of the n-th scan signal S(n). The m-th data line DLm receives the reference voltage Vref.

[0137] Referring to the method of driving the pixel circuit PC1, the high voltage initH of the first driving signal Vinit is applied to the first node N1 and thus, a voltage defined as the following Equation 4 may be applied to the first node N1.

Equation 4

$$ELVDD_L + V_{th,T1} + \alpha \cdot \Delta V_{data} + \Delta V_{init}$$

In Equation 4, a difference voltage ΔVinit represents a difference voltage between the high and low voltages initH and initL of the first driving signal Vinit.

[0138] When the voltage defined as the following Equation 4 is applied to the control electrode CE1 of the first transistor T1, the first transistor T1 is turned on based on the difference voltage ΔVinit.

[0139] The second transistor T2 is turned off in response to the low voltage VGL of the n-th scan signal S(n) and the third transistor T3 is turned off in response to the low voltage VGL of the second driving signal Vcomp.

[0140] Therefore, the first transistor T1 is turned on and thus, a driving current ID corresponding to the data voltage may flow through the organic light emitting diode OLED. The organic light emitting diode OLED may emit the light.

[0141] According to the embodiment of the invention, the pixel circuit may include only three transistors and two capacitors and thus, an ultra high definition display may be easily designed using the pixel circuit. In addition, the length of the compensating period in the frame period may be freely controlled and thus, a sufficient compensation period is obtained. In addition, whether the organic light emitting diode emits or not the light may be controlled by adjusting a level of the first power source signal ELVDD.

[0142] FIG. 8 is a circuit diagram illustrating a pixel circuit according to an embodiment of the invention.

[0143] Referring to FIG. 8, the pixel circuit PC2 may include a first transistor T1, a second transistor T2, a third transistor T3, a first capacitor Cst, a second capacitor Cpr and an organic light emitting diode OLED.

[0144] The pixel circuit PC2 may include three transistors and two capacitors as the pixel circuit PC1 described in the previous embodiment. However, each of the first, second and third transistors T1, T2 and T3 according to the embodiment may be a P-type transistor. The P-type transistor is turned on when a control electrode of the P-type transistor receives a low voltage and is turned off when the control electrode of the P-type transistor receives a high voltage. According to this embodiment, the low voltage may be a turn-on voltage of the transistor and the high voltage may be a turn-off voltage of the transistor.

[0145] Hereinafter, the same reference numerals are used to refer to the same or like parts as those described in the previous embodiments, and the same detailed explanations are not repeated unless necessary.

[0146] The first transistor T1 may include a control electrode CE1 connected to a first node N1, a first electrode E11 connected to a second voltage line VL2 and a second electrode E12 connected to a second node N2. The second voltage line VL2 is configured to receive the first power source signal ELVDD.

[0147] The first power source signal ELVDD may have a high voltage which is a voltage of a normal positive power source signal and a low voltage which is a predetermined low voltage for driving the pixel circuit PC2.

[0148] The second transistor T2 may include a control electrode CE2 connected to the n-th scan line SLn, a first

electrode E21 connected to the first node N1 and a second electrode E22 connected to the second node N2. The n-th scan line SLn is configured to receive an n-th scan signal S(n). The n-th scan signal S(n) may have a low voltage which turns on the second transistor T2 and a high voltage which turns off the second transistor T2.

[0149] The third transistor T3 may include a control electrode CE3 connected to the third voltage line VL3, a first electrode E31 connected to the first voltage line VL1 and a second electrode E32 connected to the second node N2. The first voltage line VL1 is configured to receive a first driving signal Vinit and the third voltage line VL3 is configured to receive a second driving signal Vcomp.

[0150] The first driving signal Vinit may have high and low voltages which are predetermined high and low voltages for driving the pixel circuit PC2.

[0151] The second driving signal Vcomp may have a low voltage which turns on the third transistor T3 and a high voltage which turns off the third transistor T3. For example, the high and low voltages of the second driving signal Vcomp may be equal to those of the n-th scan signal S(n), respectively.

[0152] The first capacitor Cst may be connected between the first voltage line VL1 and the first node N1. The first capacitor Cst may store a node voltage applied to the first node N1.

[0153] The second capacitor Cpr may be connected between the second node N2 and m-th data line DLm. The second capacitor Cpr may store the data voltage applied to the m-th data line DLm.

[0154] The first and second capacitors Cst and Cpr may be connected to the first node in series N1 through the second transistor T2. The data voltage applied to the m-th data line DLm may be divided by a voltage division ratio of the first and second capacitors Cst and Cpr and then, divided data voltage may be applied to the first node N1.

[0155] The organic light emitting diode OLED may include an anode electrode connected to the second node N2 and a cathode electrode which receives the second power source signal ELVSS. The second power source signal ELVSS may have a low voltage of a normal negative power source signal.

[0156] When the transistor T1 is turned on, a driving current corresponding to the data voltage of the first node N1 may flow through the organic light emitting diode OLED and thus, the organic light emitting diode OLED may emit the light.

[0157] FIG. 9 is a timing chart illustrating a plurality of input signals of a display apparatus according to an embodiment of the invention.

[0158] Referring to FIGS. 8 and 9, the frame period may include a first period 'a' during which the anode electrode of the organic light emitting diode OLED is initialized, a second period 'b' during which the threshold voltage of the first transistor T1 is compensated, a third period 'c' during which the data voltage is programmed and a fourth period 'd' during which the organic light emitting diode OLED emit the light.

[0159] Referring to the first period 'a', a first voltage line VL1 receives a low voltage initL of the first driving signal Vinit. The third voltage line VL3 may receive a low voltage VGL of the second driving signal Vcomp. The second voltage line VL2 may receive a low voltage $ELVDD_L$ of the first power source signal ELVDD. The cathode electrode of the organic light emitting diode OLED may receive a second power source signal ELVSS.

[0160] The low voltage initL of the first driving signal Vinit and the second power source signal ELVSS may be defined as the following Equation 5.

Equation 5

$$ELVSS > ELVDD_L > init_L$$

[0161] For example, the low voltage initL of the first driving signal Vinit may be about -6 V, the low voltage ELVDDL of the first power source signal ELVDD may be about -2 V, and the second power source signal ELVSS may be about 0 V.

[0162] The plurality of scan lines SL1,.., SLn,..., SLN may simultaneously receive the low voltages VGL of the plurality of scan signals S(1),.., S(n),.. S(N). Thus, an n-th scan line SLn receives the low voltage VGL of an n-th scan signal S(n). For example, the low voltage VGL of the scan signal may be about -10 V.

[0163] The plurality of data lines DL1,.., DLm,..., DLM may receive a reference voltage Vref. The reference voltage Vref may be equal to or lower than a lowest voltage in a voltage range of the data voltage. For example, when the voltage range of the data voltage is about 1.5 V to about 4.5 V, the reference voltage Vref may be equal to or lower than about 1.5 V.

[0164] Referring to a method of driving the pixel circuit PC2 in the first period 'a', the low voltage initL of the first driving signal Vinit is applied to the first node N1. The first transistor T1 is turned on in response to the low voltage initL of the first driving signal Vinit applied to the first node N1. The second transistor T2 is turned on in response to the low voltage VGL of the n-th scan signal S(n). The anode electrode of the organic light emitting diode OLED connected to the second node N2 may be initialized by the low voltage initL of the first driving signal Vinit.

[0165] The low voltage $ELVDD_L$ of the first power source signal ELVDD may be higher than the low voltage initL of the first driving signal Vinit. The low voltage ELVDDL of the first power source signal ELVDD is applied to the second node N2 through the turned-on first transistor T1.

[0166] During the first period 'a', the anode electrodes of the organic light emitting diodes OLED in all pixels may be initialized by the low voltage initL of the first driving signal Vinit, simultaneously.

[0167] Referring to the second period 'b', the first voltage line VL1 is configured to receive the low voltage initL of the first driving signal Vinit, the third voltage line VL3 is configured to receive the high voltage VGH of second driving signal Vcomp, and the second voltage line VL2 is configured to receive a low voltage $ELVDD_L$ of the first power source signal ELVDD. The cathode electrode of the organic light emitting diode OLED is configured to receive the second power source signal ELVSS.

[0168] The plurality of scan lines SL1,.., SLn,..., SLN is configured to simultaneously receive low voltages VGL of the plurality of scan signals S(1),.., S(n),.. S(N) as the first period 'a'.

[0169] The plurality of data lines DL1,.., DLm,..., DLM is configured to receive the reference voltage Vref as the first period 'a'.

[0170] Referring to the method of driving the pixel circuit PC2 in the second period 'b', the second transistor T2 is turned on in response to the low voltage VGL of the n-th scan signal S(n). The third transistor T3 is turned off in response to the high voltage VGH of the second driving signal Vcomp.

[0171] The control electrode CE1 and the second electrode E12 of the first transistor T1 are connected to each other through the turned-on second transistor T2. The first transistor T1 of the P-type transistor includes the first electrode E11 receiving the low voltage EVDDL of the first power source signal ELVDD and the second electrode E12 receiving the low voltage initL of the first driving signal. Thus, the first electrode E11 of the first transistor T1 may drive as the source and the second electrode E12 may drive as the drain. Therefore, the gate and the drain of the first transistor T1 may be connected through the turned-on second transistor T2 and thus, the first transistor T1 may be diode-connected. The first node N1 connected to the control electrode CE1 of the first transistor T1 receives a voltage corresponding to a difference voltage between the low voltage $ELVDD_L$ of the first power source signal and the threshold voltage Vth,T1 of the first transistor T1. When the first transistor T1 is the P-type transistor, the threshold voltage of the first transistor T1 may be a negative voltage. Hereinafter, the threshold voltage of the first transistor T1 being the P-type transistor may be an absolute value of the threshold voltage being the negative number.

[0172] Therefore, the threshold voltages of the first transistors T1 in all pixels may be simultaneously compensated using the difference voltage between the low voltage ELVDDL of the first power source signal ELVDD and the threshold voltage Vth,T1 of corresponding first transistor T1.

[0173] Referring to the third period 'c', the first voltage line VL1 is configured to receive the low voltage initL of the first driving signal Vinit, the third voltage line VL3 is configured to receive the high voltage VGH of the second driving signal Vcomp, and the second voltage line VL2 is configured to receive the low voltage ELVDDL of the first power source signal ELVDD. The cathode electrode of the organic light emitting diode OLED is configured to receive the second power source signal ELVSS.

[0174] The plurality of scan lines SL1,.., SLn,.., SLN is configured to sequentially receive low voltages VGL of the plurality of scan signals S(1),.., S(n),.. S(N). The plurality of data lines DL1,.., DLm,..., DLM is configured to receive the data voltage DATA corresponding to the plurality of horizontal lines in synchronization with the low voltages VGL of the plurality of scan signals S(1),.., S(n),.. S(N).

[0175] Therefore, the n-th scan line SLn receives the low voltage VGL of an n-th scan signal S(n) during an n-th horizontal period Hn of the third period 'c'. The m-th data line DLm receives an n-th data voltage Vdata(n) of an n-th horizontal line corresponding to the n-th horizontal period Hn during the n-th horizontal period Hn.

[0176] Referring to the method of driving the pixel circuit PC2 in the third period 'c', the low voltage $ELVDD_L$ of the first power source signal ELVDD is applied to the first electrode E11 of the first transistor T1, and a voltage corresponding to the n-th data voltage Vdata(n) is applied to the second electrode E12 of the first transistor T1. A high voltage higher than a voltage of the first electrode E11 of the first transistor T1 is applied to the second electrode E12 of the first transistor T1 and thus, a current may not flow through the first transistor T1.

[0177] The second transistor T2 is turned on in response to the low voltage VGL of the n-th scan signal S(n), and then the first node N1 is connected to the second node N2. The first capacitor Cst and the second capacitor Cpr are connected to the first node N1 in series through the turned-on second transistor T2.

[0178] The first transistor T1 which has the control electrode CE1 connected to the first node N1 is turned off. The first node N1 receives a voltage corresponding to a difference voltage between the low voltage $ELVDD_L$ of the first power source signal ELVDD and the threshold voltage Vth,T1 of the first transistor T1.

[0179] The third transistor T3 is turned off in response to the high voltage VGH of the second driving signal Vcomp.

[0180] The n-th data voltage Vdata(n) corresponding to the pixel circuit PC2 is applied to the m-th data line DLm. The m-th data line DLm receives a difference voltage (ΔVdata = Vdata(n)-Vref) between the n-th data voltage Vdata(n) and the reference voltage Vref.

[0181] The first and second capacitors Cst and Cpr which are connected to the first node N1 in series has a voltage division ratio α corresponding to the first node N1.

[0182] The difference voltage ΔVdata is divided by the voltage division ratio α of the first and second capacitors Cst and Cpr and the divided voltage α ΔVdata corresponding to the n-th data voltage Vdata(n) is applied to the first node N1.

[0183] Therefore, a voltage defined as the following Equation 6 may be applied to the first node N1 during the n-th horizontal period Hn.

Equation 6

$$ELVDD_L - V_{th,T1} + \alpha \cdot \Delta V_{data}$$

[0184] According to this embodiment of the invention, the third period 'c' may include a first holding period h1 corresponding to an early period of the third period 'c' and a second holding period h2 corresponding to a late period of the third period 'c'.

[0185] The first holding period h1 may correspond to a period which is before a first horizontal period in which the data voltage Vdata(1) of a first horizontal line is applied to the plurality of data lines DL1,.., DLm,..., DLM. During the first holding period h1, the reference voltage Vref is applied to the plurality of data lines DL1,.., DLm,..., DLM and thus, the plurality of data lines DL1,.., DLm,..., DLM may hold the reference voltage Vref before the first horizontal period.

[0186] The second holding period h2 may correspond to a period which is after an N-th horizontal period in which the data voltage Vdata(N) of an N-th horizontal line, that is a last horizontal line, is applied to the plurality of data lines DL1,.., DLm,..., DLM. During the second holding period h2, the reference voltage Vref is applied to the plurality of data lines DL1,.., DLm,..., DLM and thus, the plurality of data lines DL1,.., DLm,..., DLM may hold the reference voltage Vref after the N-th horizontal period.

[0187] Referring to the fourth period 'd', the high voltage initH of the first driving signal Vinit is applied to the first voltage line VL1. The high voltage initH of the first driving signal Vinit may be determined to a predetermined voltage for turning on the first transistor T1. For example, the high voltage initH of the first driving signal Vinit may be about 2.5 V.

[0188] The third voltage line VL3 is configured to receive the high voltage VGH of the second driving signal Vcomp.

[0189] The second voltage line VL2 is configured to receive the high voltage ELVDDH of the first power source signal ELVDD. For example, the high voltage ELVDDH of the first power source signal ELVDD may be about 7 V.

[0190] The cathode electrode of the organic light emitting diode OLED is configured to receive the second power source signal ELVSS.

[0191] The plurality of scan lines SL1,.., SLn,, SLN is configured to simultaneously receive high voltages VGH of the plurality of scan signals S(1),.., S(n),.. S(N).

[0192] The plurality of data lines DL1,.., DLm, ..., DLM is configured to simultaneously receive the reference voltage Vref.

[0193] Referring to the method of driving the pixel circuit PC2 in the fourth period 'd', the first node N1 may have a node voltage as the following Equation 7.

Equation 7

$$ELVDD_L - V_{th,T1} + \alpha \cdot \Delta V_{data} + \Delta V_{init}$$

In Equation 7, the difference voltage ΔVinit represents a difference voltage between the high and low voltages initH and initL of the first driving signal Vinit.

[0194] When the node voltage defined as the following Equation 7 is applied to the control electrode CE1 of the first transistor T1, the first transistor T1 is turned on based on the difference voltage ΔVinit. Then, the high voltage $ELVDD_H$ of the first power source signal ELVDD is applied to the first electrode E11 of the first transistor T1 and thus, a driving current corresponding to the data voltage applied to the first node N, may flow through the organic light emitting diode OLED.

[0195] The second transistor T2 is turned off in response to the high voltage VGH of the n-th scan signal S(n) and the third transistor T3 is turned off in response to the high voltage VGH of the second driving signal Vcomp.

[0196] Therefore, during the fourth period 'd', driving currents corresponding to data voltages applied to the plurality of pixels, may flow through organic light emitting diodes OLEDs in the plurality of pixels and thus, the organic light emitting diodes OLEDs in the plurality of pixels may simultaneously emit the light.

[0197] According to this embodiment of the invention, the pixel circuit may include only three transistors and two capacitors and thus, an ultra high definition display may be easily designed using the pixel circuit. In addition, the compensating period in the frame period may be freely controlled and thus, sufficiently obtained. In addition, whether the organic light emitting diode emits or not the light may be controlled by adjusting a level of the first power source signal.

[0198] FIGS. 10 to 12 are circuit diagrams illustrating pixel circuits according to embodiments of the invention.

[0199] Referring to FIG. 10, a pixel circuit PC3 may include a first transistor T1, a second transistor T2, a third transistor T3, a first capacitor Cst, a second capacitor Cpr and an organic light emitting diode OLED. According to this embodiment, the second transistor T2 may have a dual gate structure to avoid a leakage current.

[0200] Each of the first, second and third transistors T1, T2 and T3 in the pixel circuit PC3 may be a N-type transistor. The pixel circuit PC3 having the N-type transistor may drive as the pixel circuit PC1 described in the previous embodiment referring to FIGS. 2 and 3.

[0201] Alternatively, each of the first, second and third transistors T1, T2 and T3 in the pixel circuit PC3 may be an P-type transistor. The pixel circuit PC3 having the P-type transistor may drive as the pixel circuit PC2 described in the previous embodiment referring to FIGS. 8 and 9.

[0202] Referring to FIG. 11, a pixel circuit PC4 may include a first transistor T1, a second transistor T2, a third

transistor T3, a first capacitor Cst, a second capacitor Cpr and an organic light emitting diode OLED. According to this embodiment, the third transistor T3 may have a dual gate structure to avoid a leakage current.

[0203] Each of the first, second and third transistors T1, T2 and T3 in the pixel circuit PC4 may be a N-type transistor. The pixel circuit PC4 having the N-type transistor may drive as the pixel circuit PC1 described in the previous embodiment referring to FIGS. 2 and 3.

[0204] Alternatively, each of the first, second and third transistors T1, T2 and T3 in the pixel circuit PC4 may be an P-type transistor. The pixel circuit PC4 having the P-type transistor may drive as the pixel circuit PC2 described in the previous embodiment referring to FIGS. 8 and 9.

[0205] Referring to FIG. 12, a pixel circuit PC5 may include a first transistor T1, a second transistor T2, a third transistor T3, a first capacitor Cst, a second capacitor Cpr and an organic light emitting diode OLED. According to this embodiment, the second and third transistors T2 and T3 may have a dual gate structure to avoid a leakage current.

[0206] Each of the first, second and third transistors T1, T2 and T3 in the pixel circuit PC5 may be a N-type transistor. The pixel circuit PC5 having the N-type transistor may drive as the pixel circuit PC1 described in the previous embodiment referring to FIGS. 2 and 3.

[0207] Alternatively, each of the first, second and third transistors T1, T2 and T3 in the pixel circuit PC5 may be an P-type transistor. The pixel circuit PC5 having the P-type transistor may drive as the pixel circuit PC2 described in the previous embodiment referring to FIGS. 8 and 9.

[0208] According to this embodiment, the pixel circuit includes only three transistors and two capacitors and thus, an ultra high definition display may be easily designed using the pixel circuit. In addition, the length of the compensating period in the frame period may be freely controlled and thus, a sufficient compensating period is obtained. In addition, whether the organic light emitting diode emits or not the light may be controlled by adjusting a level of the first power source signal. In addition, the leakage current of the transistor may be avoided.

[0209] FIG. 13 is a plan view illustrating a display part of a display apparatus according to an embodiment of the invention.

[0210] Referring to FIGS. 2 and 13, the pixel circuit may be formed in a pixel circuit area PA. Thus, the first voltage line VL1, the second voltage line VL2, the third voltage line VL3, the n-th scan line SLn, the m-th data line DLm, first transistor T1, the second transistor T2, the third transistor T3, the first capacitor Cst and the second capacitor Cpr may be formed in the pixel circuit area PA.

[0211] The first voltage line VL1 may transfer a first driving signal Vinit and extend in the first direction D1.

[0212] The second voltage line VL2 may transfer a first power source signal ELVDD and extend in the first direction D1.

[0213] The third voltage line VL3 may transfer a second driving signal Vcomp and extend in the second direction D2.

[0214] The n-th scan line SLn may transfer an n-th scan signal S(n) and extend in the second direction D2.

[0215] The m-th data line DLm may transfer a data voltage and extend in the first direction D1. The m-th data line DLm may be formed across a central area of the pixel circuit area PA.

[0216] The first transistor T1 may include a control electrode CE1, a first electrode E11, and a second electrode E12. The control electrode CE1 may have an island shape and be formed in the central area of the pixel circuit area PA. The first electrode E11 may be defined in a portion area of the second voltage line VL2 which is connected to an active pattern ACT through a first contact part CH1. The second electrode E12 may be defined in a portion area of the second capacitor Cpr which is connected to the active pattern ACT through a second contact part CH2.

[0217] The second transistor T2 may include a control electrode CE2, a first electrode E21, and a second electrode E22. The control electrode CE2 may be defined in a portion area of the n-th scan line SLn. The first electrode E21 may be defined as an electrode which is connected to the active pattern ACT through a third contact part CH3. The second electrode E22 may be defined in a portion area of the second capacitor Cpr which is connected to the active pattern ACT through the second contact part CH2. The first electrode E21 may be connected to the control electrode CE1 of the first transistor T1 through a fourth contact part CH4.

[0218] The third transistor T3 may include a control electrode CE3, a first electrode E31, and a second electrode E32. The control electrode CE3 may be defined in a portion area of the third voltage line VL2. The first electrode E31 may be defined in a portion area of the third voltage line VL3 which is connected to the active pattern ACT through a fifth contact part CH5. The second electrode E32 may be defined in a portion area of the second capacitor Cpr which is connected to the active pattern ACT through the second contact part CH2.

[0219] The third voltage line VL3 may be connected to the third voltage line VL3 which is formed in an adjacent pixel circuit area, through a connection line and a sixth contact part CH6.

[0220] The first capacitor Cst may be defined in an overlapping area in which an electrode extending in the second direction D2 from the first voltage line VL1 overlaps with the control electrode CE1 of the first transistor T1.

[0221] The second capacitor Cpr may be defined in an overlapping area in which an electrode having the island shape in the central area of the pixel circuit area PA overlaps with the m-th data line DLm. The second capacitor Cpr may overlap with the first capacitor Cst.

[0222] FIG. 14 is a cross-sectional view taken along a line I-I' of FIG. 13. FIGS. 15 to 19 are plan views illus-

trating a method of manufacturing of the display part according to an embodiment of the invention.

[0223] Referring to FIGS. 2, 14 and 15, the display part may include a base substrate 111.

[0224] The base substrate 111 may include an insulation material. For example, the base substrate 111 may include a glass, a transparent plastic, a transparent metal oxide, etc.

[0225] The active pattern ACT may be disposed on the base substrate 111. The active pattern ACT may include silicon. Alternatively, the active pattern ACT may be formed of a semiconductor oxide including a binary compound (ABx), a ternary compound (ABxCy), a quaternary compound (ABxCyDz), etc. which contain indium, zinc, gallium, tin, titanium, aluminum, hafnium (Hf), zirconium (Zr), magnesium (Mg), etc. These compounds may be used alone or in combination thereof.

[0226] The active pattern ACT may include first to sixth areas a1, a2, a3, a4, a5 and a6. The first to sixth areas a1, a2, a3, a4, a5 and a6 may be doped with an impurity, and thus may have electrical conductivity higher than those of other regions of the active pattern ACT. The first to sixth areas a1, a2, a3, a4, a5 and a6 may be first and second electrodes of first, second and third transistors T1, T2 and T3. Boundaries between the first to sixth areas a1, a2, a3, a4, a5 and a6 may not be clearly defined and first to sixth areas a1, a2, a3, a4, a5 and a6 may be electrically connected to each other.

[0227] A gate insulating layer 112 may be disposed on the active pattern ACT. The gate insulating layer 112 may include a silicon compound, metal oxide, etc. For example, the gate insulation layer may include silicon oxide, silicon nitride, silicon oxynitride, aluminum oxide, tantalum oxide, hafnium oxide, zirconium oxide, titanium oxide, etc., which may be used alone or in combination thereof. In one embodiment, the gate insulation layer 112 may have a multilayer structure including a silicon oxide layer and silicon nitride layer.

[0228] A first conductive pattern MET1 which is patterned from a first conductive layer, may be disposed on the gate insulating layer 112. The first conductive layer may include metal, alloy, metal nitride, conductive metal oxide, transparent conductive material, etc., which may be used alone or in combination thereof.

[0229] The first conductive pattern MET1 may include the n-th scan line SLn, the control electrode CE2 of the second transistor T2, the third voltage line VL3, the control electrode CE3 of the third transistor T3, the control electrode CE1 of the first transistor T1, and the first capacitor electrode CSE1 of the first capacitor Cst.

[0230] The n-th scan line SLn may extend in the second direction D2.

[0231] The control electrode CE2 of the second transistor T2 may be defined in a portion area of the n-th scan line SLn.

[0232] The third voltage line VL3 may be disposed in parallel with the n-th scan line SLn.

[0233] The control electrode CE3 of the third transistor T3 may be defined in a portion area of the third voltage line VL3.

[0234] The control electrode CE1 of the first transistor T1 may have an island shape and be disposed in a central area of the pixel circuit area PA.

[0235] The first capacitor electrode CSE1 of the first capacitor Cst may be defined in a portion area of the control electrode CE1.

[0236] Referring to FIGS. 2, 14 and 16, a first insulating interlayer 113 may be disposed on the first conductive pattern MET1. The first insulating interlayer 113 may be formed of a silicon oxide, a silicon nitride, a silicon oxynitride, and etc. These may be used alone or in combination with each other.

[0237] The pixel circuit area PA may include a third contact part CH3, a fourth contact part CH4 and a fifth contact part CH5. The gate insulating layer 112 and the first insulating interlayer 113 are etched to form the third and fifth contact parts CH3 and CH5. The insulating interlayer 113 are etched to form the fourth contact part CH4.

[0238] A second conductive pattern MET2 which is patterned from a second conductive layer, may be disposed on the first insulating interlayer 113. The second conductive layer metal, alloy, metal nitride, conductive metal oxide, transparent conductive material, etc., which may be used alone or in combination thereof.

[0239] The second conductive pattern MET2 may include the first voltage line VL1, a second capacitor electrode CSE2 of the first capacitor Cst, a first electrode E21 of the second transistor T2 and the first electrode E31 of the third transistor T3.

[0240] The first voltage line VL1 may extend in the first direction D1. The second capacitor electrode CSE2 of the first capacitor Cst may extend in the second direction D2 from the first voltage line VL1. The first capacitor Cst may be defined by the first electrode CSE1 of the first conductive pattern MET1 and the second capacitor electrode CSE2 of the second conductive pattern MET2.

[0241] A first end portion of the first electrode E21 may be connected to the active pattern ACT through the third contact part CH3 and a second end portion of the first electrode E21 may be connected to the control electrode CE1 of the first transistor T1 through the fourth contact part CH4.

[0242] The first electrode E31 of the third transistor T3 may be defined in a portion area of the first voltage line VL1 and be connected to the active pattern ACT through the fifth contact part CH5.

[0243] Referring to FIGS. 2, 14 and 17, a second insulating interlayer 114 may be disposed on the second conductive pattern MET2. The pixel circuit area PA may include a sixth contact part CH6 in which the first and second insulating interlayers 113 and 114 are etched.

[0244] A third conductive pattern MET3 which is patterned from a third conductive layer, may be disposed on the second insulating interlayer 114. The third conductive pattern MET3 may include the m-th data line

DLm, a third capacitor electrode CPE1 of the second capacitor Cpr and a connection electrode EE.

[0245] The m-th data line DLm may extend in the first direction D1 and be disposed in the central area of the pixel circuit area PA.

[0246] The third capacitor electrode CPE1 of the second capacitor Cpr may extend from the m-th data line DLm.

[0247] The connection electrode EE may be connected to the third voltage line VL3 and a third voltage line VL3 which is disposed in an adjacent pixel circuit area, through the sixth contact part CH6.

[0248] Referring to FIGS. 2, 14 and 18, a third insulating interlayer 115 may be disposed on the third conductive pattern MET3. The pixel circuit area PA may include a first contact part CH1 and a second contact part CH2 in which the gate insulating layer 112, the first insulating interlayer 113, the second insulating interlayer 114 and the third insulating interlayer 115 are etched.

[0249] A fourth conductive pattern MET4 which is patterned from a fourth conductive layer may be disposed on the third insulating interlayer 115.

[0250] The fourth conductive pattern MET4 may include the second voltage line VL2, the first electrode E11 of the first transistor T1, a fourth capacitor electrode CPE2 of the second capacitor Cpr, the second electrode E12 of the first transistor T1, the second electrode E22 of the second transistor T2 and the second electrode E32 of the third transistor T3.

[0251] The second voltage line VL2 may extend in the first direction D1 and may define a width of the pixel circuit area PA in the first direction D1 together with a second voltage line VL2 in the adjacent pixel circuit area PA.

[0252] The first electrode E11 of the first transistor T1 may be defined in a portion area of the second voltage line VL2 connected to the active pattern AC through the first contact part CH1.

[0253] The fourth capacitor electrode CPE2 of the second capacitor Cpr may have an island shape and be disposed in the central area of the pixel circuit area PA. The second capacitor Cpr may be defined by the third capacitor electrode CPE1 of the third conductive pattern MET3 and the fourth capacitor electrode CPE2 of the fourth conductive pattern MET4.

[0254] The second electrode E12 of the first transistor T1, the second electrode E22 of the second transistor T2 and the second electrode E32 of the third transistor T3 may respectively defined in portion areas of the fourth capacitor electrode CPE2 connected to the active pattern ACT through the second contact part CH2.

[0255] Referring to FIGS. 2, 14 and 19, a fourth insulating interlayer 116 may be disposed on the fourth conductive pattern MET4. The fourth insulating interlayer 116 may be formed with a high thickness to sufficiently cover the fourth conductive pattern MET4.

[0256] The pixel circuit area PA may include a seventh contact part CH7 in which the fourth insulating interlayer 116 is etched.

[0257] A first pixel electrode PE1 may be disposed on the fourth insulating interlayer 116. The first pixel electrode PE1 may correspond to the anode electrode of the organic light emitting diode.

[0258] A pixel defining layer 117 may be disposed on the fourth insulating interlayer 116 on which the first pixel electrode PE1 is formed.

[0259] The pixel defining layer 117 may form an opening on a portion area of the first pixel electrode PE1, and the organic light emitting layer EL may be disposed in the opening. Thus, the organic light emitting layer EL may be on the first pixel electrode PE1 exposed through the opening of the pixel defined layer 117.

[0260] A second pixel electrode PE2 may be disposed on the organic light emitting layer EL. The second pixel electrode PE2 may correspond to the cathode electrode of the organic light emitting diode. The second pixel electrode PE2 may be commonly disposed in the plurality of pixel circuit areas.

[0261] According to embodiments of the invention, the pixel circuit may include only three transistors and two capacitors and thus, an ultra high definition display may be easily designed using the pixel circuit. In addition, the length of the compensating period in the frame period may be freely controlled and thus, a sufficient compensating period is obtained. In addition, whether the organic light emitting diode emits or not the light may be controlled by adjusting a level of the first power source signal.

[0262] The foregoing description is illustrative of the inventive concept and is not to be construed as limiting thereof. Although a few embodiments of the inventive concept have been described, those skilled in the art will readily appreciate that many modifications are possible without materially departing from the novel teachings and advantages of the inventive concept. Accordingly, all such modifications are intended to be included within the scope of the inventive concept as defined in the claims. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function which scope is defined by the claims. Therefore, it is to be understood that the foregoing is illustrative of the inventive concept and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the appended claims.

Claims

1. A display apparatus comprising:
   a plurality of pixels (P), wherein each pixel (P) of the plurality of pixels (P) comprises:

   a first capacitor (Cst) connected between a first voltage line (VL1) configured to receive a first driving signal (Vinit) and a first node (N1);
   a first transistor (T1) comprising a control elec-

trode (CE1) connected to the first node (N1), a first electrode (E11) connected to a second voltage line (VL2) configured to receive a first power source signal (ELVDD) and a second electrode (E12) connected to a second node (N2);
an organic light emitting diode (OLED) comprising an anode electrode connected to the second node (N2) and a cathode electrode configured to receive a second power source signal (ELVSS);
a second capacitor (Cpr) connected between an m-th data line (DLm) and the second node (N2), wherein 'm' is a natural number; and
a second transistor (T2) comprising a control electrode (CE2) connected to an n-th scan line (S(n)), wherein 'n' is a natural number, a first electrode (E21) connected to the first node (N1) and a second electrode (E22) connected to the second node (N2), wherein the pixel (P) further comprises:
a third transistor (T3) comprising a control electrode (CE3) connected to a third voltage line (VL3) configured to receive a second driving signal (Vcomp), a first electrode (E31) connected to the first voltage line (VL1) and a second electrode (E32) connected to the second node (N2).

2. A display apparatus according to claim 1, wherein each of the first, second and third transistors (T1, T2, T3) is an N-type transistor.

3. A display apparatus according to claim 2, wherein during a first period (a) of a frame period, the first voltage line (VL1) is configured to receive a low voltage (initL) of a first driving signal (Vinit), the second voltage line (VL2) is configured to receive a high voltage (ELVDDH) of the first power source signal (ELVDD), the third voltage line (VL3) is configured to receive a high voltage (VGH) of the second driving signal (Vcomp) and the n-th scan line (S(n)) is configured to receive a high voltage (VGH) of a scan signal (S(n)).

4. A display apparatus according to claim 3, wherein during a second period (b) of the frame period, the first voltage line (VL1) is configured to receive a low voltage (initL) of the first driving signal (Vinit), the second voltage line (VL2) is configured to receive a low voltage (ELVDDL) of the first power source signal (ELVDD) lower than the low voltage (initL) of the first driving signal (Vinit), the third voltage line (VL3) is configured to receive a low voltage (VGL) of the second driving signal (Vcomp), and the n-th scan line (S(n)) is configured to receive a high voltage (VGH) of the scan signal (VGH).

5. A display apparatus according to claim 4, wherein during a third period (c) of the frame period, the first voltage line (VL1) is configured to receive a low voltage (initL) of the first driving signal (Vinit), the second voltage line (VL2) is configured to receive a high voltage (ELVDDH) of the first power source signal (ELVDD), the third voltage line (VL3) is configured to receive a low voltage (VGL) of the second driving signal (Vcomp), the n-th scan line (S(n)) receives a high voltage (VGH) of the scan signal (S(n)) during an n-th horizontal period in the third period (c), and the m-th data line (DLm) is configured to receive a data voltage (DATA) corresponding to a plurality of horizontal lines.

6. A display apparatus according to claim 5, wherein during the n-th horizontal period (Hn), a data voltage (Vdata(n)) corresponding to an n-th horizontal line is divided by a voltage division ratio (α) of the first and second capacitors (Cst, Cpr) which are connected in series and the divided voltage ($\alpha.\Delta$Vdata) is applied to the first node (N1).

7. A display apparatus according to claim 5, wherein the m-th data line (DLm) is configured to receive a reference voltage (Vref) before the m-th data line (DLm) receives a data voltage (Vdata(1)) corresponding to a first horizontal line of a plurality of horizontal lines, and
the m-th data line (DLm) is configured to receive a reference voltage (Vref) after the m-th data line (DLm) receives a data voltage (Vdata(N)) corresponding to a last horizontal line of a plurality of horizontal lines.

8. A display apparatus according to claim 7, wherein the m-th data line (DLm) is configured to receive a reference voltage (Vref) before the first voltage line (VL1) receives a high voltage (initH) of the first driving signal (Vinit) and,
the reference voltage (Vref) is equal to or lower than a lowest voltage in a voltage range of the data voltage.

9. A display apparatus according to claim 5, wherein during a fourth period (d) of the frame period, the first voltage line (VL1) is configured to receive a high voltage (initH) of the first driving signal (Vinit), the second voltage line (VL2) is configured to receive a high voltage (ELVDDH)of the first power source signal (ELVDD), the third voltage line (VL3) is configured to receive a low voltage (VGL) of the second driving signal (Vcomp), and the n-th scan line (S(n)) is configured to receive a low voltage (VGL) of the scan signal (S(n)).

10. A display apparatus according to claim 9, wherein when a difference voltage between the high voltage (VGH) and the low voltage (VGL) of the first driving signal (Vinit) is applied to the first node (N1),

the first transistor (T1) is turned on and a driving current (ID) corresponding to the data voltage (Vdata(1)) applied to the first node (N1) flows through the organic light emitting diode (OLED).

11. A display apparatus according to claim 1, wherein each of the first, second and third transistors (T1, T2, T3) is a P-type transistor.

12. A display apparatus according to claim 11, wherein during a first period (a), the first voltage line (VL1) is configured to receive a low voltage (VGL) of the first driving signal (Vinit), the second voltage line (VL2) is configured to receive a low voltage (ELVDDL) of the first power source signal (ELVDD), the third voltage line (VL3) is configured to receive a low voltage (VGL) of the second driving signal (Vcomp), and the n-th scan line (S(n)) is configured to receive a low voltage (VGL) of the scan signal (S(n)).

13. A display apparatus according to claim 12, wherein the low voltage (ELVDDL) of the first power source signal (ELVDD) is higher than the low voltage (initL) of the first driving signal (Vinit).

14. A display apparatus according to claim 12, wherein during a second period (b) of the frame period, the first voltage line (VL1) is configured to receive a low voltage (ELVDDL) of the first driving signal (ELVDD), the second voltage line (VL2) is configured to receive a low voltage (ELVDDL) of the first power source signal (ELVDD), the third voltage line (VL3) is configured to receive a high voltage (VGH) of the second driving signal (Vcomp) and the n-th scan line (S(n)) is configured to receive a low voltage (VGL) of the scan signal (S(n)).

15. A display apparatus according to claim 14, wherein during a third period (c) of the fame period, the first voltage line (VL1) is configured to receive a low voltage (initL) of the first driving signal (Vinit), the second voltage line (VL2) is configured to receive a low voltage (ELVDDL) of the first power source signal (ELVDD), the third voltage line (VL3) is configured to receive a high voltage (VGL) of the second driving signal (Vcomp), the n-th scan line (S(n)) is configured to receive a low voltage (VGL) of the scan signal (S(n)) during an n-th horizontal period in the third period (c), and the m-th data line (DLm) is configured to receive a data voltage (Vdata(n)) corresponding to a plurality of horizontal lines.

16. A display apparatus according to claim 15, wherein during the n-th horizontal period, a data voltage (Vdata(n)) corresponding to an n-th horizontal line is divided by a voltage division ratio (α) of the first and second capacitors (Cst, Cpr) which are connected in series and the divided voltage ($\alpha.\Delta$Vdata) is applied to the first node (N1).

17. A display apparatus according to claim 15, wherein the m-th data line (DLm) is configured to receive a reference voltage (Vref) before the m-th data line (DLm) receives a data voltage (Vdata(1)) corresponding to a first horizontal line of a plurality of horizontal lines, and
the m-th data line (DLm) is configured to receive a reference voltage (Vref) after the m-th data line (DLm) receives a data voltage (Vdata(N)) corresponding to a last horizontal line of a plurality of horizontal lines.

18. A display apparatus according to claim 17, wherein the m-th data line (DLm) is configured to receive a reference voltage (Vref) before the first voltage line (VL1) receives a high voltage (initH) of the first driving signal (Vinit), and
the reference voltage (Vref) is equal to or lower than a lowest voltage in a voltage range of the data voltage.

19. A display apparatus according to claim 15, wherein during a fourth period (d) of the frame period, the first voltage line (VL1) is configured to receive a high voltage (ELVDDH) of the first driving signal (ELVDD), the second voltage line (VL2) is configured to receive a high voltage (ELVDDH) of the first power source signal (ELVDD), the third voltage line (VL3) is configured to receive a high voltage (VGH) of the second driving signal (Vcomp), and the n-th scan line (S(n)) is configured to receive a high voltage (VGH) of the scan signal (S(n)).

20. A display apparatus according to claim 19, wherein when a difference voltage between the high voltage (initH) and the low voltage (initL) of the first driving signal (Vinit) is applied to the first node (N1),
the first transistor (T1) is turned on and a driving current (ID) corresponding to the data voltage (ELVDDL + Vth.T1 + $\alpha.\Delta$Vdata + ΔVinit) applied to the first node (N1) flows through the organic light emitting diode (OLED).

21. A display apparatus according to claim 1, wherein at least one of the second and third transistors (T2, T3) has a dual gate structure.

22. A method of driving the display apparatus according to Claim 1, the method comprising:

applying, in a first period (a) of a frame, a low voltage of the first driving signal (Vinit) to the anode electrode of the organic light emitting diode (OLED) to initialize the anode electrode;
applying, in a second period (b) of the frame following the first period (a), a low voltage of the

first power source signal (ELVDD) to the first electrode (E11) of the first transistor (T1) to diode-connect the first transistor (T1);
dividing, in a third period (c) of the frame following the second period (b), a data voltage applied to a data line (DLm) using the first and second capacitors (Cst, (Cpr) which are connected in series to apply divided voltage to the control electrode (CE1) of the first transistor (T1); and
applying, in a fourth period (d) of the frame following the third period (c), a high voltage of the first driving signal (Vinit) to the control electrode (CE1) of the first transistor (T1) to emit a light from the organic light emitting diode (OLED).

23. A method according to claim 22, wherein when the first transistor (T1) is an N-type transistor, the low voltage (ELVDDL) of the first power source signal (ELVDD) is lower than the low voltage (initL) of the first driving signal (Vinit), and
the low voltages (ELVDDL, initL) of the first power source signal (ELVDD) and the first driving signal (Vinit) are lower than a voltage of second power source signal (ELVSS) applied to a cathode electrode of the organic light emitting diode (OLED).

24. A method according to claim 22, wherein when the first transistor (T1) is a P-type transistor, the low voltage (ELVDDL) of the first power source signal (ELVDD) is higher than the low voltage (initL) of the first driving signal (Vinit), and
the low voltages (ELVDDL, initL) of the first power source signal (ELVDD) and the first driving signal (Vinit) are lower than a voltage of second power source signal (ELVSS) applied to a cathode electrode of the organic light emitting diode (OLED).

25. A method according to claim 22, wherein a difference between the high (initH) and low (initL) voltages of the first driving signal (Vinit) is applied to a control electrode (CE1) of the first transistor (T1), a high voltage (initH) of the first driving signal (Vinit) being preset based on a turn-on voltage of the first transistor (T1).

26. A method according to claim 22, further comprising:

applying a reference voltage (Vref) to a data line before the data line receives a data voltage (Vdata(1)) corresponding to a first horizontal line of a plurality of horizontal lines, and
applying the reference voltage (Vref) to the data line after the data line receives a data voltage (Vdata(N)) corresponding to a last horizontal line of a plurality of horizontal lines.

27. A method according to claim 26, wherein the data line receives the reference voltage (Vref) before a control electrode (CE1) of the first transistor (T1) receives the high voltage (initH) of the first driving signal (Vinit).

28. A method according to claim 22, wherein each of initializing the anode electrode, diode-coupling the first transistor (T1) and emitting the light from the organic light emitting diode (OLED) is simultaneously performed in all pixels (P).

Patentansprüche

1. Anzeigevorrichtung, umfassend:
eine Vielzahl von Pixeln (P), wobei jedes Pixel (P) der Vielzahl von Pixeln (P) umfasst:

einen ersten Kondensator (Cst), der zwischen eine erste Spannungsleitung (VL1), die zum Empfangen eines ersten Ansteuersignals (Vinit) konfiguriert ist, und einen ersten Knoten (N1) geschaltet ist;
einen ersten Transistor (T1), umfassend eine Steuerelektrode (CE1), die mit dem ersten Knoten (N1) verbunden ist, eine erste Elektrode (E11), die mit einer zweiten Spannungsleitung (VL2) verbunden ist, die zum Empfangen eines ersten Energiequellensignals (ELVDD) konfiguriert ist, und eine zweite Elektrode (E12), die mit einem zweiten Knoten (N2) verbunden ist;
eine organische Leuchtdiode (OLED), umfassend eine Anodenelektrode, die mit dem zweiten Knoten (N2) verbunden ist, und eine Kathodenelektrode, die zum Empfangen eines zweiten Energiequellensignals (ELVSS) konfiguriert ist;
einen zweiten Kondensator (Cpr), der zwischen eine m-te Datenleitung (DLm) und den zweiten Knoten (N2) geschaltet ist, wobei ‚m' eine natürliche Zahl ist; und
einen zweiten Transistor (T2), umfassend eine Steuerelektrode (CE2), die mit einer n-ten Abtastleitung (S (n)) verbunden ist, wobei ‚n' eine natürliche Zahl ist, und eine erste Elektrode (E21), die mit dem ersten Knoten (N1) verbunden ist, und eine zweite Elektrode (E22), die mit dem zweiten Knoten (N2) verbunden ist, wobei das Pixel (P) ferner umfasst:
einen dritten Transistor (T3), umfassend eine Steuerelektrode (CE3), die mit einer dritten Spannungsleitung (VL3) verbunden ist, die zum Empfangen eines zweiten Ansteuersignals (Vcomp) konfiguriert ist, eine erste Elektrode (E31), die mit der ersten Spannungsleitung (VL1) verbunden ist, und eine zweite Elektrode (E32), die mit dem zweiten Knoten (N2) verbunden ist.

2. Anzeigevorrichtung nach Anspruch 1, wobei jeder des ersten, zweiten und dritten Transistors (T1, T2, T3) ein Transistor vom N-Typ ist.

3. Anzeigevorrichtung nach Anspruch 2, wobei während einer ersten Periode (a) einer Rahmenperiode die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer niedrigen Spannung (initL) eines ersten Ansteuersignals (Vinit), die zweite Spannungsleitung (VL2) konfiguriert ist zum Empfangen einer hohen Spannung (ELVDDH) des ersten Energiequellensignals (ELVDD), die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer hohen Spannung (VGH) des zweiten Ansteuersignals (Vcomp) und die n-te Abtastzeile (S(n)) konfiguriert ist zum Empfangen einer hohen Spannung (VGH) des Abtastsignals (S(n)).

4. Anzeigevorrichtung nach Anspruch 3, wobei während einer zweiten Periode (b) der Rahmenperiode die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer niedrigen Spannung (initL) des ersten Ansteuersignals (Vinit), die zweite Spannungsleitung (VL2) konfiguriert ist zum Empfangen einer niedrigen Spannung (ELVDDL) des ersten Energiequellensignals (ELVDD), die niedriger als die niedrige Spannung (initL) des ersten Ansteuersignals (Vinit) ist, die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des zweiten Ansteuersignals (Vcomp) und die n-te Abtastzeile (S(n)) konfiguriert ist zum Empfangen einer hohen Spannung (VGH) des Abtastsignals (VGH).

5. Anzeigevorrichtung nach Anspruch 4, wobei während einer dritten Periode (c) der Rahmenperiode die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer niedrigen Spannung (initL) des ersten Ansteuersignals (Vinit), die zweite Spannungsleitung (VL2) konfiguriert ist zum Empfangen einer hohen Spannung (ELVDDH) des ersten Energiequellensignals (ELVDD), die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des zweiten Ansteuersignals (Vcomp), die n-te Abtastzeile (S(n)) während einer n-ten Horizontalperiode in der dritten Periode (c) eine hohe Spannung (VGH) des Abtastsignals (S(n)) empfängt und die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Datenspannung (DATA), die einer Vielzahl von horizontalen Zeilen entspricht.

6. Anzeigevorrichtung nach Anspruch 5, wobei während der n-ten Horizontalperiode (Hn) eine Datenspannung (Vdata(N)), die einer n-ten Horizontalzeile entspricht, durch ein Spannungsteilungsverhältnis (α) des ersten und zweiten Kondensators (Cst, Cpr) geteilt wird, die in Reihe geschaltet sind, und die geteilte Spannung ($\alpha.\Delta$Vdata) an den ersten Knoten (N1) angelegt wird.

7. Anzeigevorrichtung nach Anspruch 5, wobei die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Referenzspannung (Vref), bevor die m-te Datenleitung (DLm) eine Datenspannung (Vdata(1)) empfängt, die einer ersten horizontalen Zeile der Vielzahl von horizontalen Zeilen entspricht, und die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Referenzspannung (Vref), nachdem die m-te Datenleitung (DLm) eine Datenspannung (Vdata(N)) empfängt, die einer letzten horizontalen Zeile der Vielzahl von horizontalen Zeilen entspricht.

8. Anzeigevorrichtung nach Anspruch 7, wobei die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Referenzspannung (Vref), bevor die erste Spannungsleitung (VL1) eine hohe Spannung (initH) des ersten Ansteuersignals (Vinit) empfängt, und die Referenzspannung (Vref) gleich oder niedriger als eine niedrigste Spannung in einem Spannungsbereich der Datenspannung ist.

9. Anzeigevorrichtung nach Anspruch 5, wobei während einer vierten Periode (d) der Rahmenperiode die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer hohen Spannung (initH) des ersten Ansteuersignals (Vinit), die zweite Spannungsleitung (VL2) konfiguriert ist zum Empfangen einer hohen Spannung (ELVDDH) des ersten Energiequellensignals (ELVDD), die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des zweiten Ansteuersignals (Vcomp) und die n-te Abtastzeile (S(n)) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des Abtastsignals (S(n)).

10. Anzeigevorrichtung nach Anspruch 9, wobei, wenn eine Differenzspannung zwischen der hohen Spannung (VGH) und der niedrigen Spannung (VGL) des ersten Ansteuersignals (Vinit) an den ersten Knoten (N1) angelegt wird, der erste Transistor (T1) eingeschaltet wird und ein Ansteuerstrom (ID), der der Datenspannung (Vdata(1)) entspricht, die am ersten Knoten (N1) anliegt, durch die organische Leuchtdiode (OLED) fließt.

11. Anzeigevorrichtung nach Anspruch 1, wobei jeder des ersten, zweiten und dritten Transistors (T1, T2, T3) ein Transistor vom P-Typ ist.

12. Anzeigevorrichtung nach Anspruch 11, wobei während einer ersten Periode (a) die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des ersten Ansteuersignals (Vinit), die zweite Spannungsleitung (VL2) kon-

figuriert ist zum Empfangen einer niedrigen Spannung (ELVDDL) des ersten Energiequellensignals (ELVDD), die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des zweiten Ansteuersignals (Vcomp) und die n-te Abtastzeile (S(n)) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des Abtastsignals (S(n)).

13. Anzeigevorrichtung nach Anspruch 12, wobei die niedrige Spannung (ELVDDL) des ersten Energiequellensignals (ELVDD) höher ist als die niedrige Spannung (initL) des ersten Ansteuersignals (Vinit).

14. Anzeigevorrichtung nach Anspruch 12, wobei während einer zweiten Periode (b) der Rahmenperiode die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer niedrigen Spannung (ELVDDL) des ersten Ansteuersignals (ELVDD), die zweite Spannungsleitung (VL2) konfiguriert ist zum Empfangen einer niedrigen Spannung (ELVDDL) des ersten Energiequellensignals (ELVDD), die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer hohen Spannung (VGL) des zweiten Ansteuersignals (Vcomp) und die n-te Abtastzeile (S(n)) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des Abtastsignals (S(n)).

15. Anzeigevorrichtung nach Anspruch 14, wobei während einer dritten Periode (c) der Rahmenperiode die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer niedrigen Spannung (initL) des ersten Ansteuersignals (Vinit), die zweite Spannungsleitung (VL2) konfiguriert ist zum Empfangen einer niedrigen Spannung (ELVDDL) des ersten Energiequellensignals (ELVDD), die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer hohen Spannung (VGH) des zweiten Ansteuersignals (Vcomp), die n-te Abtastzeile (S(n)) konfiguriert ist zum Empfangen einer niedrigen Spannung (VGL) des Abtastsignals (S(n)) während einer n-ten Horizontalperiode in der dritten Periode (c) und die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Datenspannung (Vdata(n))), die einer Vielzahl von horizontalen Zeilen entspricht.

16. Anzeigevorrichtung nach Anspruch 15, wobei während der n-ten Horizontalperiode eine Datenspannung (Vdata(N)), die einer n-ten Horizontalzeile entspricht, durch ein Spannungsteilungsverhältnis (α) des ersten und zweiten Kondensators (Cst, Cpr) geteilt wird, die in Reihe geschaltet sind, und die geteilte Spannung ($\alpha.\Delta$Vdata) an den ersten Knoten (N1) angelegt wird.

17. Anzeigevorrichtung nach Anspruch 15, wobei die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Referenzspannung (Vref), bevor die m-te Datenleitung (DLm) eine Datenspannung (Vdata(1)) empfängt, die einer ersten horizontalen Zeile einer Vielzahl von horizontalen Zeilen entspricht, und
die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Referenzspannung (Vref), nachdem die m-te Datenleitung (DLm) eine Datenspannung (Vdata(N)) empfängt, die einer letzten horizontalen Zeile einer Vielzahl von horizontalen Zeilen entspricht.

18. Anzeigevorrichtung nach Anspruch 17, wobei die m-te Datenleitung (DLm) konfiguriert ist zum Empfangen einer Referenzspannung (Vref), bevor die erste Spannungsleitung (VL1) eine hohe Spannung (initH) des ersten Ansteuersignals (Vinit) empfängt, und
die Referenzspannung (Vref) gleich oder niedriger als eine niedrigste Spannung in einem Spannungsbereich der Datenspannung ist.

19. Anzeigevorrichtung nach Anspruch 15, wobei während einer vierten Periode (d) der Rahmenperiode die erste Spannungsleitung (VL1) konfiguriert ist zum Empfangen einer hohen Spannung (ELVDDH) des ersten Ansteuersignals (ELVDD), die zweite Spannungsleitung (VL2) konfiguriert ist zum Empfangen einer hohen Spannung (ELVDDH) des ersten Energiequellensignals (ELVDD), die dritte Spannungsleitung (VL3) konfiguriert ist zum Empfangen einer hohen Spannung (VGH) des zweiten Ansteuersignals (Vcomp) und die n-te Abtastzeile (S(n)) konfiguriert ist zum Empfangen einer hohen Spannung (VGH) des Abtastsignals (S(n)).

20. Anzeigevorrichtung nach Anspruch 19, wobei, wenn eine Differenzspannung zwischen der hohen Spannung (initH) und der niedrigen Spannung (initL) des ersten Ansteuersignals (Vinit) an den ersten Knoten (N1) angelegt wird,
der erste Transistor (T1) eingeschaltet wird und ein Ansteuerstrom (ID), der der Datenspannung (ELVDDL + Vth.T1 + $\alpha.\Delta$Vdata + ΔVinit) entspricht, die am ersten Knoten (N1) anliegt, durch die organische Leuchtdiode (OLED) fließt.

21. Anzeigevorrichtung nach Anspruch 1, wobei mindestens einer des zweiten und dritten Transistors (T2, T3) eine Doppelgate-Struktur aufweist.

22. Verfahren zum Ansteuern der Anzeigevorrichtung nach Anspruch 1, wobei das Verfahren umfasst:
Anlegen, in einer ersten Periode (a) eines Rahmens, einer niedrigen Spannung des ersten Ansteuersignals (Vinit) an die Anodenelektrode der organischen Leuchtdiode (OLED), um die Anodenelektrode zu initialisieren;

Anlegen, in einer zweiten Periode (b) des Rahmens, die auf die erste Periode (a) folgt, einer

niedrigen Spannung des ersten Energiequellensignals (ELVDD) an die erste Elektrode (E11) des ersten Transistors (T1), um eine Diodenverbindung mit dem ersten Transistor (T1) herzustellen;

Teilen, in einer dritten Periode (c) des Rahmens, die auf die zweite Periode (b) folgt, einer an eine Datenleitung (DLm) angelegten Datenspannung unter Verwendung des ersten und des zweiten Kondensators (Cst, Cpr), die in Reihe geschaltet sind, um geteilte Spannung an die Steuerelektrode (CE1) des ersten Transistors (T1) anzulegen; und

Anlegen, in einer vierten Periode (d) des Rahmens, die auf die dritte Periode (c) folgt, einer hohen Spannung des ersten Ansteuersignals (Vinit) an die Steuerelektrode (CE1) des ersten Transistors (T1), um Licht von der organischen Leuchtdiode (OLED) zu emittieren.

23. Verfahren nach Anspruch 22, wobei, wenn der erste Transistor (T1) ein Transistor vom N-Typ ist, die niedrige Spannung (ELVDDL) des ersten Energiequellensignals (ELVDD) niedriger ist als die niedrige Spannung (initL) des ersten Ansteuersignals (Vinit) und

die niedrigen Spannungen (ELVDDL, initL) des ersten Energiequellensignals (ELVDD) und des ersten Ansteuersignals (Vinit) niedriger sind als eine Spannung des zweiten Energiequellensignals (ELVSS), die an eine Kathodenelektrode der organischen Leuchtdiode (OLED) angelegt wird.

24. Verfahren nach Anspruch 22, wobei, wenn der erste Transistor (T1) ein Transistor vom P-Typ ist, die niedrige Spannung (ELVDDL) des ersten Energiequellensignals (ELVDD) höher ist als die niedrige Spannung (initL) des ersten Ansteuersignals (Vinit) und

die niedrigen Spannungen (ELVDDL, initL) des ersten Energiequellensignals (ELVDD) und des ersten Ansteuersignals (Vinit) niedriger sind als eine Spannung des zweiten Energiequellensignals (ELVSS), die an eine Kathodenelektrode der organischen Leuchtdiode (OLED) angelegt wird.

25. Verfahren nach Anspruch 22, wobei eine Differenz zwischen der hohen (initH) und der niedrigen (initL) Spannung des ersten Ansteuersignals (Vinit) an eine Steuerelektrode (CE1) des ersten Transistors (T1) angelegt wird, wobei eine hohe Spannung (initH) des ersten Ansteuersignals (Vinit) basierend auf einer Einschaltspannung des ersten Transistors (T1) voreingestellt ist.

26. Verfahren nach Anspruch 22, ferner umfassend:

Anlegen einer Referenzspannung (Vref) an eine Datenleitung, bevor die Datenleitung eine Datenspannung (Vdata(1)) empfängt, die einer ersten horizontalen Zeile einer Vielzahl von horizontalen Zeilen entspricht, und

Anlegen der Referenzspannung (Vref) an die Datenleitung, nachdem die Datenleitung eine Datenspannung (Vdata(N)) empfangen hat, die einer letzten horizontalen Zeile der Vielzahl von horizontalen Zeilen entspricht.

27. Verfahren nach Anspruch 26, wobei die Datenleitung die Referenzspannung (Vref) empfängt, bevor eine Steuerelektrode (CE1) des ersten Transistors (T1) die hohe Spannung (initH) des ersten Ansteuersignals (Vinit) empfängt.

28. Verfahren nach Anspruch 22, wobei jedes des Initialisieren der Anodenelektrode, Diodenkoppeln des ersten Transistors (T1) und Emittieren des Lichts von der organischen Leuchtdiode (OLED) gleichzeitig in allen Pixeln (P) durchgeführt wird.

Revendications

1. Afficheur comprenant :
une pluralité de pixels (P), dans lequel chaque pixel (P) de la pluralité de pixels (P) comprend :

un premier condensateur (Cst) connecté entre une première ligne de tension (VL1), configurée de manière à recevoir un premier signal de commande (Vinit), et un premier nœud (N1) ;

un premier transistor (T1) comprenant une électrode de commande (CE1) connectée au premier nœud (N1), une première électrode (E11) connectée à une deuxième ligne de tension (VL2), configurée de manière à recevoir un premier signal de source de puissance (ELVDD), et une seconde électrode (E12) connectée à un second nœud (N2) ;

une diode électroluminescente organique (OLED) comprenant une électrode anodique, connectée au second nœud (N2), et une électrode cathodique, configurée de manière à recevoir un second signal de source de puissance (ELVSS) ;

un second condensateur (Cpr) connecté entre une m-ième ligne de données (DLm) et le second nœud (N2), dans lequel « m » est un nombre naturel ; et

un deuxième transistor (T2) comprenant une électrode de commande (CE2) connectée à une n-ième ligne de balayage (S(n)), dans lequel « n » est un nombre naturel, une première électrode (E21) connectée au premier nœud (N1), et une seconde électrode (E22), connectée au second nœud (N2), dans lequel le pixel (P) com-

prend en outre :
un troisième transistor (T3) comprenant une électrode de commande (CE3), connectée à une troisième ligne de tension (VL3), configurée de manière à recevoir un second signal de commande (Vcomp), une première électrode (E31), connectée à la première ligne de tension (VL1), et une seconde électrode (E32), connectée au second nœud (N2).

2. Afficheur selon la revendication 1, dans lequel chaque transistor parmi les premier, deuxième et troisième transistors (T1, T2, T3) correspond à un transistor de type N.

3. Afficheur selon la revendication 2, dans lequel, au cours d'une première période (a) d'une période de trame, la première ligne de tension (VL1) est configurée de manière à recevoir une basse tension (initL) d'un premier signal de commande (Vinit), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une haute tension (ELVDDH) du premier signal de source de puissance (ELVDD), la troisième ligne de tension (VL3) est configurée de manière à recevoir une haute tension (VGH) du second signal de commande (Vcomp) et la n-ième ligne de balayage (S(n)) est configurée de manière à recevoir une haute tension (VGH) du signal de balayage (S(n)).

4. Afficheur selon la revendication 3, dans lequel, au cours d'une deuxième période (b) de la période de trame, la première ligne de tension (VL1) est configurée de manière à recevoir une basse tension (initL) du premier signal de commande (Vinit), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une basse tension (ELVDDL) du premier signal de source de puissance (ELVDD), inférieure à la basse tension (initL) du premier signal de commande (Vinit), la troisième ligne de tension (VL3) est configurée de manière à recevoir une basse tension (VGL) du second signal de commande (Vcomp), et la n-ième ligne de balayage (S(n)) est configurée de manière à recevoir une haute tension (VGH) du signal de balayage (VGH).

5. Afficheur selon la revendication 4, dans lequel, au cours d'une troisième période (c) de la période de trame, la première ligne de tension (VL1) est configurée de manière à recevoir une basse tension (initL) du premier signal de commande (Vinit), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une haute tension (ELVDDH) du premier signal de source de puissance (ELVDD), la troisième ligne de tension (VL3) est configurée de manière à recevoir une basse tension (VGL) du second signal de commande (Vcomp), la n-ième ligne de balayage (S(n)) reçoit une haute tension (VGH) du signal de balayage (S(n)) au cours d'une n-ième période horizontale dans la troisième période (c), et la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de données (DATA) correspondant à une pluralité de lignes horizontales.

6. Afficheur selon la revendication 5, dans lequel, au cours de la n-ième période horizontale (Hn), une tension de données (Vdata(n)) correspondant à une n-ième ligne horizontale, est divisée par un rapport de division de tension (α) des premier et second condensateurs (Cst, Cpr) qui sont connectés en série, et la tension divisée ($\alpha.\Delta$Vdata) est appliquée au premier nœud (N1).

7. Afficheur selon la revendication 5, dans lequel la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de référence (Vref) avant que la m-ième ligne de données (DLm) reçoive une tension de données (Vdata(1)) correspondant à une première ligne horizontale d'une pluralité de lignes horizontales ; et
la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de référence (Vref) après que la m-ième ligne de données (DLm) a reçu une tension de données (Vdata(N)) correspondant à une dernière ligne horizontale d'une pluralité de lignes horizontales.

8. Afficheur selon la revendication 7, dans lequel la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de référence (Vref) avant que la première ligne de tension (VL1) reçoive une haute tension (initH) du premier signal de commande (Vinit) ; et
la tension de référence (Vref) est égale ou inférieure à une tension la plus basse dans une plage de tension de la tension de données.

9. Afficheur selon la revendication 5, dans lequel, au cours d'une quatrième période (d) de la période de trame, la première ligne de tension (VL1) est configurée de manière à recevoir une haute tension (initH) du premier signal de commande (Vinit), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une haute tension (ELVDDH) du premier signal de source de puissance (ELVDD), la troisième ligne de tension (VL3) est configurée de manière à recevoir une basse tension (VGL) du second signal de commande (Vcomp), et la n-ième ligne de balayage (S(n)) est configurée de manière à recevoir une basse tension (VGL) du signal de balayage (S(n)).

10. Afficheur selon la revendication 9, dans lequel, lorsqu'une tension différentielle entre la haute tension (VGH) et la basse tension (VGL) du premier signal

de commande (Vinit) est appliquée au premier nœud (N1) :
le premier transistor (T1) est mis sous tension et un courant de commande (ID) correspondant à la tension de données (Vdata(1)) appliquée au premier nœud (N1) circule à travers la diode électroluminescente organique (OLED).

11. Afficheur selon la revendication 1, dans lequel chaque transistor parmi les premier, deuxième et troisième transistors (T1, T2, T3) correspond à un transistor de type P.

12. Afficheur selon la revendication 11, dans lequel, au cours d'une première période (a), la première ligne de tension (VL1) est configurée de manière à recevoir une basse tension (VGL) du premier signal de commande (Vinit), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une basse tension (ELVDDL) du premier signal de source de puissance (ELVDD), la troisième ligne de tension (VL3) est configurée de manière à recevoir une basse tension (VGL) du second signal de commande (Vcomp), et la n-ième ligne de balayage (S(n)) est configurée de manière à recevoir une basse tension (VGL) du signal de balayage (S(n)).

13. Afficheur selon la revendication 12, dans lequel la basse tension (ELVDDL) du premier signal de source de puissance (ELVDD) est supérieure à la basse tension (initL) du premier signal de commande (Vinit).

14. Afficheur selon la revendication 12, dans lequel, au cours d'une deuxième période (b) de la période de trame, la première ligne de tension (VL1) est configurée de manière à recevoir une basse tension (ELVDDL) du premier signal de commande (ELVDD), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une basse tension (ELVDDL) du premier signal de source de puissance (ELVDD), la troisième ligne de tension (VL3) est configurée de manière à recevoir une haute tension (VGH) du second signal de commande (Vcomp) et la n-ième ligne de balayage (S(n)) est configurée de manière à recevoir une basse tension (VGL) du signal de balayage (S(n)).

15. Afficheur selon la revendication 14, dans lequel, au cours d'une troisième période (c) de la période de trame, la première ligne de tension (VL1) est configurée de manière à recevoir une basse tension (initL) du premier signal de commande (Vinit), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une basse tension (ELVDDL) du premier signal de source de puissance (ELVDD), la troisième ligne de tension (VL3) est configurée de manière à recevoir une haute tension (VGL) du second signal de commande (Vcomp), la n-ième ligne de balayage (S(n)) est configurée de manière à recevoir une basse tension (VGL) du signal de balayage (S(n)) au cours d'une n-ième période horizontale dans la troisième période (c), et la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de données (Vdata(n)) correspondant à une pluralité de lignes horizontales.

16. Afficheur selon la revendication 15, dans lequel, au cours de la n-ième période horizontale, une tension de données (Vdata(n)) correspondant à une n-ième ligne horizontale, est divisée par un rapport de division de tension (α) des premier et second condensateurs (Cst, Cpr) qui sont connectés en série, et la tension divisée ($\alpha.\Delta$Vdata) est appliquée au premier nœud (N1).

17. Afficheur selon la revendication 15, dans lequel la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de référence (Vref) avant que la m-ième ligne de données (DLm) reçoive une tension de données (Vdata(1)) correspondant à une première ligne horizontale d'une pluralité de lignes horizontales ; et
la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de référence (Vref) après que la m-ième ligne de données (DLm) a reçu une tension de données (Vdata(N)) correspondant à une dernière ligne horizontale d'une pluralité de lignes horizontales.

18. Afficheur selon la revendication 17, dans lequel la m-ième ligne de données (DLm) est configurée de manière à recevoir une tension de référence (Vref) avant que la première ligne de tension (VL1) reçoive une haute tension (initH) du premier signal de commande (Vinit) ; et
la tension de référence (Vref) est égale ou inférieure à une tension la plus basse dans une plage de tension de la tension de données.

19. Afficheur selon la revendication 15, dans lequel, au cours d'une quatrième période (d) de la période de trame, la première ligne de tension (VL1) est configurée de manière à recevoir une haute tension (ELVDDH) du premier signal de commande (ELVDD), la deuxième ligne de tension (VL2) est configurée de manière à recevoir une haute tension (ELVDDH) du premier signal de source de puissance (ELVDD), la troisième ligne de tension (VL3) est configurée de manière à recevoir une haute tension (VGH) du second signal de commande (Vcomp), et la n-ième ligne de balayage (S(n)) est configurée de manière à recevoir une haute tension (VGH) du signal de balayage (S(n)).

20. Afficheur selon la revendication 19, dans lequel, lors-

qu'une tension différentielle entre la haute tension (initH) et la basse tension (initL) du premier signal de commande (Vinit) est appliquée au premier nœud (N1) ;
le premier transistor (T1) est mis sous tension et un courant de commande (ID) correspondant à la tension de données (ELVDDL + Vth.T1 + $\alpha.\Delta$Vdata + ΔVinit) appliquée au premier nœud (N1) circule à travers la diode électroluminescente organique (OLED).

21. Afficheur selon la revendication 1, dans lequel au moins l'un des deuxième et troisième transistors (T2, T3) présente une structure à double grille.

22. Procédé de commande de l'afficheur selon la revendication 1, le procédé comprenant les étapes ci-dessous consistant à :

appliquer, au cours d'une première période (a) d'une trame, une basse tension du premier signal de commande (Vinit) à l'électrode anodique de la diode électroluminescente organique (OLED) en vue d'initialiser l'électrode anodique ;
appliquer, au cours d'une deuxième période (b) de la trame, laquelle suit la première période (a), une basse tension du premier signal de source de puissance (ELVDD), à la première électrode (E11) du premier transistor (T1), en vue de connecter en diode le premier transistor (T1) ;
diviser, au cours d'une troisième période (c) de la trame, laquelle suit la deuxième période (b), une tension de données appliquée à une ligne de données (DLm), en utilisant les premier et second condensateurs (Cst, Cpr) qui sont connectés en série, en vue d'appliquer une tension divisée à l'électrode de commande (CE1) du premier transistor (T1) ; et
appliquer, au cours d'une quatrième période (d) de la trame, laquelle suit la troisième période (c), une haute tension du premier signal de commande (Vinit), à l'électrode de commande (CE1) du premier transistor (T1), en vue d'émettre une lumière à partir de la diode électroluminescente organique (OLED).

23. Procédé selon la revendication 22, dans lequel, lorsque le premier transistor (T1) est un transistor de type N, la basse tension (ELVDDL) du premier signal de source de puissance (ELVDD) est inférieure à la basse tension (initL) du premier signal de commande (Vinit) ; et
les basses tensions (ELVDDL, initL) du premier signal de source de puissance (ELVDD) et du premier signal de commande (Vinit) sont inférieures à une tension du second signal de source de puissance (ELVSS) appliquée à une électrode cathodique de la diode électroluminescente organique (OLED).

24. Procédé selon la revendication 22, dans lequel, lorsque le premier transistor (T1) est un transistor de type P, la basse tension (ELVDDL) du premier signal de source de puissance (ELVDD) est supérieure à la basse tension (initL) du premier signal de commande (Vinit) ; et
les basses tensions (ELVDDL, initL) du premier signal de source de puissance (ELVDD) et du premier signal de commande (Vinit) sont inférieures à une tension du second signal de source de puissance (ELVSS) appliquée à une électrode cathodique de la diode électroluminescente organique (OLED).

25. Procédé selon la revendication 22, dans lequel une différence entre les tensions haute (initH) et basse (initL) du premier signal de commande (Vinit) est appliquée à une électrode de commande (CE1) du premier transistor (T1), une haute tension (initH) du premier signal de commande (Vinit) étant prédéfinie sur la base d'une tension d'activation du premier transistor (T1).

26. Procédé selon la revendication 22, comprenant en outre les étapes ci-dessous consistant à :

appliquer une tension de référence (Vref) à une ligne de données avant que la ligne de données reçoive une tension de données (Vdata(1)) correspondant à une première ligne horizontale d'une pluralité de lignes horizontales ; et
appliquer la tension de référence (Vref) à la ligne de données après que la ligne de données a reçu une tension de données (Vdata(N)) correspondant à une dernière ligne horizontale d'une pluralité de lignes horizontales.

27. Procédé selon la revendication 26, dans lequel la ligne de données reçoit la tension de référence (Vref) avant qu'une électrode de commande (CE1) du premier transistor (T1) reçoive la haute tension (initH) du premier signal de commande (Vinit).

28. Procédé selon la revendication 22, dans lequel chaque étape, parmi une étape d'initialisation de l'électrode anodique, une étape de couplage par diode du premier transistor (T1) et une étape d'émission de la lumière à partir de la diode électroluminescente organique (OLED), est mise en œuvre simultanément dans tous les pixels (P).

FIG. 1

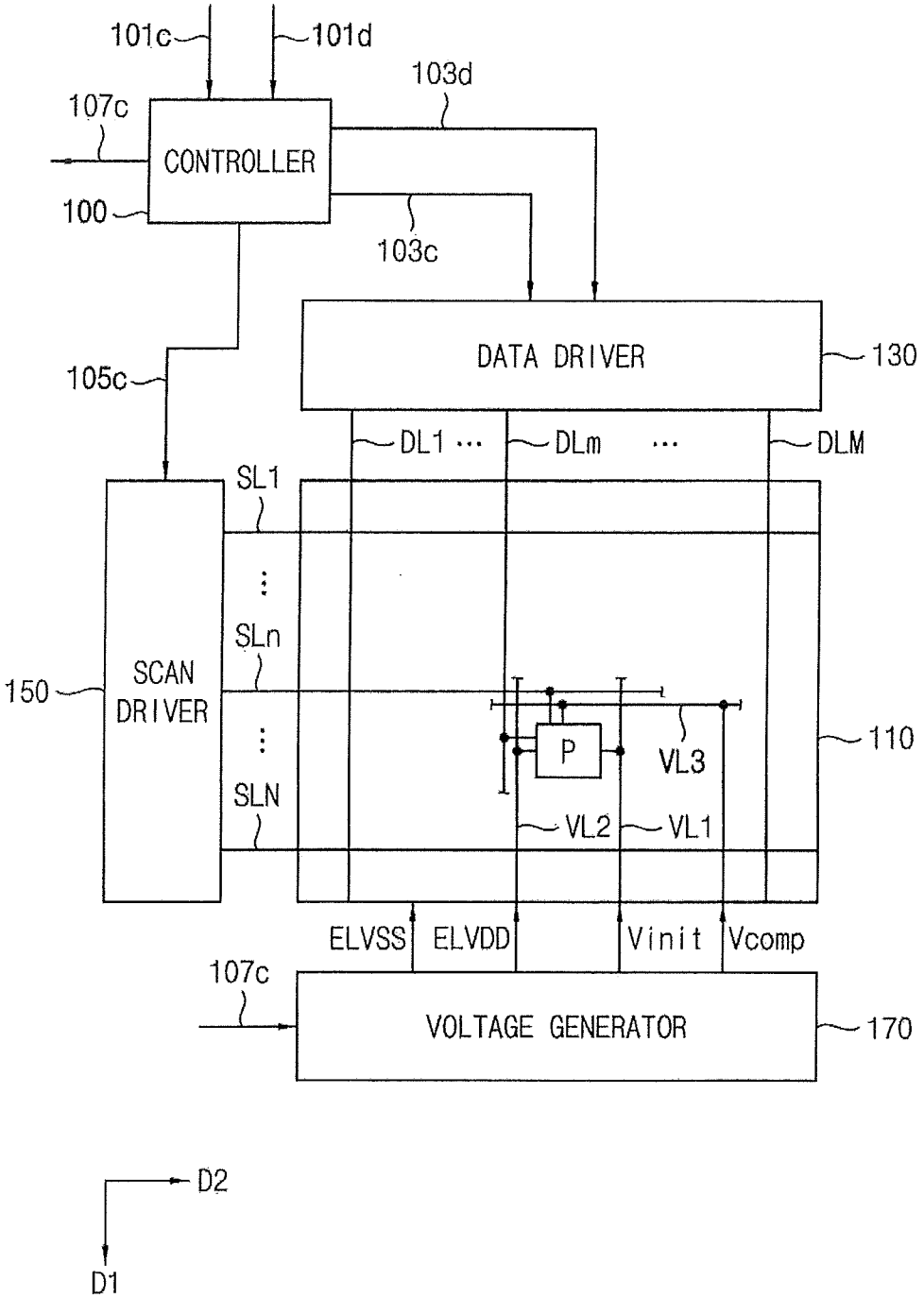

101c
101d
103d
107c
CONTROLLER
100
103c
105c
DATA DRIVER
130
DL1 ... DLm ... DLM
SL1
SLn
SCAN DRIVER
150
SLN
P
VL3
110
VL2
VL1
ELVSS
ELVDD
Vinit
Vcomp
107c
VOLTAGE GENERATOR
170
D2
D1

FIG. 2

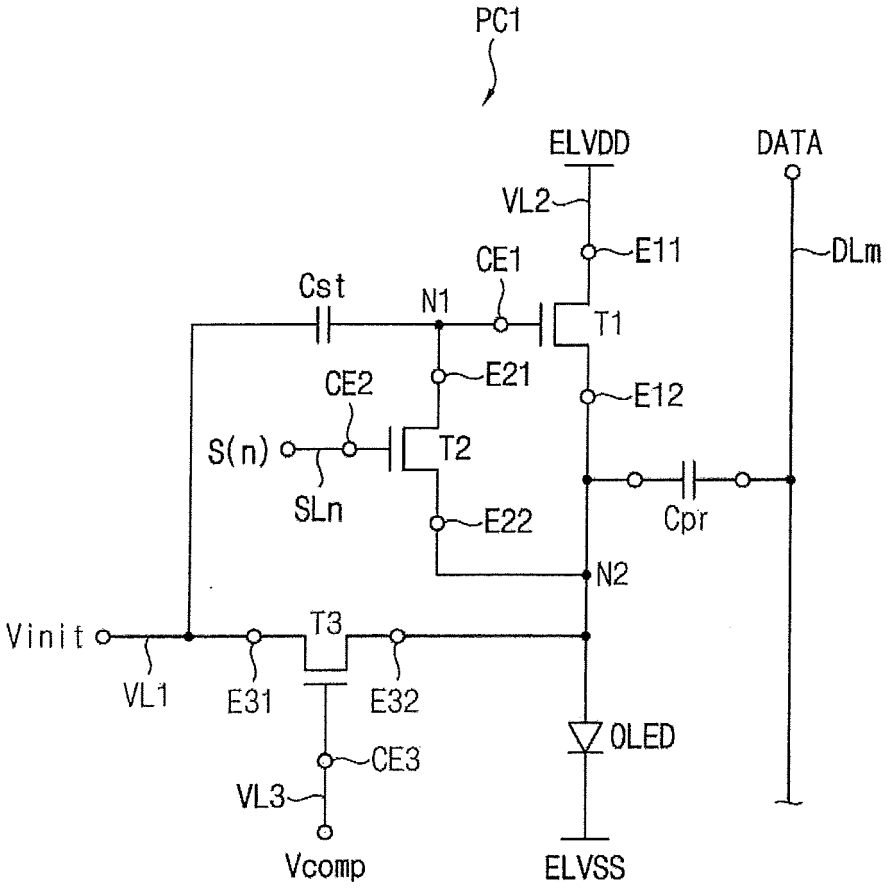

PC1
ELVDD
DATA
VL2
E11
DLm
CE1
Cst
N1
T1
E21
E12
CE2
S(n)
T2
SLn
E22
Cpr
N2
Vinit
T3
VL1
E31
E32
OLED
CE3
VL3
Vcomp
ELVSS

FIG. 3

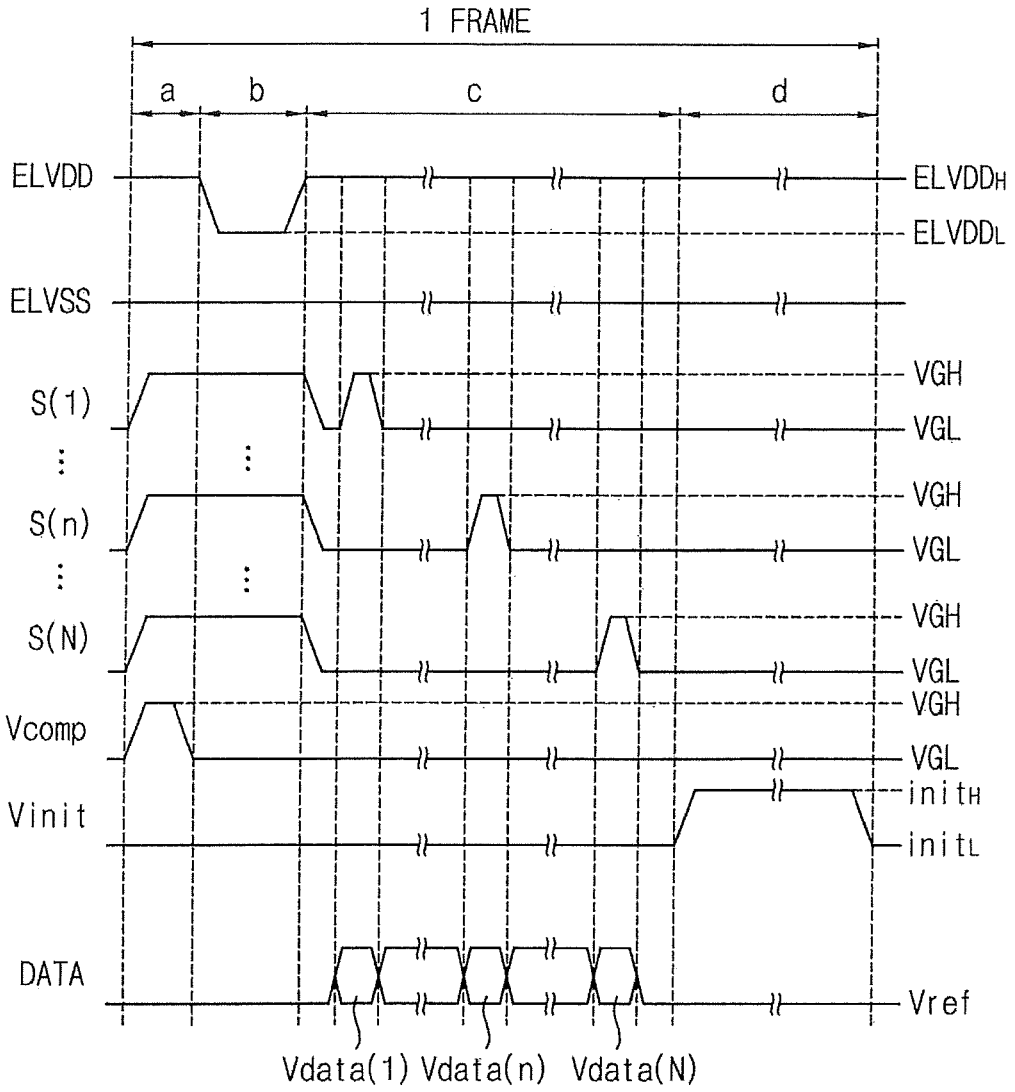

1 FRAME
a
b
c
d
ELVDD
ELVDDH
ELVDDL
ELVSS
S(1)
VGH
VGL
S(n)
VGH
VGL
S(N)
VGH
VGL
Vcomp
VGH
VGL
Vinit
initH
initL
DATA
Vref
Vdata(1)
Vdata(n)
Vdata(N)

FIG. 4A

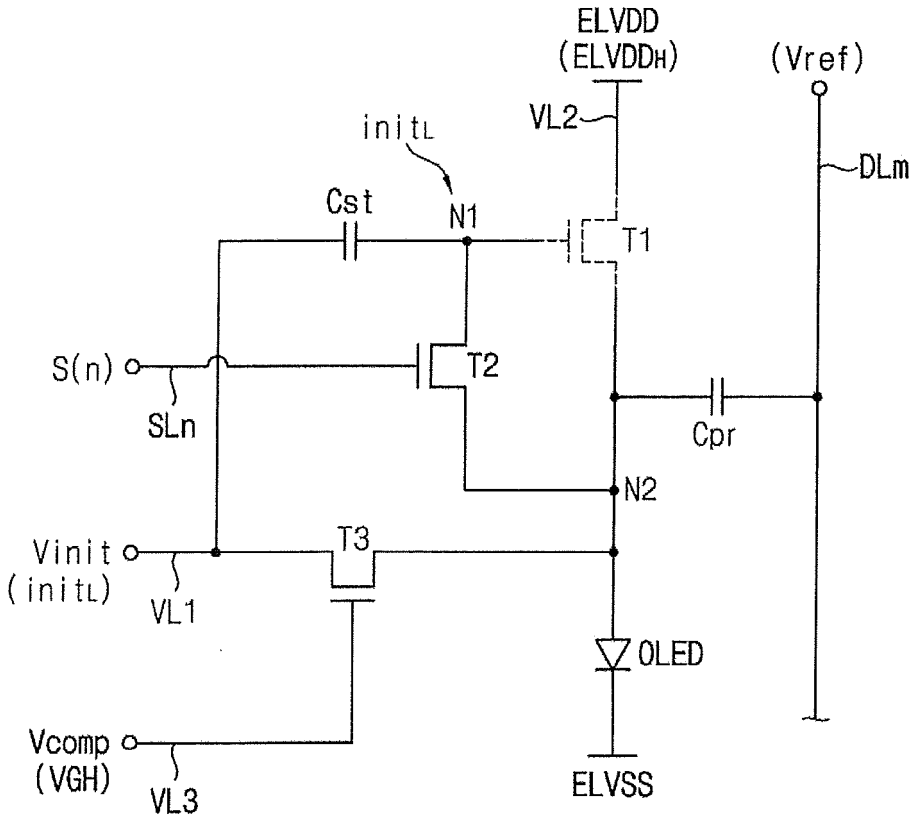

ELVDD
(ELVDDH)
(Vref)
VL2
initL
DLm
Cst
N1
T1
S(n)
T2
SLn
Cpr
N2
Vinit
(initL)
T3
VL1
OLED
Vcomp
(VGH)
VL3
ELVSS

FIG. 4B

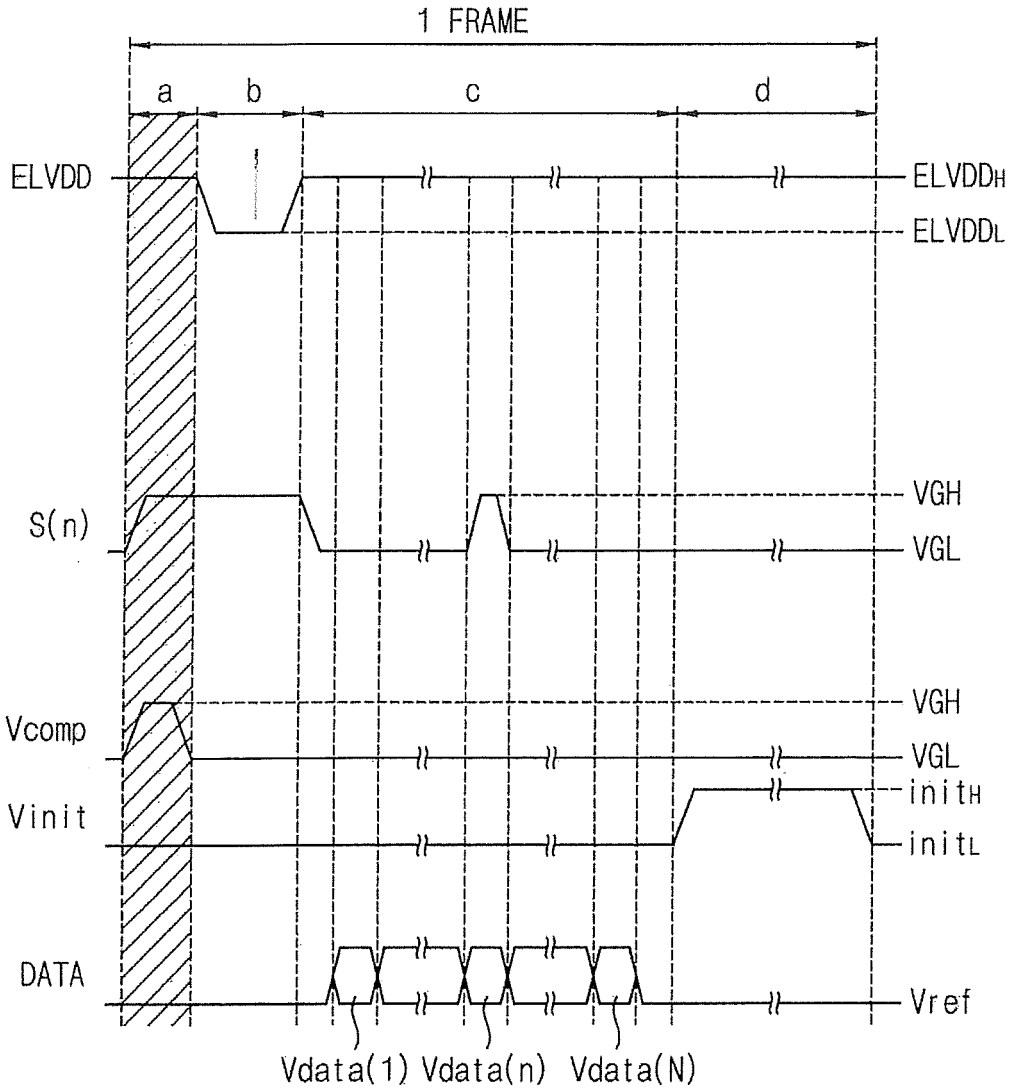

1 FRAME
a
b
c
d
ELVDD
ELVDDH
ELVDDL
S(n)
VGH
VGL
Vcomp
VGH
VGL
Vinit
initH
initL
DATA
Vref
Vdata(1)
Vdata(n)
Vdata(N)

FIG. 5A

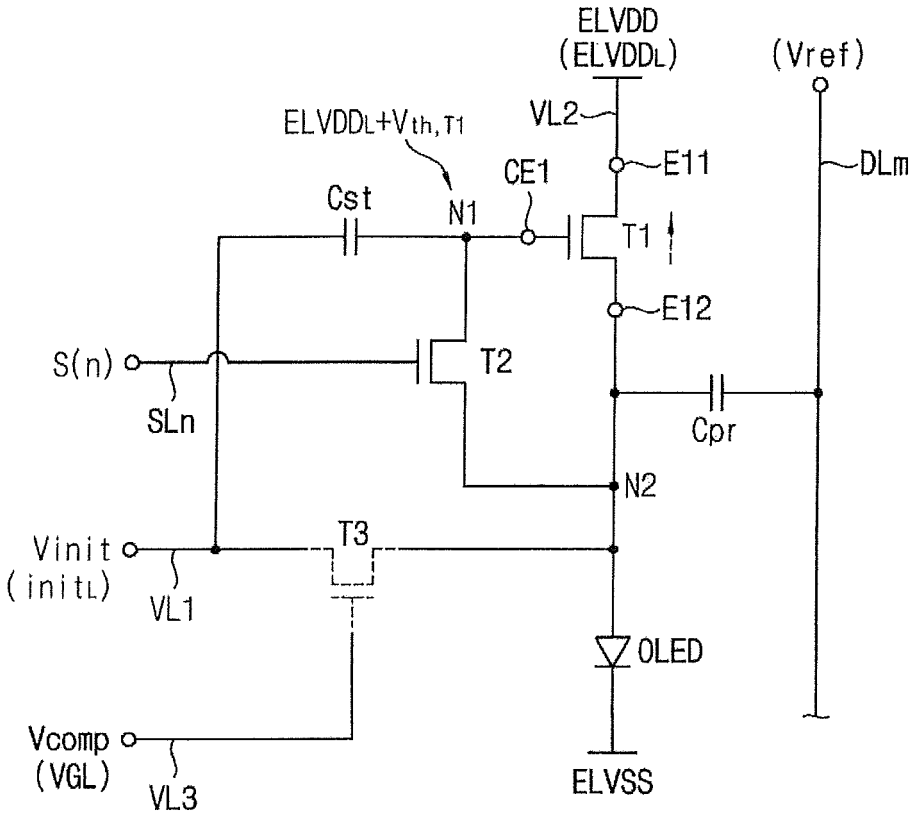

ELVDD
(ELVDDL)
(Vref)
ELVDDL+Vth,T1
VL2
E11
DLm
CE1
Cst
N1
T1
E12
S(n)
T2
SLn
Cpr
N2
Vinit
(initL)
T3
VL1
OLED
Vcomp
(VGL)
VL3
ELVSS

FIG. 5B

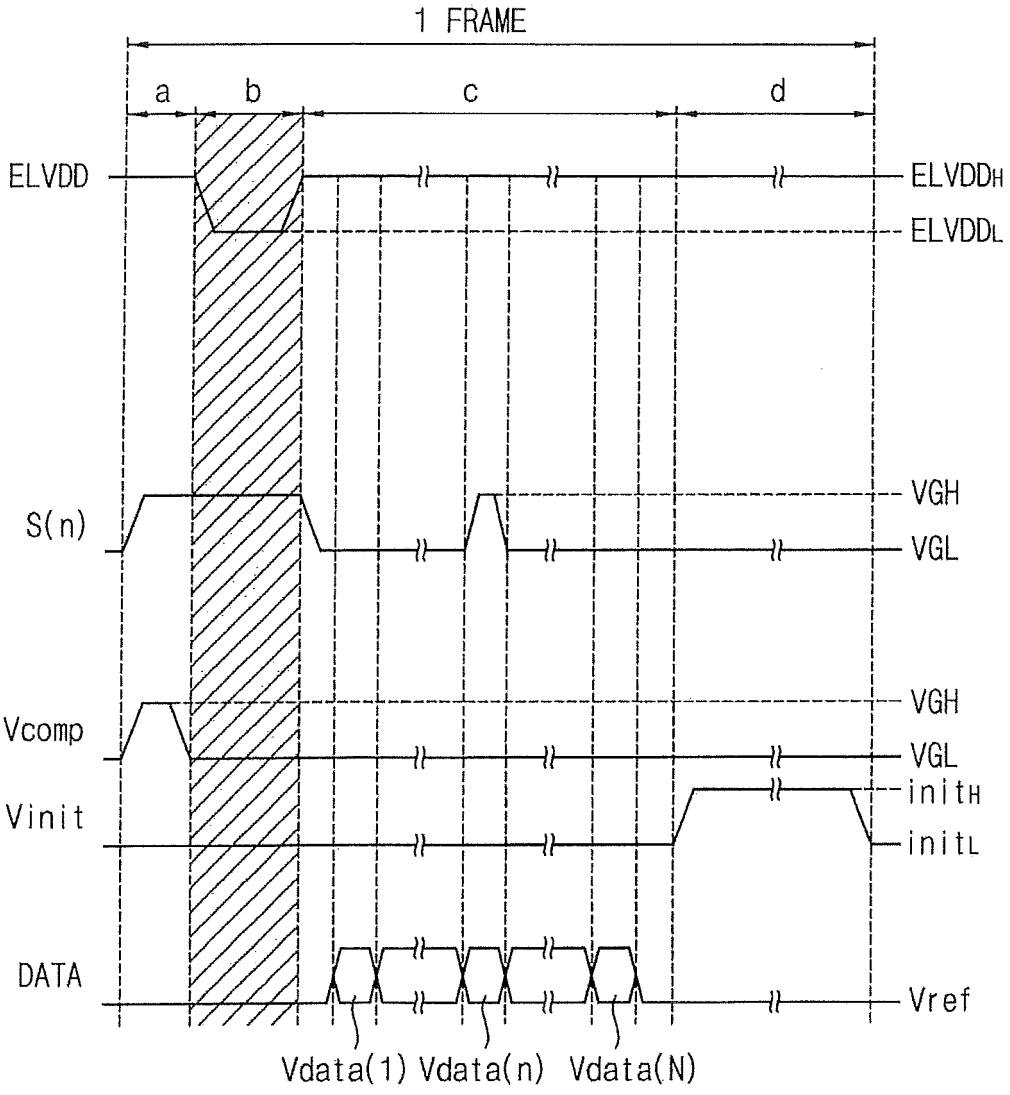

1 FRAME
a
b
c
d
ELVDD
ELVDDH
ELVDDL
S(n)
VGH
VGL
Vcomp
VGH
VGL
Vinit
initH
initL
DATA
Vref
Vdata(1)
Vdata(n)
Vdata(N)

FIG. 6A

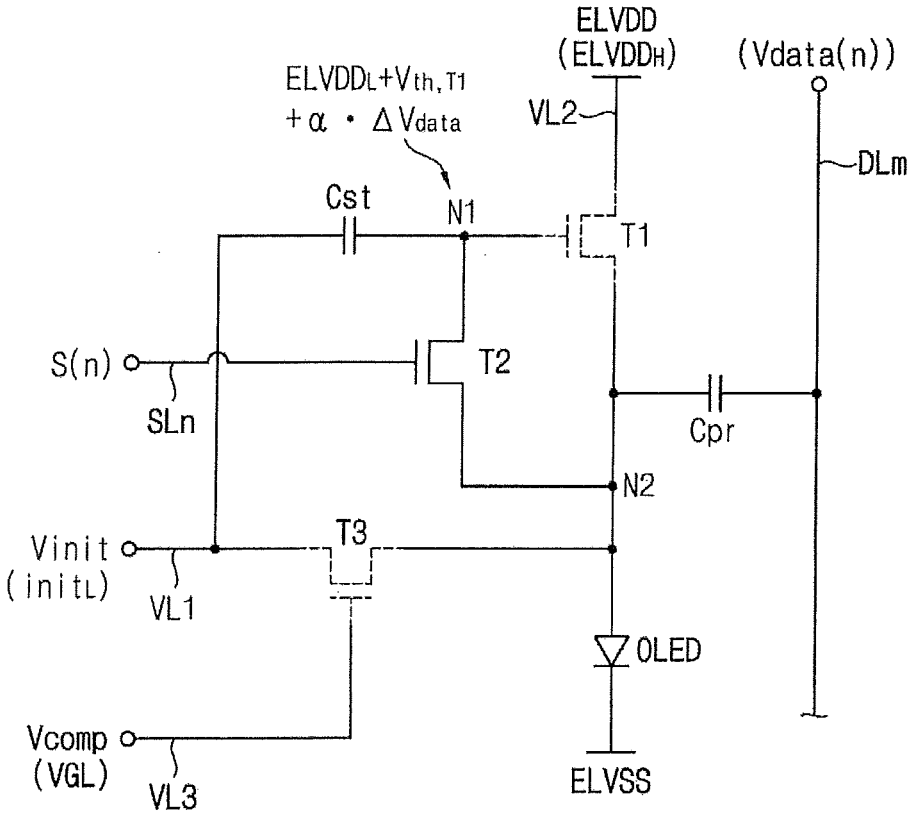

ELVDD
(ELVDDH)
(Vdata(n))
ELVDDL+Vth,T1
+α • ΔVdata
VL2
DLm
Cst
N1
T1
S(n)
T2
SLn
Cpr
N2
Vinit
(initL)
T3
VL1
OLED
Vcomp
(VGL)
VL3
ELVSS

FIG. 6B

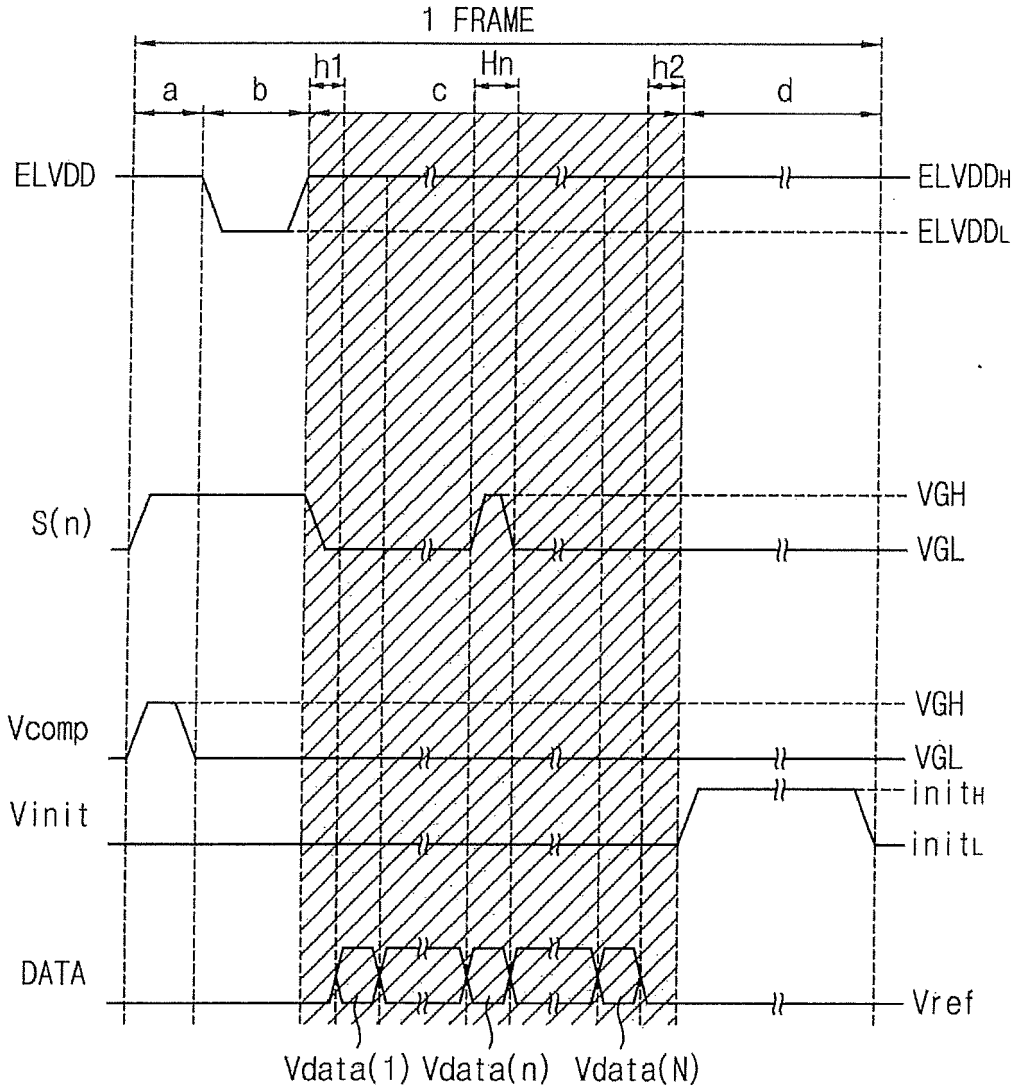

1 FRAME
a
b
h1
c
Hn
h2
d
ELVDD
ELVDDH
ELVDDL
S(n)
VGH
VGL
Vcomp
VGH
VGL
Vinit
initH
initL
DATA
Vref
Vdata(1)
Vdata(n)
Vdata(N)

FIG. 7A

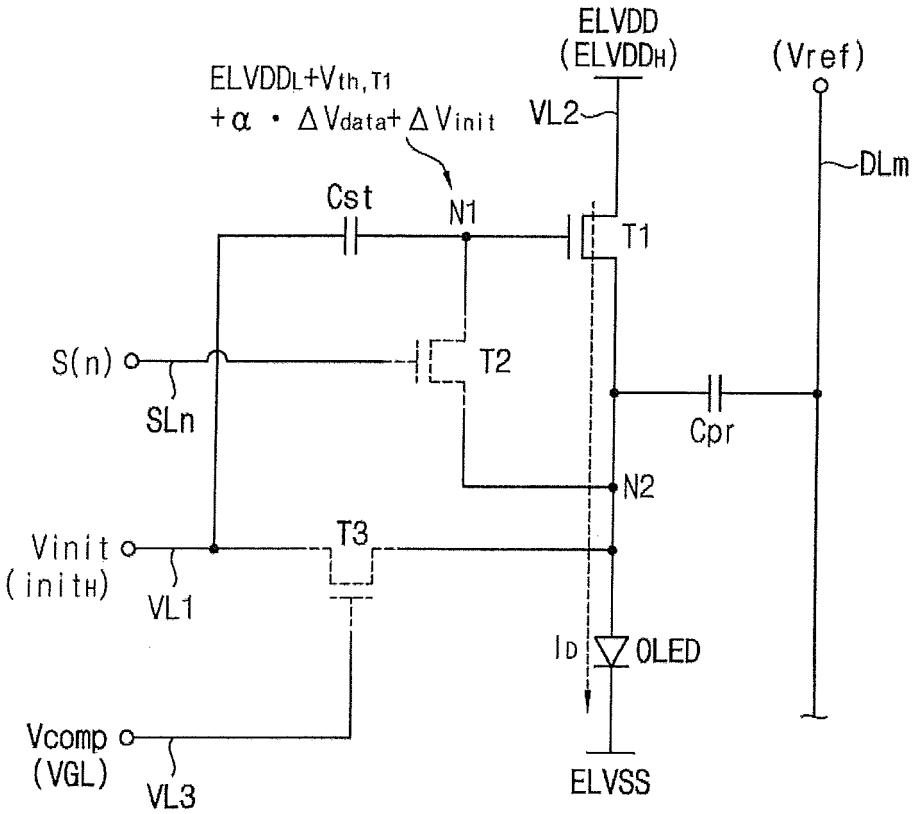

ELVDD
(ELVDDH)
(Vref)
ELVDDL+Vth,T1
+α · ΔVdata+ ΔVinit
VL2
DLm
Cst
N1
T1
S(n)
T2
SLn
Cpr
N2
Vinit
(initH)
T3
VL1
ID
OLED
Vcomp
(VGL)
VL3
ELVSS

FIG. 7B

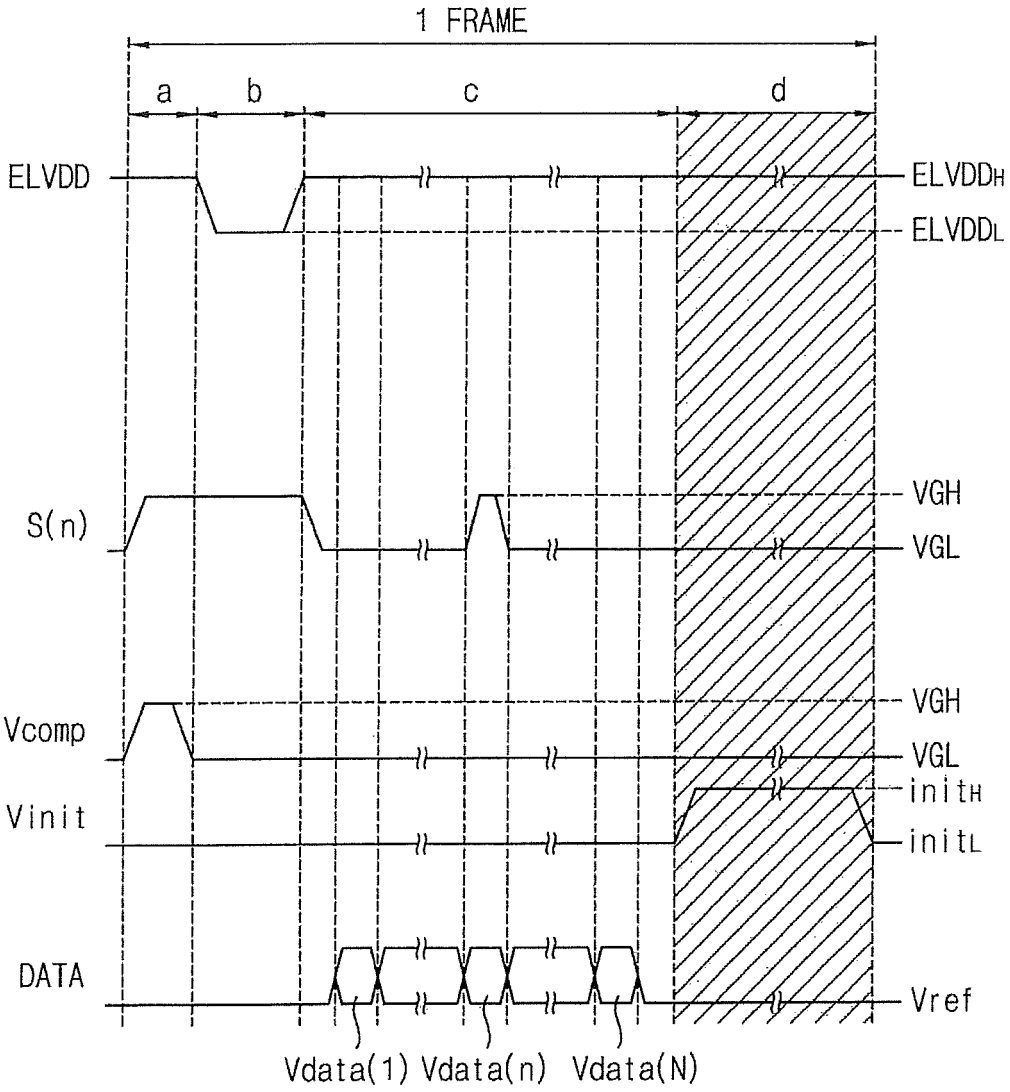

1 FRAME
a
b
c
d
ELVDD
ELVDDH
ELVDDL
S(n)
VGH
VGL
Vcomp
VGH
VGL
Vinit
initH
initL
DATA
Vref
Vdata(1)
Vdata(n)
Vdata(N)

FIG. 8

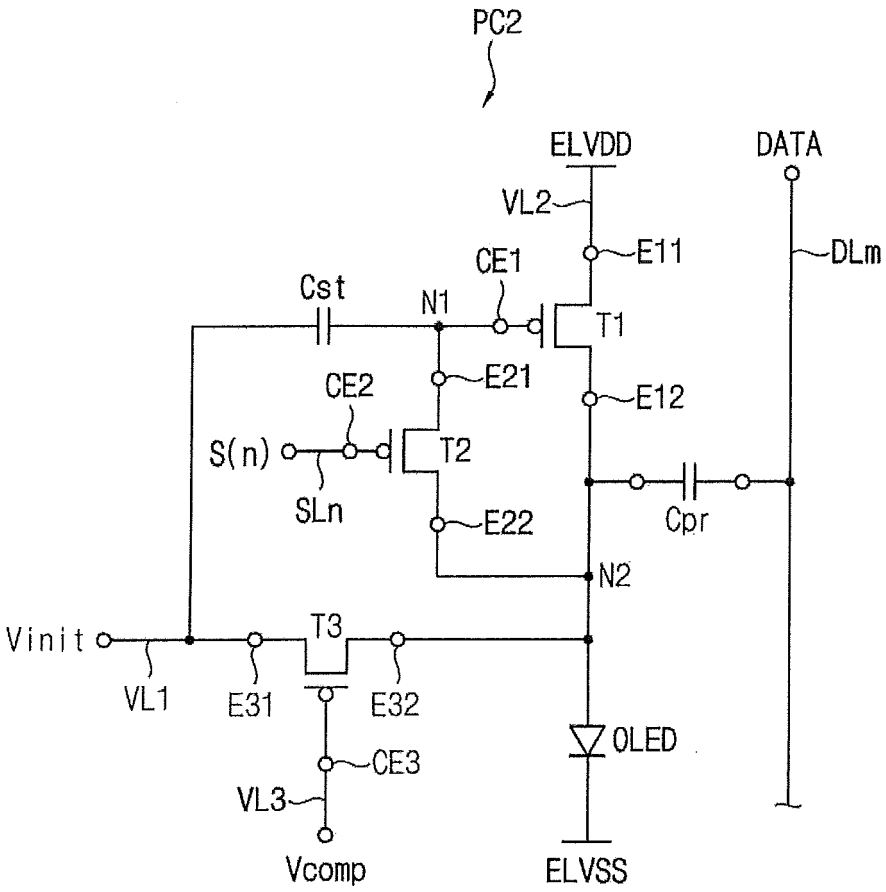

PC2
ELVDD
DATA
VL2
E11
DLm
CE1
Cst
N1
T1
E21
E12
CE2
S(n)
T2
SLn
Cpr
E22
N2
Vinit
T3
VL1
E31
E32
OLED
CE3
VL3
Vcomp
ELVSS

FIG. 9

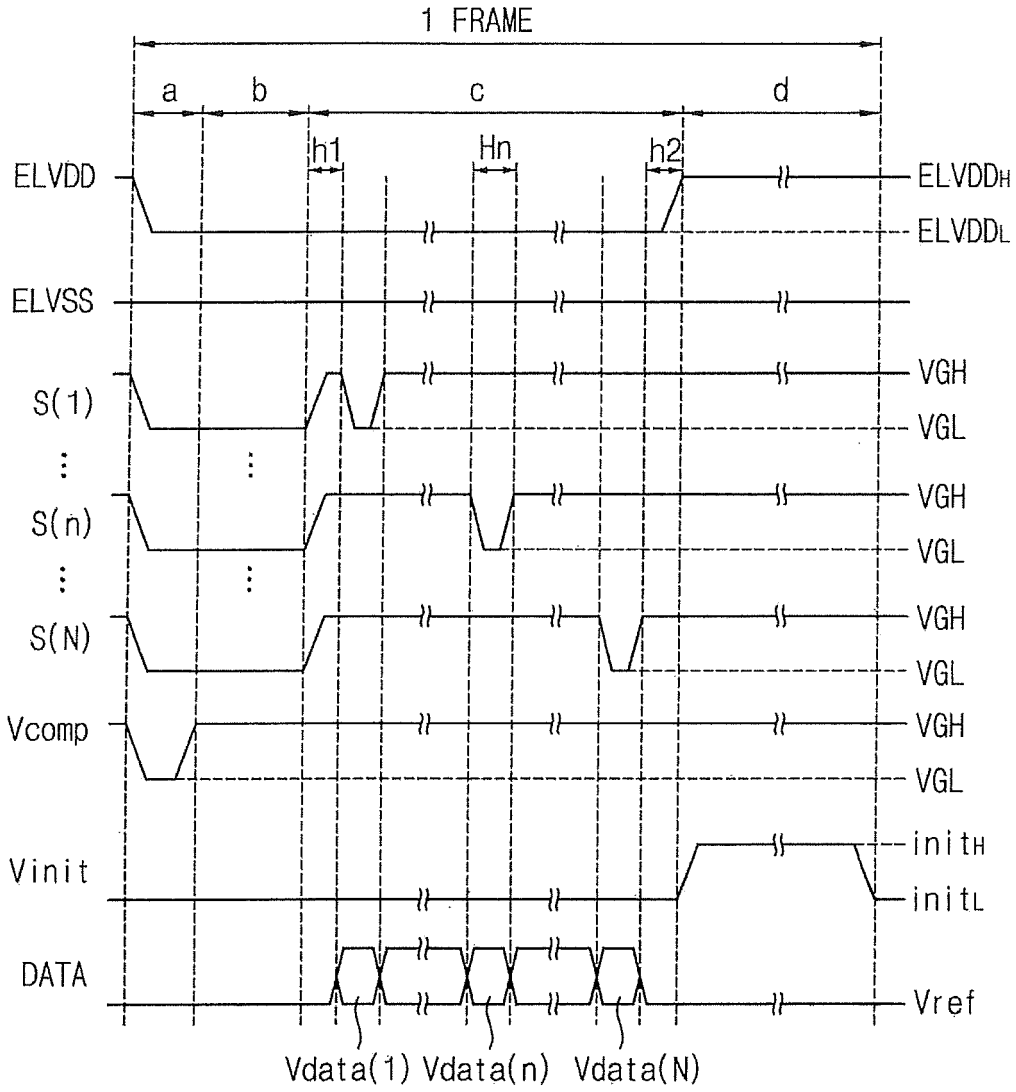

1 FRAME
a
b
c
d
h1
Hn
h2
ELVDD
ELVDDH
ELVDDL
ELVSS
S(1)
S(n)
S(N)
VGH
VGL
Vcomp
Vinit
initH
initL
DATA
Vref
Vdata(1)
Vdata(n)
Vdata(N)

FIG. 10

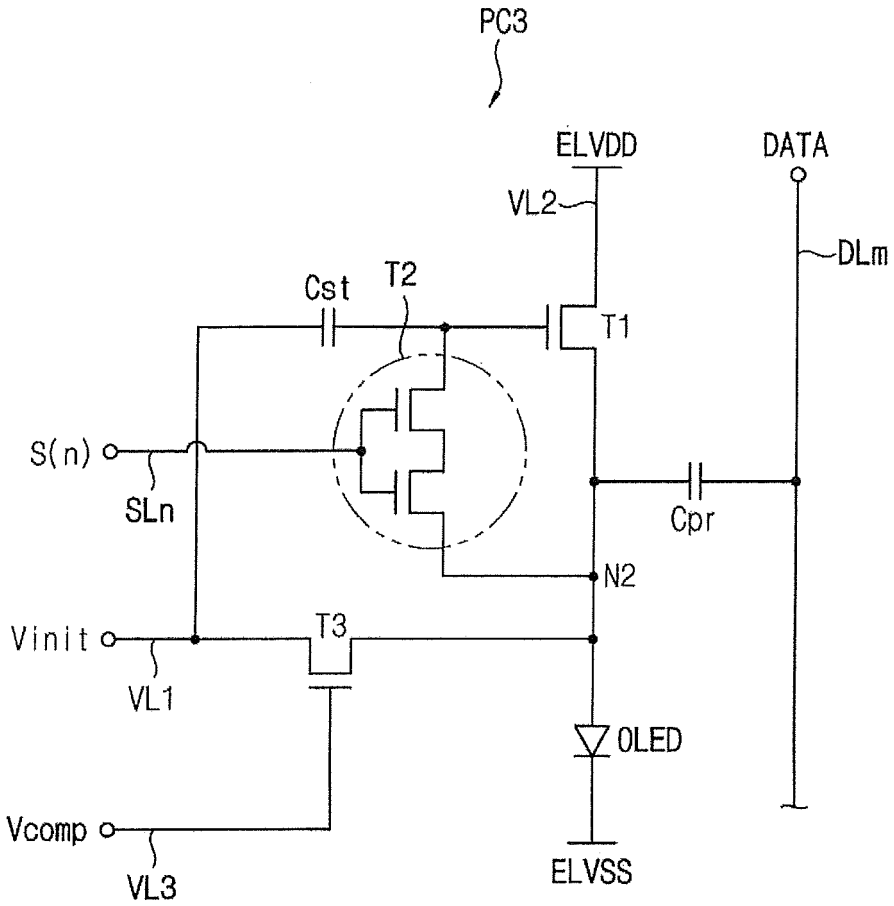

PC3
ELVDD
DATA
VL2
DLm
Cst
T2
T1
S(n)
SLn
Cpr
N2
Vinit
T3
VL1
OLED
Vcomp
VL3
ELVSS

FIG. 11

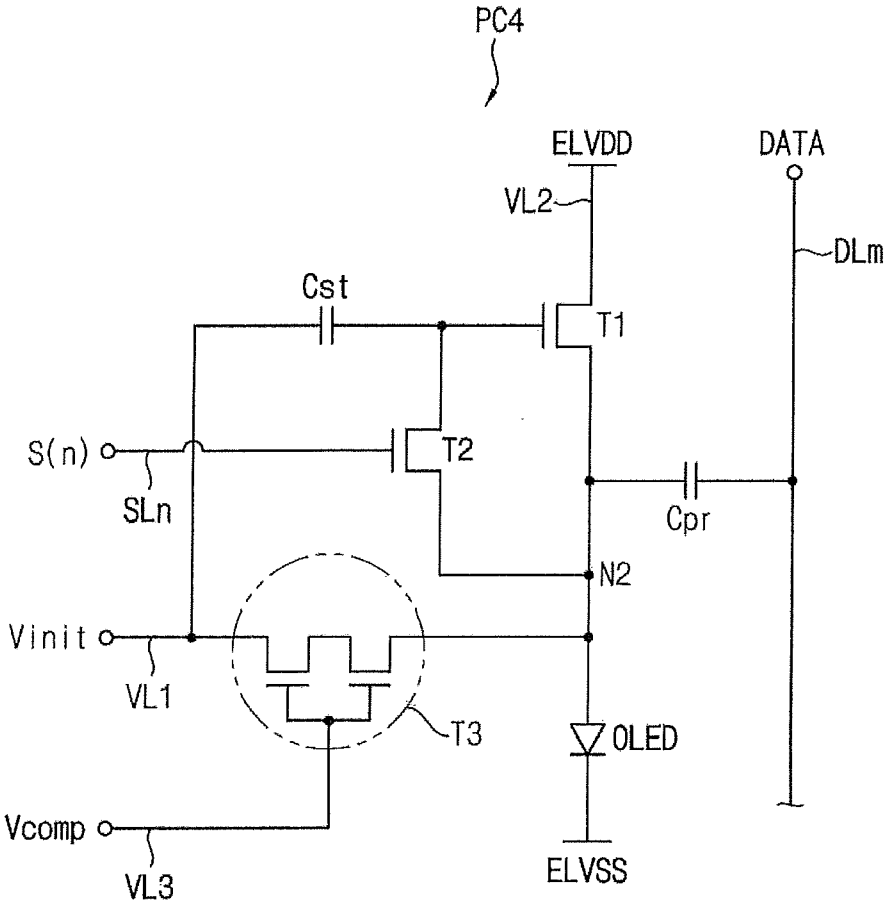

PC4
ELVDD
DATA
VL2
DLm
Cst
T1
S(n)
T2
SLn
Cpr
N2
Vinit
VL1
T3
OLED
Vcomp
VL3
ELVSS

FIG. 12

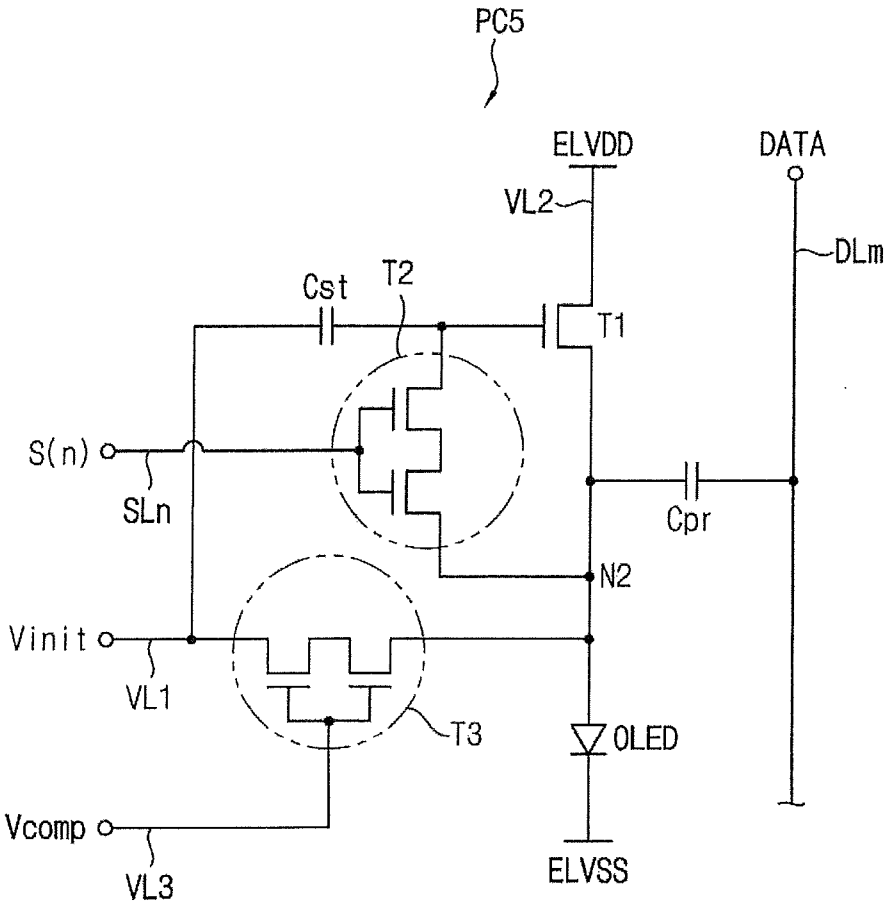

PC5
ELVDD
DATA
VL2
DLm
Cst
T2
T1
S(n)
SLn
Cpr
N2
Vinit
VL1
T3
OLED
Vcomp
VL3
ELVSS

FIG. 13

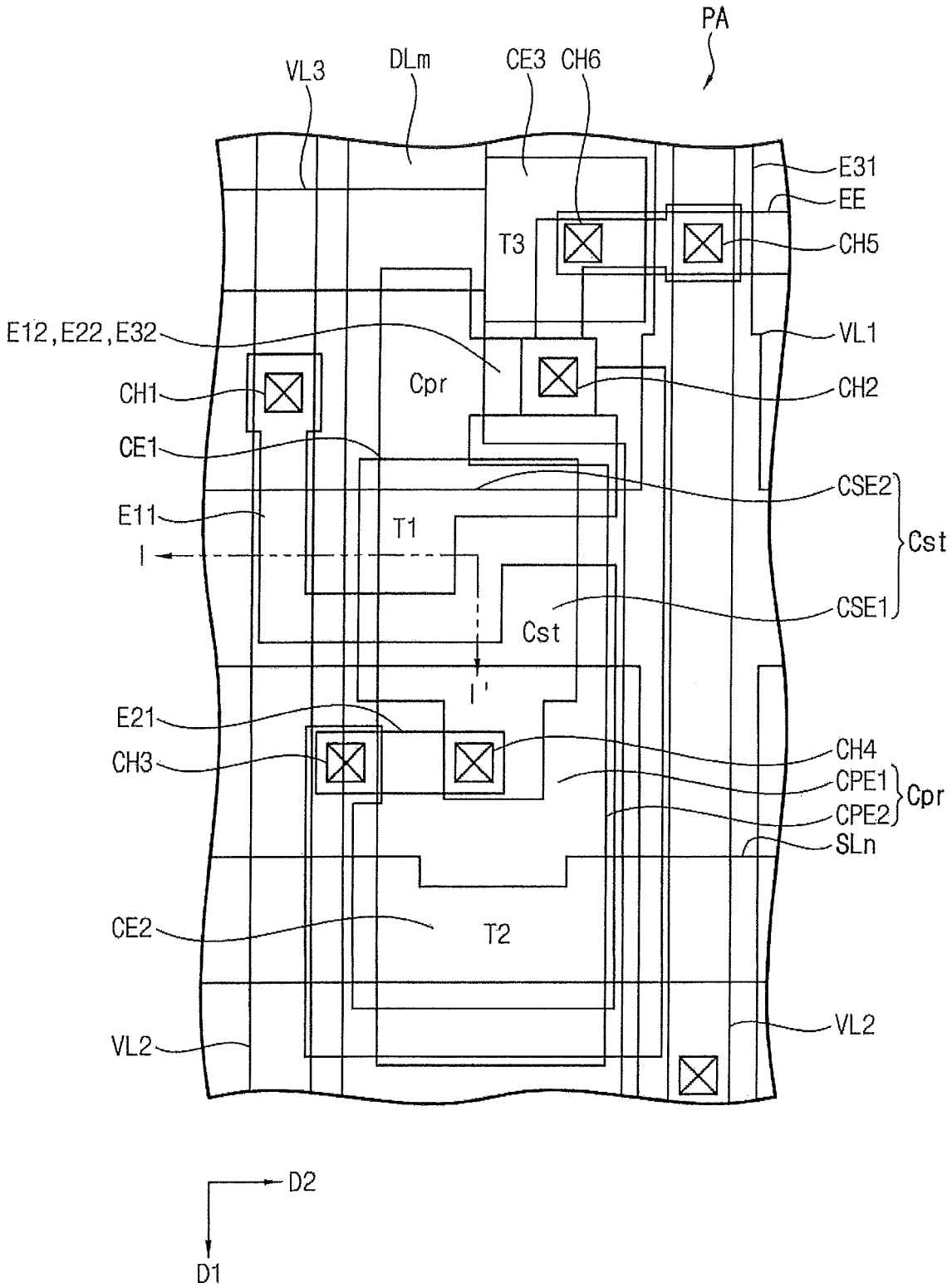

PA
VL3
DLm
CE3
CH6
E31
EE
T3
CH5
E12,E22,E32
VL1
CH1
Cpr
CH2
CE1
CSE2
Cst
E11
T1
I
CSE1
Cst
I'
E21
CH3
CH4
CPE1
Cpr
CPE2
SLn
CE2
T2
VL2
VL2
D2
D1

FIG. 14

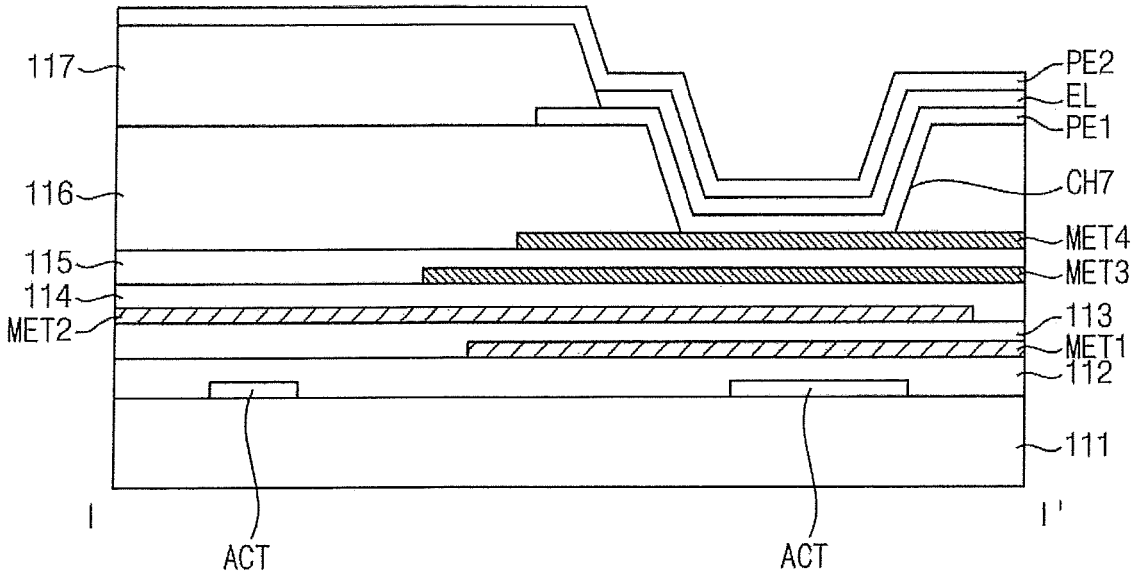

117
116
115
114
MET2
PE2
EL
PE1
CH7
MET4
MET3
113
MET1
112
111
I
I'
ACT
ACT

FIG. 15

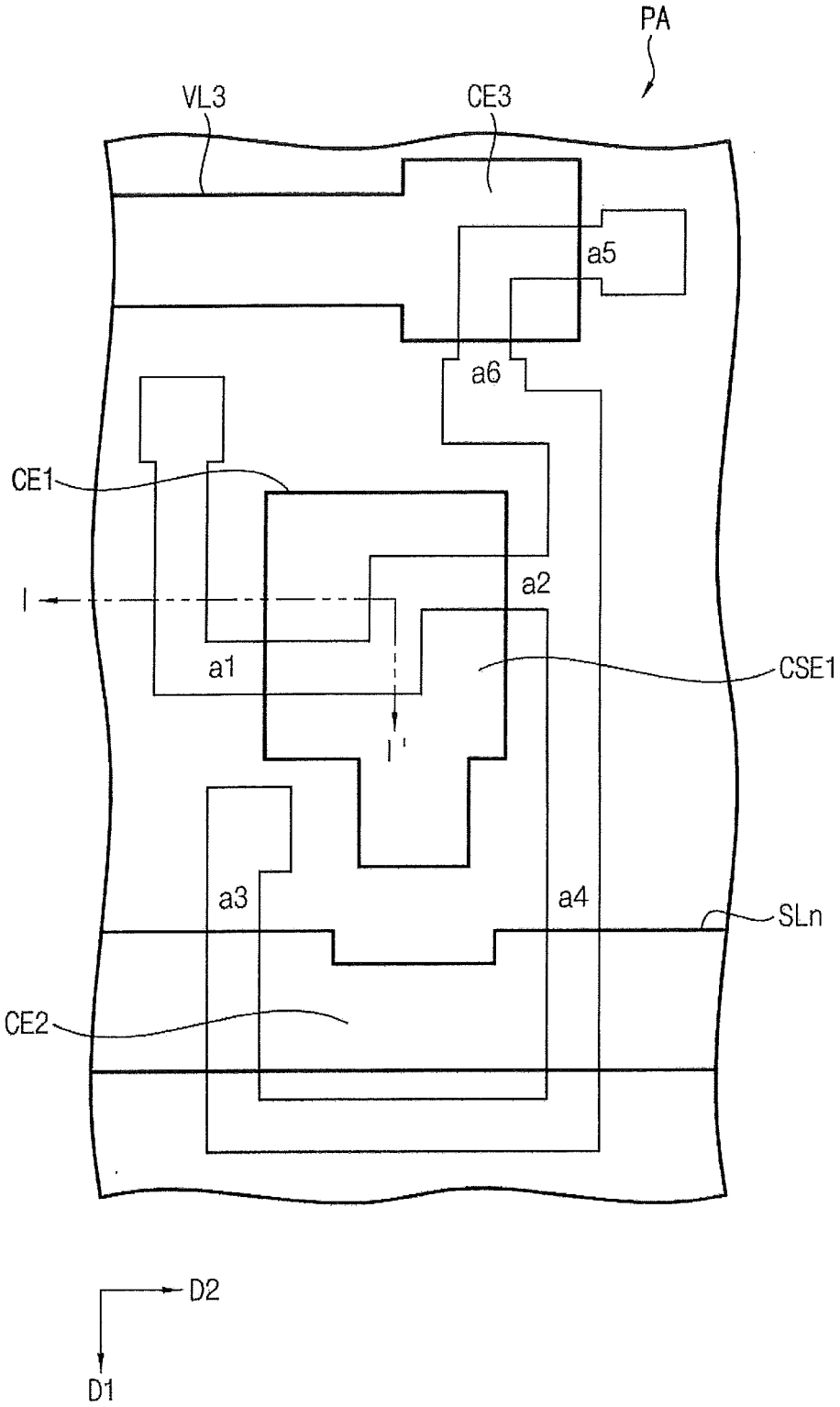


FIG. 16

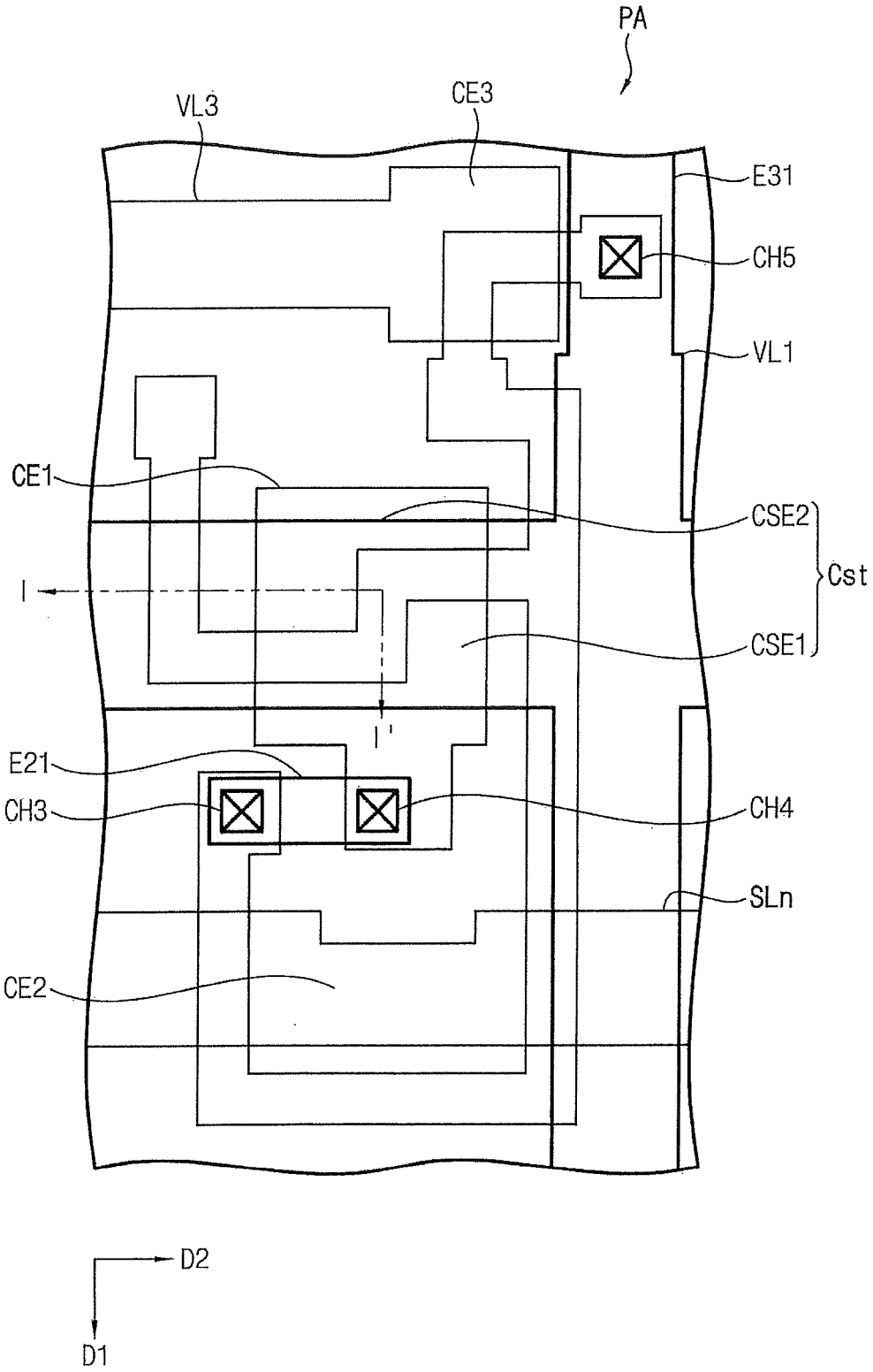

PA
VL3
CE3
E31
CH5
VL1
CE1
CSE2
Cst
I
CSE1
I'
E21
CH3
CH4
SLn
CE2
D2
D1

FIG. 17

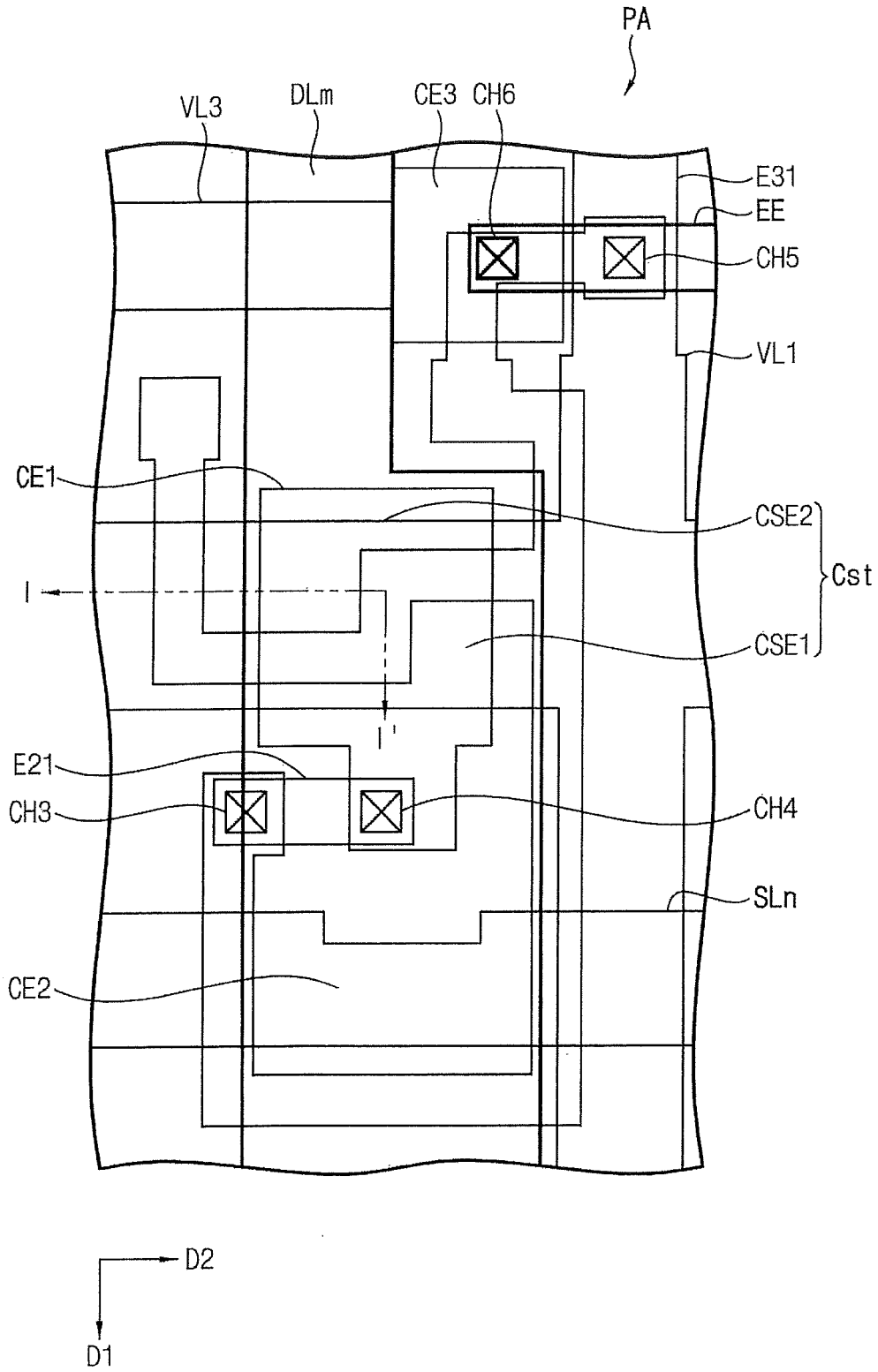

PA
VL3
DLm
CE3
CH6
E31
EE
CH5
VL1
CE1
CSE2
Cst
I
CSE1
I'
E21
CH3
CH4
SLn
CE2
D2
D1

FIG. 18

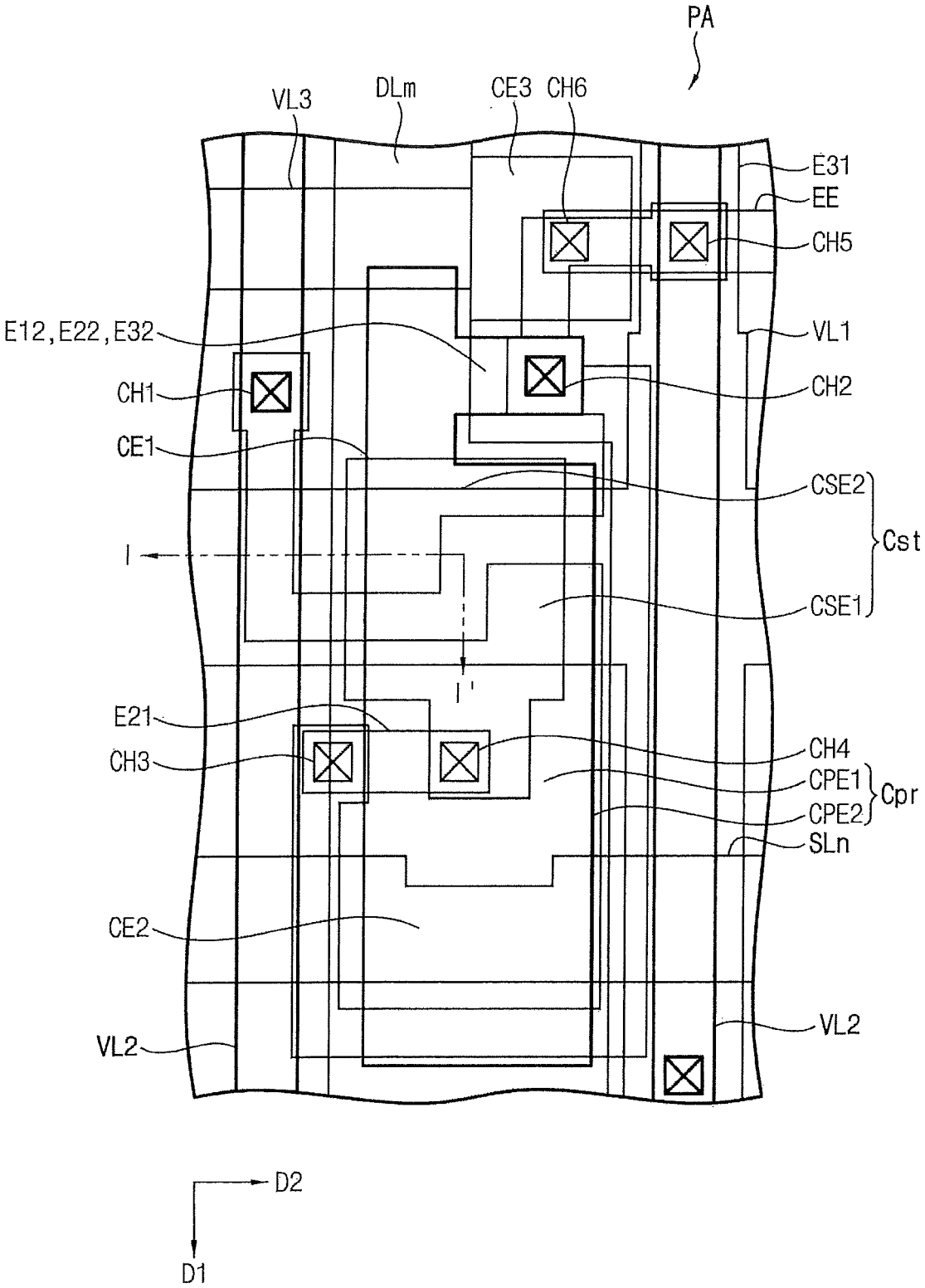
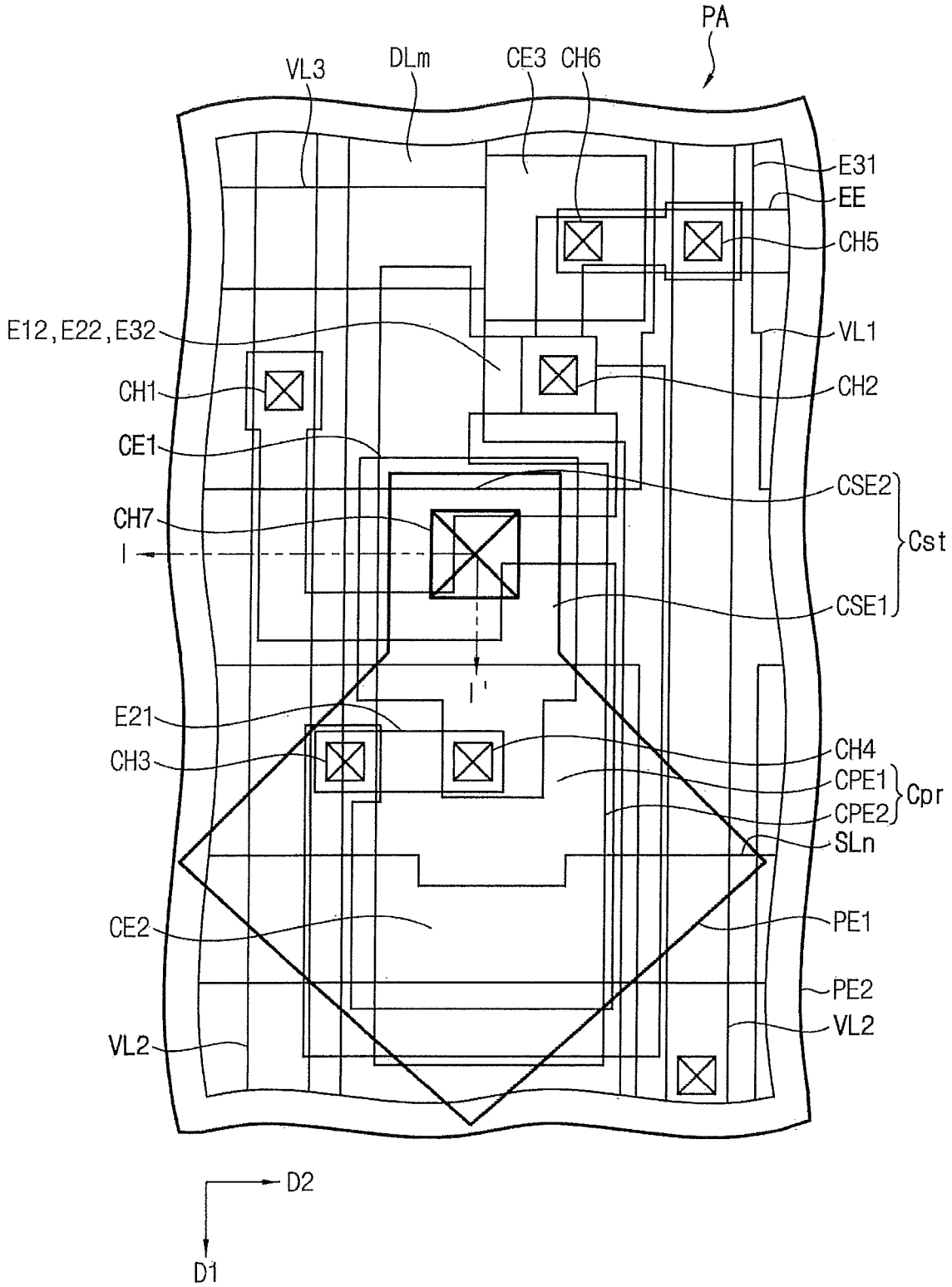

PA
VL3
DLm
CE3
CH6
E31
EE
CH5
E12,E22,E32
VL1
CH1
CH2
CE1
CSE2
Cst
I
CSE1
I'
E21
CH3
CH4
CPE1
Cpr
CPE2
SLn
CE2
VL2
VL2
D2
D1

FIG. 19


PA
VL3
DLm
CE3
CH6
E31
EE
CH5
E12,E22,E32
VL1
CH1
CH2
CE1
CSE2
Cst
CH7
I
I'
CSE1
E21
CH4
CH3
CPE1
Cpr
CPE2
SLn
CE2
PE1
PE2
VL2
VL2
D2
D1

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 2008136795 A **[0003]**
- US 2006044244 A **[0003]**

专利名称(译)	显示装置及其控制方法		
公开(公告)号	EP3246913B1	公开(公告)日	2019-12-18
申请号	EP2017171826	申请日	2017-05-18
[标]申请(专利权)人(译)	三星显示有限公司 汉阳大学校产学协力团		
申请(专利权)人(译)	三星DISPLAY CO.，LTD. 产学合作基础汉阳大学		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD. 产学合作基础汉阳大学		
[标]发明人	CHAI CHONG CHUL KWON OH KYONG KEUM NACK HYEON OH KYONG HWAN SEO YOUNG WAN HER YONG KOO HWANG IN JAE		
发明人	CHAI, CHONG-CHUL KWON, OH KYONG KEUM, NACK-HYEON OH, KYONG-HWAN SEO, YOUNG-WAN HER, YONG-KOO HWANG, IN-JAE		
IPC分类号	G09G3/3233 H01L27/32 G09G3/3266		
CPC分类号	G09G3/3225 G09G3/3266 G09G3/3275 G09G3/3233 G09G2300/0426 G09G2300/0819 G09G2300/0852 G09G2300/0866 G09G2310/063 G09G2320/043 G09G2330/021 G09G3/3258 G09G2320/02		
优先权	1020160061093 2016-05-18 KR		
其他公开文献	EP3246913A2 EP3246913A3		
外部链接	Espacenet		

摘要(译)

显示设备包括多个像素。 像素包括：第一电容器，其连接在接收第一驱动信号的第一电压线与第一节点之间；第一晶体管，其包括连接至第一节点的控制电极；第一电极，其连接至接收第一电源信号的第二电压线。 连接到第二节点的第二电极，包括连接到第二节点的阳极和接收第二电源信号的阴极的有机发光二极管，连接在第m条数据线和第二节点之间的第二电容器（其中，“ m”是自然数）和第二晶体管，第二晶体管包括连接至第n条扫描线的控制电极（其中，“ n”是自然数），连接至第一节点的第一电极和第二电极。 电极连接到第二节点。

Equation 1

$$ELVDD_L + V_{th,T1} < Init_L < ELVSS + V_{th,OLED}$$