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(54) PIXEL CIRCUIT, DISPLAY DEVICE, AND METHOD OF DRIVING PIXEL CIRCUIT

PIXELSCHALTUNG, ANZEIGEVORRICHTUNG UND VERFAHREN ZUM ANSTEUERN DIESER PIXELSCHALTUNG

CIRCUIT DE PIXEL, DISPOSITIF D'AFFICHAGE ET METHODE DE PILOTAGE DE CE CIRCUIT DE PIXEL

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(73) Proprietor: **Sony Corporation**
Tokyo 108-0075 (JP)

(72) Inventors:
- **Uchino, Katsuhide**
  Tokyo, 108-0075 (JP)
- **Yamashita, Junichi**
  Tokyo, 108-0075 (JP)
- **Yamamoto, Tetsuro**
  Tokyo, 108-0075 (JP)

(74) Representative: **Witte, Weller & Partner Patentanwälte mbB**
Postfach 10 54 62
70047 Stuttgart (DE)

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Description

TECHNICAL FIELD

[0001] The present invention relates to a display device comprised of pixel circuits arrayed in a matrix, in particular a so-called active matrix type image display device controlled in value of current flowing through the electro-optic elements by insulating gate type field effect transistors provided inside the pixel circuits, and a method of driving a pixel circuit.

BACKGROUND ART

[0002] In an image display device, for example, a liquid crystal display, a large number of pixels are arranged in a matrix and the light intensity is controlled for every pixel in accordance with the image information to be displayed so as to display an image.

[0003] This same is true for an organic EL display etc. An organic EL display is a so-called self-light emitting type display having a light emitting element in each pixel circuit and has the advantages that the viewability of the image is higher in comparison with a liquid crystal display, a backlight is unnecessary, the response speed is high, etc.

[0004] Further, it greatly differs from a liquid crystal display etc. in the point that the gradations of the color generation are obtained by controlling the luminance of each light emitting element by the value of the current flowing through the light emitting element, that is, each light emitting element is a current controlled type.

[0005] An organic EL display, in the same way as a liquid crystal display, may be driven by a simple matrix and an active matrix system. While the former has a simple structure, it has the problem that realization of a large sized and high definition display Is difficult. For this reason, much effort is being devoted to development of the active matrix system of controlling the current flowing through the light emitting element inside each pixel circuit by an active element provided inside the pixel circuit, generally, a TFT (thin film transistor).

[0006] FIG. 1 is a block diagram of the configuration of a general organic EL display device.

[0007] This display device 1 has, as shown in FIG. 1, a pixel array portion 2 comprised of pixel circuits (PXLC) 2a arranged in an m x n matrix, a horizontal selector (HSEL) 3, a write scanner (WSCN) 4, data lines DTL1 to DTLn selected by the horizontal selector 3 and supplied with a data signal in accordance with the luminance information, and scanning lines WSL1 to WSLm selectively driven by the write scanner 4.

[0008] Note that the horizontal selector 3 and the write scanner 4 are sometimes formed around the pixels by MOSICs etc. when formed on polycrystalline silicon.

[0009] FIG. 2 is a circuit diagram of an example of the configuration of a pixel circuit 2a of FIG. 1 (refer to for example U.S. Patent No. 5,684,365 and Patent Publication 2: Japanese Unexamined Patent Publication (Kokai) No. 8-234683).

[0010] The pixel circuit of FIG. 2 has the simplest circuit configuration among the large number of proposed circuits and is a so-called two-transistor drive type circuit.

[0011] The pixel circuit 2a of FIG. 2 has a p-channel thin film FET (hereinafter, referred to as TFT) 11 and TFT 12, a capacitor C11, and a light emitting element constituted by an organic EL element (OLED) 13. Further, in FIG. 2, DTL indicates a data line, and WSL indicates a scanning line.

[0012] An organic EL element has a rectification property in many cases, so sometimes is referred to as an OLED (organic light emitting diode). The symbol of a diode is used as the light emitting element in FIG. 2 and the other figures, but a rectification property Is not always required for an OLED in the following explanation.

[0013] In the pixel circuit 2a of FIG. 2, a source of the TFT 11 is connected to a power source potential VCC, and a cathode of the light emitting element 13 is connected to a ground potential GND. The operation of the pixel circuit 2a of FIG. 2 is as follows.

<Step ST1>:

[0014] When the scanning line WSL is made a selected state (low level here) and a write potential Vdata is supplied to the data line DTL, the TFT 12 becomes conductive, the capacitor C11 is charged or discharged, and the gate potential of the TFT 11 becomes Vdata.

<Step ST2>:

[0015] When the scanning line WSL is made a non-selected state (high level here), the data line DTL and the TFT 11 are electrically separated, but the gate potential of the TFT 11 is held stably by the capacitor C11.

<Step ST3>:

[0016] The current flowing through the TFT 11 and the light emitting element 13 becomes a value in accordance with a gate-source voltage Vgs of the TFT 11, while the light emitting element 13 is continuously emitting light with a luminance in accordance with the current value.

[0017] As in the above step ST1, the operation of selecting the scanning line WSL and transmitting the luminance information given to the data line to the inside of a pixel will be referred to as "writing" below.

[0018] As explained above, in the pixel circuit 2a of FIG. 2, if once the Vdata is written, the light emitting element 13 continues to emit light with a constant luminance in the period up to the next rewrite operation.

[0019] As explained above, in the pixel circuit 2a, by changing a gate application voltage of the drive transistor constituted by the TFT 11, the value of the current flowing through the EL element 13 is controlled.

[0020] At this time, the source of the p-channel drive transistor is connected to the power source potential Vcc, so this TFT 11 is always operating in a saturated region. Accordingly, it becomes a constant current source having a value shown in the following equation 1.

$$Ids = 1/2 \cdot \mu(W/L)Cox(Vgs-|Vth|)^2 \qquad (1)$$

[0021] Here, μ indicates the mobility of a carrier, Cox indicates a gate capacitance per unit area, W indicates a gate width, L indicates a gate length, and Vth indicates the threshold value of the TFT 11.

[0022] In a simple matrix type image display device, each light emitting element emits light only at a selected instant, while in an active matrix, as explained above, each light emitting element continues emitting light even after the end of the write operation. Therefore, it becomes advantageous in especially a large sized and high definition display in the point that the peak luminance and peak current of each light emitting element can belowered in comparison with a simple matrix.

[0023] FIG. 3 is a view of the change along with elapse of the current-voltage (I-V) characteristic of an organic EL element. In FIG. 3, the curve shown by the solid line indicates the characteristic in the initial state, while the curve shown by the broken line indicates the characteristic after change with elapse.

[0024] In general, the I-V characteristic of an organic EL element ends up deteriorating along with elapse as shown in FIG. 3.

[0025] However, since the two-transistor drive system of FIG. 2 is a constant current drive system, a constant current is continuously supplied to the organic EL element as explained above. Even if the I-V characteristic of the organic EL element deteriorates, the luminance of the emitted light will not change along with elapse.

[0026] The pixel circuit 2a of FIG. 2 is comprised of p-channel TFTs, but if it were possible to configure it by n-channel TFTs, it would be possible to use an amorphous silicon (a-Si) process in the past in the fabrication of the TFTs. This would enable a reduction in the cost of TFT boards.

[0027] Next, consider a pixel circuit replacing the transistors with n-channel TFTs.

[0028] FIG. 4 is a circuit diagram of a pixel circuit replacing the p-channel TFTs of the circuit of FIG. 2 with n-channel TFTs.

[0029] The pixel circuit 2b of FIG. 4 has an n-channel TFT 21 and TFT 22, a capacitor C21, and a light emitting element constituted by an organic EL element (OLED) 23. Further, in FIG. 4, DTL indicates a data line, and WSL indicates a scanning line.

[0030] In the pixel circuit 2b, the drain side of the drive transistor constituted by the TFT 21 Is connected to the power source potential Vcc, and the source is connected to the anode of the organic EL light emitting element 23, whereby a source-follower circuit is formed.

[0031] FIG. 5 is a view of the operating point of a drive transistor constituted by the TFT 21 and an EL element 23 in the initial state. In FIG. 5, the abscissa indicates the drain-source voltage Vds of the TFT 21, while the ordinate indicates the drain-source current Ids.

[0032] As shown in FIG. 5, the source voltage is determined by the operating point of the drive transistor constituted by the TFT 21 and the EL light emitting element 23. The voltage differs in value depending on the gate voltage.

[0033] This TFT 21 is driven in the saturated region, so a current Ids of the value of the above equation 1 is supplied for the Vgs for the source voltage of the operating point.

[0034] However, here too, similarly, the I-V characteristic of the organic EL element ends up deteriorating along with elapse. As shown in FIG. 6, the operating point ends up fluctuating due to this deteriorating along with elapse. The source voltage fluctuates even if supplying the same gate voltage.

[0035] Due to this, the gate-source voltage Vgs of the drive transistor constituted by the TFT 21 ends up changing and the value of the current flowing fluctuates. The value of the current flowing through the organic EL element 23 simultaneously changes, so if the I-V characteristic of the organic EL element 23 deteriorates, the luminance of the emitted light will end up changing along with elapse in the source-follower circuit of FIG. 4.

[0036] Further, as shown in FIG. 7, a circuit configuration where the source of the drive transistor constituted by the n-channel TFT 21 is connected to the ground potential GND, the drain is connected to the cathode of the organic EL light emitting element 23, and the anode of the organic EL light emitting element 23 is connected to the power source potential Vcc may be considered.

[0037] With this system, in the same way as when driven by the p-channel TFT of FIG. 2 , the potential of the source is fixed, the drive transistor constituted by the TFT 21 operates as a constant current source, and a change in the luminance due to deterioration of the I-V characteristic of the organic EL element can be prevented.

[0038] With this system, however, the drive transistor has to be connected to the cathode side of the organic EL light emitting element. This cathodic connection requires development of new anode-cathode electrodes. This is considered extremely difficult with the current level of technology.

[0039] From the above, in the past systems, no organic EL light emitting element using a n-channel transistor free of change in luminance has been developed.

[0040] A display and a driving method thereof are disclosed in US 2003/0090446 A1.

DISCLOSURE OF THE INVENTION

[0041] An object of the present invention is to provide an improved display device.

[0042] To achieve the above object, according to the present invention there is provided a display device as defined in claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0043]

FIG. 1 is a block diagram of the configuration of a general organic EL display device.

FIG. 2 is a circuit diagram of an example of the configuration of a pixel circuit of FIG. 1.

FIG. 3 is a graph of the change along with elapse of the current-voltage (I-V) characteristic of an organic EL device.

FIG. 4 is a circuit diagram of a pixel circuit in which p-channel TFTs of the circuit of FIG. 2 are replaced by n-channel TFTs.

FIG. 5 is a graph showing the operating point of a drive transistor constituted by a TFT and an EL light emitting elment in the initial state.

FIG. 6 is a graph showing the operating point of a drive transistor constituted by a TFT and an EL light emitting element after change along with elapse.

FIG. 7 is a circuit diagram of a pixel circuit connecting a source of a drive transistor constituted by an n-channel TFT to a ground potential.

FIG. 8 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a first example not part of the invention.

FIG. 9 is a circuit diagram of a specific configuration of a pixel circuit according to the first example not part of the invention in the organic EL display device of FIG. 1.

FIGS. 10A to 10F are views of equivalent circuits for explaining the operation of the circuit of FIG. 9.

FIGS. 11A to 11F are timing charts for explaining the operation of the circuit of FIG. 9.

FIG. 12 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a second example not part of the invention.

FIG. 13 is a circuit diagram of a specific configuration of a pixel circuit according to the second example not part of the invention in the organic EL display device of FIG. 12.

FIGS. 14A to 14E are views of equivalent circuits for explaining the operation of the circuit of FIG. 13.

FIGS. 15A to 15F are timing charts for explaining the operation of the circuit of FIG. 13.

FIG. 16 is a circuit diagram of another example of the configuration of a pixel circuit according to the second example not part of the invention.

FIG. 17 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a third example not part of the invention.

FIG. 18 is a circuit diagram of a specific configuration of a pixel circuit according to the third example not part of the invention in the organic EL display device of FIG. 17.

FIGS. 19A to 19E are views of equivalent circuits for explaining the operation of the circuit of FIG. 18.

FIGS. 20A to 20F are timing charts for explaining the operation of the circuit of FIG. 18.

FIGS. 21 is a circuit diagram of another example of the configuration of a pixel circuit according to the third example not part of the invention.

FIG. 22 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a fourth example not part of the invention

FIG. 23 is a circuit diagram of a specific configuration of a pixel circuit according to the fourth example not part of the invention in the organic EL display device of FIG. 22.

FIGS. 24A to 24E are views of equivalent circuits for explaining the operation of the circuit of FIG. 23.

FIGS. 25A to 25H are timing charts for explaining the operation of the circuit of FIG. 23.

FIG. 26 is a circuit diagram of a pixel circuit having a fixed voltage line as the power source potential VCC.

FIG. 27 is a circuit diagram of a pixel circuit having a fixed voltage line as the ground potential GND.

FIG. 28 is a circuit diagram of another example of the configuration of a pixel circuit according to the fourth example not part of the invention.

FIG. 29 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a fifth example not part of the invention.

FIG. 30 is a circuit diagram of a specific configuration pf a pixel circuit according to the fifth example not part of the invention in the organic EL display device of FIG. 29.

FIGS. 31A to 31E are views of equivalent circuits for explaining the operation of the circuit of FIG. 30.

FIGS. 32A to 32H are timing charts for explaining the operation of the circuit of FIG. 30 .

FIG. 33 is a circuit diagram of a pixel circuit having a fixed voltage line as the power source potential VCC.

FIG. 34 is a circuit diagram of a pixel circuit having a fixed voltage line as the ground potential GND.

FIG. 35 is a circuit diagram of another example of the configuration of a pixel circuit according to the fifth example not part of the invention.

FIG. 36 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a first embodiment.

FIG. 37 is a circuit diagram of a specific configuration of a pixel circuit according to the first embodiment in the organic EL display device of FIG. 36

FIGS. 38A to 38F are views of equivalent circuits for explaining the operation of the circuit of FIG. 37.

FIG. 39 is a view of an equivalent circuit for explaining the operation of the circuit of FIG. 37.

FIGS. 40A to 40H are timing charts for explaining the operation of the circuit of FIG. 37.

BEST MODE FOR WORKING THE INVENTION

[0044] Below, an embodiment of the present invention will be described with reference to figures 37-40. The other embodiments are illustrative examples.

<First example not part of the invention>

[0045] FIG. 8 is a block diagram of the configuration of an organic EL display device employing pixel circuits according to the first example not part of the invention.

[0046] FIG. 9 is a circuit diagram of the concrete configuration of a pixel circuit according to the first example not part of the invention in the organic EL display device of FIG. 8.

[0047] This display device 100 has, as shown in FIG. 8 and FIG. 9, a pixel array portion 102 having pixel circuits (PXLC) 101 arranged in an m x n matrix, a horizontal selector (HSEL) 103, a write scanner (WSCN) 104, a drive scanner (DSCN) 105, data lines DTL101 to DTL10n selected by the horizontal selector 103 and supplied with a data signal in accordance with the luminance information, scanning lines WSL101 to WSL10m selectively driven by the write scanner 104, and drive lines DSL101 to DSL10m selectively driven by the drive scanner 105.

[0048] Note that while the pixel circuits 101 are arranged in an m x n matrix in the pixel array portion 102, FIG. 9 shows an example wherein the pixel circuits are arranged in a 2 (= m) x 3 (= n) matrix for the simplification of the drawing.

[0049] Further, in FIG. 9, the concrete configuration of one pixel circuit Is shown for simplification of the drawing.

[0050] The pixel circuit 101 according to the first example not part of the invention has, as shown in FIG. 9, an n-channel TFT 111 to TFT 113, a capacitor C111, a light emitting element 114 made of an organic EL element (OLED), and nodes ND111 and ND112.

[0051] Further, in FIG. 9, DTL101 indicates a data line, WSL101 indicates a scanning line, and DSL101 indicates a drive line.

[0052] Among these components, TFT 111 configures the field effect transistor according to the present invention, TFT 112 configures the first switch, TFT 113 configures the second switch, and the capacitor C111 configures the pixel capacitance element according to the present invention.

[0053] Further, the scanning line WSL101 corresponds to the first control line according to the present invention, while the drive line DSL101 corresponds to the second control line.

[0054] Further, the supply line (power source potential) of the power source voltage Vcc corresponds to the first reference potential, while the ground potential GND corresponds to the second reference potential.

[0055] In the pixel circuit 101, a light emitting element (OLED) 114 is connected between a source of the TFT 111 and the second reference potential (in this present example not part of the invention, the ground potential GND). Specifically, the anode of the light emitting element 114 is connected to the source of the TFT 111, while the cathode side is connected to the ground potential GND. The connection point of the anode of the light emitting element 114 and the source of the TFT 111 constitutes a node ND111.

[0056] The source of the TFT 111 is connected to a drain of the TFT 113 and a first electrode of the capacitor C111, while the gate of the TFT 111 is connected to a node ND112.

[0057] The source of the TFT 113 is connected to a fixed potential (in the present example not part of the invention, a ground potential GND), while the gate of the TFT 113 is connected to the drive line DSL101. Further, a second electrode of the capacitor C111 is connected to the node ND112.

[0058] A source and a drain of the TFT 112 as first switch are connected to the data line DTL101 and node ND112. Further, a gate of the TFT 112 is connected to the scanning line WSL101.

[0059] In this way, the pixel cicuit 101 according to the present example not part of the invention is configured with a capacitor C111 connected between the gate and source of the TFT 111 as the drive transistor and with a source potential of the TFT 111 connected to a fixed potential through the TFT 113 as the switching transistor.

[0060] Next, the operation of the above configuration will be explained focusing on the operation of a pixel circuit with reference to FIGS. 10A to 10F and FIGS. 11A to 11F.

[0061] Note that FIG. 11A shows a scanning signal ws[101] applied to the first row scanning line WSL101 of the pixel array, FIG. 11B shows a scanning signal ws[102] applied to the second row scanning line WSL102 of the pixel array, FIG. 11C shows a drive signal ds[101] applied to the first row drive line DSL101 of the pixel array, FIG. 11D shows a drive signal ds[101] applied to the second row drive line DSL102 of the pixel array, FIG. 11E shows a gate potential Vg of the TFT 111, and FIG. 11F shows a source potential Vs of the TFT 111.

[0062] First, at the time of the ordinary emitting state of the EL light emitting element 114, as shown in FIGS. 11A to 11D, the scanning signals ws[101], ws[102],.. to the scanning lines WSL101, WSL102,... are selectively set to the low level by the write scanner 104, and the drive signals ds[101], ds[102],... to the drive lines DSL101, DSL102,... are selectively set to the low level by the drive scanner 105.

[0063] As a result, in the pixel circuits 101, as shown in FIG. 10A, the TFT 112 and TFT 113 are held in the off state.

[0064] Next, in the non-emitting period of the EL element 114, as shown in FIGS. 11A to 11D, the scanning signals ws[101], ws[102],.. to the scanning lines WSL101, WSL102,... are held at the low level by the write scanner 104, and the drive signals ds[101], ds[102],... to the drive lines DSL101, DSL102,... are selectively set to the high level by the drive scanner 105.

[0065] As a result, in the pixel circuits 101, as shown in FIG. 10B, the TFT 112 is held In the off state and the TFT 113 is turned off.

[0066] At this time, current flows through the TFT 113 and, as shown in FIG. 11F, the source potential Vs of the TFT 111 falls to the ground potential GND. Therefore, the voltage applied to the EL light emitting element 114 also becomes 0V and the EL light emitting element 114 becomes non-emitting in state.

[0067] Next, in the non-emitting period of the EL light emitting element 114, as shown in FIGS. 11A to 11D, the drive signals ds[101], ds[102],.. to the drive lines DSL101, DSL102,... are held at the high level by the drive scanner 105, and the scanning signals ws[101], ws[102],... to the scanning lines WSL101, WSL102,... are selectively set to the high level by the write scanner 104.

[0068] As a result, in the pixel circuits 101, as shown in FIG. 10C, the TFT 113 is held in the on state and the TFT 112 is turned on. Due to this, the horizontal selector 103 writes the input signal (Vin) propagated to the data line DTL101 into the capacitor C111 as the pixel capacitor.

[0069] At this time, as shown in FIG. 11F, the source potential Vs of the TFT 111 as the drive transistor is at the ground potential level (GND level), so, as shown in FIGS. 11E and 11F, the potential difference between the gate and source of the TFT 111 becomes equal to the voltage Vin of the input signal.

[0070] After this, in the non-emitting period of the EL light emitting element 114, as shown in FIGS. 11A to 11D, the drive signals ds[101], ds[102],... to the drive lines DSL101, DSL102,... are held at the high level by the drive scanner 105 and the scanning signals ws[101], ws[102],... to the scanning lines WSL101, WSL102,... are selectively set to the low level by the write scanner 104.

[0071] As a result, in the pixel circuit 101, as shown in FIG. 10D, the TFT 112 is turned off and the write operation of the input signal to the capacitor C111 as the pixel capacitor ends.

[0072] After this, as shown in FIGS. 11A to 11D, the scanning signals ws[101], ws[102],... to the scanning lines WSL101, are held at the low level by the write scanner 104 and the drive signals ds[101], ds[102],... to the drive lines DSL101, DSL102,... are selectively set to the low level by the drive scanner 104.

[0073] As a result, in the pixel circuit 101, as shown in FIG. 10E, the TFT 113 is turned off.

[0074] By turning the TFT 113 off, as shown in FIG. 11F, the source potential Vs of the TFT 111 as the drive transistor rises and current also flows to the EL light emitting element 114.

[0075] The source potential Vs of the TFT 111 fluctuates, but despite this, since there is a capacitor between the gate and source of the TFT 111, as shown in FIGS. 11E and 11F, the gate-source potential is constantly held at Vin.

[0076] At this time, the TFT 111 as the drive transistor drives in the saturated region, so the current Ids flowing through the TFT 111 becomes the value shown in the above equation 1. This value is determined by the gate source potential Vin of the TFT 111. This current Ids similarly flows to the EL light emitting element 114, whereby the EL light emitting element 114 emits light.

[0077] The equivalent circuit of the EL light emitting element 114 becomes as shown in FIG. 10F, so at this time the potential of the node ND111 rises to the gate potential by which the current Ids flows through the EL light emitting element 114.

[0078] Along with this rise in potential, the potential of the node ND112 also similarly rises through the capacitor 111 (pixel capacitor Cs). Due to this, as explained above, the gate-source potential of the TFT 111 is held at Vin.

[0079] Here, consider the problems in the past source-follower system in the circuit of the present invention. In this circuit as well, the EL light emitting element deteriorates in its I-V characteristic along with the increase in the emitting period. Therefore, even If the drive transistor sends the same current, the potential applied to the EL light emitting element changes and the potential of the node ND111 falls.

[0080] However, in this circuit, the potential of the node ND111 falls while the gate-source potential of the drive transistor is held constant, so the current flowing through the drive transistor (TFT 111) does not change. Accordingly, the current flowing through the EL light emitting element also does not change. Even if the I-V characteristic of the EL light emitting element deteriorates, a current corresponding to the input voltage Vin constantly flows. Therefore, the past problem can be solved.

[0081] As explained above, according to the present first example not part of the invention, the source of the TFT 111 as the drive transistor is connected to the anode of the light emitting element 114, the drain is connected to the power source potential Vcc, a capacitor C111 is connected between the gate and source of the TFT 111, and the source potential of the TFT 111 is connected to a fixed potential through the TFT 113 as the switching transistor, so the following effects can be obtained.

[0082] Source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL light emitting element along with elapse becomes possible.

[0083] A source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of an EL light emitting element while using current anode-cathode electrodes.

[0084] Further, it is possible to configure transistors of a pixel circuit by only n-channel transistors and possible to use the a-SI process in the fabrication of the TFTs. Due to this, there is the advantage that a reduction of the cost of TFT boards becomes possible.

<Second example not part of the invention>

[0085] FIG. 12 is a block diagram of the configuration of an organic EL display device employing pixel circuits according to a second example not part of the invention.

[0086] FIG. 13 is a circuit diagram of the concrete configuration of a pixel circuit according to the second example not part of the invention in the organic EL display device of FIG. 12.

[0087] The display device 200, as shown in FIG. 12 and FIG. 13, has a pixel array portion 202 having pixel circuits (PXLC) 201 arranged in an m x n matrix, a horizontal selector (HSEL) 203, a write scanner (WSCN) 204, a drive scanner (DSCN) 205, data lines DTL201 to DTL20n selected by the horizontal selector 203 and supplied with a data signal in accordance with the luminance Information, scanning lines WSL201 to WSL20m selectively driven by the write scanner 204, and drive lines DSL201 to DSL20m selectively driven by the drive scanner 205.

[0088] Note that while the pixel circuits 201 are arranged in an m x n matrix in the pixel array portion 202, FIG. 12 shows an example wherein the pixel circuits are arranged in a 2 (= m) x 3 (= n) matrix for the simplification of the drawing.

[0089] Further, in FIG. 13 as well, the concrete configuration of one pixel circuit is shown for simplification of the drawing.

[0090] Each pixel circuit 201 according to the second example not part of the invention has, as shown in FIG. 13, an n-channel TFT 211 to TFT 213, a capacitor C211, a light emitting element 214 made of an organic EL element (OLED), and nodes ND211 and ND212.

[0091] Further, in FIG. 13, DTL201 indicates a data line, WSL201 indicates a scanning line, and DSL201 indicates a drive line.

[0092] Among these components, the TFT 211 configures the field effect transistor according to the present invention, the TFT 212 configures the first switch, the TFT 213 configures the second switch, and the capacitor C211 configures the pixel capacitance element according to the present invention.

[0093] Further, the scanning line WSL 201 corresponds to the first control line according to the present invention, while the drive line DSL201 corresponds to the second control line.

[0094] Further, the supply line of the power source voltage Vcc (power source potential) corresponds to the first reference potential, while the ground potential GND corresponds to the reference potential.

[0095] In each pixel circuit 201, a source and a drain of the TFT 213 are connected between a source of the TFT 211 and an anode of the light emitting element 214, a drain of the TFT 211 is connected to the power source potential Vcc, and a cathode of the light emitting element 214 is connected to the ground potential GND. That is, the TFT 211 as the drive transistor, the TFT 213 as the switching transistor, and the light emitting element 214 are connected in series between the power source potential Vcc and the ground potential GND. Further, the connection point of the anode of the light emitting element 214 and the source of the TFT 213 constitutes a node ND211.

[0096] A gate of the TFT 211 is connected to the node ND212. Further, the capacitor C211 as a pixel capacitor Cs connected between the nodes ND211 and ND212, that is, between the gate of the TFT 211 and the anode of the light emitting element 214. A first electrode of the capacitor C211 is connected to the node ND211, while a second electrode is connected to the node ND212.

[0097] A gate of the TFT 213 is connected to the drive line DSL201. Further, a source and a drain of the TFT 212 as the first switch are connected to the data line DTL201 and the node ND212. Further, a gate of the TFT 212 is connected to the scanning line WSL201.

[0098] In this way, the pixel circuit 201 according to the present example not part of the invention is configured with the source of the TFT 211 as the drive transistor and the anode of the light emitting element 214 connected by the TFT 213 as the switching transistor, while a capacitor C211 connected between the gate of the TFT 211 and the anode of the light emitting element 214.

[0099] Next, the operation of the above configuration will be explained focusing on the operation of a pixel circuit with reference to FIGS. 14A to 14E and FIGS. 15A to 15F.

[0100] Note that FIG. 15A shows a scanning signal ws[201] applied to the first row scanning line WSL201 of the pixel array, FIG. 15B shows a scanning signal ws[202] applied to the second row scanning line WSL202 of the pixel array, FIG. 15C shows a drive signal ds[201] applied to the first row drive line DSL201 of the pixel array, FIG. 15D shows a drive signal ds[202] applied to the second row drivd line DSL202 of the pixel array, FIG. 15E shows a gate potential Vg of the TFT 211, and FIG. 15F shows an anode side potential of the TFT 211, that is, the potential VND211 of the node ND211.

[0101] First, at the ordinary emitting state of the EL light emitting element 214, as shown in FIGS. 15A to 15D, the scanning signals ws[201], ws[202],.. to the scanning lines WSL201, WSL202,... are selectively set to the low level by the write scanner 204, and the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are selectively set to the high level by the drive scanner 205.

[0102] As a result, in the pixel circuit 201, as shown in FIG. 14A, the TFT 212 is held in the off state and the TFT 213 is held in the on state.

[0103] At this time, the current Ids flows to the TFT 211 as the drive transistor and the EL light emitting element 214.

[0104] Next, in the non-emitting period of the EL light emitting element 214, as shown in FIGS. 15A to 15D, the scanning signals ws[201], ws[202],.. to the scanning lines WSL201, WSL202,... are held at the low level by the write scanner 204, and the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are selectively set to the low level by the drive scanner 205.

[0105] As a result, in the pixel circuit 201, as shown in FIG. 14B, the TFT 212 is held in the off state and the TFT 213 is turned off.

[0106] At this time, the potential held at the EL light emitting element 214 falls since the source of supply disappears. The potential falls to the threshold voltage Vth of the EL light emitting element 214. However, since current also flows to the EL light emitting element 214, if the non-emitting period continues, the potential will fall to GND.

[0107] On the other hand, the TFT 211 as thr drive transistor is held in the on state since the gate potential is high. This boosting is performed in a short period. After boosting to the Vcc, no current is supplied to the TFT 211.

[0108] That is, in the pixel circuit 201 of the second example not part of the invention, it is possible to operate without the supply of current in the pixel circuit during the non-emitting period and therefore possible to suppress the power consumption of the panel.

[0109] Next, in the non-emitting period of the EL light emitting element 214, as shown in FIGS. 15A to 15D, the drive signals ds[201], ds[202],.. to the drive lines DSL201, DSL202,... are held at the low level by the drive scanner 205, and the scanning signals ws[201], ws[202],... to the scanning lines WSL201, WSL202,... are selectively set to the high level by the write scanner 204.

[0110] As a result, in the pixel circuit 201, as shown in FIG. 14C, the TFT 213 is held in the off state and the TFT 212 is turned on. Due to this, the input signal (Vin) propagated to the data line DTL201 by the horizontal selector 203 is written into the capacitor C211 as the pixel capacitor Cs.

[0111] At this time, as shown in FIG. 15F, since the anode side potential Va of the TFT 213 as the switching transistor, that is, the potential VND211 of the node ND211, is at the ground potential level (GND level), the capacitor C211 as the pixel capacitor Cs is held at a potential equal to the voltage Vin of the input signal.

[0112] After this, in the non-emitting period of the EL light emitting element 214, as shown in FIGS. 15A to 15D, the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are held at the low level by the drive scanner 205, and the scanning signals ws[201], ws[202],... to the scanning lines WSL201, WSL202,... are selectively set to the low level by the write scanner 204.

[0113] As a result, in the pixel circuit 201, as shown in FIG. 14D, the TFT 212 is turned off and the write operation of the input signal to the capacitor C211 as the pixel capacitor ends.

[0114] After this, as shown in FIGS. 15A to 15D, the scanning signals ws[201], ws[202],... to the scanning lines WSL201, WSL202,... are held at the low level by the write scanner 204, and the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are selectively set to the high level by the drive scanner 205.

[0115] As a result, in the pixel circuit 201, as shown in FIG. 14E, the TFT 213 is turned on.

[0116] By turning the TFT 213 on, current flows to the EL light emitting element 214 and the source potential of the TFT 211 falls. The source potential of the TFT 211 as the drive transistor fluctuates, but despite this, since there is a capacitor between the gate of the TFT 211 and the anode of the light emitting element 214, the gate-source potential is held at Vin. At this time, the TFT 211 as the drive transistor is driven in the saturated region, so the current Ids flowing through the TFT 211 becomes the value shown in the above equation 1. This is the gate-source voltage Vgs of the drive transistor.

[0117] Here, the TFT 213 operates in the nonsaturated region, so this is viewed as a simple resistance value. Accordingly, the gate-source voltage of the TFT 211 is Vin minus the value of the voltage drop due to the TFT 211. That is, the current flowing through the TFT 211 can be said to be determined by the Vin.

[0118] Due to the above, even if the EL light emitting element 214 deteriorates in its I-V characteristic along with the increase in the emitting period, in the pixel circuit 201 of the second example not part of the invention, the potential of the node ND211 falls while the potential between the gate and source of the TFT 211 as thr drive transistor by is held constant, so the current flowing through the TFT 211 does not change.

[0119] Accordingly, the current flowing through the EL light emitting element 214 also does not change. Even if the I-V characteristic of the EL light emitting element 214 deteriorates, the current corresponding to the input voltage Vin constantly flows and therefore the past problem can be solved.

[0120] In addition, by raising the on voltage of the gate of the TFT 213, it is possible to suppress variation in the resistance value due to variation in the threshold value Vth of the TFT 213.

[0121] Note that, in FIG. 13, the potential of the cathode electrode of the light emitting element 214 is made the ground potential GND, but this may be made any other potential as well.

[0122] Further, as shown in FIG. 16, the transistors of the pixel circuits need not be n-channel transistors, p-channel TFTs 221 to 223 may also be used to form each pixel circuit. In this case, the power source is connected to the anode side of the EL light emitting element 224, while the TFT 221 as the drive transistor is connected to the cathode side.

[0123] Further, the TFT 212 and TFT 213 as the switching transistors may also be transistors of different polarities from the TFT 211 as the drive transistor.

[0124] Here, the pixel circuit 201 according to the second example not part of the invention and the pixel circuit 101 according to the first example not part of the invention explained above will be compared.

[0125] The basic difference between the pixel circuit 201 according to the second example not part of the invention and the pixel circuit 101 according to the first example not part of the invention lies in the difference in the position of connection of the TFT 213 and TFT 113 as the switching transistors.

[0126] In general, the I-V characteristic of an organic EL element ends up deteriorating along with elapse. However, in the pixel circuit 101 according to the first example not part of the invention, the potential difference Vs between the gate and source of the TFT 111 is held constant, so the current flowing through the TFT 111 is constant, therefore even if the I-V characteristic of the organic EL element deteriorates, the luminance is held.

[0127] In the pixel circuit 101 according to the first embodiment, when the TFT 112 is off and the TFT 113 is on, the source potential Vs of the drive transistor TFT 111 becomes the ground potential and the organic EL element 114 does not emit light and enters a non-emitting period. Simultaneously, the first electrode (one side) of the pixel capacitor also becomes the ground potential GND. However, even in the non-emitting period, the gate-source voltage continues to be held and current flows in the pixel circuit 101 from the power source (Vcc) to the GND.

[0128] In general, an organic EL element has an emitting period and a non-emitting period. The luminance of a panel is determined by the product of the intensity of the emission and the emitting period. Usually, the shorter the emitting period, the better the moving picture characteristics become, so it is preferable to use the panel in a short emitting period. To obtain the same luminance as with when shortening the emitting period, it is necessary to raise the intensity of the emission of the organic EL element and necessary to run a greater current through the drive transistor.

[0129] Here, the pixel circuit 101 according to the first example not part of the invention will be considered further.

[0130] In the pixel circuit 101 according to the first example not part of the invention, as explained above, current flows even during the non-emitting period. Therefore, if shortening the emitting period and raising the amount of current run, current continuously flows even during the non-emitting period, so the current consumption increases.

[0131] Further, in the pixel circuit 101 according to the first example not part of the invention, power source potential WCC and ground potential GND lines are necessary in the panel. Therefore, it Is necessary to lay two types of lines inside the panel at the TFT side. The Vcc and GND have to be laid by a low resistance to prevent a voltage drop. Accordingly, if laying two types of lines, the layout area of the lines has to be Increased. For this reason, if the pitch between pixels becomes smaller along with the higher definition of panels, laying of the transistors etc. is liable to become difficult. Simultaneously, the regions where the Vcc lines and GND lines overlap in the panel are liable to increase and the improvement of the yield is liable to be kept down.

[0132] As opposed to this, according to the pixel circuit 201 according to the second example not part of the invention, the effects of the above first example not part of the invention can be obtained of course and also the effects of reduction of the consumed current and lines and improvement of the yield can be obtained.

[0133] According to the second example not part of the invention, source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL light emitting element along with elapse becomes possible.

[0134] A source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of an EL light emitting element while using current anode-cathode electrodes.

[0135] Further, it is possible to configure transistors of a pixel circuit by only n-channel transistors and possible to use the a-Si process in the fabrication of the TFTs. Due to this, a reduction of the cost of TFT boards becomes possible.

[0136] Further, according to the second example not part of the invention, it is possible to slash the number of GND lines at the TFT side and layout of the surrounding lines and layout of the pixels become easier.

[0137] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board, and possible to improve the yield.

[0138] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board so as to lay the Vcc lines at a low resistance, and possible to obtain an image quality of a high uniformity.

<Third example not part of the invention>

[0139] FIG. 17 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a third example not part of the invention.

[0140] FIG. 18 is a circuit diagram of the concrete configuration of a pixel circuit according to the third example not part of the invention in the organic EL display device of FIG. 17.

[0141] The display device 200A according to the third example not part of the invention differs from the display device 200 according to the second example not part of the invention in the position of connection of the capacitor C211 as the pixel capacitor Cs in the pixel circuit.

[0142] Specifically, in the pixel circuit 201 according to the second example not part of the invention, the capacitor C211 is connected between the gate of the TFT 211 as the drive transistor and the anode side of the EL light emitting element 214.

[0143] As opposed to this, in the pixel circuit 201A according to the third example not part of the invention, the capacitor C211 is connected between the gate and source of the TFT 211 as the drive transistor. Specifically, a first electrode of the capacitor C211 is connected to the connection point (node ND211A) of the source of the TFT 211 and the TFT 213 as the switching transistor and a second electrode is connected to the node ND212.

[0144] The rest of the configuration is similar to that of the second example not part of the invention explained above.

[0145] Next, the operation of the above configuration will be explained focusing on the operation of a pixel circuit with reference to FIGS. 19A to 19E and FIGS. 20A to 20F.

[0146] First, at the ordinary emitting state of the EL light emitting element 214, as shown in FIGS. 20A to 20D, the scanning signals ws[201], ws[202],.. to the scanning lines WSL201, WSL202,... are selectively set to the low level by the write scanner 204, and the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are selectively set to the high level by the drive scanner 205.

[0147] As a result, in the pixel circuit 201A, as shown in FIG. 19A, the TFT 212 is held in the off state and the TFT 213 is held in the on state.

[0148] At this time, the current Ids flows to the TFT 211 as the drive transistor and the EL light emitting element 214.

[0149] Next, in the non-emitting period of the EL light emitting element 214, as shown in FIGS. 20A to 20D, the scanning signals ws[201], ws[202],.. to the scanning lines WSL201, WSL202,... are held at the low level by the write scanner 204, and the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are selectively set to the low level by the drive scanner 205.

[0150] As a result, in the pixel circuit 201A, as shown in FIG. 19B, the TFT 212 is held in the off state and the TFT 213 is turned off.

[0151] At this time, the potential held at the EL light emitting element 214 falls since the source of supply disappears. The potential falls to the threshold voltage Vth of the EL light emitting element 214. However, since off current also flows to the EL light emitting element 214, if the non-emitting period continues, the potential will fall to GND.

[0152] On the other hand, the TFT 211 as the drive transistor is held in the on state since the gate potential is high. As shown in FIG. 20F, the source potential Vs of the TFT 211 is boosted to the power source voltage Vcc. This boosting is performed in a short period. After boosting to the Vcc, no current is supplied to the TFT 211.

[0153] That is, in the pixel circuit 201A of the third example not part of the invention, it is possible to operate without the supply of current in the pixel circuit during the non-emitting period and therefore possible to suppress the power consumption of the panel.

[0154] Next, in the non-emitting period of the EL light emitting element 214, as shown in FIGS. 20A to 20D, the drive signals ds[201], ds[202],.. to the drive lines DSL201, DSL202,... are held at the low level by the drive scanner 205, and the scanning signals ws[201], ws[202],... to the scanning lines WSL201, WSL202,... are selectively set to the high level by the write scanner 204.

[0155] As a result, in the pixel circuit 201A, as shown in FIG. 19C, the TFT 213 is held in the off state and the TFT 212 is turned on. Due to this, the input signal (Vin) propagated to the data line DTL201 by the horizontal selector 203 is written into the capacitor C211 as the pixel capacitor Cs.

[0156] At this time, as shown in FIG. 20F, since the source Vs of the TFT 213 as the switching transistor is the power source potential Vcc, the capacitor C211 as the pixel capacitor Cs is held at a potential equal to (Vin-Vcc) with respect to the voltage Vin of the input signal.

[0157] After this, in the non-emitting period of the EL light emitting element 214, as shown in FIGS. 20A to 20D, the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are held at the low level by the drive scanner 205, and the scanning signals ws[201], ws[202],... to the scanning lines WSL201, WSL202,... are selectively set to the low level by the write scanner 204.

[0158] As a result, in the pixel circuit 201A, as shown in FIG. 19D, the TFT 212 is turned off and the write operation of the input signal to the capacitor C211 as the pixel capacitor ends.

[0159] After this, as shown in FIGS. 20A to 20D, the scanning signals ws[201], ws[202],... to the scanning lines WSL201, WSL202,... are held at the low level by the write scanner 204, and the drive signals ds[201], ds[202],... to the drive lines DSL201, DSL202,... are selectively set to the high level by the drive scanner 205.

[0160] As a result, in the pixel circuit 201A, as shown in FIG. 19E, the TFT 213 is turned on.

[0161] By turning the TFT 213 on, current flows to the EL light emitting element 214 and the source potential of the TFT 211 falls. The source potential of the TFT 211 as the drive transistor fluctuates, but despite this, since there is a capacitor between the gate and source of the TFT 211, the other transistors etc. are not connected, so the gate-source voltage of the TFT 211 is constantly held at (Vin-Vcc). At this time, the TFT 211 as the drive transistor is driven in the saturated region, so the current Ids flowing through the TFT 211 becomes the value shown in the above equation 1. This is the gate-source voltage Vgs of the drive transistor, that is, (Vin-Vcc).

[0162] That is, the current flowing through the TFT 211 can be said to be determined by the Vin.

[0163] Due to the above, even if the EL light emitting element 214 deteriorates in its I-V characteristic along with the increase in the emitting period, in the pixel circuit 201A of the third example not part of the invention, the potential of the node ND211A falls while the potential between the gate and source of the TFT 211 as the drive transistor is held constant, so the current flowing through the TFT 211 does not change.

[0164] Accordingly, the current flowing through the EL light emitting element 214 also does not change. Even if the I-V characteristic of the EL light emitting element 214 deteriorates, the current corresponding to the input voltage Vin constantly flows and therefore the past problem can be solved.

[0165] In addition, since there is no transistor etc. other than the pixel capacitor Cs between the gate and source of the TFT 211, variation in the threshold value Vth will not cause any change of the gate-source voltage Vgs of the TFT 211 as the drive transistor like in the past system.

[0166] Note that, in FIG. 18, the potential of the cathode electrode of the light emitting element 214 is made the ground potential GND, but this may be made any other potential as well. Rather, making this the negative power source enables the potential of the Vcc to be lowered and enables the potential of the input signal voltage to be lowered. Due to this, design without burdening the external IC becomes possible.

[0167] Further, since no GND lines are required, the number of input pins to the panel can be slashed and pixel layout also becomes easier. In addition, since there are no longer intersecting parts of the Vcc and GND lines in the panel, the yield can also be easily improved.

[0168] Further, as shown in FIG. 21, the transistors of the pixel circuits need not be n-channel transistors. p-channel TFTs 231 to 233 may also be used to form each pixel circuit. In this case, the power source is connected to the anode side of the EL element 234, while the TFT 231 as the drive transistor is connected to the cathode side.

[0169] Further, the TFT 212 and TFT 213 as the switching transistors may also be transistors of different polarities from the TFT 211 as the drive transistor.

[0170] According to the third example not part of the invention, source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL light emitting element along with elapse becomes possible.

[0171] A source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of an EL light emitting element while using current anode-cathode electrodes.

[0172] Further, it is possible to configure transistors of a pixel circuit by only n-channel transistors and possible to use the a-Si process in the fabrication of the TFTs. Due to this, a reduction of the cost of TFT boards becomes possible.

[0173] Further, according to the third embodiment, it is possible to slash the number of GND lines at the TFT side and layout of the surrounding lines and layout of the pixels become easier.

[0174] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board, and possible to improve the yield.

[0175] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board so as to lay the Vcc lines at a low resistance, and possible to obtain an image quality of a high uniformity.

<Fourth example not part of the invention>

[0176] FIG. 22 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a fourth example not part of the invention.

[0177] FIG. 23 is a circuit diagram of the concrete configuration of a pixel circuit according to the fourth example not part of the invention in the organic EL display device of FIG. 22.

[0178] The display device 300, as shown in FIG. 22 and FIG. 23, has a pixel array portion 302 having pixel circuits (PXLC) 301 arranged in an m x n matrix, a horizontal selector (HSEL) 303, a first write scanner (WSCN1) 304, a second write scanner (WSCN2) 305, a drive scanner (DSCN) 36, a constant voltage source (CVS) 307, data lines DTL301 to DTL30n selected by the horizontal selector 303 and supplied with a data signal In accordance with the luminance information, scanning lines WSL301 to WSL30m selectively driven by the write scanner 304, scanning lines WSL311 to WSL31m selectively driven by the write scanner 305, and drive lines DSL301 to DSL30m selectively driven by the drive scanner 306.

[0179] Note that while the pixel circuits 301 are arranged in an m x n matrix in the pixel array portion 302, FIG. 22 shows an example wherein the pixel circuits are arranged in a 2 (= m) x 3 (= n) matrix for the simplification of the drawing.

[0180] Further, in FIG. 23 as well, the concrete configuration of one pixel circuit is shown for simplification of the drawing.

[0181] Each pixel circuit 301 according to the fourth example not part of the invention has, as shown in FIG. 23, an n-channel TFT 311 to TFT 314, a capacitor C311, a light emitting element 315 made of an organic EL element (OLED), and nodes ND311 and ND312.

[0182] Further, in FIG. 23, DTL301 indicates a data line, WSL301 and WSL311 indicate scanning lines, and DSL301 indicates a drive line.

[0183] Among these components, the TFT 311 configures the field effect transistor according to the present invention, the TFT 312 configures the first switch, the TFT 313 configures the second switch, the TFT 314 configures the third switch, and the capacitor C311 configures the pixel capacitance element according to the present invention.

[0184] Further, the scanning line WSL301 corresponds to the first control line according to the present invention, the drive line DSL301 corresponds to the second control line, and the scanning line WSL311 corresponds to the third control line.

[0185] Further, the supply line of the power source voltage Vcc (power source potential) corresponds to the first reference potential, while the ground potential GND corresponds to the reference potential.

[0186] In each pixel circuit 301, a source and a drain of the TFT 313 are connected between a source of the TFT 311 and an anode of the light emitting element 315, a drain of the TFT 311 is connected to the power source potential Vcc, and a cathode of the light emitting element 315 is connected to the ground potential GND. That is, the TFT 311 as the drive transistor, the TFT 313 as the switching transistor, and the light emitting element 315 are connected in series between the power source potential Vcc and the ground potential GND. Further, the connection point of the anode of the light emitting element 315 and the TFT 313 constitutes a node ND311.

[0187] A gate of the TFT 311 is connected to the node ND312. Further, the capacitor C311 as a pixel capacitor Cs is connected between the nodes ND311 and ND312, that is, between the gate of the TFT 311 and the node ND311 (anode of the light emitting element 315). A first electrode of the capacitor C311 is connected to the node ND311, while a second electrode is connected to the node ND312.

[0188] A gate of the TFT 313 is connected to the drive line DSL301. Further, a source and a drain of the TFT 312 as the first switch are connected to the data line DTL301 and the node ND312. Further, a gate of the TFT 312 is connected to the scanning line WSL301.

[0189] Further, a source and a drain of the TFT 314 are connected between the node ND311 and the constant voltage source 307. A gate of the TFT 314 is connected to the scanning line WSL311.

[0190] In this way, the pixel circuit 301 according to the present example not part of the invention is configured with the source of the TFT 311 as the drive transistor and the anode of the light emitting element 315 connected by the TFT 313 as the switching transistor, a capacitor C311 connected between the gate of the TFT 311 and the node ND311 (anode of the light emitting element 315), and a node ND311 is connected through the TFT 314 to the constant voltage source 307 (fixed voltage line).

[0191] Next, the operation of the above configuration will be explained focusing on the operation of a pixel circuit with reference to FIGS. 24A to 24E and FIGS. 25A to 25H.

[0192] Note that FIG. 25A shows a scanning signal ws[301] applied to the first row scanning line WSL301 of the pixel array, FIG. 25B shows a scanning signal ws[302] applied to the second row scanning line WSL302 of the pixel array, FIG. 25C shows a scanning signal ws[311] applied to the first row scanning line WSL311 of the pixel array, FIG. 25D shows a scanning signal ws[312] applied to the second row scanning line WSL312 of the pixel array, FIG. 25E shows a drive signal ds[301] applied to the first row drivd line DSL301 of the pixel array, FIG. 25F shows a drive signal ds[302] applied to the second row drive line DSL302 of the pixel array, FIG. 25G shows a gate potential Vg of the TFT 311, and FIG. 25H shows an anode side potential of the TFT 311, that is, the potential VND311 of the node ND311.

[0193] First, at the ordinary emitting state of the EL light emitting element 315, as shown in FIGS. 25A to 25F, the scanning signals ws[301], ws[302],.. to the scanning lines WSL301, WSL302,... are selectively set to the low level by the write scanner 304, the scanning signals ws[311], ws[312],.. to the scanning lines WSL311, WSL312,... are selectively set to the low level by the write scanner 305, and the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are selectively set to the high level by the drive scanner 306.

[0194] As a result, in the pixel circuit 301, as shown in FIG. 24A, the TFTs 312 and 314 are held in the off state and the TFT 313 Is held in the on state.

[0195] At this time, since the TFT 311 as the drive transistor is driven in the saturated region, the current Ids flows to the TFT 311 and the EL element 315 with respect to the gate-source voltage Vgs.

[0196] Next, in the non-emitting period of the EL light emitting element 315, as shown in FIGS. 25A to 25F, the scanning signals ws[301], ws[302],.. to the scanning lines WSL301, WSL302,... are held at the low level by the write scanner 304, the scanning signals ws[311], ws[312],.. to the scanning lines WSL311, WSL312,... are held at the low level by the write scanner 305, and the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are selectively set to the low level by the drive scanner 306.

[0197] As a result, in the pixel circuit 301, as shown in FIG. 248, the TFT 312 and the TFT 314 are held in the off state and the TFT 313 is turned off.

[0198] At this time, the potential held at the EL light emitting element 315 falls since the source of supply disappears. The potential falls to the threshold voltage Vth of the EL light emitting element 315. However, since off current also flows to the EL light emitting element 315, if the non-emitting period continues, the potential will fall to GND.

[0199] On the other hand, the TFT 311 as the drive transistor is held in the on state since the gate potential is high. As shown in FIG. 25G, the source potential of the TFT 311 is boosted to the power source voltage Vcc. This boosting is performed in a short period. After boosting to the Vcc, no current is supplied to the TFT 311.

[0200] That is, in the pixel circuit 301 of the fourth example not part of the invention, it is possible to operate without the supply of current in the pixel circuit during the non-emitting period and therefore possible to suppress the power consumption of the panel.

[0201] Next, in the non-emitting period of the EL light emitting element 315, as shown in FIGS. 25A to 25F, the drive signals ds[301], ds[302],.. to the drive lines DSL301, DSL302,... are held at the low level by the drive scanner 306, the scanning signals ws[301], ws[302],... to the scanning lines WSL301, WSL302,... are selectively set to the high level by the write scanner 304, and the scanning signals ws[311], ws[312],... to the scanning lines WSL311, WSL312,... are selectively set to the high level by the write scanner 305.

[0202] As a result, in the pixel circuit 301, as shown in FIG. 24C, the TFT 312 and TFT 314 are turned on while the TFT 313 is held in the off state. Due to this, the input signal (Vin) propagated to the data line DTL301 by the horizontal selector 303 is written into the capacitor C311 as the pixel capacitor Cs.

[0203] When writing this signal line voltage, it is important that the TFT 314 be turned on. If there were no TFT 314, if the TFT 312 were turned on and the video signal were written In the pixel capacor Cs, coupling would enter the source potential Vs of the TFT 311. As opposed to this, if turning on the TFT 314 connecting the node ND311 to the constant voltage source 307, it will be connected to the low impedance line, so the voltage of the line would be written into the source potential side (node ND311) of the TFT 311.

[0204] At this time, if making the potential of the line Vo, the source potential (potential of the node ND311) of the TFT 311 as the drive transistor becomes Vo, so a potential equal to (Vin-Vo) is held with respect to the voltage Vin of the input signal at the pixel capacitor Cs.

[0205] After this, in the non-emitting period of the EL light emitting element 315, as shown in FIGS. 25A to 25F, the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are held at the low level by the drive scanner 306, the scanning signals ws[311], ws[312],... to the scanning lines WSL311, WSL312,... are held at the high level by the write scanner 306, and the scanning signals ws[301], ws[302],... to the scanning lines WSL301, WSL302,... are selectively set to the low level by the write scanner 304.

[0206] As a result, in the pixel circuit 301, as shown in FIG. 24D, the TFT 312 is turned off and the write operation of the input signal to the capacitor C311 as the pixel capacitor ends.

[0207] At this time, the source potential of the TFT 311 (potential of node ND311) has to hold the low impedance, so the TFT 314 is left on.

[0208] After this, as shown in FIGS. 25A to 25F, while the drive signals ws[301], ws[302],... to the scanning lines WSL301, WSL302,... are held at the low level by the write scanner 304, the scanning signals ws[311], ws[312],... to the scanning lines WSL311, WSL312,... are set to the low level by the write scanner 305, then the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are selectively set to the high level by the drive scanner 306.

[0209] As a result, in the pixel circuit 301, as shown in FIG. 24E, the TFT 314 is turned off and the TFT 313 becomes on.

[0210] By turning the TFT 313 on, current flows to the EL light emitting element 315 and the source potential of the TFT 311 falls. The source potential of the TFT 311 as the drive transistor fluctuates, but despite this, since there is a capacitor between the gate and source of the TFT 311, the gate-source voltage of the TFT 311 is constantly held at (Vin-Vo).

[0211] At this time, the TFT 311 as the drive transistor is driven in the saturated region, so the current Ids flowing through the TFT 311 becomes the value shown in the above equation 1. This is the gate-source voltage Vgs of the drive transistor, that is, (Vin-Vo).

[0212] That is, the current flowing through the TFT 311 can be said to be determined by the Vin.

[0213] In this way, by turning the TFT 314 on during a signal write period to make the source of the TFT 311 low in impedance, it is possible to make the source side of the TFT 311 of the pixel capacitor a fixed potential at all times, there is no need to consider deterioration of image quality due to coupling at the time of a signal line write operation, and it is possible to write the signal line voltage in a short time. Further, it is possible to increase the pixel capacity to take measures against leak characteristics.

[0214] Due to the above, even if the EL light emitting element 315 deteriorates in its I-V characteristic along with the increase in the emitting period, in the pixel circuit 301 of the fourth example not part of the invention, the potential of the node ND311 falls while the potential between the gate and source of the TFT 311 as the drive transistor is held constant, so the current flowing through the TFT 311 does not change.

[0215] Accordingly, the current flowing through the EL light emitting element 315 also does not change. Even If the I-V characteristic of the EL light emitting element 315 deteriorates, the current corresponding to the input voltage Vin constantly flows and therefore the past problem can be solved.

[0216] In addition, since there is no transistor etc. other than the pixel capacitor Cs between the gate and source of the TFT 311, variation In the threshold value Vth will not cause any change of the gate-source voltage Vgs of the TFT 311 as the drive transistor like in the past system.

[0217] Note that the potential of the line connected to the TFT 314 (constant voltage source) is not limited, but as shown in FIG. 26, if making the potential the same as Vcc, slashing the number of signal lines becomes possible. Due to this, the layout of the panel lines and pixel parts becomes easy. Further, the number of pads for panel input becomes possible.

[0218] On the other hand, the gate-source voltage Vgs of the TFT 311 as the drive transistor, as explained above, is determined by Vin-Vo. Accordingly, for example as shown in FIG. 27, if setting Vo to a low potential such as the ground potential GND, the input signal voltage Vin can be prepared by the low potential near the GND level and boosting of the signal of the nearby ICs is not required. Further, it is possible to reduce the on voltage of the TFT 313 as the switching transistor and possible to eliminate the burden on the external ICs in design.

[0219] Further, in FIG. 23, the potential of the cathode electrode of the light emitting element 315 is made the ground potential GND, but this may be made any other potential as well. Rather, making this the negative power source enables the potential of the Vcc to be lowered and enables the potential of the input signal voltage to be lowered. Due to this, design without burdening the external IC becomes possible.

[0220] Further, as shown in FIG. 28, the transistors of the pixel circuits need not be n-channel transistors p-channel TFTs 321 to 324 may also be used to form each pixel circuit. In this case, the power source potential Vcc is connected to the anode side of the EL light emitting element 324, while the TFT 321 as the drive transistor is connected to the cathode side.

[0221] Further, the TFT 312, TFT 313, and TFT 314 as the switching transistors may also be transistors of different polarities from the TFT 311 as the drive transistor.

[0222] According to the fourth example not part of the invention, source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL element along with elapse becomes possible.

[0223] A source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of an EL light emitting element while using current anode-cathode electrodes.

[0224] Further, it is possible to configure transistors of a pixel circuit by only n-channel transistors and possible to use the a-Si process in the fabrication of the TFTs. Due to this, a reduction of the cost of TFT boards becomes possible.

[0225] Further, according to the fourth example not part of the invention, it is possible to write the signal line voltage in a short time even with for example a black signal and possible to obtain an image quality with a high uniformity. Simultaneously, it is possible to increase the signal line capacity and suppress leakage characteristics.

[0226] Further, it is possible to slash the number of GND lines at the TFT side and layout of the surrounding lines and layout of the pixels become easier.

[0227] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board, and possible to improve the yield.

[0228] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board so as to lay the Vcc lines at a low resistance, and possible to obtain an image quality of a high uniformity.

[0229] Still further, it is possible to make the input signal voltage near the GND and possible to lighten the load on the external drive system.

<Fifth example not part of the invention>

[0230] FIG. 29 is a block diagram of the configuration of an organic EL display device employing a pixel circuit according to a fifth example not part of the invention.

[0231] FIG. 30 is a circuit diagram of the concrete configuration of a pixel circuit according to the fifth example not part of the invention in the organic EL display device of FIG. 29.

[0232] The display device 300A according to the fifth example not part of the invention differs from the display device 300 according to the fourth example not part of the invention in the position of connection of the capacitor C311 as the pixel capacitor Cs in the pixel circuit.

[0233] Specifically, in the pixel circuit 301 according to the fourth example not part of the invention, the capacitor C311 is connected between the gate of the TFT 311 as the drive transistor and the anode side of the EL light emitting element 315.

[0234] As opposed to this, in the pixel circuit 301A according to the fifth example not part of the invention, the capacitor C311 is connected between the gate and source of the TFT 311 as the drive transistor. Specifically, a first electrode of the capacitor C311 is connected to the connection point (node ND311A) of the source of the TFT 311 and the TFT 313 as the switching transistor and a second electrode is connected to the node ND312.

[0235] The rest of the configuration is similar to that of the fourth example not part of the invention explained above.

[0236] Next, the operation of the above configuration will be explained focusing on the operation of a pixel circuit with reference to FIGS. 31A to 31E and FIGS. 32A to 32H.

[0237] First, at the ordinary emitting state of the EL light emitting element 315, as shown in FIGS. 32A to 32F, the scanning signals ws[301], ws[302],.. to the scanning lines WSL301, WSL302,... are selectively set to the low level by the write scanner 304, the scanning signals ws[311], ws[312],.. to the scanning lines WSL311, WSL312,... are selectively set to the low level by the write scanner 305, and the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are selectively set to the high level by the drive scanner 306.

[0238] As a result, in the pixel circuit 301, as shown in FIG. 31A, the TFTs 312 and 314 are held in the off state and the TFT 313 is held in the on state.

[0239] At this time, the TFT 311 as the drive transistor is driven in the saturated region, so the current Ids flows to the TFT 311 and the EL light emitting element 315 with respect to the gate-source voltage Vgs.

[0240] Next, in the non-emitting period of the EL light emitting element 315, as shown in FIGS. 32A to 32F, the scanning signals ws[301], ws[302],.. to the scanning lines WSL301, WSL302,... are selectively held at the low level by the write scanner 304, the scanning signals ws[311], ws[312],.. to the scanning lines WSL311, WSL312,... are selectively held at the low level by the write scanner 305, and the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are selectively set to the low level by the drive scanner 306.

[0241] As a result, in the pixel circuit 301, as shown in FIG. 318, the TFT 312 and TFT 314 are held in the off state and the TFT 313 is turned off.

[0242] At this time, the potential held at the EL light emitting element 315 falls since the source of supply disappears and the EL light emitting element 315 does not emit light. The potential falls to the threshold voltage Vth of the EL light emitting element 315. However, since off current also flows to the EL light emitting element 315, if the non-emitting period continues, the potential will fall to GND.

[0243] On the other hand, along with the voltage drop of the anode side of the EL light emitting element 315, the gate potential of the TFT 311 as the drive transistor falls through the capacitor C311. In parallel with this, current flows to the TFT 311 and the source potential rises.

[0244] Due to this, the TFT 311 becomes cut off and no current flows to the TFT 311.

[0245] That is, in the pixel circuit 301A of the fifth example not part of the invention, it is possible to operate without the supply of current in the pixel circuit during the non-emitting period and therefore possible to suppress the power consumption of the panel.

[0246] Next, in the non-emitting period of the EL light emitting element 315, as shown in FIGS. 32A to 32F, while the drive signals ds[301], ds[302],.. to the drive lines DSL301, DSL302,... are held at the low level by the drive scanner 306, the scanning signals ws[301], ws[302],... to the scanning lines WSL301, WSL302,... are selectively set to the high level by the write scanner 304, and the scanning signals ws[311], ws[312],.., to the scanning lines WSL311, WSL312,... are selectively set to the high level by the write scanner 305.

[0247] As a result, in the pixel circuit 301A, as shown in FIG. 31C, the TFT 313 is held in the off state and the TFT 312 and TFT 314 are turned on. Due to this, the input signal (Vin) propagated to the data line DTL301 by the horizontal selector 303 is written into the capacitor C311 as the pixel capacitor Cs.

[0248] When writing this signal line voltage, it is important that the TFT 314 be turned on. If there were no TFT 314, if the TFT 312 were turned on and the video signal were written in the pixel capacor Cs, coupling would enter the source potential Vs of the TFT 311. As opposed to this, if turning on the TFT 314 connecting the node ND311 to the constant voltage source 307, it will be connected to the low impedance line, so the voltage of the line would be written into the source potential of the TFT 311.

[0249] At this time, if making the potential of the line Vo, the source potential of the TFT 311 as the drive transistor becomes Vo, so a potential equal to (Vin-Vo) is held with respect to the voltage Vin of the input signal at the pixel capacitor Cs.

[0250] After this, in the non-emitting period of the EL light emitting element 315, as shown in FIGS. 32A to 32F, the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are held at the low level by the drive scanner 306, the scanning signals ws[311], ws[312],... to the scanning lines WSL311, WSL312,... are held at the high level by the write scanner 305, and the scanning signals ws[301], ws[302],... to the scanning lines WSL301, WSL302,... are selectively set to the low level by the write scanner 304.

[0251] As a result, in the pixel circuit 301A, as shown in FIG. 31D, the TFT 312 is turned off and the write operation of the input signal to the capacitor C311 as the pixel capacitor ends.

[0252] At this time, the source potential of the TFT 311 has to hold the low impedance, so the TFT 314 is left on.

[0253] After this, as shown in FIGS. 32A to 32F, while the scanning signals ws[301], ws[302],... to the scanning lines WSL301, WSL302,... are held at the low level by the write scanner 304, scanning signals ws[311], ws[312],... to the scanning lines WSL311, WSL312,... are set to the low level by the write scanner 305, then the drive signals ds[301], ds[302],... to the drive lines DSL301, DSL302,... are selectively set to the high level by the drive scanner 306.

[0254] As a result, in the pixel circuit 301, as shown in FIG. 31E, the TFT 314 is turned off and the TFT 313 becomes on.

[0255] By turning the TFT 313 on, current flows to the EL light emitting element 315 and the source potential of the TFT 311 falls. The source potential of the TFT 311 as the drive transistor fluctuates, but despite this, since there is a capacity between the gate and source of the TFT 311, the gate-source voltage of the TFT 311 is constantly held at (Vin-Vcc).

[0256] Here, the TFT 313 drives in the non-saturated region, so this is viewed as a simple resistance value. Accordingly, the gate-source voltage of the TFT 311 is (Vin-Vo) minus the value of the voltage drop due to the TFT 313. That is, the current flowing through the TFT 311 can be said to be determined by the Vin.

[0257] In this way, by turning the TFT 314 on during a signal write period to make the source of the TFT 311 low in impedance, it is possible to make the source side of the TFT 311 of the pixel capacitor a fixed potential at all times, there is no need to consider deterioration of image quality due to coupling at the time of a signal line write operation, and it is possible to write the signal line voltage in a short time. Further, it is possible to increase the pixel capacity to take measures against leak characteristics.

[0258] At this time, the TFT 311 as the drive transistor constituted by is driven in the saturated region, so the current Ids flowing through the TFT 311 becomes the value shown in the above equation 1. This is the gate-source voltage Vgs of the drive transistor, that is, (Vin-Vcc).

[0259] That is, the current flowing through the TFT 311 can be said to be determined by the Vin.

[0260] Due to the above, even if the EL light emitting element 315 deteriorates in its I-V characteristic along with the increase in the emitting period, in the pixel circuit 201A of the fifth example not part of the invention, the potential of the node ND311 falls while the potential between the gate and source of the TFT 311 as the drive transistor is held constant, so the current flowing through the TFT 311 does not change.

[0261] Accordingly, the current flowing through the EL light emitting element 315 also does not change. Even if the I-V characteristic of the EL light emitting element 315 deteriorates, the current corresponding to the input voltage Vin constantly flows and therefore the past problem can be solved.

[0262] Note that the potential of the line connected to the TFT 314 (constant voltage source) is not limited, but as shown in FIG. 33, if making the potential the same as Vcc, slashing the number of signal lines becomes possible. Due to this, the layout of the panel lines and pixel parts becomes easy. Further, the number of pads for panel input becomes possible.

[0263] On the other hand, the gate-source voltage Vgs of the TFT 311 as the drive transistor, as explained above, is determined by Vin-Vo. Accordingly, for example as shown in FIG. 34, if setting Vo to a low potential such as the ground potential GND, the input signal voltage Vin can be prepared by the low potential near the GND level and boosting of the signal of the nearby ICs is not required. Further, it is possible to reduce the on voltage of the TFT 313 as the switching transistor and possible to eliminate the burden on the external ICs in design.

[0264] Further, in FIG. 30, the potential of the cathode electrode of the light emitting element 315 is made the ground potential GND, but this may be made any other potential as well. Rather, making this the negative power source enables the potential of the Vcc to be lowered and enables the potential of the input signal voltage to be lowered. Due to this, design without burdening the external IC becomes possible.

[0265] Further, as shown in FIG. 35, the transistors of the pixel circuits need not be n-channel transistors. p-channel TFTs 321 to 324 may also be used to form each pixel circuit. In this case, the power source is connected to the anode side of the EL light emitting element 325, while the TFT 321 as the drive transistor is connected to the cathode side.

[0266] Further, the TFT 312, TFT 313, and TFT 314 as the switching transistors may also be transistors of different polarities from the TFT 311 as the drive transistor.

[0267] According to the fifth example not part of the invention, source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL element along with elapse becomes possible.

[0268] A source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of an EL light emitting element while using current anode-cathode electrodes.

[0269] Further, it is possible to configure transistors of a pixel circuit by only n-channel transistors and possible to use the a-Si process in the fabrication of the TFTs. Due to this, a reduction of the cost of TFT boards becomes possible.

[0270] Further, according to the fifth example not part of the invention, it is possible to write the signal line voltage in a short time even with for example a black signal and possible to obtain an image quality with a high uniformity. Simultaneously, it is possible to increase the signal line capacity and suppress leakage characteristics.

[0271] Further, it is possible to slash the number of GND lines at the TFT side and layout of the surrounding lines and layout of the pixels become easier.

[0272] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board, and possible to improve the yield.

[0273] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board so as to lay the Vcc lines at a low resistance, and possible to obtain an image quality of a high uniformity.

[0274] Still further, it is possible to make the input signal voltage near the GND and possible to lighten the load on the external drive system.

<First Embodiment>

[0275] FIG. 36 is a block diagram of the configuration of an organic EL display device employing pixel circuits according to a first embodiment.

[0276] FIG. 37 is a circuit diagram of the concrete configuration of a pixel circuit according to the first embodiment in the organic EL display device of FIG. 36.

[0277] This display device 400 has, as shown in FIG. 36 and FIG. 37, a pixel array portion 402 having pixel circuits (PXLC) 401 arranged in an m x n matrix, a horizontal selector (HSEL) 403, a write scanner (WSCN) 404, a first drive scanner (DSCN1) 405, a second drive scanner (DSCN2) 406, a third drive scanner (DSCN3) 407, data lines DTL401 to DTL40n selected by the horizontal selector 403 and supplied with a data signal in accordance with the luminance information, scanning lines WSL401 to WSL40m selectively driven by the write scanner 404, drive lines DSL401 to DSL40m selectively driven by the first drive scanner 405, drive lines DSL411 to DSL41m selectively driven by the second drive scanner 406, and drive lines DSL421 to DSL42m selectively driven by the third drive scanner 407.

[0278] Note that while the pixel circuits 401 are arranged in an m x n matrix in the pixel array portion 402, FIG. 36 shows an example wherein the pixel circuits are arranged in a 2 (= m) x 3 (= n) matrix for the simplification of the drawing.

[0279] Further, in FIG. 37, the concrete configuration of one pixel circuit is shown for simplification of the drawing.

[0280] The pixel circuit 401 according to the first embodiment has, as shown in FIG. 37, n-channel TFT 411 to TFT 415, a capacitor C411, a light emitting element 416 made of an organic EL element (OLED), and nodes ND411 and ND412.

[0281] Further, in FIG. 37, DTL401 indicates a data line, WSL401 indicates a scanning line, and DSL401, DSL411, and DSL421 indicate drive lines.

[0282] Among these components, TFT 411 configures the field effect transistor according to the present invention, TFT 412 configures the first switch, TFT 413 configures the second switch, TFT 414 configures the third switch, TFT 415 configures the fourth switch, and the capacitor C411 configures the pixel capacitance element according to the present invention.

[0283] Further, the scanning line WSL401 corresponds to the first control line according to the present invention, the drive line DSL401 corresponds to the second control line, the drive line DSL411 corresponds to the third control line, and the drive line DSL421 corresponds to the fourth control line.

[0284] Further, the supply line (power source potential) of the power source voltage Vcc corresponds to the first reference potential, while the ground potential GND corresponds to the second reference potential.

[0285] In each pixel circuit 401, a source and a drain of the TFT 414 are connected between a source of the TFT 411 and the node ND411, a source and a drain of the TFT 413 are connected between the node ND411 and an anode of the light emitting element 416, a drain of the TFT 411 is connected to the power source potential Vcc, and a cathode of the light emitting element 416 is connected to the ground potential GND. That is, the TFT 411 as the drive transistor, the TFT 414 and TFT 413 as the switching transistors, and the light emitting element 416 are connected in series between the power source potential Vcc and the ground potential GND.

[0286] A gate of the TFT 411 is connected to the node ND412. Further, the capacitor C411 as a pixel capacitor Cs is connected between the gate and source of the TFT 411. A first electrode of the capacitor C411 is connected to the node ND411, while a second electrode is connected to the node ND412.

[0287] A gate of the TFT 413 is connected to the drive line DSL401. Further, a gate of the TFT 414 is connected to the drive line DSL411. Further, a source and a drain of the TFT 412 as the first switch are connected between the data line DTL401 and the node ND411 (connection point with first electrode of capacitor C411). Further, a gate of the TFT 412 is connected to the scanning line WSL401.

[0288] Further, a source and a drain of the TFT 415 are connected between the node ND412 and the power source potential Vcc. A gate of the TFT 415 is connected to the drive line DSL421.

[0289] In this way, the pixel circuit 401 according to the present embodiment is configured with the source of the TFT 411 as the drive transistor and the anode of the light emitting element 416 connected by the TFT 414 and TFT 413 as the switching transistors, a capacitor C411 connected between the gate of the TFT 411 and the source side node ND411, and the gate of the TFT 411 (node ND412) connected through the TFT 415 to the power source potential Vcc (fixed voltage line).

[0290] Next, the operation of the above configuration will be explained focusing on the operation of a pixel circuit with reference to FIGS. 38A to 38F, FIG. 39, and FIGS. 40A to 40H.

[0291] FIG. 40A shows a scanning signal ws[401] applied to the first row scanning line WSL401 of the pixel array, FIG. 40B shows a scanning signal ws[402] applied to the second row scanning line WSL402 of the pixel array, FIG. 40C shows drive signals ds[401] and ds[411] applied to the first row drive lines DSL401 and DSL411 of the pixel array, FIG. 40D shows drive signals ds[402] and d[412] applied to the second row drive lines DSL402 and DSL412 of the pixel array, FIG. 40E shows a drive signal ds[421] applied to the first row drive line DSL421 of the pixel array, FIG. 40F shows a drive signal ds[422] applied to the second row drive line DSL421 of the pixel array, FIG. 40G shows a gate potential Vg of the TFT 411, that is, the potential VND412 of the node ND412, and FIG. 40H shows an anode side potential of the TFT 411, that is, the potential VND411 of the node ND411.

[0292] Note that there is no problem no matter which of the TFT 413 and TFT 414 turns on or off, so as shown in FIG. 40C and FIG. 40D, the drive signals DS[401] and ds[411] and the drive signals ds[402] and ds[412] applied to the drive lines DSL401 and DSL411 and the drive lines DSL402 and DSL412 are made the same timing.

[0293] First, at the ordinary emitting state of the EL light emitting element 416, as shown in FIGS. 40A to 40F, the scanning signals ws[401], ws[402],.. to the scanning lines WSL401, WSL402,... are selectively set to the low level by the write scanner 404, the drive signals ds[401], ds[402],... to the drive lines DSL401, DSL402,... are selectively set to the high level by the drive scanner 405, the drive signals ds[411], ds[412],... to the drive lines DSL411, DSL412,... are selectively set to the high level by the drive scanner 406, and the drive signals ds[421], ds[422],... to the drive lines DSL421, DSL422,... are selectively set to the low level by the drive scanner 407.

[0294] As a result, in the pixel circuit 401, as shown in FIG. 38A, the TFT 414 and TFT 413 are held in the on state and the TFT 412 and TFT 415 is held in the off state.

[0295] First, at the ordinary non-emitting state of the EL light emitting element 416, as shown in FIGS. 40A to 40F, the scanning signals ws[401], ws[402],.. to the scanning lines WSL401, WSL402,... are held at the low level by the write scanner 404, the drive signals ds[421], ds[422],... to the drive lines DSL421, DSL422,... are held at the low level by the drive scanner 407, the drive signals ds[401], ds[402],... to the drive lines DSL401, DSL402,... are selectively set to the low level by the drive scanner 405, and the drive signals ds[411], ds[412],... to the drive lines DSL411, DSL412,... are selectively set to the low level by the drive scanner 406.

[0296] As a result, in the pixel circuit 401, as shown in FIG. 38B, the TFT 412 and TFT 415 are held in the off state and the TFTs 413 and 414 are turned off.

[0297] At this time, the potential held at the EL light emitting element 416 falls since the source of supply disappears. The EL light emitting element 416 stops emitting light. The potential falls to the threshold voltage Vth of the EL light emitting element 416. However, since off current also flows to the EL light emitting element 416, if the non-emitting period continues, the potential will fall to GND.

[0298] On the other hand, the TFT 411 as the drive transistor is held in the on state since the gate potential is high. The source potential of the TFT 411 is boosted to the power source voltage Vcc. This boosting is performed In a short period. After boosting to the Vcc, no current is supplied to the TFT 411.

[0299] That is, in the pixel circuit 401 of the first embodiment, it is possible to operate without the supply of current in the pixel circuit during the non-emitting period and therefore possible to suppress the power consumption of the panel.

[0300] In this state, next, as shown in FIGS. 40A to 40F, the drive signals ds[401], ds[402],... to the drive lines DSL401, DSL402,... are held at the low level by the drive scanner 405, the drive signals ds[411], ds[412],... to the drive lines DSL411, DSL412,... are held at the low level by the drive scanner 406, and in that state the drive signals ds[421], ds[422],... to the drive lines DSL421, DSL422,... are set to the high level by the drive scanner 407, then the scanning signals ws[401], ws[402],.. to the scanning lines WSL401, WSL402,... are selectively set to the high level by the write scanner 404.

[0301] As a result, in the pixel circuit 401, as shown in FIG. 38C, the TFT 413 and TFT 414 are held in the off state and the TFT 412 and TFT 415 are turned on. Due to this, the input signal propagated to the data line DTL401 by the horizontal selector 403 is written into the capacitor C411 as the pixel capacitor Cs.

[0302] At this time, the capacitor C411 as the pixel capacitor Cs holds a potential equal to the difference (Vcc-Vin) between the power source voltage Vcc and the input voltage Vin.

[0303] After this, in the non-emitting period of the EL light emitting element 416, as shown in FIGS. 40A to 40F, the drive signals ds[401], ds[402],... to the drive lines DSL401, DSL402,... are held at the low level by the drive scanner 405, the drive signals ds[411], ds[412],... to the drive lines DSL411, DSL412,... are held at the low level by the drive scanner 406, and in that state the drive signals ds[421], ds[422],... to the drive lines DSL421, DSL422,... are selectively set to the low level by the drive scanner 407, then the scanning signals ws[401], ws[402],.. to the scanning lines WSL401, WSL402,... are selectively set to the low level by the write scanner 404.

[0304] As a result, in the pixel circuit 401, as shown in FIG. 38D, the TFT 415 and TFT 412 turn off and the writing of the input signal to the capacitor C411 as the pixel capacitor ends.

[0305] At this time, the capacitor C411 holds a potential equal to the difference (Vcc-Vin) between the power source voltage Vcc and the input voltage Vin regardless of the potential of the capacitor end.

[0306] After this, as shown in FIGS. 40A to 40F, the drive signals ds[401], ds[402],... to the drive lines DSL401, DSL402,... are held at the low level by the drive scanner 405, the drive signals ds[421], ds[422],... to the drive lines DSL421, DSL422,... are held at the low level by the drive scanner 407, the scanning signals ws[401], ws[402],.. to the scanning lines WSL401, WSL402,... are held at the low level by the write scanner 404, and in that state the drive signals ds[411], ds[412],... to the drive lines DSL411, DSL412,... are selectively set to the high level by the drive scanner 406.

[0307] As a result, in the pixel circuit 401, as shown in FIG. 38E, the TFT414 turns on. By the TFT 414 turning on, the gate-source potential of the drive transistor TFT411 becomes the potential difference (Vcc-Vin) charged into the capacitor C411 as the pixel capacitor. Further, as shown in FIG. 40H, regardless of the value of the source potential of the TFT 411, the potential difference is held and the source potential of the drive transistor 411 rises to Vcc.

[0308] Further, as shown in FIGS. 40A to 40F, the drive signals ds[421], ds[422],... to the drive lines DSL421, DSL422,... are held at the low level by the drive scanner 407, the scanning signals ws[401], ws[402],.. to the scanning lines WSL401, WSL402,... are held at the low level by the write scanner 404, the drive signals ds[411], ds[412],... to the drive lines DSL411, DSL412,... are held at the high level by the drive scanner 406, and in that state the drive signals ds[401], ds[402],... to the drive lines DSL401, DSL402,... are selectively held at the high level by the drive scanner 405.

[0309] As a result, at the pixel circuit 401, as shown in FIG. 38F, TFT 413 turns on.

[0310] By turning the TFT 413 on, the source potential of the TFT 411 falls. In this way, despite the fact that the source potential of the TFT 411 as the drive transistor fluctuates, since there is a capacitance between the gate of the TFT 411 and the anode of the EL light emitting element 416, the gate-source potential of the TFT 411 is constantly held at (Vcc-Vin).

[0311] At this time, the TFT 411 as the drive transistor is driven in the saturated region, so the current value Ids flowing to the TFT 411 becomes the value shown in the above-mentioned equation 1. This is determined by the gate-source voltage Vgs of the drive transistor TFT 411.

[0312] This current also flows to the EL light emitting element 416. The EL light emitting element 416 emits light by a luminance proportional to the current value.

[0313] The equivalent circuit of the EL light emitting element can be described by transistors as shown in FIG. 39, so in FIG. 39, the potential of the node ND411 stops after rising to the gate potential at which the current Ids flows to the light emitting element 416. Along with the change of this potential, the potential of the node ND412 also changes. If the final potential of the node ND411 is Vx, the potential of the node ND412 is described as (Vx+Vcc-Vin) and the gate-source potential of the TFT 411 as the drive transistor is held at (Vx+Vcc).

[0314] Due to the above, even if the EL light emitting element 416 deteriorates in I-V characteristic along with the increase in the emitting time, in the pixel circuit 401 of the first embodiment, the potential of the node ND411 drops while the gate-source potential of the TFT 411 as the drive transistor is held constant, so the current flowing through the TFT 411 does not change.

[0315] Accordingly, the current flowing through the EL light emitting element 416 also does not change. Even if the I-V characteristic of the EL light emitting element 416 deteriorates, a current corresponding to the gate-source potential (Vcc-Vin) constantly flows. Therefore, the past problem relating to deterioration along with elapse of the EL can be solved.

[0316] Further, in the circuit of the present invention, since the fixed potential is only the power source Vcc in the pixel, no GND line which has to be laid thick is necessary. Due to this, it is possible to reduce the pixel area. Further, in the non-emitting period, the TFTs 413 and 414 are off and no current is run through the circuit. That is, by not running current through the circuit during the non-emitting period, it Is possible to reduce the power consumption.

[0317] As explained above, according to the first embodiment, the source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL element along with elapse becomes possible.

[0318] A source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of a light emitting element while using current anode-cathode electrodes.

[0319] Further, it is possible to configure transistors of a pixel circuit by only n-channel transistors and possible to use the a-Si process in the fabrication of the TFTs. Due to this, a reduction of the cost of TFT boards becomes possible.

[0320] Further, in the present invention, it is possible to use the pixel power source for the fixed potential, so it is possible to reduce the pixel area and possible to expect higher definition of the panel.

[0321] Still further, by not running a current through the circuit while the EL light emitting element is not emitting light, the power consumption can be reduced.

[0322] As explained above, according to the present invention, source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL element along with elapse becomes possible.

[0323] A source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of a light emitting element while using current anode-cathode electrodes.

[0324] Further, it is possible to configure transistors of a pixel circuit by only n-channel transistors and possible to use the a-Si process in the fabrication of the TFTs. Due to this, a reduction of the cost of TFT boards becomes possible.

[0325] Further, it is possible to write the signal line voltage in a short time even with for example a black signal and possible to obtain an image quality with a high uniformity. Simultaneously, it is possible to increase the signal line capacity and suppress leakage characteristics.

[0326] Further, it is possible to slash the number of GND lines at the TFT side and layout of the surrounding lines and layout of the pixels become easier.

[0327] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board, and possible to improve the yield.

[0328] Further, it is possible to slash the number of GND lines at the TFT side, possible to eliminate the overlap of the GND lines and Vcc lines at the TFT board so as to lay the Vcc lines at a low resistance, and possible to obtain an image quality of a high uniformity.

[0329] Further, in the present Invention, it is possible to use the pixel power source for the fixed potential, so it is possible to reduce the pixel area and possible to look forward to higher definition of the panel.

[0330] Still further, by not running a current through the circuit while the EL light emitting element is not emitting light, the power consumption can be reduced.

[0331] Still further, it is possible to make the input signal voltage near the GND and possible to lighten the load on the external drive system.

INDUSTRIAL APPLICABILITY

[0332] According to the pixel circuit, display device, and method of driving a pixel circuit of the present invention, source-follower output with no deterioration in luminance even with a change in the I-V characteristic of an EL element along with elapse becomes possible and a source-follower circuit of n-channel transistors becomes possible, so it is possible to use an n-channel transistor as a drive element of an EL element while using current anode-cathode electrodes, therefore the invention can be applied even to a large-sized and high definition active matrix type display.

Claims

1. A display device (400) comprising a plurality of pixel circuits (402) arranged in a matrix, wherein each of the pixel circuits (401) includes:

an electro-optic element (416),
a capacitor (C411) having a first electrode and a second electrode and configured to store a voltage dependent on a set image signal voltage,
a drive transistor (411) configured to control a current flow of a current path from a power supply line to the electro-optic element (416), in response to the voltage stored in the capacitor (C411),
a first transistor (412) connected to a first node (ND411) and configured to provide the set image signal voltage from a data line (DTL401), the current flow of the current path being dependent on the set image signal voltage,
a second transistor (413) and a third transistor (414), each configured to switch the current flow of the current path, and
a fourth transistor (415) connected to a second node (ND412) and configured to apply a prede-

termined potential to the capacitor (C411), while the second transistor (413) and the third transistor (414) are set in a non-conductive state,
wherein the second transistor (413), the third transistor (414) and the drive transistor (411) are arranged so as to form the current path from the power supply line to the electro-optic element (416),
wherein the first electrode of the capacitor (C411) is connected to a source electrode of the drive transistor (411) via the first node (ND411) and the third transistor (414) and
wherein the second electrode of the capacitor (C411) is connected to a gate electrode of the drive transistor (411) via the second node (ND412).

2. The display device (400) according to the claim 1, wherein a control node of the second transistor and a control node of the third transistor in any one of the pixel circuits(401) are configured to receive a control signal based on the same timing.

3. The display device (400) according to the claim 1, wherein the first transistor (412) is connected between the data line (DTL401) and a current path portion, the current path portion forming a part of the current path between the second transistor (413) and the third transistor (414) and/or wherein the second transistor (413) and the third transistor (414) are directly connected to each other at the current path portion, so that no active element is arranged between the second (413) and the third transistor (414).

4. The display device (400) according to the claim 1, wherein the capacitor (C411) is configured to set a voltage between a current electrode and a gate electrode of the drive transistor (411), and one of the pixel circuits (401) is driven such that the third transistor (414) isolates the current electrode from the capacitor (C411) during a non-emission period, and connects the current electrode to the capacitor (C411) during an emission period.

5. The display device (400) according to the claim 1, wherein a first electrode of the capacitor is connected a gate electrode of the drive transistor (411), and one of the pixel circuit (401) is driven such that the third transistor (414) isolates the current node from the capacitor (C411) during a non-emission period, and connects the current node to a potential corresponding to a potential of a second node of the capacitor (C411) so as to apply the voltage stored in the capacitor (C411) between the gate node and the current node of the drive transistor (411), during an emission period.

6. The display device (400) according to the claim 1, wherein one of the pixel circuit (401) is driven so as to:
successively set the fourth transistor (415) and the first transistor (412) to a conductive state in a non-emission period, and set the second transistor (413) and the third transistor (413) to simultaneously conduct in an emission period.

7. The display device (400) according to the claim 6, wherein the one of the pixel circuit (401) is driven such that the fourth transistor (415) and the first transistor (412) are set in non-conductive states in the emission period.

8. The display device (400) according to the claim 1, wherein the first transistor (412), the second transistor (413), third transistor (414) and the fourth transistors (415) are TFTs of the same type, in particular n-type TFTs.

9. The display device (400) according to the claim 1, wherein at least one of the plurality of pixel circuits (402), in particular each of the plurality of pixel circuits (402), include only transistors of a same type.

10. The display device (400) according to the claim 1, wherein the electro-optic element (416) is organic EL element which emits light in response to the current flow.

11. The display device (400) according to the claim 1, wherein active elements within the current path from the power supply line to the electro-optic element (416) only include the drive transistor (411), the second transistor (413), and the third transistor (414) in a given one of the pixel circuits (401) and/or wherein the drive transistor (411), the third transistor (414), the second transistor (413) and the electro-optic element (416) are connected in this order, in the one of the pixel circuits (401).

12. The display device (400) according to the claim 1, wherein the electro-optic element (416) is connected between the second transistor (413) and a cathode potential line, and wherein the electro-optic elements (416) in the plurality of pixel circuits (402) are connected to a common cathode potential line.

13. The display device (400) according to the claim 1 wherein the first transistor (412), the fourth transistor (415) and at least one of the second transistor (413) or the third transistor (414), in one of the pixel circuits (401), are controlled by different control lines.

14. The display device (400) according to claim 1, further comprising a control circuit configured to control the plurality of pixel circuits (402),
wherein each of the pixel circuits (401) is disposed

in a pixel array area (402), and the control circuit includes:

a first circuit (404, 407) disposed on one side of the pixel array area (402), and a second circuit (405, 406) disposed on another side of the pixel array area (402).

15. The display device (400) according to claim 14, wherein the first circuit (404, 407) is configured to switch the first transistor (412) and the fourth transistor (415) of at least one of the pixel circuits (401), and the second circuit (405, 406) is configured to switch the second transistor (413) and the third transistor (414) of at least one of the pixel circuits (401).

16. The display device (400) according to claim 15, wherein the first circuit (404, 407) includes a first scanner (404) and a second scanner (407), each configured to switch the first transistor (412) and the fourth transistor (415), respectively, of at least one of the pixel circuits (401) and/or wherein the second circuit (405, 406) includes a third scanner (406) and a fourth scanner (405), each configured to switch the second transistor (413) and the third transistor (414), respectively, of at least one of the pixel circuits (401).

17. The display device (400) according to claim 14, wherein the first circuit (404, 407) and the second circuit (405, 406) are disposed so as to sandwich the pixel array area (402).

18. The display device (400) according to claim 1, wherein the second transistor (413) and the third transistor (414) in one of the pixel circuits (401) are configured to be switched based on the same timing.

Patentansprüche

1. Anzeigevorrichtung (400), umfassend eine Vielzahl von Pixelschaltungen (402), die in einer Matrix angeordnet sind, wobei jede der Pixelschaltungen (401) aufweist:

ein elektrooptisches Element (416),
einen Kondensator (C411), der eine erste Elektrode und eine zweite Elektrode hat und ausgelegt ist, eine Spannung in Abhängigkeit von einer eingestellten Bildsignalspannung zu speichern,
einen Treibertransistor (411), der ausgelegt ist, einen Stromfluss eines Stromwegs von einer Energiezufuhrleitung zum elektrooptischen Element (416) zu steuern, ansprechend auf die im Kondensator (C411) gespeicherte Spannung,
einen ersten Transistor (412), der mit einem ersten Knoten (ND411) verbunden und ausgelegt ist, die eingestellte Bildsignalspannung von einer Datenleitung (DTL401) zu liefern, wobei der Stromfluss des Stromwegs von der eingestellten Bildsignalspannung abhängig ist,
einen zweiten Transistor (413) und einen dritten Transistor (414), die jeweils ausgelegt sind, den Stromfluss des Stromwegs umzuschalten, und
einen vierten Transistor (415), der mit einem zweiten Knoten (ND412) verbunden und ausgelegt ist, ein vorherbestimmtes Potential an den Kondensator (C411) anzulegen, während der zweite Transistor (413) und der dritte Transistor (414) in einem nicht-leitfähigen Zustand eingestellt sind,
wobei der zweite Transistor (413), der dritte Transistor (414) und der Treibertransistor (411) derart angeordnet sind, dass sie den Stromweg von der Energiezufuhrleitung zum elektrooptischen Element (416) bilden,
wobei die erste Elektrode des Kondensators (C411) mit einer Source-Elektrode des Treibertransistors (411) über den ersten Knoten (ND411) und den dritten Transistor (414) verbunden ist, und
wobei die zweite Elektrode des Kondensators (C411) mit einer Gate-Elektrode des Treibertransistors (411) über den zweiten Knoten (ND412) verbunden ist.

2. Anzeigevorrichtung (400) nach Anspruch 1, wobei ein Steuerknoten des zweiten Transistors und ein Steuerknoten des dritten Transistors in irgendeiner der Pixelschaltungen (401) ausgelegt sind, ein Steuersignal auf der Basis derselben Zeiteinstellung zu empfangen.

3. Anzeigevorrichtung (400) nach Anspruch 1, wobei der erste Transistor (412) zwischen der Datenleitung (DTL401) und einem Stromwegabschnitt angeschlossen ist, wobei der Stromwegabschnitt einen Teil des Stromwegs zwischen dem zweiten Transistor (413) und dem dritten Transistor (414) bildet, und/oder wobei der zweite Transistor (413) und der dritte Transistor (414) direkt miteinander am Stromwegabschnitt derart verbunden sind, dass kein aktives Element zwischen dem zweiten (413) und dem dritten Transistor (414) angeordnet ist.

4. Anzeigevorrichtung (400) nach Anspruch 1, wobei der Kondensator (C411) ausgelegt ist, eine Spannung zwischen einer Stromelektrode und einer Gate-Elektrode des Treibertransistors (411) einzustellen, und eine der Pixelschaltungen (401) derart getrieben wird, dass der dritte Transistor (414) die Stromelektrode vom Kondensator (C411) während einer Nicht-Emissionsperiode isoliert und die Stromelektrode mit dem Kondensator (C411) während einer Emissionsperiode verbindet.

5. Anzeigevorrichtung (400) nach Anspruch 1, wobei eine erste Elektrode des Kondensators mit einer Gate-Elektrode des Treibertransistors (411) verbunden ist und eine der Pixelschaltungen (401) derart getrieben wird, dass der dritte Transistor (414) den Stromknoten vom Kondensator (C411) während einer Nicht-Emissionsperiode isoliert und den Stromknoten mit einem Potential, das einem Potential eines zweiten Knotens des Kondensators (C411) entspricht, derart verbindet, dass die im Kondensator (C411) gespeicherte Spannung zwischen dem Gate-Knoten und dem Stromknoten des Treibertransistors (411) während einer Emissionsperiode angelegt wird.

6. Anzeigevorrichtung (400) nach Anspruch 1, wobei eine der Pixelschaltungen (401) derart getrieben wird, dass: aufeinanderfolgend der vierte Transistor (415) und der erste Transistor (412) in einen leitfähigen Zustand in einer Nicht-Emissionsperiode versetzt werden und der zweite Transistor (413) und der dritte Transistor (413) in einer Emissionsperiode gleichzeitig leiten.

7. Anzeigevorrichtung (400) nach Anspruch 6, wobei eine der Pixelschaltungen (401) derart getrieben wird, dass der vierte Transistor (415) und der erste Transistor (412) in der Emissionsperiode in nicht-leitfähige Zustände versetzt werden.

8. Anzeigevorrichtung (400) nach Anspruch 1, wobei der erste Transistor (412), der zweite Transistor (413), der dritte Transistor (414) und der vierte Transistor (415) TFTs desselben Typs, insbesondere n-Typ-TFTs, sind.

9. Anzeigevorrichtung (400) nach Anspruch 1, wobei mindestens eine der Vielzahl von Pixelschaltungen (402), insbesondere jede der Vielzahl von Pixelschaltungen (402), nur Transistoren desselben Typs aufweist.

10. Anzeigevorrichtung (400) nach Anspruch 1, wobei das elektrooptische Element (416) ein organisches EL-Element ist, das ansprechend auf den Stromfluss Licht emittiert.

11. Anzeigevorrichtung (400) nach Anspruch 1, wobei aktive Elemente innerhalb des Stromwegs von der Energiezufuhrleitung zum elektrooptischen Element (416) nur den Treibertransistor (411), den zweiten Transistor (413) und den dritten Transistor (414) in einer gegebenen der Pixelschaltungen (401) aufweisen, und/oder wobei der Treibertransistor (411), der dritte Transistor (414), der zweite Transistor (413) und das elektrooptische Element (416) in dieser Reihenfolge in der einen der Pixelschaltungen (401) verbunden sind.

12. Anzeigevorrichtung (400) nach Anspruch 1, wobei das elektrooptische Element (416) zwischen dem zweiten Transistor (413) und einer Kathodenpotentialleitung angeschlossen ist, und wobei die elektrooptischen Elemente (416) in der Vielzahl von Pixelschaltungen (402) mit einer gemeinsamen Kathodenpotentialleitung verbunden sind.

13. Anzeigevorrichtung (400) nach Anspruch 1, wobei der erste Transistor (412), der vierte Transistor (415) und mindestens einer von dem zweiten Transistor (413) oder dem dritten Transistor (414) in einer der Pixelschaltungen (401) von verschiedenen Steuerleitungen gesteuert werden.

14. Anzeigevorrichtung (400) nach Anspruch 1, ferner umfassend eine Steuerschaltung, die ausgelegt ist, die Vielzahl von Pixelschaltungen (402) zu steuern, wobei jede der Pixelschaltungen (401) in einem Pixelanordnungsbereich (402) angeordnet ist und die Steuerschaltung aufweist:

eine erste Schaltung (404, 407), die auf einer Seite des Pixelanordnungsbereichs (402) angeordnet ist, und
eine zweite Schaltung (405, 406), die auf der anderen Seite des Pixelanordnungsbereichs (402) angeordnet ist.

15. Anzeigevorrichtung (400) nach Anspruch 14, wobei die erste Schaltung (404, 407) ausgelegt ist, den ersten Transistor (412) und den vierten Transistor (415) mindestens einer der Pixelschaltungen (401) umzuschalten, und die zweite Schaltung (405, 406) ausgelegt ist, den zweiten Transistor (413) und den dritten Transistor (414) mindestens einer der Pixelschaltungen (401) umzuschalten.

16. Anzeigevorrichtung (400) nach Anspruch 15, wobei die erste Schaltung (404, 407) einen ersten Scanner (404) und einen zweiten Scanner (407) aufweist, die jeweils ausgelegt sind, jeweils den ersten Transistor (412) und den vierten Transistor (415) mindestens einer der Pixelschaltungen (401) umzuschalten, und/oder wobei die zweite Schaltung (405, 406) einen dritten Scanner (406) und einen vierten Scanner (405) aufweist, die jeweils ausgelegt sind, jeweils den zweiten Transistor (413) und den dritten Transistor (414) mindestens einer der Pixelschaltungen (401) umzuschalten.

17. Anzeigevorrichtung (400) nach Anspruch 14, wobei die erste Schaltung (404, 407) und die zweite Schaltung (405, 406) derart angeordnet sind, dass sie den Pixelanordnungsbereich (402) sandwichartig dazwischen anordnen.

18. Anzeigevorrichtung (400) nach Anspruch 1, wobei der zweite Transistor (413) und der dritte Transistor (414) in einer der Pixelschaltungen (401) ausgelegt sind, auf der Basis derselben Zeiteinstellung umgeschaltet zu werden.

Revendications

1. Dispositif d'affichage (400) comprenant une pluralité de circuits de pixels (402) disposés en une matrice, dans lequel chaque circuit de pixel (401) comprend :

un élément électro-optique (416),
un condensateur (C411) ayant une première électrode et une seconde électrode, et conçu pour stocker une tension qui est fonction d'une tension de signal d'image définie,
un transistor d'actionnement (411) conçu pour commander un flux de courant d'un trajet de courant depuis une ligne d'alimentation électrique vers l'élément électro-optique (416) en réponse à la tension stockée dans le condensateur (C411),
un premier transistor (412) connecté à un premier noeud (ND411) et conçu pour fournir la tension de signal d'image définie depuis une ligne de données (DTL401), le flux de courant du trajet de courant étant fonction de la tension de signal d'image définie,
un deuxième transistor (413) et un troisième transistor (414) conçus chacun pour commuter le flux de courant du trajet de courant, et
un quatrième transistor (415) connecté à un second noeud (ND412) et conçu pour appliquer un potentiel prédéterminé au condensateur (C411) tandis que le deuxième transistor (413) et le troisième transistor (414) sont réglés à un état non conducteur,
dans lequel le deuxième transistor (413), le troisième transistor (414) et le transistor d'actionnement (411) sont disposés de manière à former le trajet de courant depuis la ligne d'alimentation électrique vers l'élément électro-optique (416),
dans lequel la première électrode du condensateur (C411) est connectée à une électrode source du transistor d'actionnement (411) via le premier noeud (ND411) et le troisième transistor (414) et
dans lequel la seconde électrode du condensateur (C411) est connectée à une électrode de grille du transistor d'actionnement (411) via le second noeud (ND412).

2. Dispositif d'affichage (400) selon la revendication 1, dans lequel un noeud de commande du deuxième transistor et un noeud de commande du troisième transistor dans l'un quelconque des circuits de pixels (401) sont conçus pour recevoir un signal de commande basé sur la même synchronisation.

3. Dispositif d'affichage (400) selon la revendication 1, dans lequel le premier transistor (412) est connecté entre la ligne de données (DTL401) et une partie du trajet de courant, la partie du trajet de courant formant une partie du trajet de courant entre le deuxième transistor (413) et le troisième transistor (414) et/ou dans lequel le deuxième transistor (413) et le troisième transistor (414) sont connectés directement l'un à l'autre au niveau de la partie de trajet de courant de sorte qu'aucun élément actif n'est disposé entre le deuxième (413) et le troisième transistor (414).

4. Dispositif d'affichage (400) selon la revendication 1, dans lequel le condensateur (C411) est conçu pour définir une tension entre une électrode de courant et une électrode de grille du transistor d'actionnement (411), et l'un des circuits de pixels (401) est actionné de sorte que le troisième transistor (414) isole l'électrode de courant du condensateur (C411) pendant une période de non-émission et connecte l'électrode de courant au condensateur (C411) pendant une période d'émission.

5. Dispositif d'affichage (400) selon la revendication 1, dans lequel une première électrode du condensateur est connectée à une électrode de grille du transistor d'actionnement (411), et un des circuits de pixels (401) est actionné de sorte que le troisième transistor (414) isole le noeud de courant du condensateur (C411) pendant une période de non-émission et connecte le noeud de courant à un potentiel correspondant à un potentiel d'un second noeud du condensateur (C411) de manière à appliquer la tension stockée dans le condensateur (C411) entre le noeud de grille et le noeud de courant du transistor d'actionnement (411) pendant une période d'émission.

6. Dispositif d'affichage (400) selon la revendication 1, dans lequel un des circuits de pixels (401) est actionné de manière à :
faire passer successivement le quatrième transistor (415) et le premier transistor (412) à un état conducteur pendant une période de non-émission, et régler le deuxième transistor (413) et le troisième transistor (413) pour qu'ils soient simultanément conducteurs pendant une période d'émission.

7. Dispositif d'affichage (400) selon la revendication 6, dans lequel un circuit de pixel (401) est actionné de sorte que le quatrième transistor (415) et le premier transistor (412) soient réglés à des états non conducteurs pendant la période d'émission.

8. Dispositif d'affichage (400) selon la revendication 1, dans lequel le premier transistor (412), le deuxième transistor (413), le troisième transistor (414) et le quatrième transistor (415) sont des TFT du même type, en particulier des TFT de type n.

9. Dispositif d'affichage (400) selon la revendication 1, dans lequel l'un au moins de la pluralité de circuits de pixels (402), en particulier chacun de la pluralité de circuits de pixels (402), comprend/comprennent uniquement des transistors du même type.

10. Dispositif d'affichage (400) selon la revendication 1, dans lequel l'élément électro-optique est un élément EL organique qui émet de la lumière en réponse au flux de courant.

11. Dispositif d'affichage (400) selon la revendication 1, dans lequel les éléments actifs dans le trajet de courant depuis la ligne d'alimentation électrique à l'élément électro-optique (416) comprennent uniquement le transistor d'actionnement (411), le deuxième transistor (413) et le troisième transistor (414) dans l'un donné des circuits de pixels (401) et/ou dans lequel le transistor d'actionnement (411), le troisième transistor (414), le deuxième transistor (413) et l'élément électro-optique (416) sont connectés dans cet ordre dans un des circuits de pixels (401).

12. Dispositif d'affichage (400) selon la revendication 1, dans lequel l'élément électro-optique (416) est connecté entre le deuxième transistor (413) et une ligne de potentiel de cathode, et dans lequel les éléments électro-optiques (416) dans la pluralité de circuits de pixels (402) sont connectés à une ligne de potentiel de cathode commune.

13. Dispositif d'affichage (400) selon la revendication 1, dans lequel le premier transistor (412), le quatrième transistor (415) et l'un au moins du deuxième transistor (413) et du troisième transistor (414), dans l'un des circuits de pixels (401), sont commandés par des lignes de commande différentes.

14. Dispositif d'affichage (400) selon la revendication 1, comprenant en outre un circuit de commande conçu pour commander la pluralité de circuits de pixels (402), dans lequel chacun des circuits de pixels (401) est disposé dans une zone de réseau de pixels (402), et le circuit de commande comprend :

   un premier circuit (404, 407) disposé sur un côté de la zone de réseau de pixels (402), et
   un second circuit (405, 406) disposé sur un autre côté de la zone de réseau de pixels (402).

15. Dispositif d'affichage (400) selon la revendication 14, dans lequel le premier circuit (404, 407) est conçu pour commuter le premier transistor (412) et le quatrième transistor (415) de l'un au moins des circuits de pixels (401), et le second circuit (405, 406) est conçu pour commuter le deuxième transistor (413) et le troisième transistor (414) de l'un au moins des circuits de pixels (401).

16. Dispositif d'affichage (400) selon la revendication 15, dans lequel le premier circuit (404, 407) comprend un premier scanner (404) et un deuxième scanner (407) chacun conçus pour commuter le premier transistor (412) et le quatrième transistor (415), respectivement, d'au moins un des circuits de pixels (401) et/ou dans lequel le second circuit (405, 406) comprend un troisième scanner (406) et un quatrième scanner (405) chacun conçus pour commuter le deuxième transistor (413) et le troisième transistor (414), respectivement, de l'un au moins des circuits de pixels (401) .

17. Dispositif d'affichage (400) selon la revendication 14, dans lequel le premier circuit (404, 407) et le second circuit (405, 406) sont disposés de manière à prendre en sandwich la zone de réseau de pixels (402).

18. Dispositif d'affichage (400) selon la revendication 1, dans lequel le deuxième transistor (413) et le troisième transistor (414) dans l'un des circuits de pixels (401) sont conçus pour être commutés selon la même synchronisation.

FIG. 1

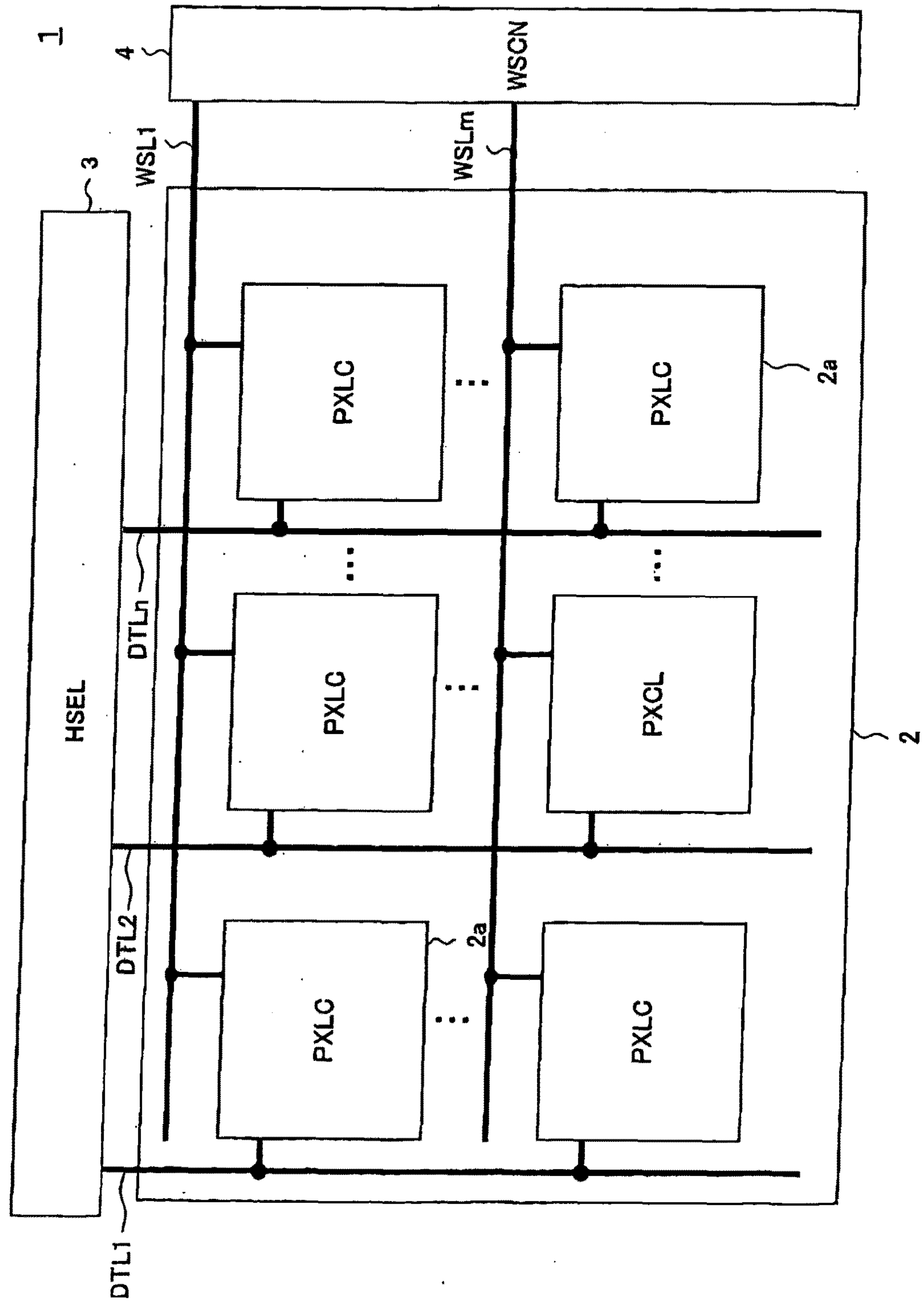

1
4
WSCN
WSL1
WSLm
3
HSEL
DTL1
DTL2
DTLn
PXLC
PXLC
PXLC
PXLC
PXCL
PXLC
2a
2a
2

FIG. 2

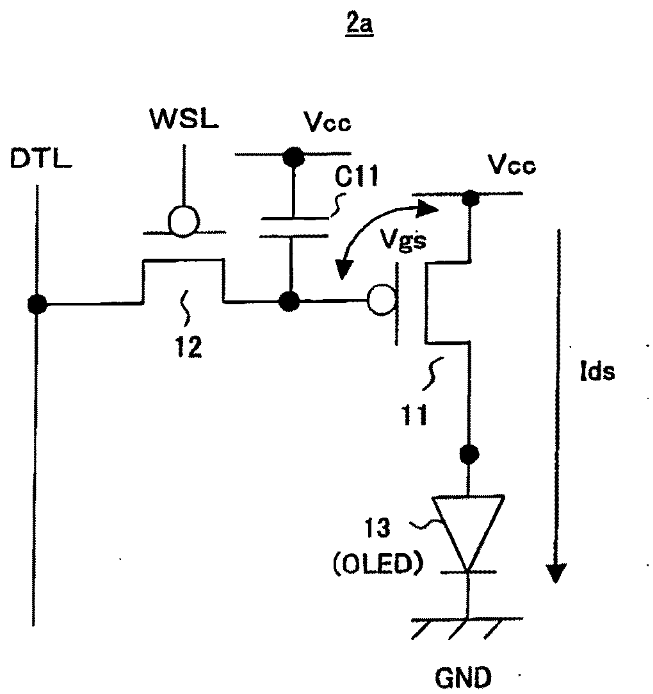


FIG. 3

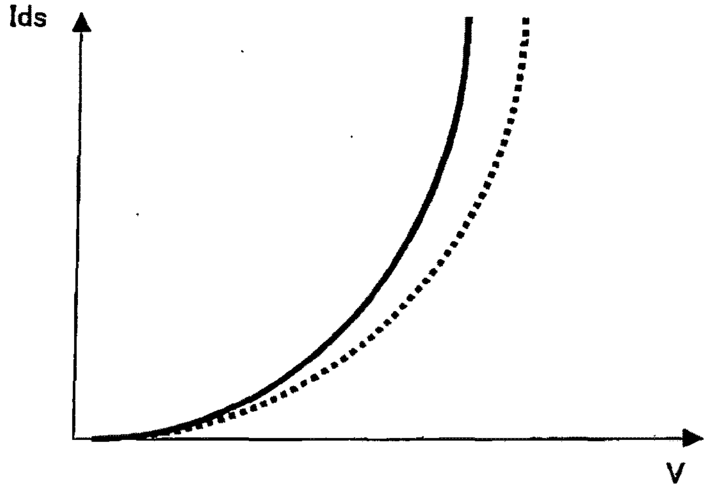


FIG. 4

2b

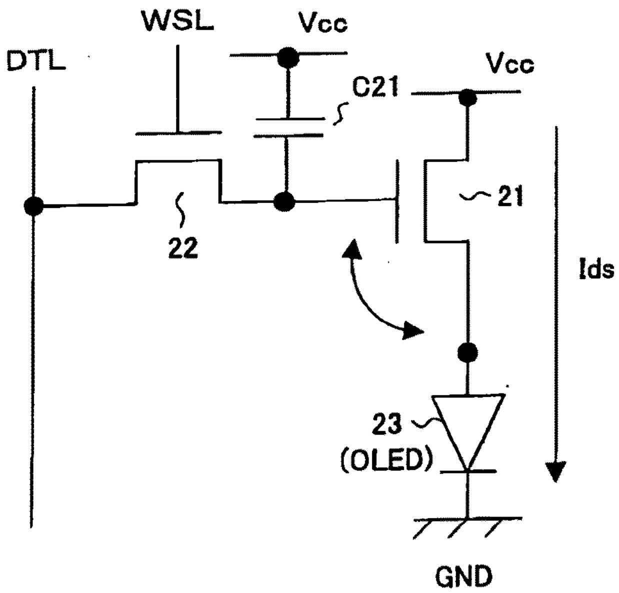


FIG. 5

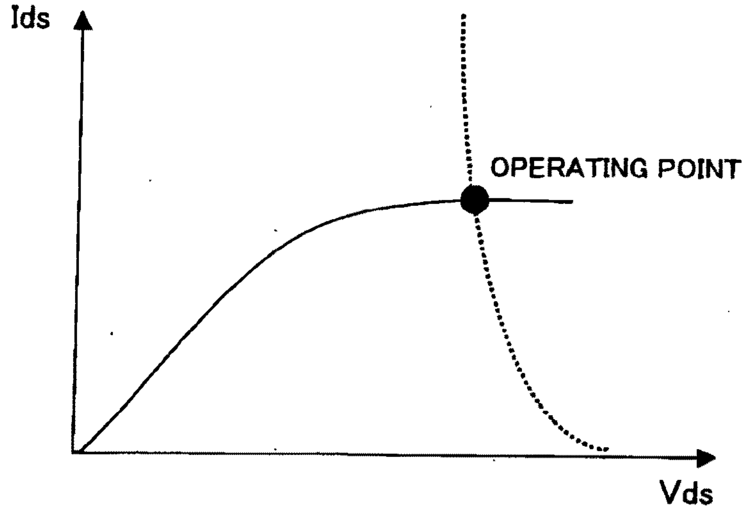


FIG. 6

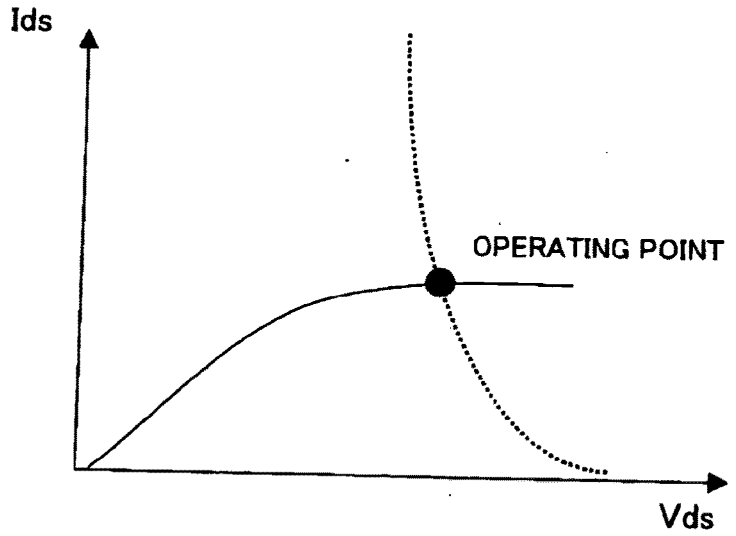


FIG. 7

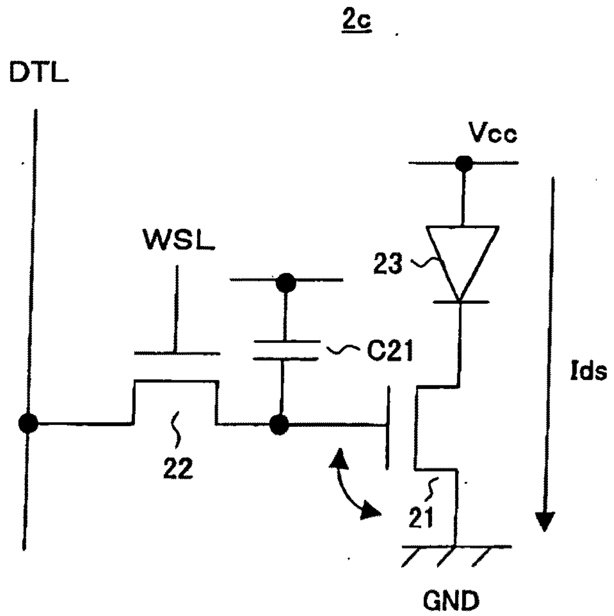


FIG. 8

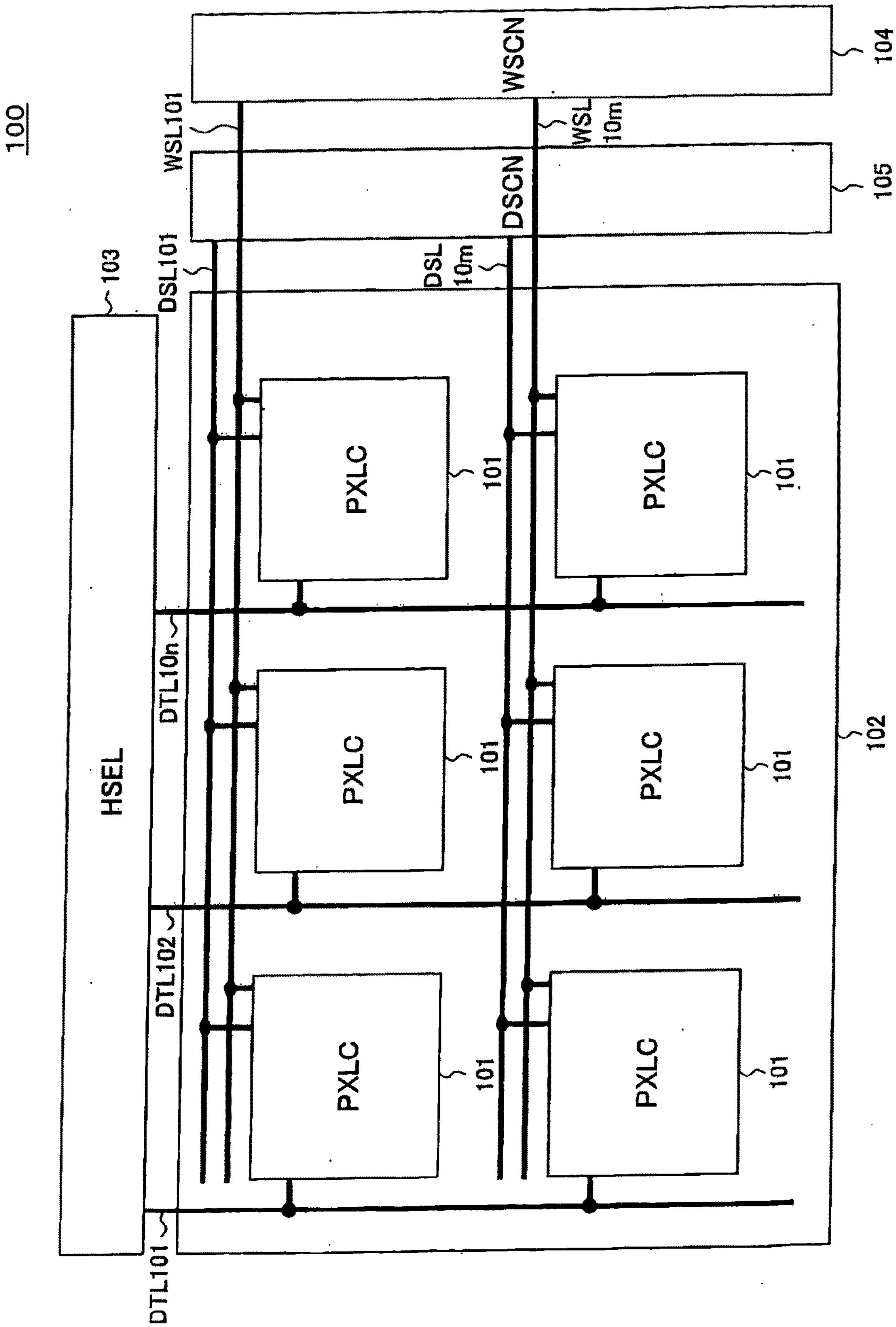
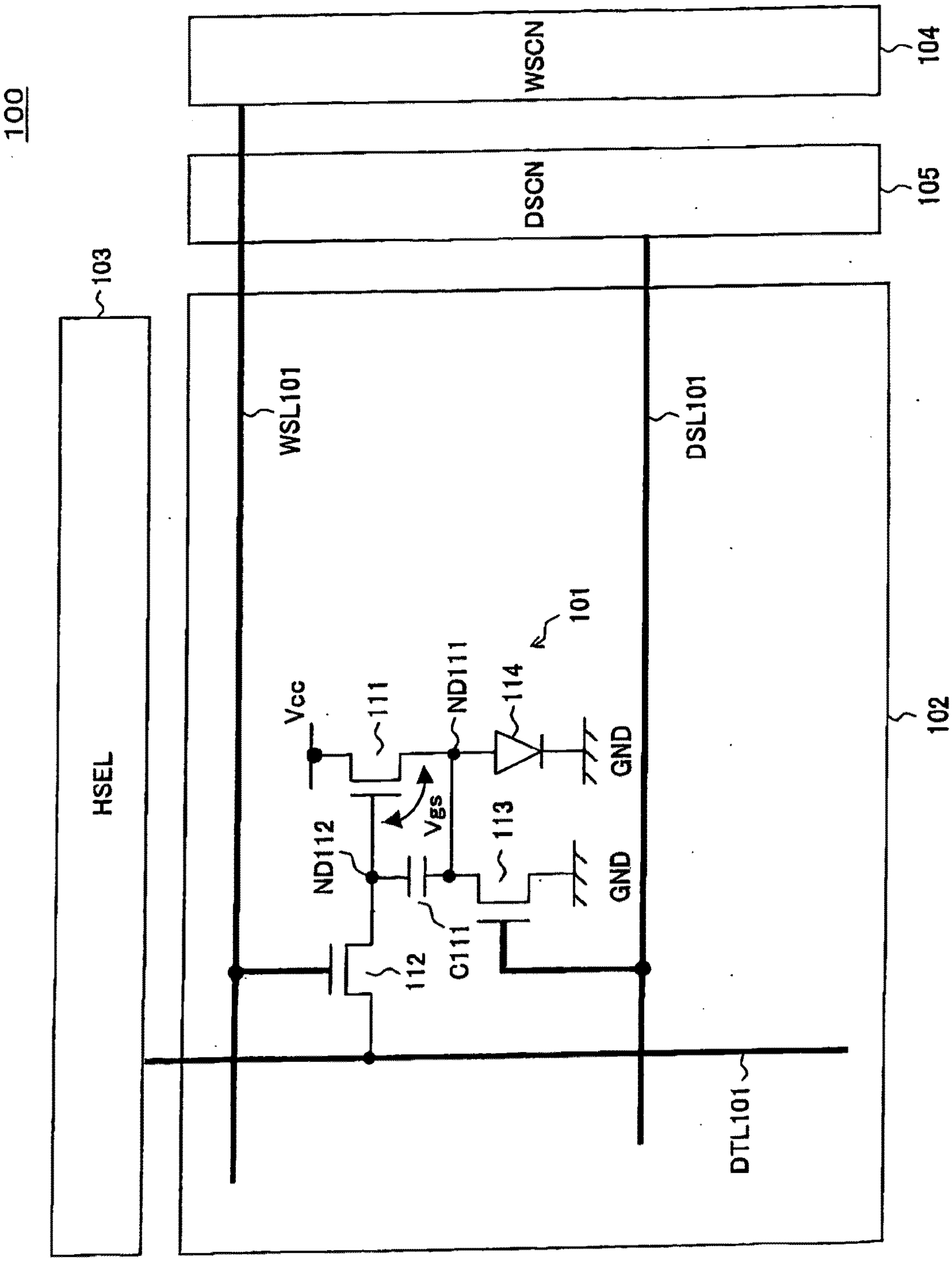

100
WSCN
104
DSCN
105
WSL101
WSL 10m
DSL101
DSL 10m
103
HSEL
PXLC
PXLC
PXLC
PXLC
PXLC
PXLC
101
101
101
101
101
101
DTL101
DTL102
DTL10n
102

FIG. 9


100
103
HSEL
WSCN
104
DSCN
105
WSL101
DSL101
101
102
Vcc
111
ND111
114
GND
Vgs
113
GND
ND112
C111
112
DTL101

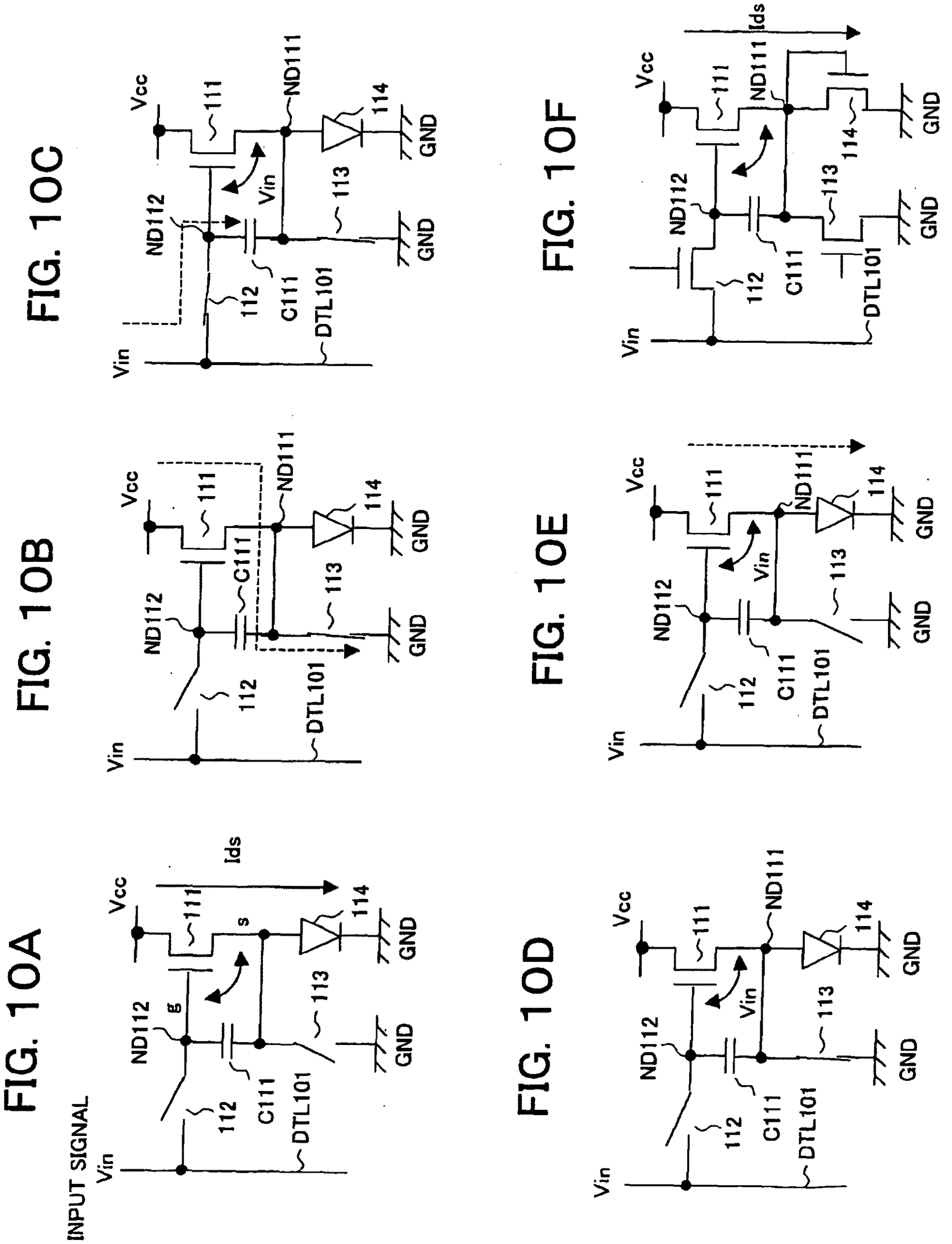


FIG. 10A

FIG. 10B

FIG. 10C

FIG. 10D

FIG. 10E

FIG. 10F

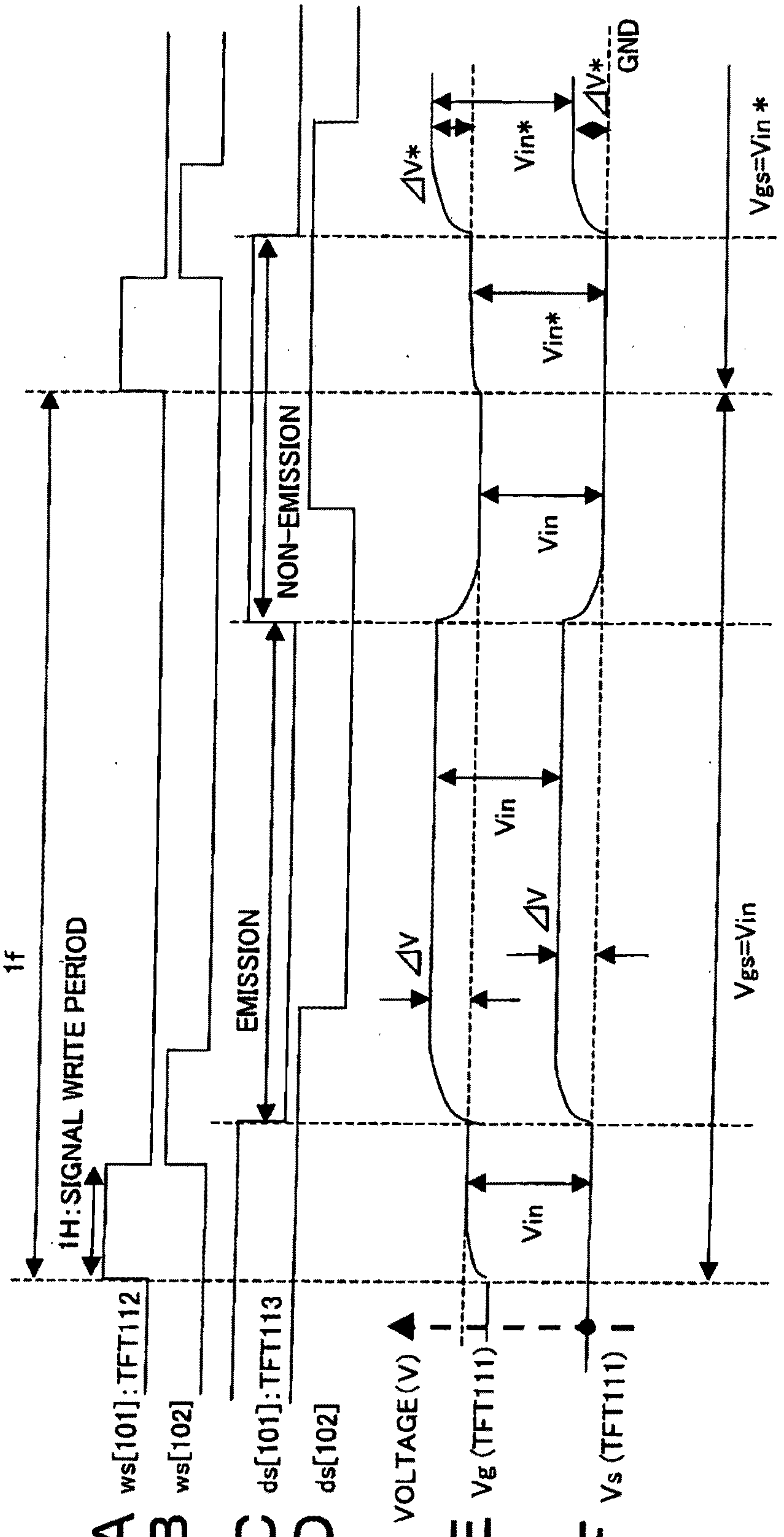


FIG. 11A
FIG. 11B
FIG. 11C
FIG. 11D
FIG. 11E
FIG. 11F

FIG. 12

200

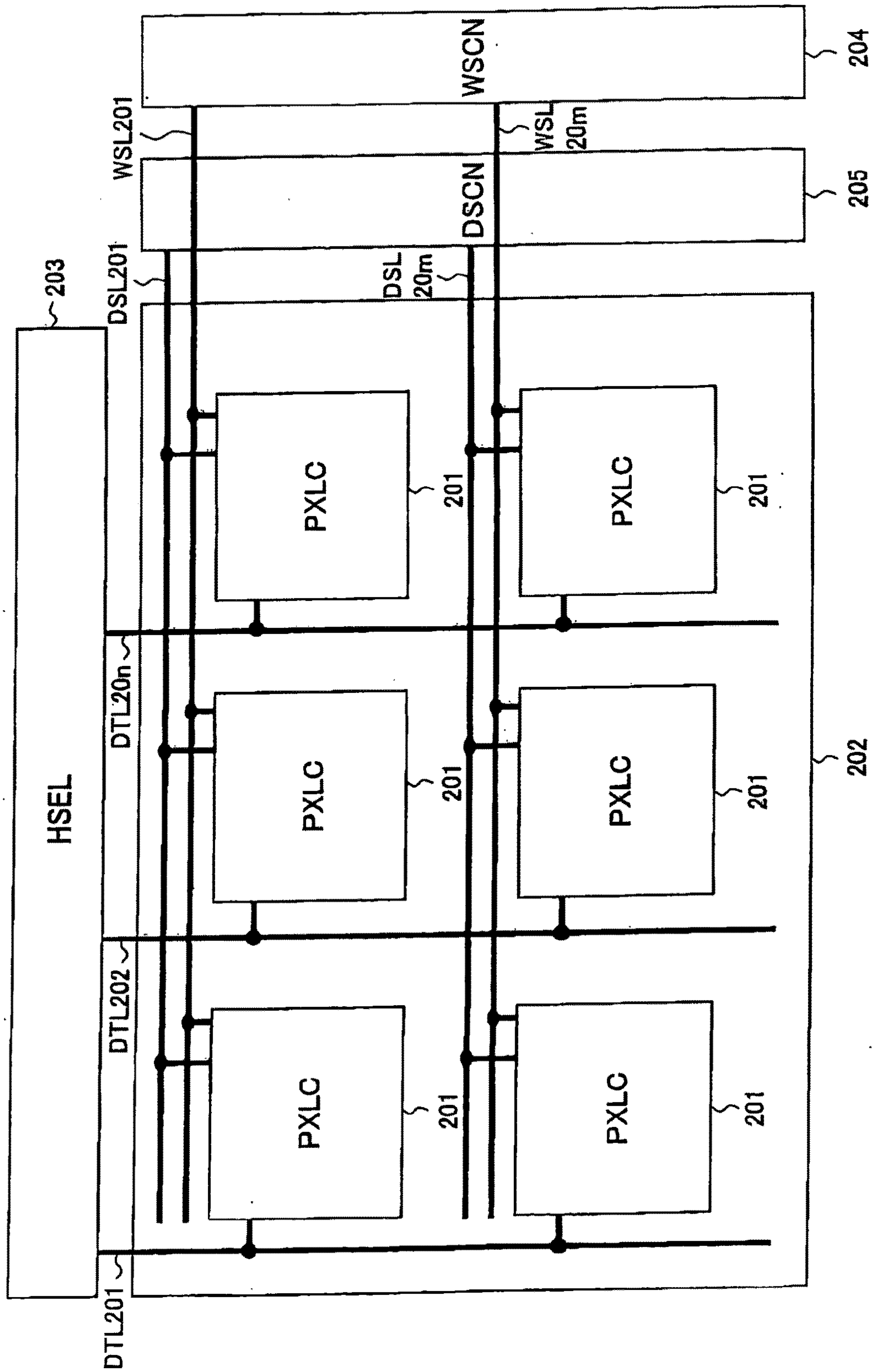
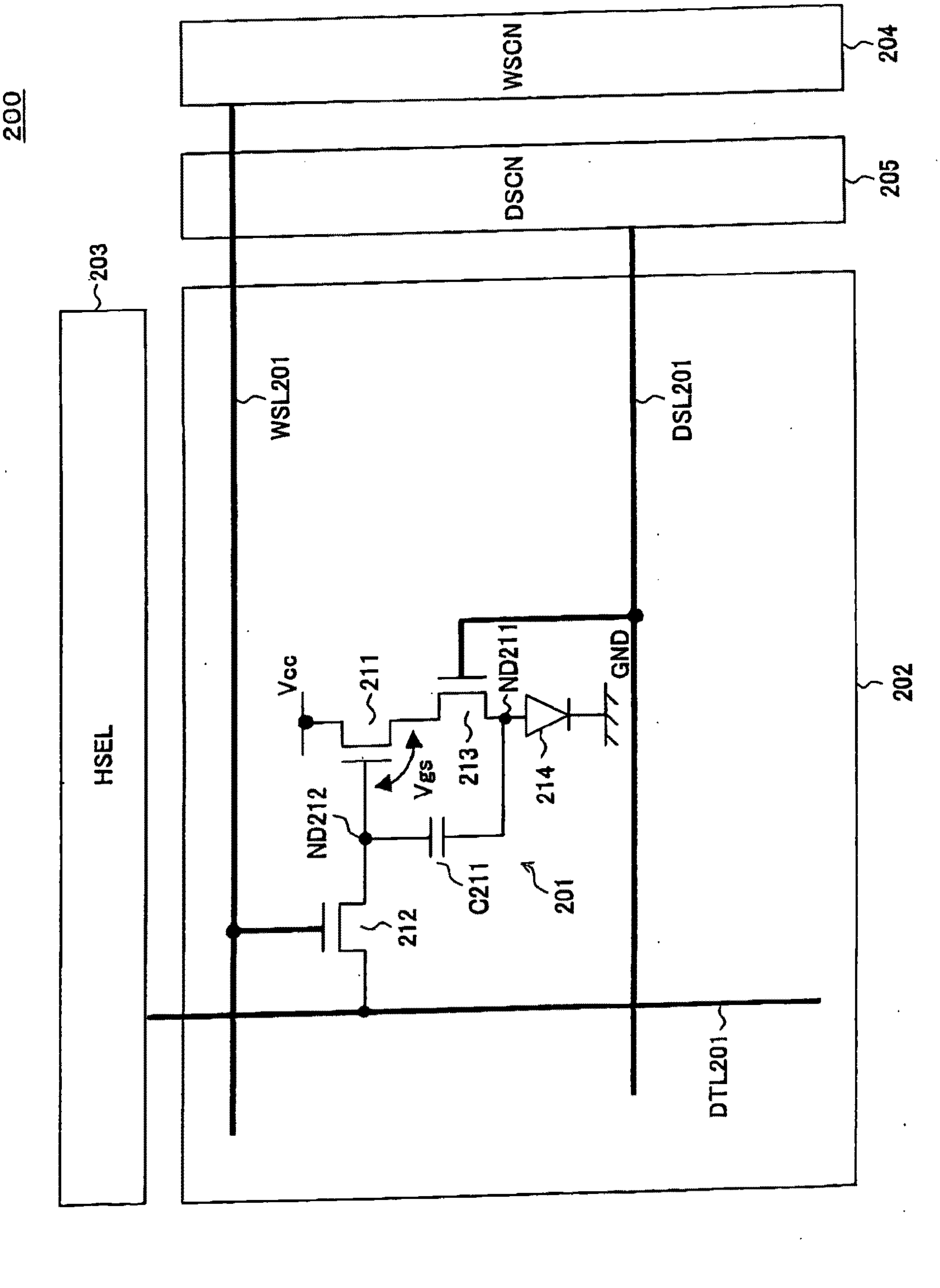

WSCN
204
WSL201
WSL 20m
DSCN
205
DSL201
DSL 20m
203
HSEL
PXLC
201
DTL20n
DTL202
DTL201
202

FIG. 13


200
WSCN
204
DSCN
205
203
HSEL
WSL201
DSL201
Vcc
211
ND211
GND
Vgs
213
214
ND212
C211
201
212
202
DTL201

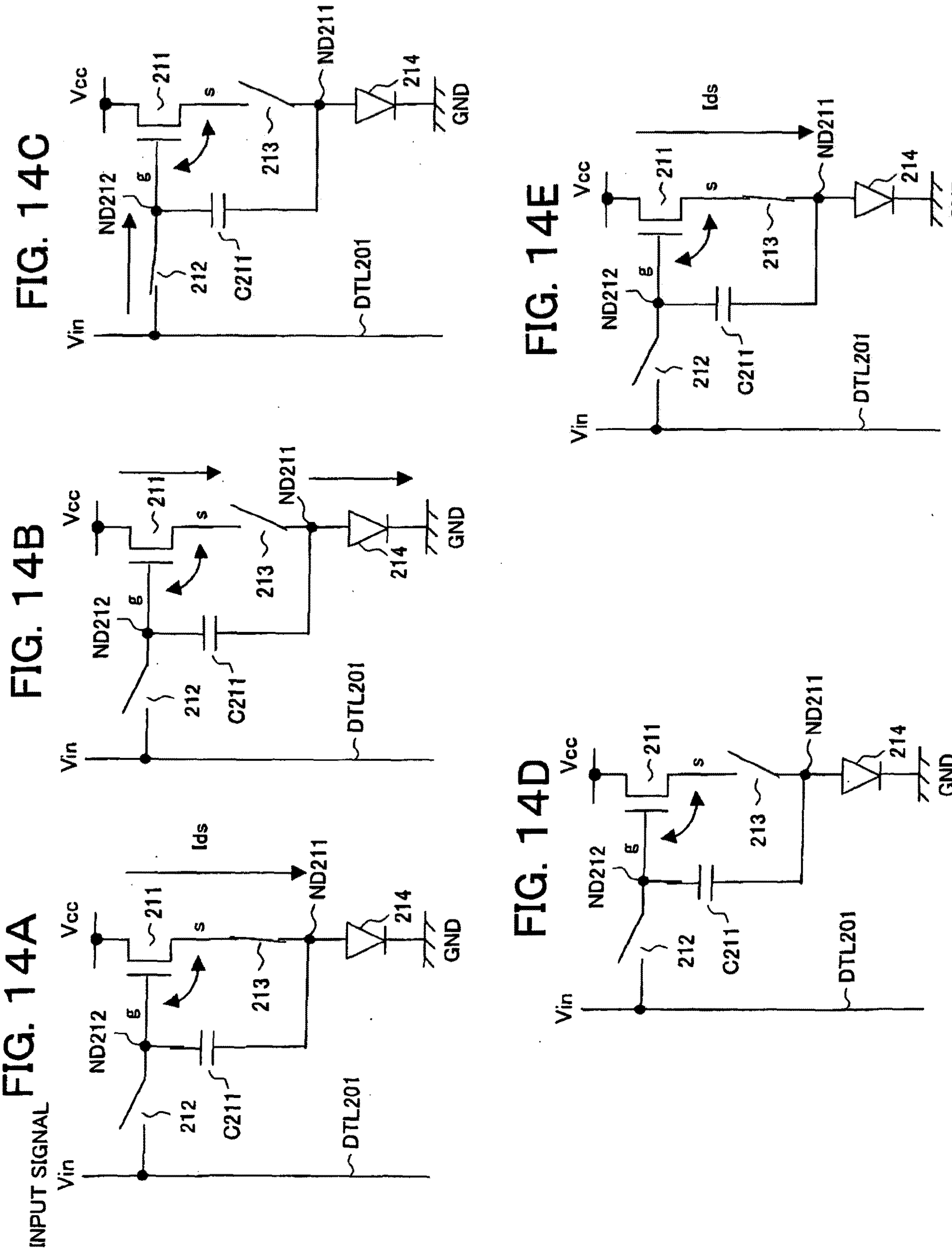


FIG. 14A

FIG. 14B

FIG. 14C

FIG. 14D

FIG. 14E

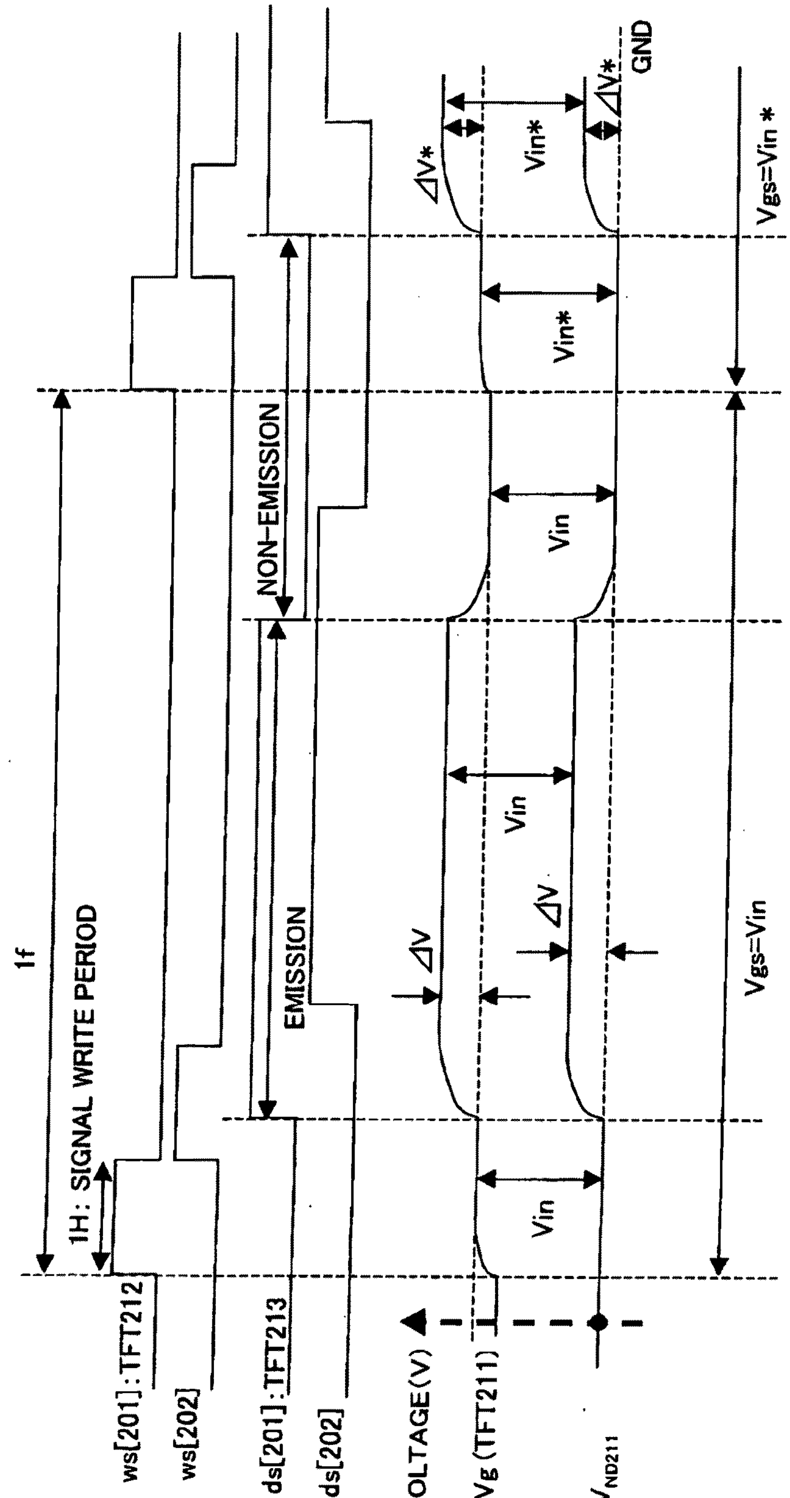


FIG. 15A
FIG. 15B
FIG. 15C
FIG. 15D
FIG. 15E
FIG. 15F

FIG. 16

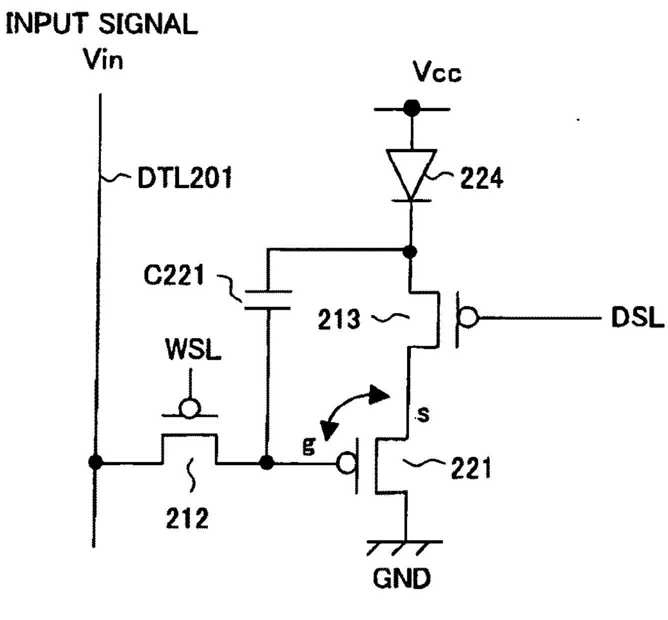

INPUT SIGNAL
Vin
Vcc
DTL201
224
C221
213
DSL
WSL
s
g
221
212
GND

FIG. 17

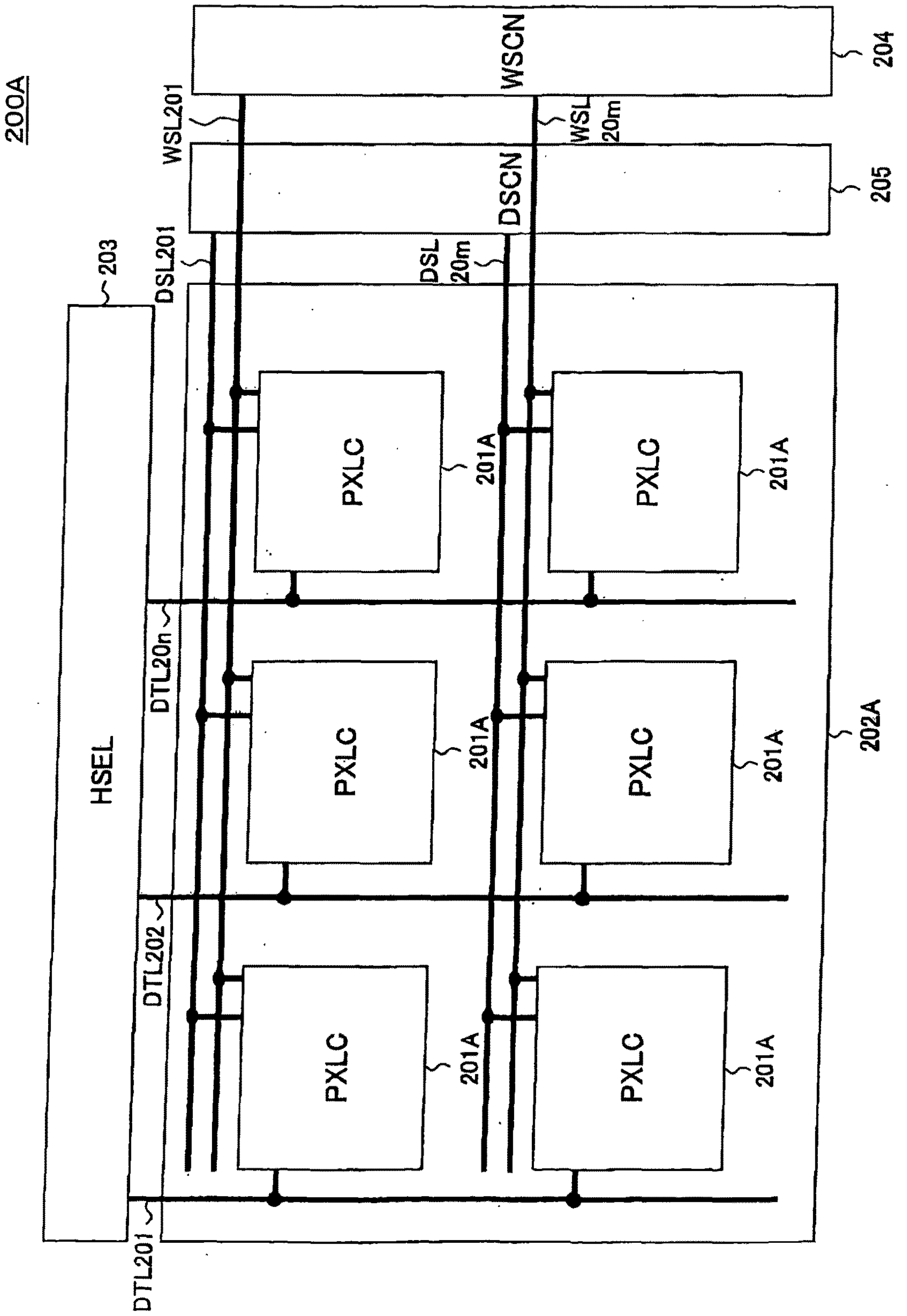

200A
WSCN
204
WSL201
WSL 20m
DSCN
205
DSL201
DSL 20m
203
HSEL
PXLC
201A
DTL20n
DTL202
DTL201
202A

FIG. 18

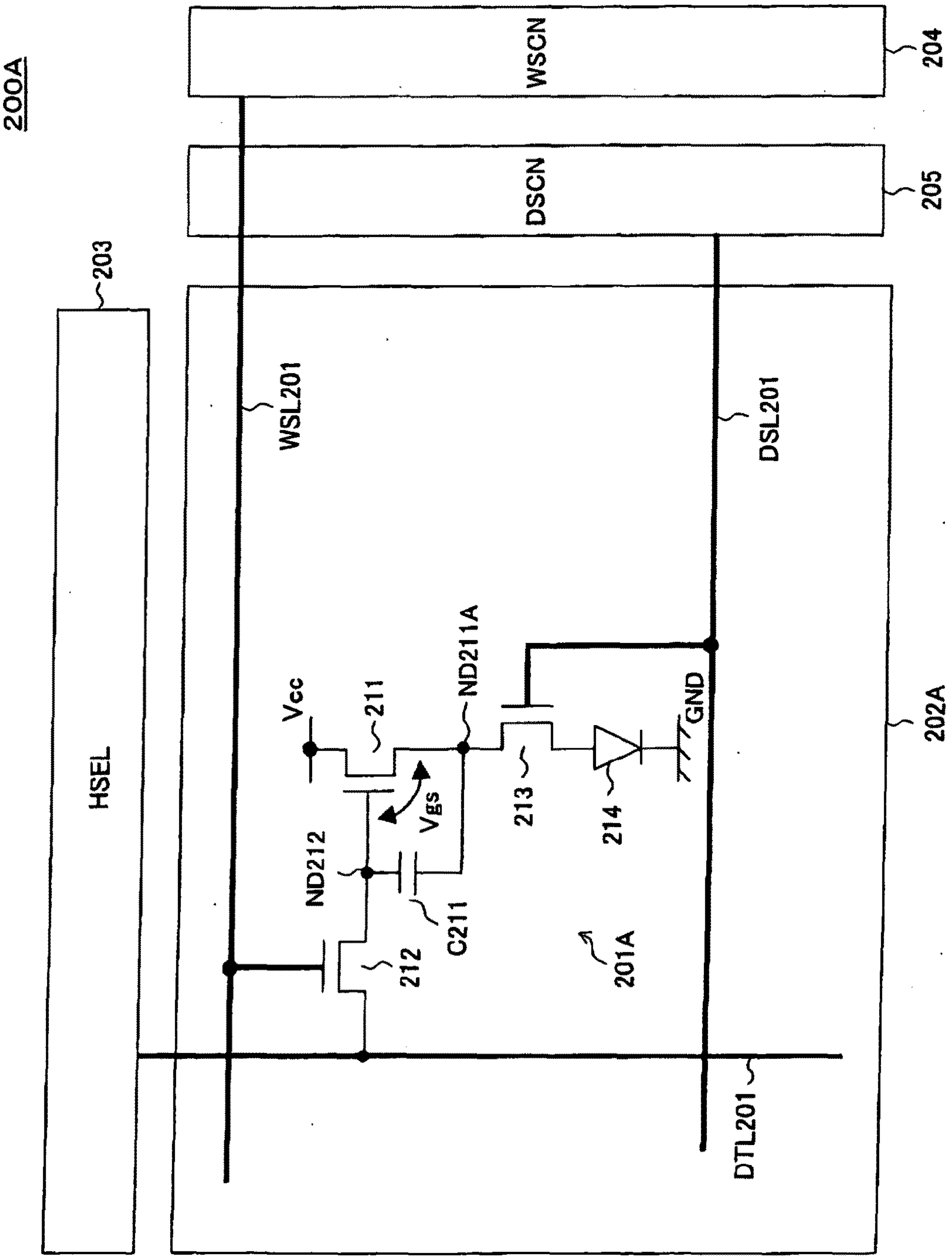

200A
WSCN
204
DSCN
205
203
HSEL
WSL201
DSL201
Vcc
211
ND211A
Vgs
ND212
C211
212
213
214
GND
201A
202A
DTL201

FIG. 19A

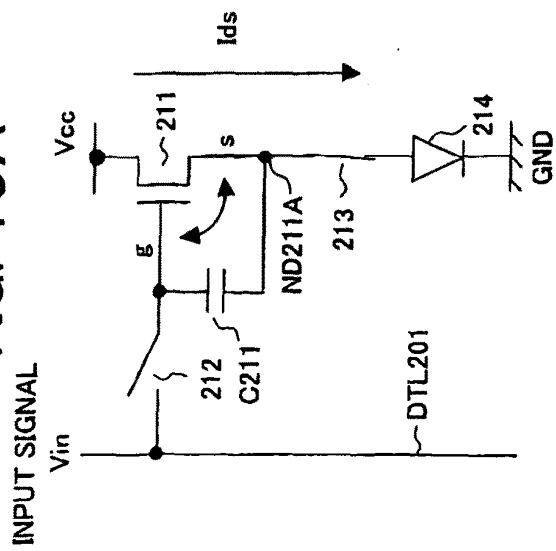


FIG. 19B

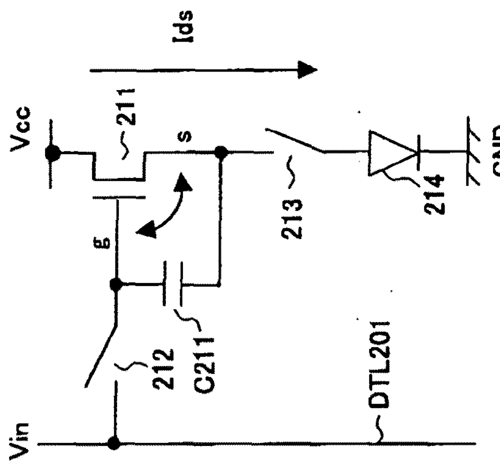


FIG. 19C

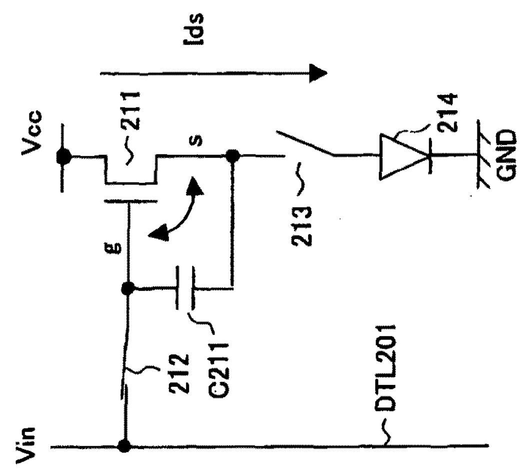


FIG. 19D

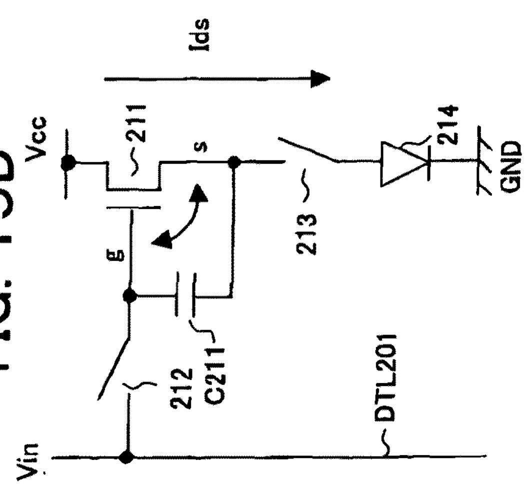
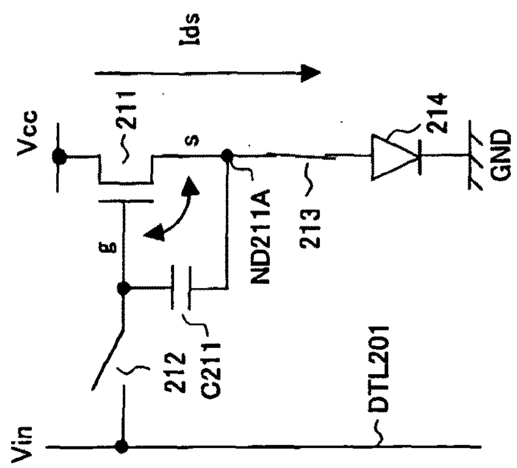


FIG. 19E



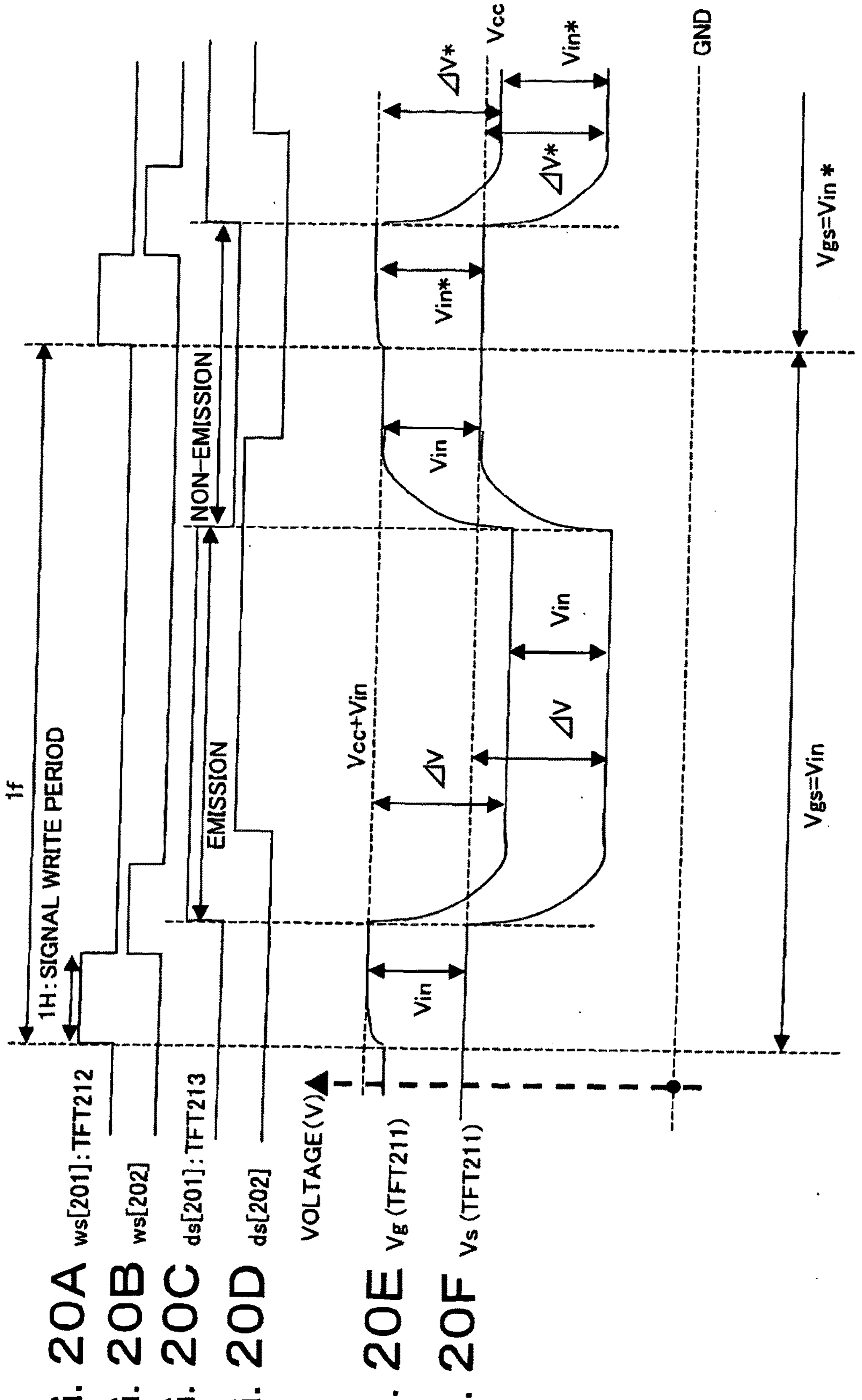


FIG. 20A
FIG. 20B
FIG. 20C
FIG. 20D
FIG. 20E
FIG. 20F

FIG. 21

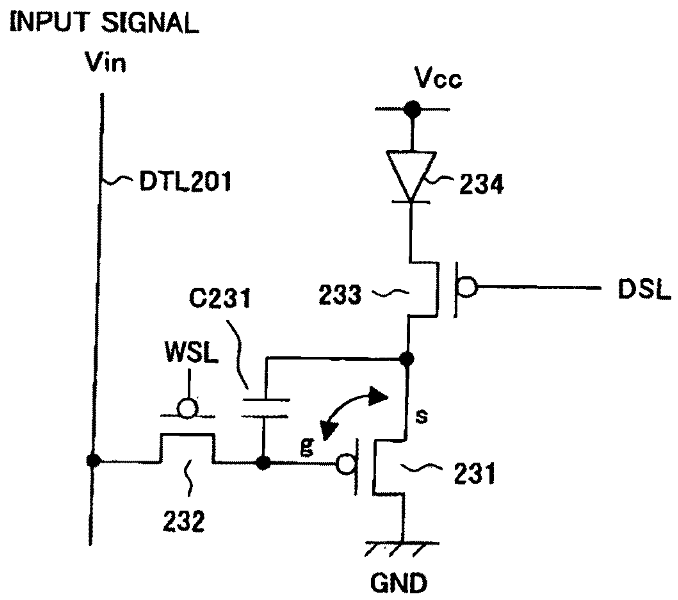

INPUT SIGNAL
Vin
Vcc
DTL201
234
233
DSL
C231
WSL
s
g
231
232
GND

FIG. 22

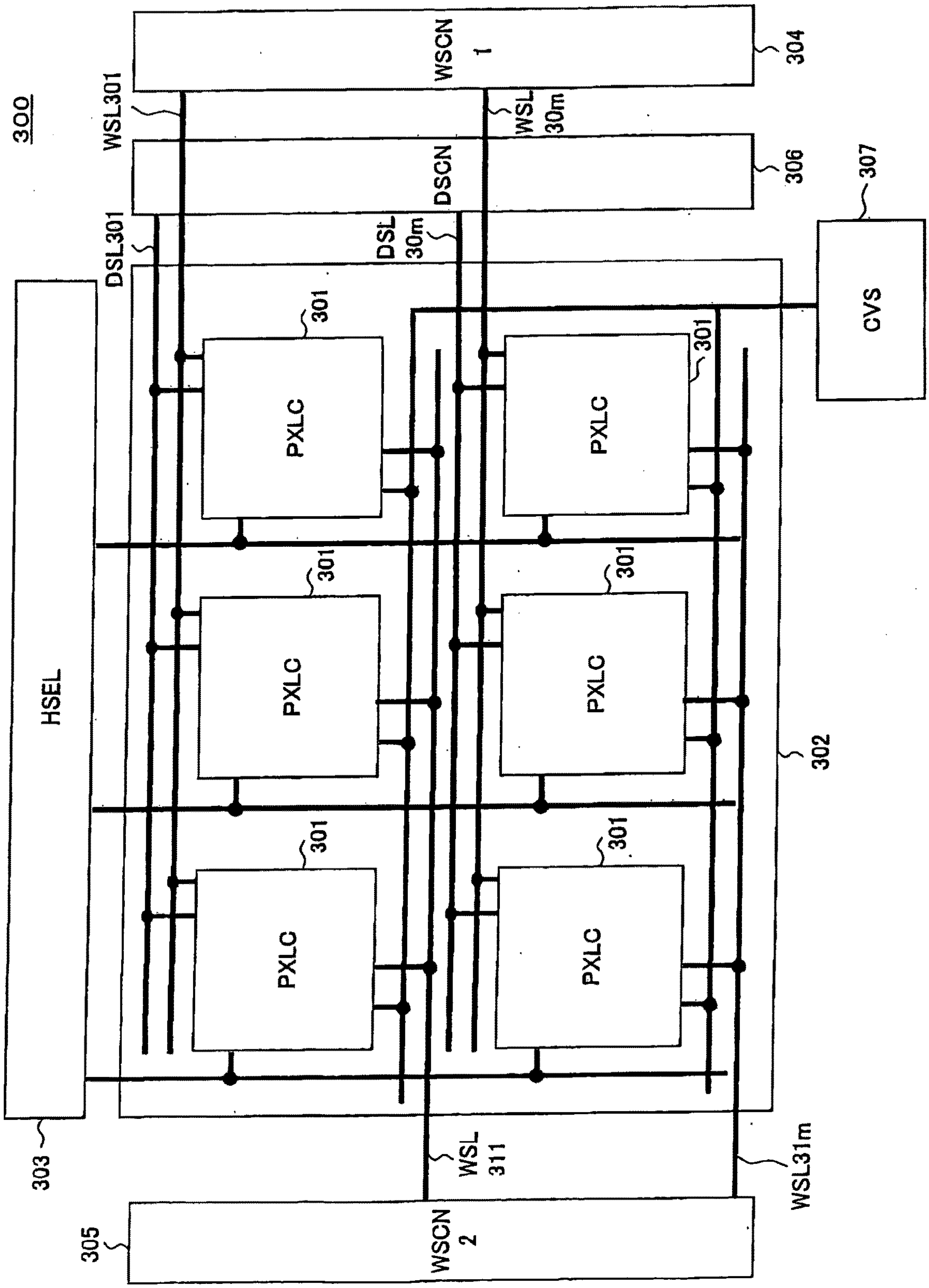
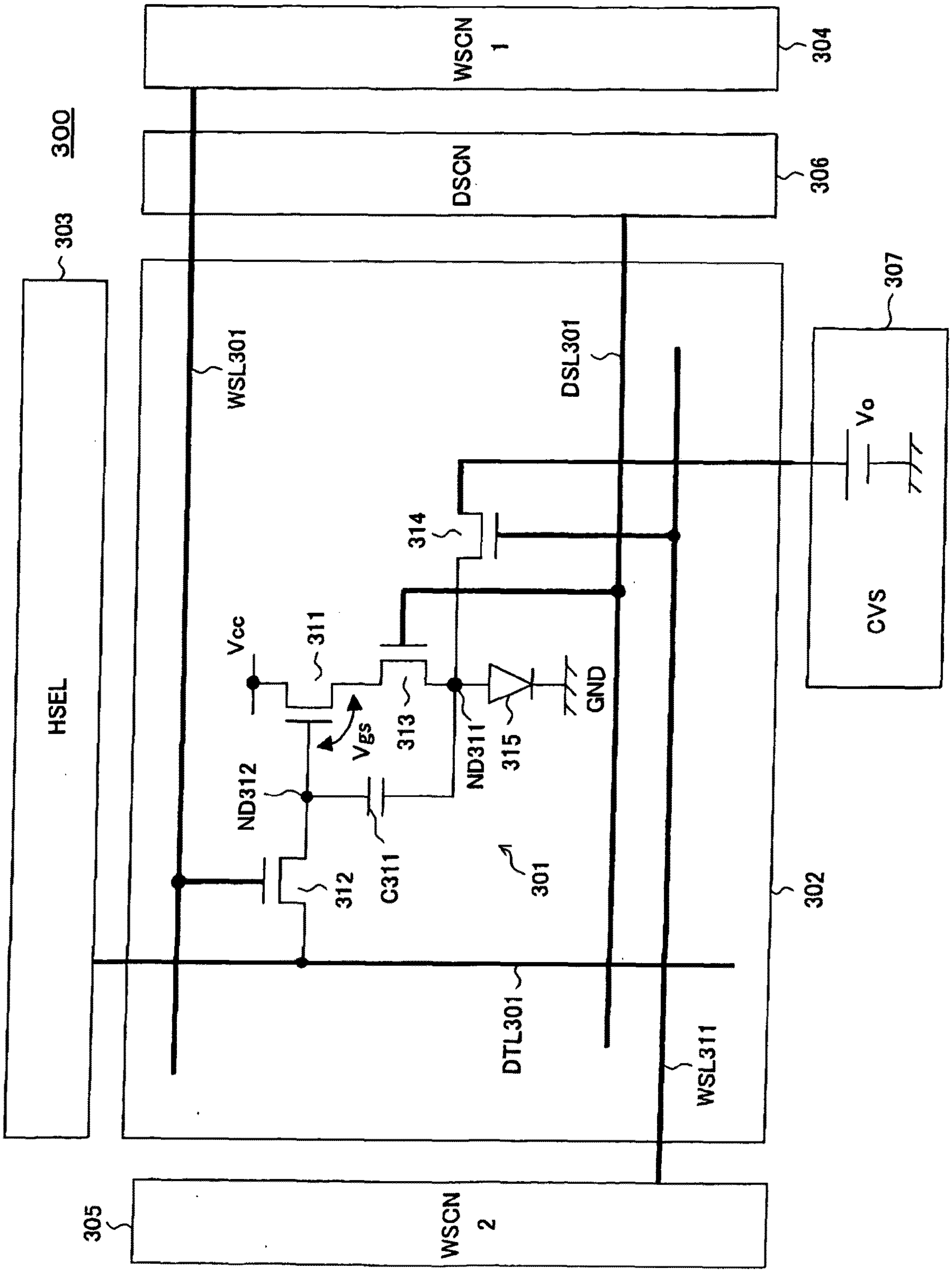

300
WSCN 1
304
WSL301
WSL 30m
DSCN
306
307
DSL301
DSL 30m
CVS
HSEL
PXLC
301
302
303
WSL 311
WSL31m
WSCN 2
305

FIG. 23


300
303
HSEL
WSCN
1
304
DSCN
306
WSL301
DSL301
307
Vo
CVS
314
Vcc
311
V_{GS}
313
ND312
ND311
315
GND
C311
312
301
302
DTL301
WSL311
305
WSCN
2

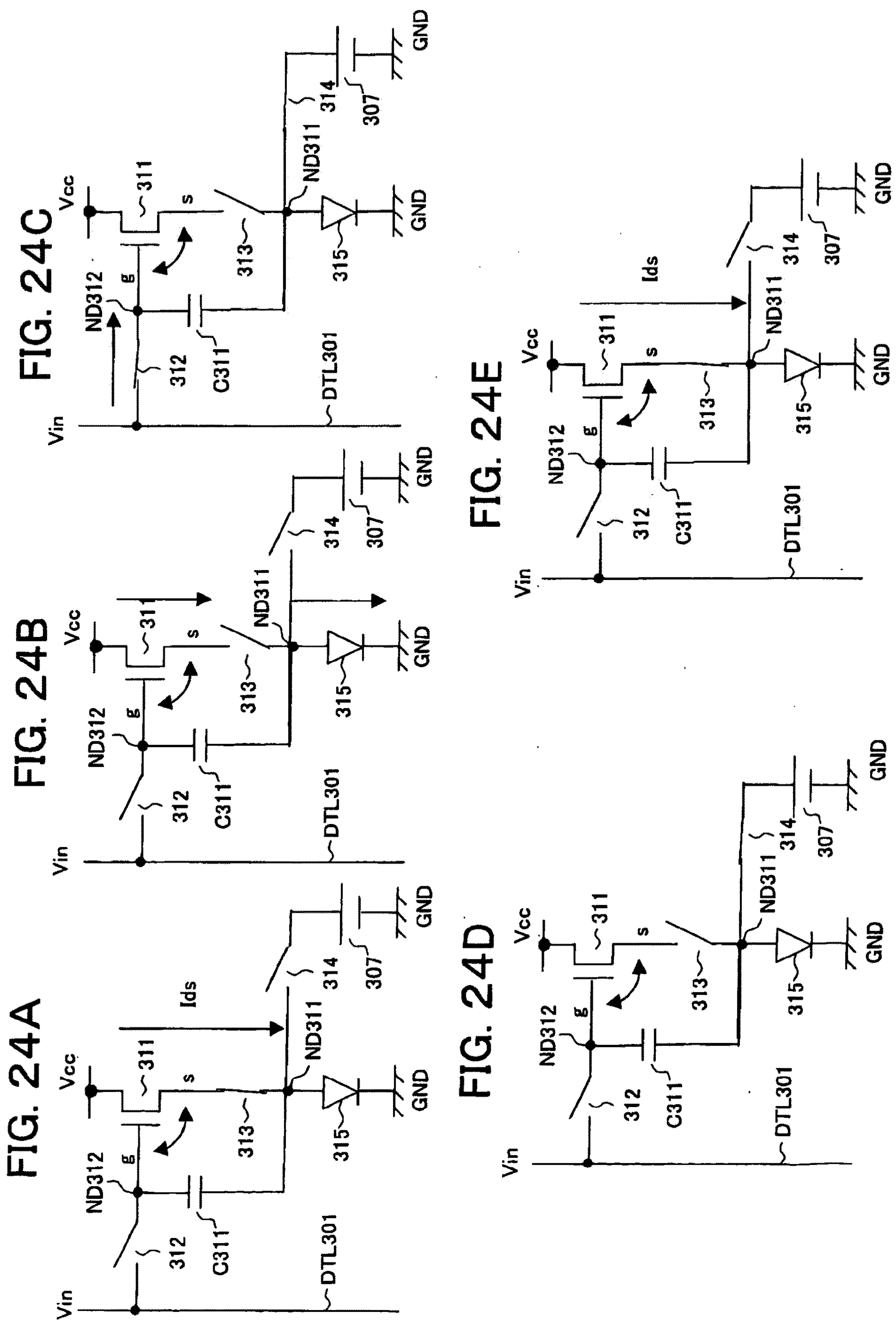


FIG. 24A

FIG. 24B

FIG. 24C

FIG. 24D

FIG. 24E

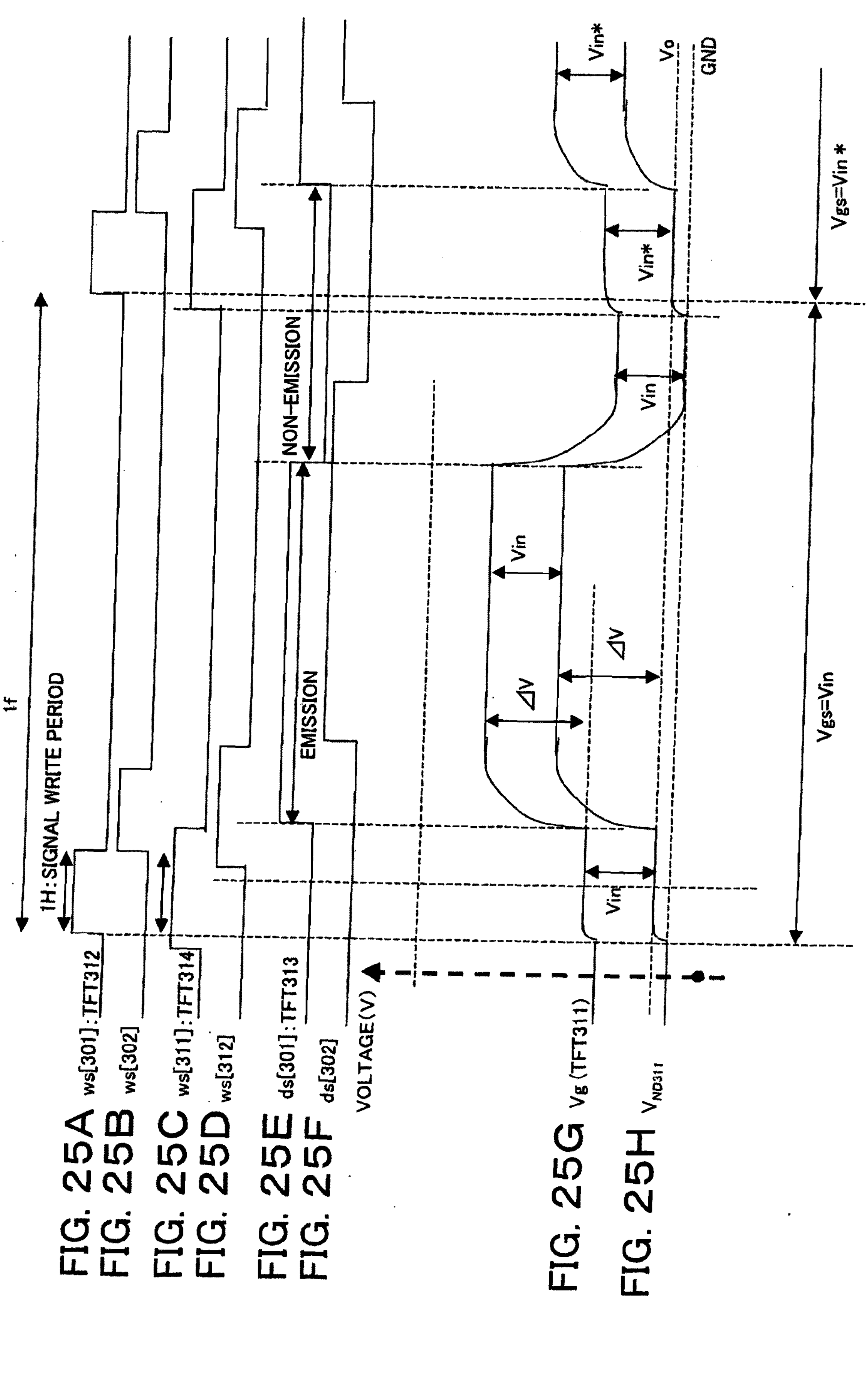


FIG. 25A FIG. 25B FIG. 25C FIG. 25D FIG. 25E FIG. 25F FIG. 25G FIG. 25H

FIG. 26

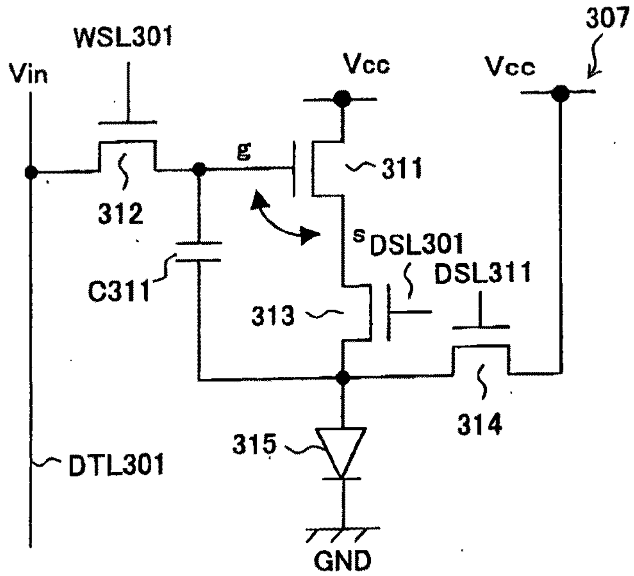

WSL301
Vin
Vcc
Vcc
307
g
311
312
s DSL301
DSL311
C311
313
314
315
DTL301
GND

FIG. 27

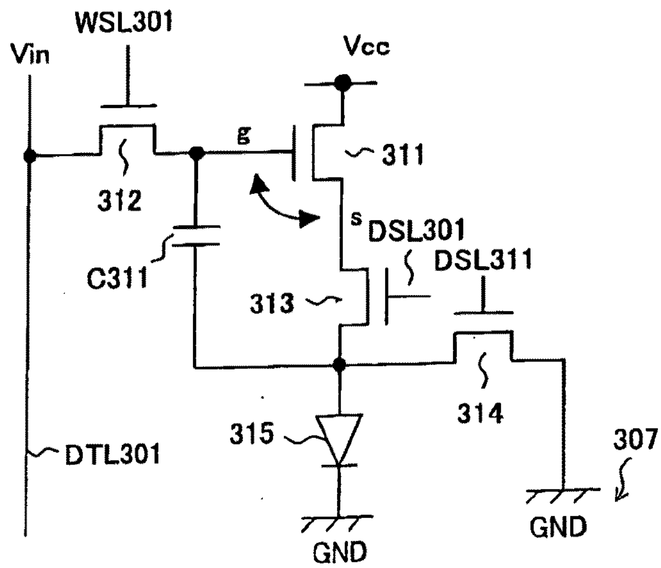

WSL301
Vin
Vcc
g
311
312
s DSL301
DSL311
C311
313
314
315
307
DTL301
GND
GND

FIG. 28

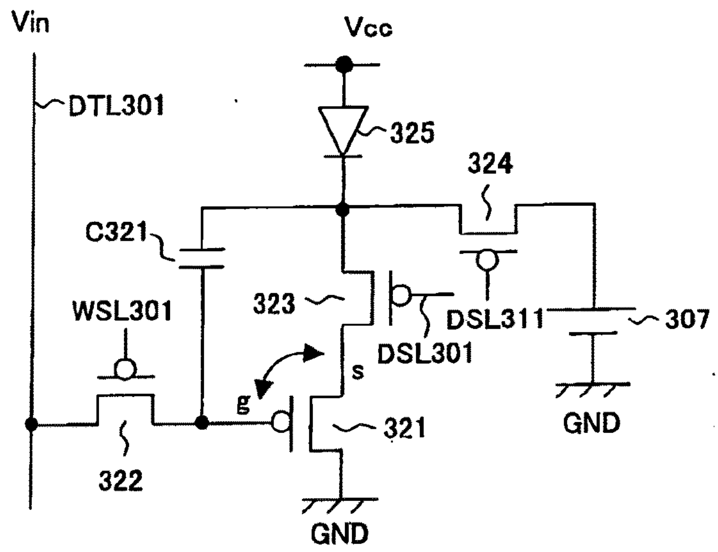

Vin
DTL301
Vcc
325
324
C321
323
WSL301
DSL311
307
DSL301
s
g
321
GND
322
GND

FIG. 29

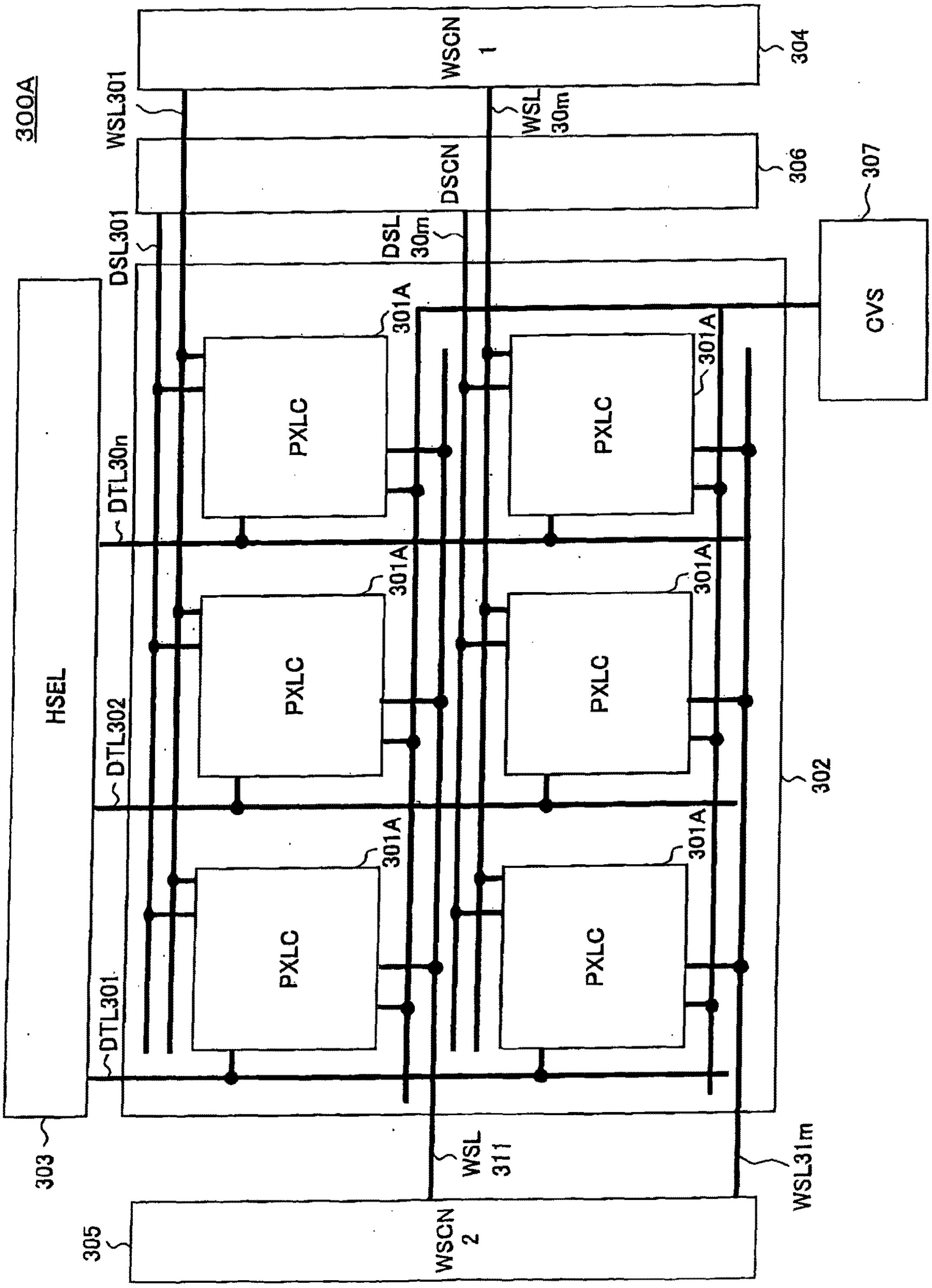

300A
WSCN 1
304
WSL301
WSL 30m
DSCN
306
307
DSL301
DSL 30m
CVS
HSEL
PXLC
301A
DTL30n
DTL302
DTL301
302
303
WSL 311
WSL31m
305
WSCN 2

FIG. 30

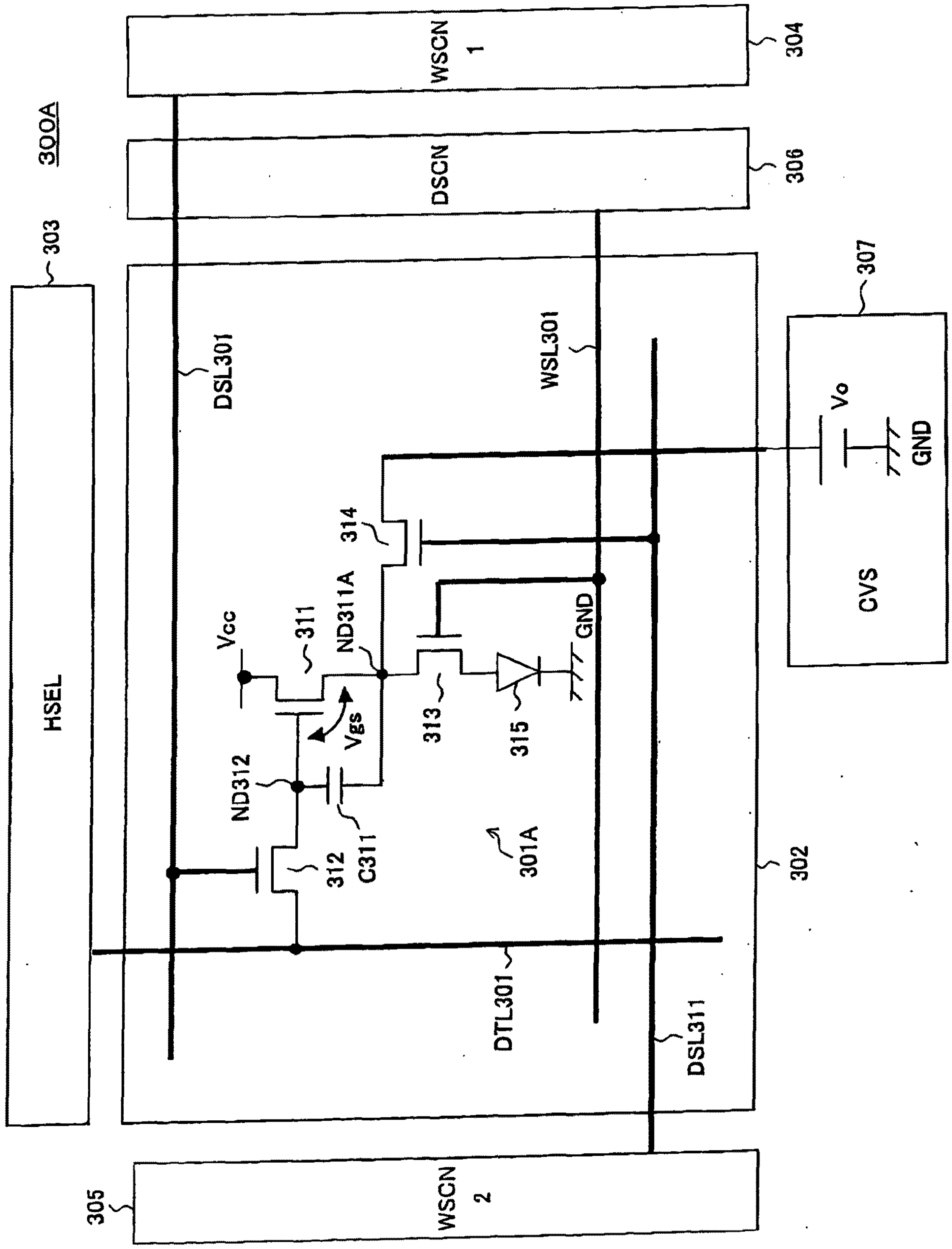

300A
HSEL
303
WSCN 1
304
DSCN
306
WSCN 2
305
302
CVS
307
Vo
GND
DSL301
WSL301
DTL301
DSL311
Vcc
311
ND311A
314
313
315
GND
Vgs
ND312
C311
312
301A

FIG. 31A

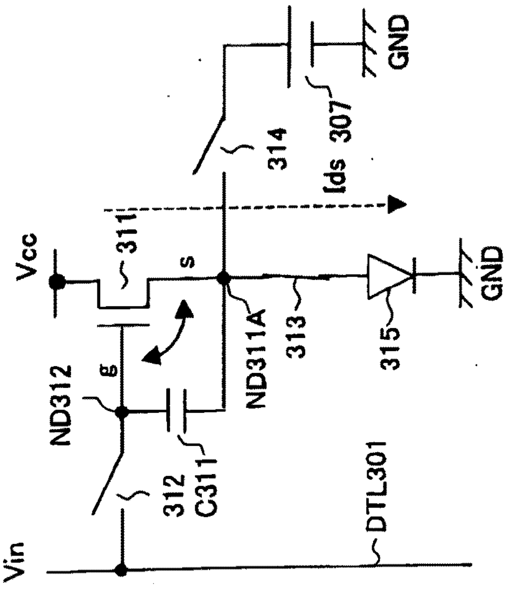


FIG. 31B

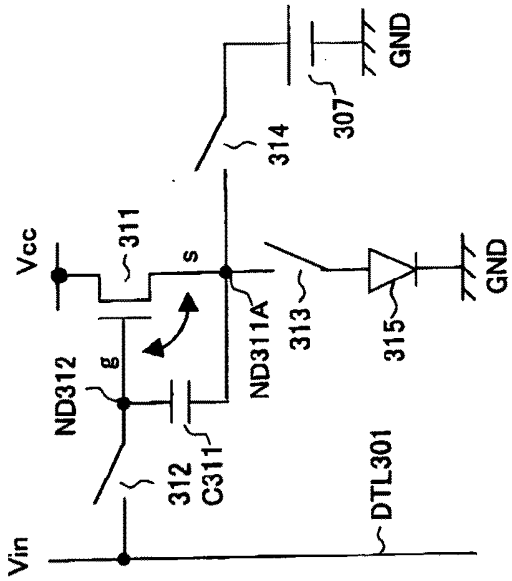


FIG. 31C

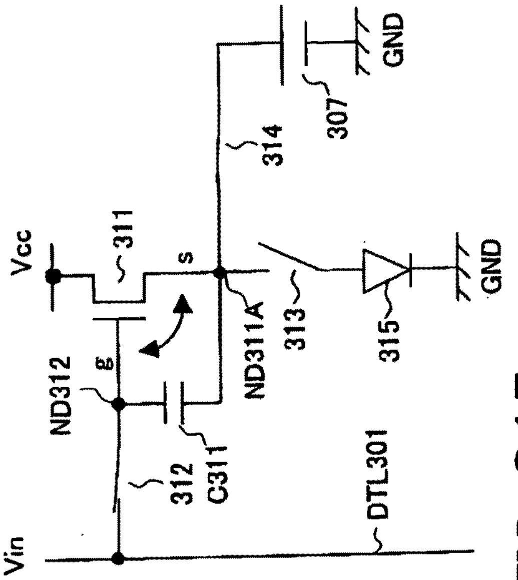


FIG. 31D

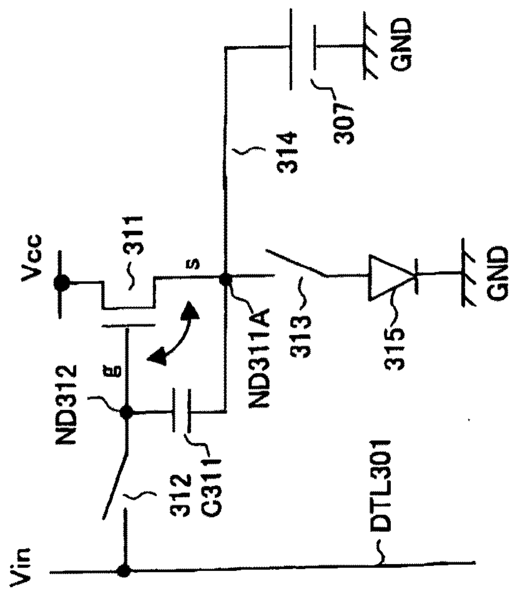
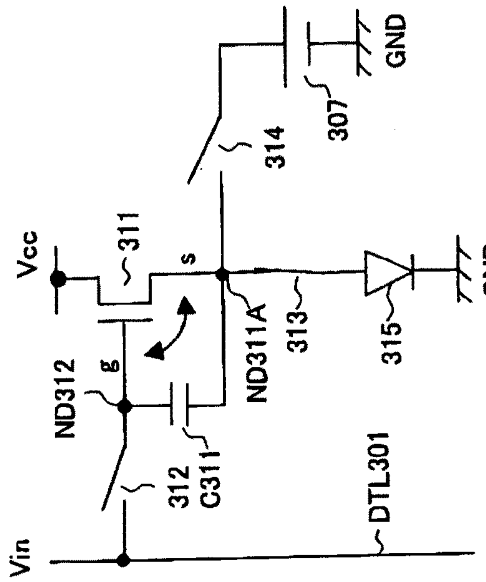


FIG. 31E



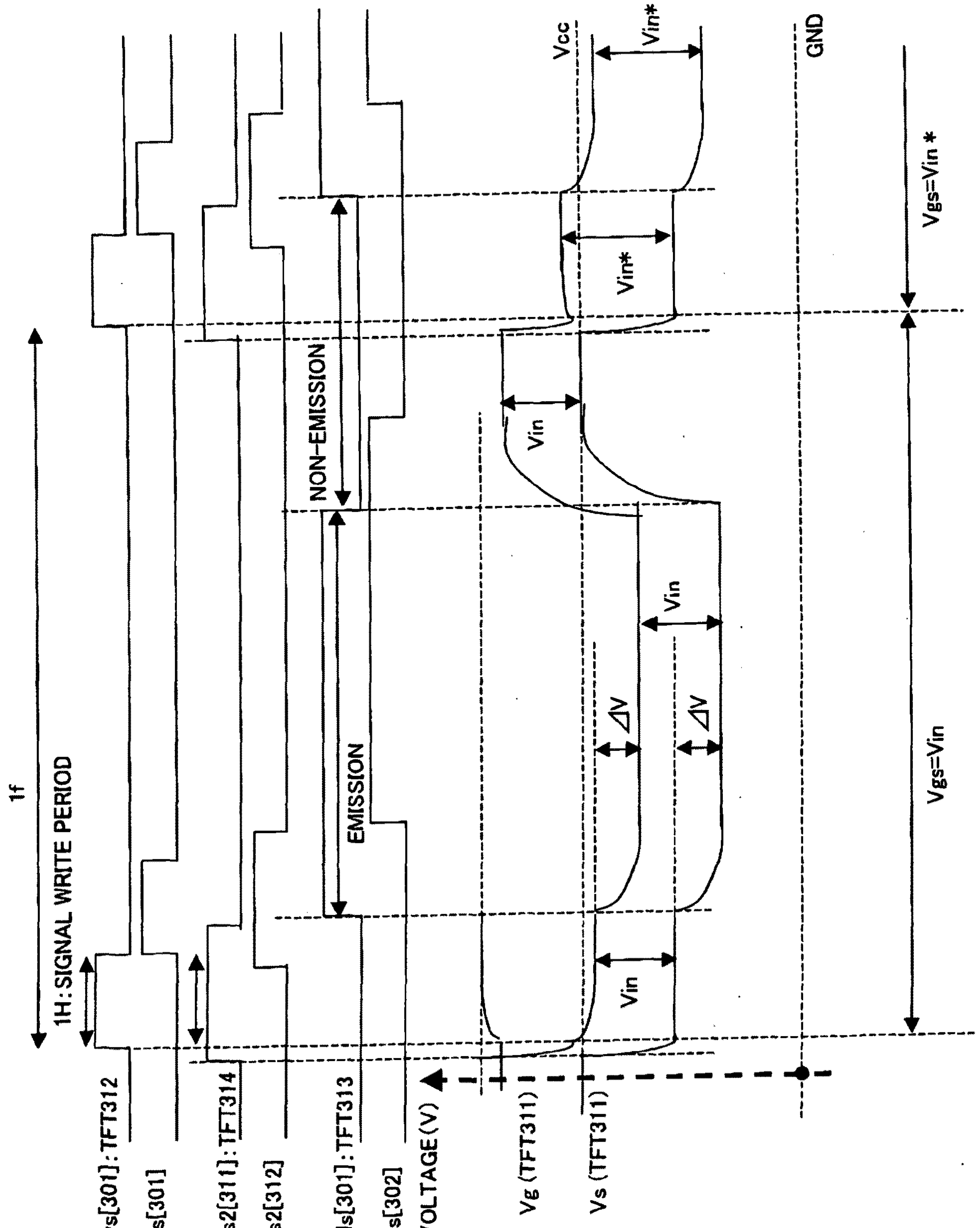


FIG. 32A
FIG. 32B
FIG. 32C
FIG. 32D
FIG. 32E
FIG. 32F
FIG. 32G
FIG. 32H

FIG. 33

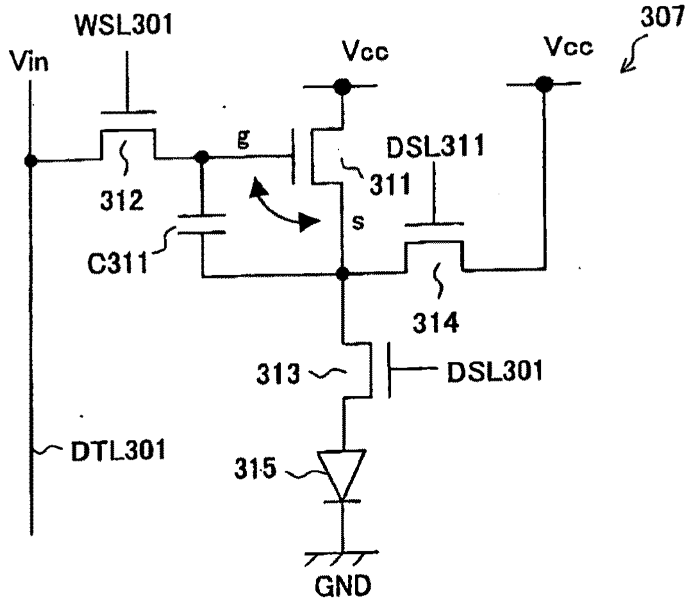

WSL301
Vin
Vcc
Vcc
307
g
DSL311
311
312
s
C311
314
313
DSL301
DTL301
315
GND

FIG. 34

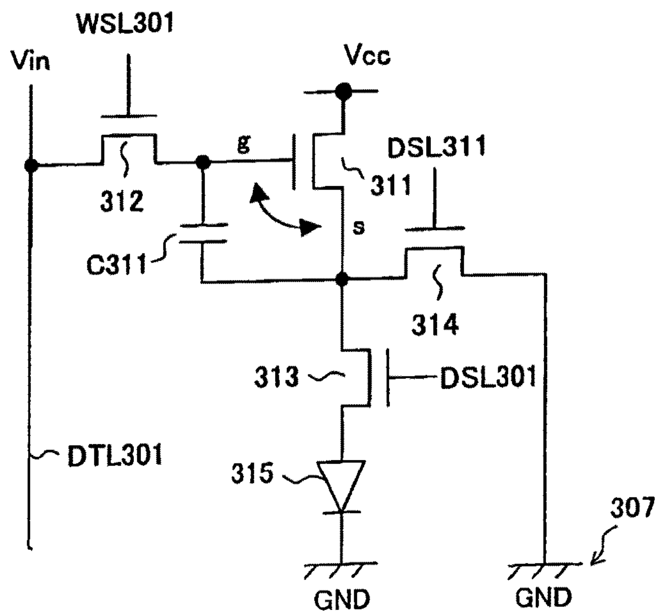

WSL301
Vin
Vcc
g
DSL311
311
312
s
C311
314
313
DSL301
DTL301
315
307
GND
GND

FIG. 35

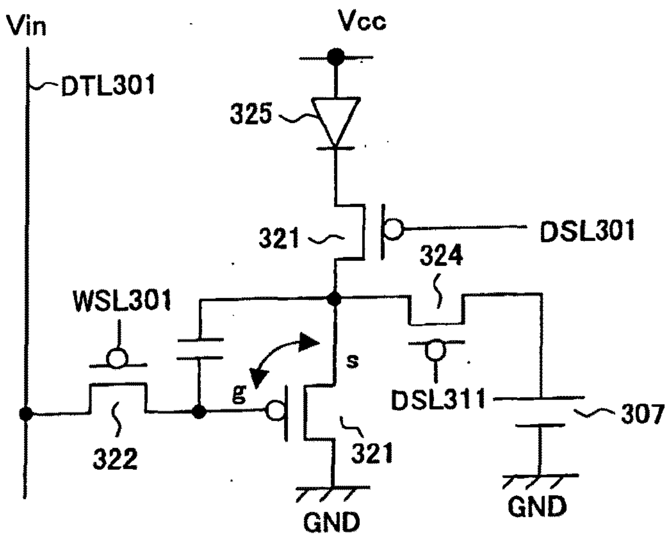
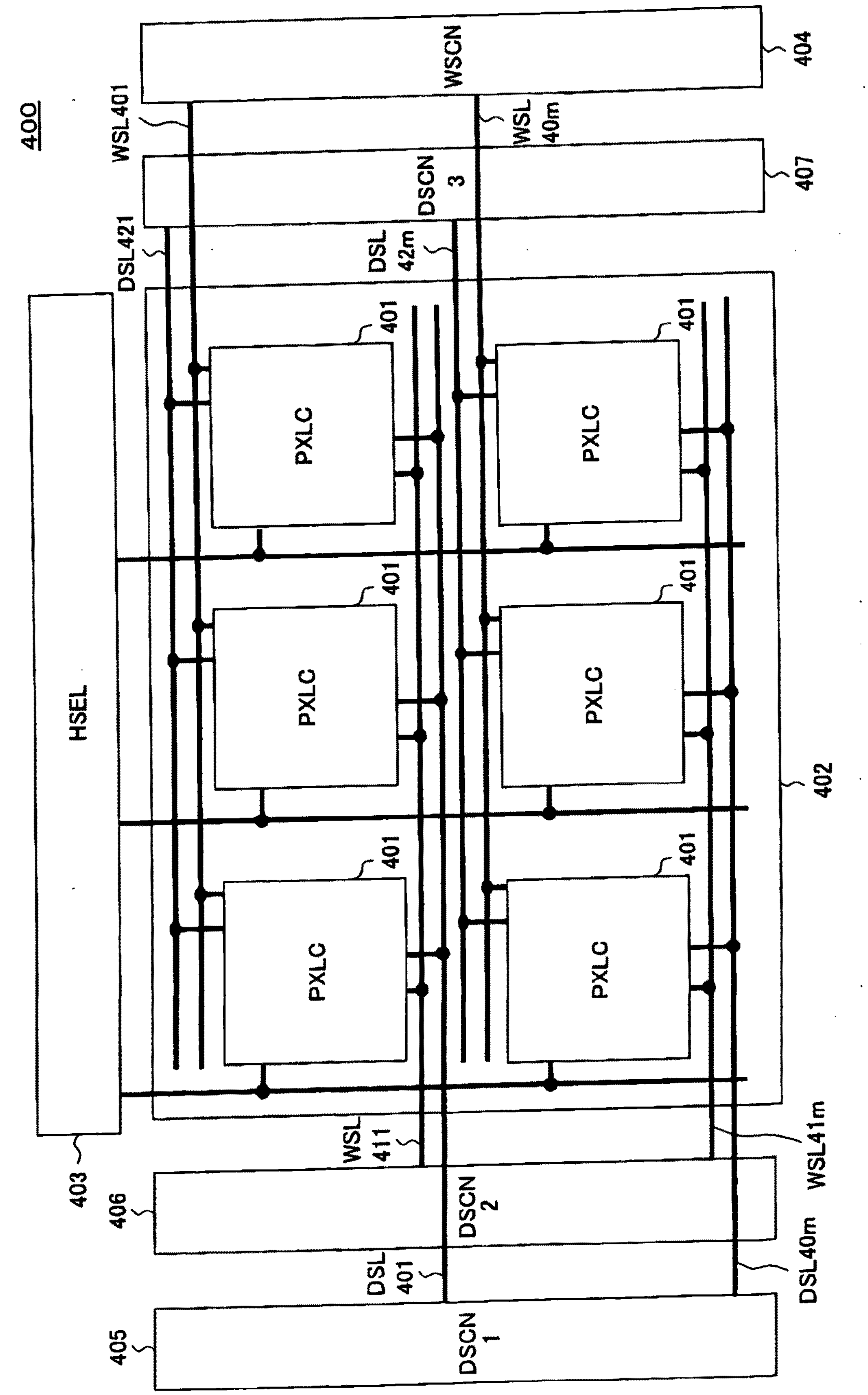

Vin
Vcc
DTL301
325
321
DSL301
324
WSL301
s
g
DSL311
307
322
321
GND
GND

FIG. 36


400
WSCN
404
WSL401
WSL 40m
DSCN 3
407
DSL421
DSL 42m
HSEL
401
PXLC
402
403
WSL 411
WSL41m
406
DSCN 2
DSL 401
DSL40m
405
DSCN 1

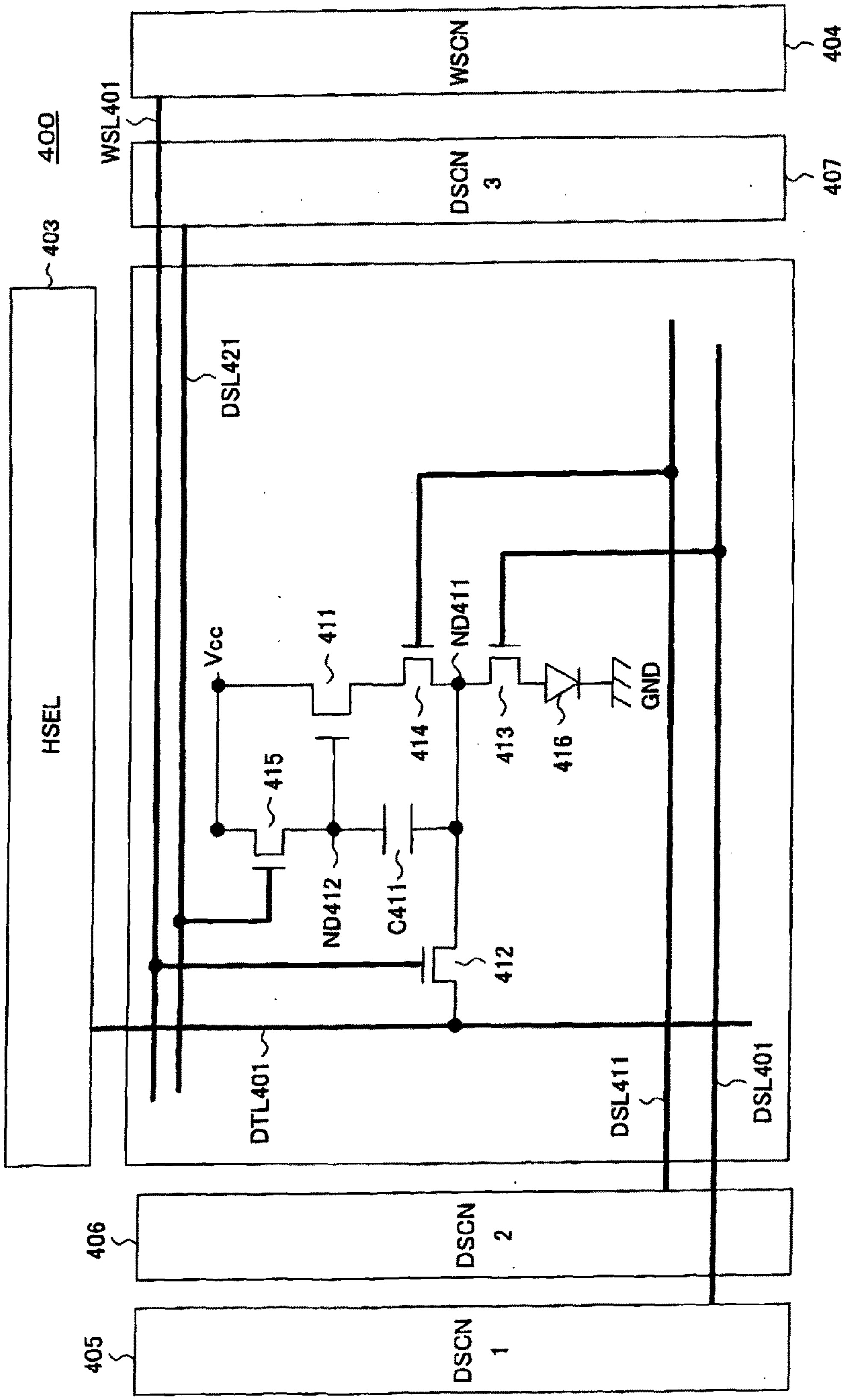

400
403
HSEL
WSCN
404
DSCN
3
407
WSL401
DSL421
Vcc
411
415
414
ND411
413
416
GND
ND412
C411
412
DTL401
DSL411
DSL401
DSCN
2
406
DSCN
1
405

FIG. 37

FIG. 38C

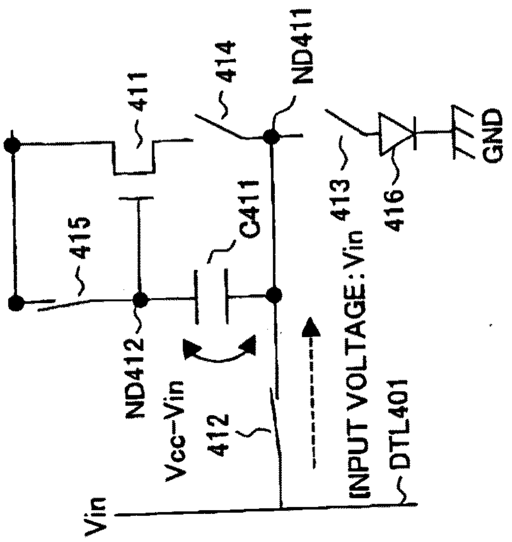


FIG. 38F

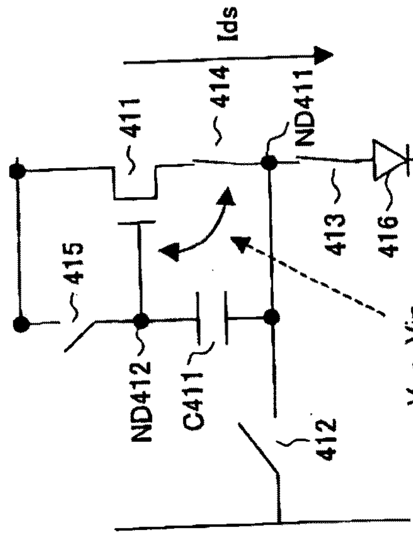


FIG. 38B

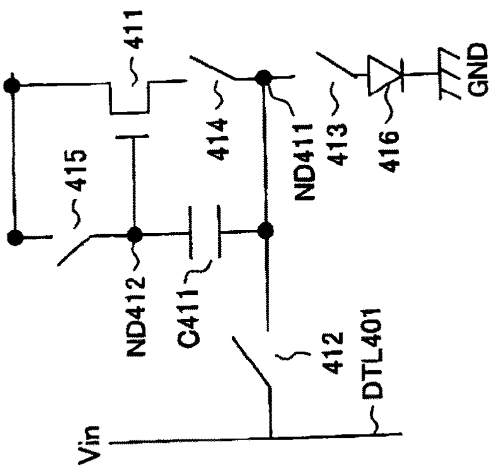


FIG. 38E

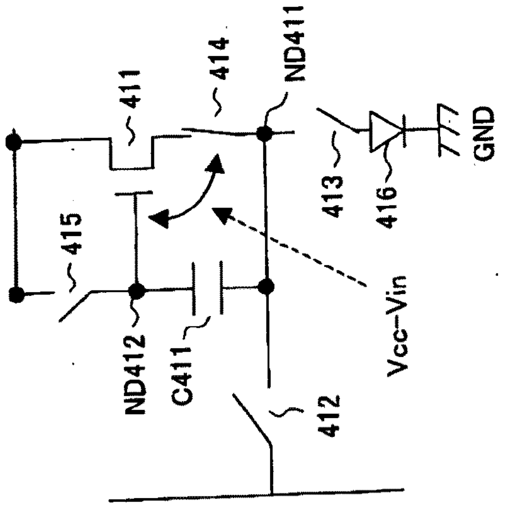


FIG. 38A

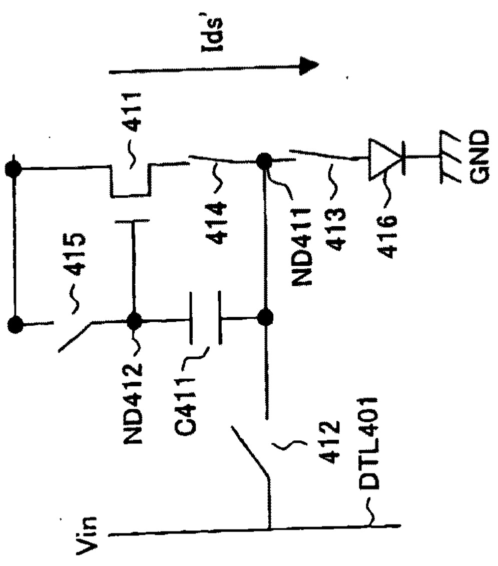


FIG. 38D

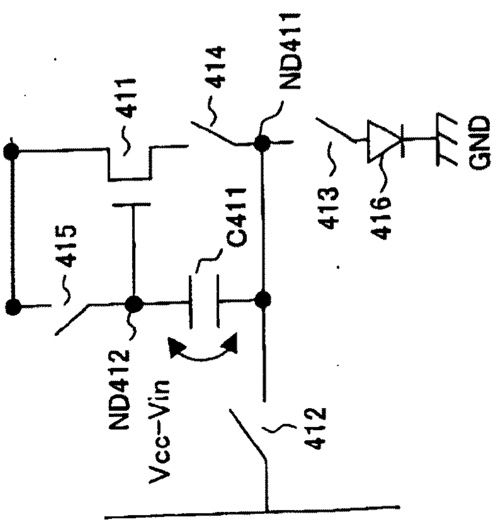
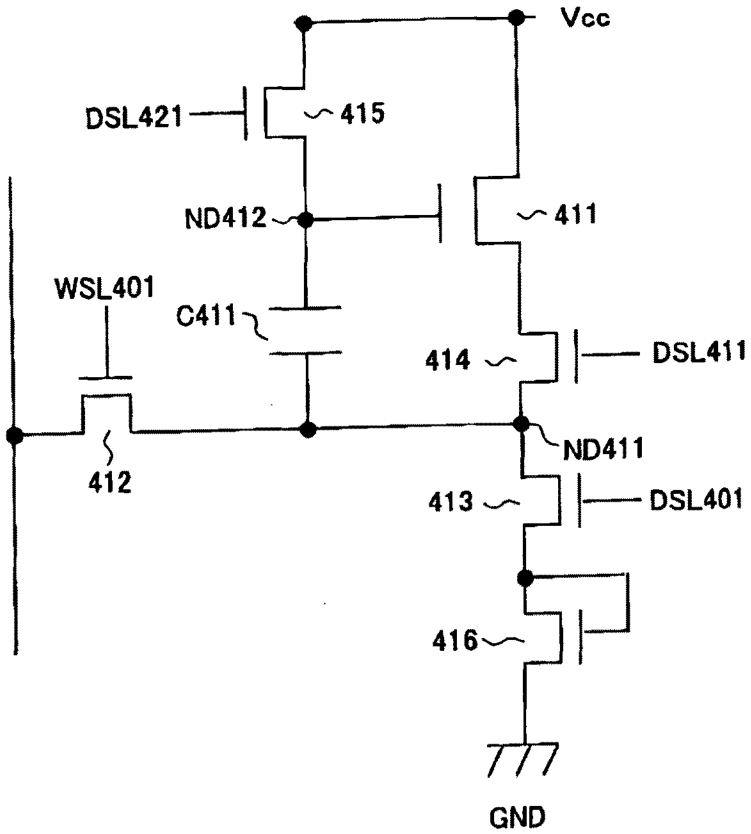


FIG. 39


Vcc
DSL421
415
ND412
411
WSL401
C411
414
DSL411
ND411
412
413
DSL401
416
GND

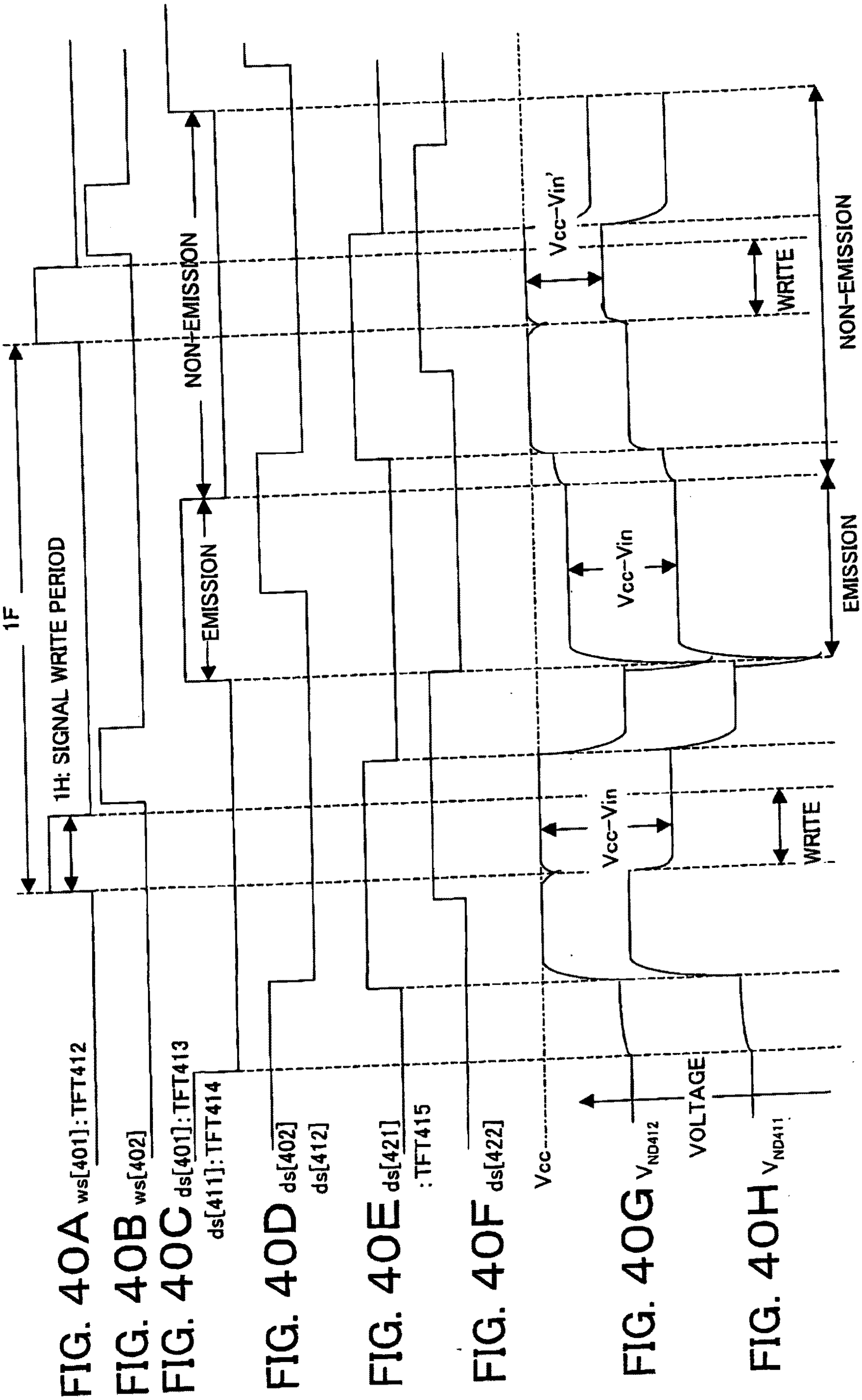


FIG. 40A ws[401]:TFT412
FIG. 40B ws[402]
FIG. 40C ds[401]:TFT413
ds[411]:TFT414
FIG. 40D ds[402]
ds[412]
FIG. 40E ds[421]
:TFT415
FIG. 40F ds[422]
Vcc
FIG. 40G V_ND412
VOLTAGE
FIG. 40H V_ND411
1F
1H: SIGNAL WRITE PERIOD
EMISSION
NON-EMISSION
Vcc−Vin
Vcc−Vin'
WRITE
WRITE
Vcc−Vin
EMISSION
NON-EMISSION

LIST OF REFERENCES

100... display device

101... pixel circuit (PXLC)

102... pixel array portion

103... horizontal selector (HSEL)

104... write scanner (WSCN)

105... drive scanner (DSCN)

DTL101 to DTL10n... data line

WSL101 to WSL10m... scanning line

DSL101 to DSL10m... drive line

111 to 113... TFT

114... light emitting element

ND111, ND112... node

200, 200A... display device

201, 201A... pixel circuit (PXLC)

202, 202A... pixel array portion

203... horizontal selector (HSEL)

204... write scanner (WSCN)

205... drive scanner (DSCN)

DTL201 to DTL210n... data line

WSL201 to WSL20m... scanning line

DSL201 to DSL20m... drive line

211 to 213... TFT

214... light emitting element

ND211, ND211A, ND212... node

300, 300A... display device

301, 301A... pixel circuit (PXLC)

302, 302A... pixel array portion

303... horizontal selector (HSEL)

304, 305... write scanner (WSCN)

306... drive scanner (DSCN)

DTL301 to DTL30n... data line

WSL301 to WSL30m, WSL311 to WSL31m... scanning line

DSL301 to DSL30m... drive line

311 to 314... TFT

ND311, ND311A, ND312... node

400... display device, 401... pixel circuit (PXLC)

402... pixel array portion

403... horizontal selector (HSEL)

404... write scanner (WSCN)

405 to 407... drive scanner (DSCN)

DTL401 to DTL40n... data line

WSL401 to WSL40m, DSL401 to DSL40m, DSL411 to DSL41m,

DSL421 to DSL42m... drive line

411 to 415... TFT

416... light emitting element

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- US 5684365 A **[0009]**
- US 8234683 B **[0009]**
- US 20030090446 A1 **[0040]**

专利名称(译)	像素电路，显示装置和驱动像素电路的方法		
公开(公告)号	EP2996108B1	公开(公告)日	2018-07-18
申请号	EP2015192807	申请日	2004-05-21
[标]申请(专利权)人(译)	索尼公司		
申请(专利权)人(译)	索尼公司		
当前申请(专利权)人(译)	索尼公司		
[标]发明人	UCHINO KATSUHIDE YAMASHITA JUNICHI YAMAMOTO TETSURO		
发明人	UCHINO, KATSUHIDE YAMASHITA, JUNICHI YAMAMOTO, TETSURO		
IPC分类号	G09G3/3233 H01L51/50 G09G3/20 G09G3/30 H01L21/8234 H01L27/06 H01L27/088 H01L29/786 H03K17/687 H05B33/14		
CPC分类号	G09G3/3233 G09G2300/043 G09G2300/0809 G09G2300/0819 G09G2300/0842 G09G2300/0861 G09G2310/0256 G09G2320/0233 G09G2320/043 G09G3/30 G09G3/3258 G09G3/3426 G09G3/36 G09G3/3648 G09G2320/045 H05B45/60		
代理机构(译)	WITTE，WELLER＆PARTNER专利律师MBB		
优先权	2003146758 2003-05-23 JP PCT/JP2004/007304 2004-05-21 WO		
其他公开文献	EP2996108A2 EP2996108A3		
外部链接	Espacenet		

摘要(译)

一种像素电路，显示装置和驱动像素电路的方法，即使随着发光元件的电流 - 电压特性的改变，也能够在没有亮度劣化的情况下实现源极跟随器输出，从而实现源极跟随器电路。 n沟道晶体管，并且能够在使用电流阳极 - 阴极电极的同时使用n沟道晶体管作为EL驱动晶体管，其中作为驱动晶体管的TFT 111的源极连接到发光元件114的阳极，漏极连接到电源电位VCC，电容器C111连接在TFT 111的栅极和源极之间，并且TFT 111的源极电位通过作为开关晶体管的TFT 113连接到固定电位。