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(54) **Organic light emitting diode display device and method for driving the same**

Organische lichtemittierende Diodenanzeigevorrichtung und Ansteuerungsverfahren dafür

Dispositif à diode d'affichage électroluminescent organique et son procédé de commande

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CN-A- 102 593 151 **US-A1- 2010 134 388**

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Description

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the priority benefit of the Korean Patent Application No. 10-2012-0152218 filed on December 24, 2012.

BACKGROUND

Field of the Invention

[0002] The present invention relates to a display device, and more particularly, to an organic light emitting diode (OLED) display device and a method of driving the same.

Discussion of the Related Art

[0003] With the advancement of information-oriented society, various requirements for display field are increasing, and thus, research is being done on various flat panel display devices that are thin and light, and have low power consumption. For example, the flat panel display devices are categorized into liquid crystal display (LCD) devices, plasma display panel (PDP) devices, OLED display devices, etc.

[0004] Especially, OLED display devices that are being actively studied recently apply data voltage (Vdata) having various levels to respective pixels to display different grayscale levels, thereby realizing an image.

[0005] To this end, each of a plurality of pixels includes one or more capacitors, an OLED, and a driving transistor that are current control elements. Especially, a current flowing in the OLED is controlled by the driving transistor, and the threshold voltage deviation of the driving transistor and the amount of a current flowing in the OLED are changed by various parameters, causing the luminance nonuniformity of a screen.

[0006] However, the threshold voltage deviation of the driving transistor occurs because the characteristic of the driving transistor is changed according to the manufacturing process variable of the driving transistor. To overcome this limitation, each pixel generally includes a compensation circuit that includes a plurality of transistors and capacitors for compensating for the threshold voltage deviation.

[0007] Recently, as consumers' requirements for high definition increase, a high-resolution OLED display device is demanded. To this end, it is necessary to integrate more pixels into an unit area for high resolution, and thus, it is required to reduce the numbers of transistors, capacitors, and lines included in the compensation circuit that compensates for a threshold voltage deviation.

[0008] US 2013/0169611 A1 discloses a pixel structure, driving method thereof and self-limiting display using the same. The pixel structure includes four transistors and two capacitors to compensate illuminating effect in both of a nonsynchronous display mode and a synchronous display mode.

[0009] US 2010/0134388 A1 discloses a method for efficiently compensating a threshold value of a driving transistor. In a state where a first switching transistor is non-conductive and a second switching transistor is conductive, a sampling transistor is made conductive and a reference voltage is supplied from a signal line to write a threshold voltage of a driving transistor to a first capacitance. After that, in a state where first and second switching transistors are non-conductive, the sampling transistor is made conductive and a signal voltage from the signal line is written to the first capacitance. Further, after that the sampling transistor is put into a nonconductive state, and the first and second switching transistors are put in a conductive state, to drive the driving transistor and supply current to a light emitting element.

SUMMARY

[0010] Accordingly, the present invention is directed to provide an organic light emitting diode (OLED) display device and a method of driving the same that substantially obviate one or more problems due to limitations and disadvantages of the related art.

[0011] An aspect of the present invention is directed to provide an OLED display device that can compensate for a threshold voltage deviation and a high-level source voltage deviation and is suitable for a large area, and a method of driving the same.

[0012] Additional advantages and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0013] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the present invention provides an OLED display device and a method of driving the OLED display device in accordance with the independent claims.

[0014] Further embodiments are described in the dependent claims.

[0015] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention. In the drawings:

FIG. 1 is a diagram schematically illustrating a configuration of an OLED display device according to embodiments of the present invention;
FIG. 2 is a diagram schematically illustrating an equivalent circuit of a sub-pixel of FIG. 1;
FIG. 3 is a timing chart of each of control signals supplied to the equivalent circuit of FIG. 2 according to a comparative example;
FIG. 4 is a timing chart showing in detail the timing chart of FIG. 3;
FIGS. 5A to 5D are diagrams for describing a method of driving the OLED display device;
FIG. 6 is a timing chart of each of control signals supplied to the equivalent circuit of FIG. 2 according to an embodiment of the present invention; and
FIG. 7 is a diagram for describing a change in a current due to a threshold voltage deviation of the OLED display device according to embodiments of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] Reference will now be made in detail to the exemplary embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0018] Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[0019] FIG. 1 is a diagram schematically illustrating a configuration of an OLED display device according to embodiments of the present invention.

[0020] As illustrated in FIG. 1, an OLED display device 100 according to embodiments of the present invention includes a panel 110, a timing controller 120, a scan driver 130, and a data driver 140.

[0021] The panel 110 includes a plurality of sub-pixels SP that are arranged in a matrix type. The sub-pixels SP included in the panel 110 emit light according to respective scan signals (which are supplied through a plurality of scan lines SL1 to SLm from the scan driver 130) and respective data signals that are supplied through a plurality of data lines DL1 to DLn from the data driver 140. Also, the emission of the sub-pixels SP may be controlled by the scan signal, data signals, a plurality of first emission control signals supplied from the scan driver 130 through a plurality of first emission control lines (not shown), and a plurality of second emission controls signal supplied from the scan driver 130 through a plurality of second emission control lines (not shown).

[0022] To this end, one sub-pixel includes an OLED, and a plurality of transistors and capacitors for driving the OLED. The detailed configuration of each of the sub-pixels SP will be described in detail with reference to FIG. 2.

[0023] The timing controller 120 receives a vertical sync signal Vsync, a horizontal sync signal Hsync, a data enable signal DE, a clock signal CLK, and video signals from the outside. Also, the timing controller 120 aligns external input video signals to digital image data RGB in units of a frame.

[0024] For example, the timing controller 120 controls the operational timing of each of the scan driver 130 and the data driver 140 with a timing signal that includes the vertical sync signal Vsync, the horizontal sync signal Hsync, the data enable signal DE, and the clock signal CLK.

[0025] To this end, the timing controller 120 generates a gate control signal GCS for controlling the operational timing of the scan driver 130 and a data control signal DCS for controlling the operational timing of the data driver 140.

[0026] The scan driver 130 generates a scan signal "Scan" that enables the operations of transistors included in each of the sub-pixels SP included in the panel 110, according to the gate control signal GCS supplied from the timing controller 120, and supplies the scan signal "Scan" to the panel 110 through the scan lines SL. Also, the scan driver 130 generates the first and second emission control signals Em and H as a type of scan signal, and supplies the first and second emission control signals Em and H to the panel 100 through the respective first and second emission control lines (not shown). Hereinafter, a scan signal applied through an nth scan line of the scan lines is assumed as a scan signal Scan[n].

[0027] The data driver 140 generates data signals with the digital image data RGB and the data control signal DCS that are supplied from the timing controller 120, and supplies the generated data signals to the panel 110 through the respective data lines DL.

[0028] Hereinafter, the detailed configuration of each sub-pixel will be described in detail with reference to FIGS. 1 and 2.

[0029] FIG. 2 is a diagram schematically illustrating an equivalent circuit of a sub-pixel of FIG. 1.

[0030] As illustrated in FIG. 2, each sub-pixel SP may include first to third transistors T1 to T3, a driving transistor Tdr, first and second capacitors C1 and C2, and an organic light emitting diode (OLED).

[0031] The first to third transistors T1 to T3 and the driving transistor Tdr, as illustrated in FIG. 2, are PMOS transistors, but are not limited thereto. As another example, an NMOS transistor may be applied thereto, in which case a voltage for turning on the PMOS transistor has a polarity opposite to that of a voltage for turning on the NMOS transistor.

[0032] First, a data voltage Vdata or a reference voltage Ref is applied to a source of the first transistor T1, the scan signal Scan[n] is applied to a gate of the first transistor T1, and a drain of the first transistor T1 is connected to a first node N1 which is a gate of the driving transistor Tdr.

[0033] For example, the data voltage Vdata or the reference voltage Ref may be applied to the source of the first transistor T1 through a data line DL, and an operation of the first transistor T1 may be controlled according to the scan signal Scan[n] supplied through a scan line SL.

[0034] Therefore, the first transistor T may be turned on according to the scan signal Scan[n], and supply the data voltage Vdata or the reference voltage Ref to the first node N1.

[0035] Here, the reference voltage Ref may be a direct current (DC) voltage having a constant level, and a plurality of the data voltages Vdata may be different successive voltages which are applied at three horizontal periods (3H). For example, when an n-1st data voltage Vdata[n-1] is applied to the source of the first transistor T1 during one horizontal period (1H), the reference voltage Ref may be applied to the source of the first transistor T1 during the next two horizontal periods (2H), and then, an nth data voltage Vdata[n] may be applied to the source of the first transistor T1 during the next one horizontal period (1H), and in succession, successive data voltages may be continuously applied to the source of the first transistor T1 at three horizontal periods (3H).

[0036] When the reference voltage Ref is applied to the first node N1, the reference voltage Ref may initialize the first node N1, which is the gate of the driving transistor Tdr, to the reference voltage Ref.

[0037] A high-level source voltage VDD may be applied to a third node N3 that is a source of the second transistor T2, a first emission control signal Em[n] may be applied to a gate of the second transistor T2, and a drain of the second transistor T2 may be connected to a second node N2 that is a source of the driving transistor Tdr.

[0038] For example, when the high-level source voltage VDD is applied to the third node N3 and the second transistor T2 is turned on according to the first emission control signal Em[n] supplied through a first emission control line, the third node N3 may be connected to the second node N2, and thus, the high-level source voltage VDD maybe applied to the second node N2.

[0039] The first capacitor C1 may be connected between the first and second nodes N1 and N2.

[0040] For example, the first capacitor C1 may sense a threshold voltage "Vth" of the driving transistor Tdr, and specifically, the first capacitor C1 may store the threshold voltage of the driving transistor Tdr.

[0041] The second capacitor C2 may be connected between the second node N2 and the third node N3 receiving the high-level source voltage VDD.

[0042] For example, when the second transistor T2 is turned off by the first emission control signal Em[n] and thus the third node N3 is disconnected from the second node N2, the high-level source voltage VDD may be continuously applied to one end of the second capacitor C2.

[0043] The gate of the driving transistor Tdr may be connected to the first node N1, the source of the driving transistor Tdr may be connected to the second node N2, and a drain of the driving transistor Tdr may be connected to a fourth node N4.

[0044] The amount of a current flowing in the below-described organic light emitting diode (OLED) may be decided by the sum "Vsg+Vth" of a source-gate voltage "Vsg" of the driving transistor Tdr and the threshold voltage "Vth" of the driving transistor Tdr, and finally decided by a compensation circuit with the data voltage Vdata and the reference voltage Ref.

[0045] Therefore, since the amount of a current flowing in the OLED is proportional to the level of the data voltage Vdata, the OLED display device according to embodiments of the present invention applies various levels of data voltages Vdata to respective sub-pixels SP to realize different gray scales, thereby displaying an image.

[0046] A second emission control signal H[n] may be applied to a gate of the third transistor T3, a source of the third transistor T3 may be connected to the fourth node N4 that is the drain of the driving transistor Tdr, and a drain of the third transistor T3 may be connected to a fifth node N5 that is an anode of the OLED.

[0047] For example, when the third transistor T3 is turned on according to the second emission control signal H[n] supplied through a second emission control line, the fourth node N4 may be connected to the fifth node N5, and thus, the OLED may emit light.

[0048] For example, when the third transistor T3 is turned off by the second emission control signal H[n], the OLED may be turned off, and, when the third transistor T3 is turned on, the emission of the OLED may be controlled by the scan signal Scan[n] and the first emission control signal Em[n].

[0049] In this example, the second emission control signal H[n] may be a separate emission control signal different from the first emission control signal Em[n], but, when the first emission control signal is an nth first emission control signal Em[n], the second emission control signal H[n] maybe an n+1st first emission control signal Em[n+1].

[0050] The anode of the OLED may be connected to the fifth node N5, and a low-level source voltage VSS may be applied to a cathode of the OLED.

[0051] Hereinafter, the operation of each sub-pixel included in the OLED display device will be described in detail with reference to FIGS. 3 and 5A to 5D.

[0052] FIG. 3 is a timing chart of each of control signals supplied to the equivalent circuit of FIG. 2 according to a comparative example.

[0053] As shown in FIG. 3, the OLED display device may fall into an initial period t1, a sensing period t2, a sampling period t3, and an emission period t4, and operate during the respective periods t1 to t4. According to the comparative example, each of the initial period t1, sensing period t2, and sampling period t3 may be one horizontal period (1H).

[0054] Hereinafter, as illustrated in FIGS. 5A to 5D, the value of a high-level source voltage applied to the third node N3 is changed by IR drop caused by the resistance of a line through which the high-level source voltage is transferred, during each of the periods t1 to t4, and thus, it is assumed that high-level source voltages VDD1 to VDD4 applied during the respective periods t1 to t4 have different values.

[0055] During the initial period t1, as shown in FIG. 3, the scan signal Scan[n] having a low level and the first and second emission control signals Em[n] and H[n] may be applied to a sub-pixel, and the reference voltage Ref may be applied to the source of the first transistor T1 through the data line.

[0056] Therefore, as illustrated in FIG. 5A, the first transistor T1 may be turned on by the scan signal Scan[n] having a low level, the second transistor T2 may be turned on by the first emission control signal Em[n] having a low level, and the third transistor T3 may be turned on by the second emission control signal H[n] having a low level.

[0057] Moreover, since the first transistor T1 is turned on, the reference voltage Ref may be supplied to the first node N1 that is the source of the first transistor T1 through the data line, and the voltage of the first node N1 may be initialized to the reference voltage Ref. Furthermore, since the second transistor T2 is turned on, the high-level source voltage VDD1 applied to the third node N3 that is the source of the second transistor T2 may be supplied to the second node N2 that is the source of the driving transistor Tdr. Also, as the third transistor T3 is turned on, the fourth node N4 may be connected to the fifth node N5.

[0058] For example, during the initial period t1, as the fourth node N4 is connected to the fifth node N5, a current flows in the OLED, but, since the initial period t1 is a very short period equal to one horizontal period (1H), light emitted from the OLED may be invisible to a viewer's eyes. The voltage of the first node N1 that is the gate of the driving transistor Tdr may merely be initialized to the reference voltage Ref.

[0059] As a result, during the initial period t1, as the third transistor T3 is turned on, a current may not flow in the OLED, but, since the first transistor T1 is turned on, the voltage of the first node N1 that is the gate of the driving transistor Tdr may be initialized to the reference voltage Ref that is a constant DC voltage.

[0060] Subsequently, during the sensing period t2, as shown in FIG. 3, the scan signal Scan[n] and second emission control signal H[n] having a low level and the first emission control signal Em[n] having a high level may be applied to the sub-pixel.

[0061] Therefore, as illustrated in FIG. 5B, the first transistor T1 may be turned on by the scan signal Scan[n] having a low level, the second transistor T2 may be turned off by the first emission control signal Em[n] having a high level, the third transistor T3 may be turned on by the second emission control signal H[n] having a low level, and the reference voltage Ref may be applied to the source of the first transistor T1 through the data line.

[0062] Moreover, as the first transistor T1 maintains a turn-on state, the reference voltage Ref may be supplied to the first node N1 that is the source of the first transistor T1 through the data line, and the voltage of the first node N1 may maintain the reference voltage Ref. Furthermore, since the second transistor T2 is turned off, a direct connection between the second and third nodes N2 and N3 may be broken, but the high-level source voltage VDD2 may be supplied to the third node N3 that is one end of the second capacitor C2. Also, as the third transistor T3 maintains a turn-on state, a connection between the fourth and fifth nodes N4 and N5 may be maintained.

[0063] For example, during the sensing period t2, although the voltage of the first node N1 maintains the reference voltage Ref, as the second transistor T2 is turned off, the direct connection between the second and third nodes N2 and N3 may be broken, and electric charges which are stored in the first and second capacitors C1 and C2 during the initial period t1 may be discharged, whereby the voltage of the second node N2 is more reduced to less than the high-level source voltage VDD1 that is the voltage of the second node N2 during the initial period t1.

[0064] As a result, during the sensing period t2, the voltage of the second node N2 may be reduced to less than the high-level source voltage VDD1, and then reduced up to a voltage "Ref + |Vth|" greater than the reference voltage Ref (which is the voltage of the first node N1 that is the gate of the driving transistor Tdr) by an absolute threshold voltage "|Vth|" of the driving transistor Tdr. Therefore, at a time when the sensing period t2 is completed, the threshold voltage "Vth" of the driving transistor Tdr may be stored in the first capacitor C1.

[0065] This reason is that since the driving transistor Tdr has a source-follower-type connection, the voltage of the second node N2 that is the source of the driving transistor Tdr is reduced, and then up to the voltage "Ref + |Vth|" greater than the reference voltage Ref (which is the voltage of the gate of the driving transistor Tdr which is a voltage until the driving transistor Tdr is turned off) by the absolute threshold voltage "|Vth|" of the driving transistor Tdr.

[0066] Therefore, during the sensing period t2, the first capacitor C1 may sense the threshold voltage "Vth" of the driving transistor Tdr.

[0067] Subsequently, during the sampling period t3, as shown in FIG. 3, the scan signal Scan[n] having a low level and the first and second emission control signals Em[n] and H[n] having a high level may be applied to the sub-pixel.

[0068] Therefore, as illustrated in FIG. 5C, the first transistor T1 may be turned on by the scan signal Scan[n] having a low level, the second and third transistors T2 and T3 may be turned off by the first and second emission control signals Em[n] and H[n] having a high level, and the data voltage Vdata may be applied to the source of the first transistor T1 through the data line.

[0069] Moreover, as the first transistor T1 is turned on, a data voltage Vdata[n] may be supplied to the first node N1 that is the source of the first transistor T1 through the data line. Furthermore, since the second transistor T2 maintains a turn-off state, the high-level source voltage VDD3 may be continuously supplied to the third node N3 that is one end of the second capacitor C2. Also, as the third transistor T3 is turned off, the fourth node N4 may be disconnected from the fifth node N5, and thus, the OLED may be turned off.

[0070] For example, during the sensing period t2, the reference voltage Ref may be supplied to the first node N1 that is one end of the first capacitor C1, and then, during the sampling period t3, as the data voltage Vdata[n] is supplied to the first node N1, the voltage of the second node N2 that is the other end of the first capacitor C1 may also be changed. However, since a voltage stored in the first capacitor C1 is maintained without any change and the first and second capacitors C1 and C2 are serially connected, the voltage of the second node N2 may be decided by a ratio of capacitances "c1" and "c2" of the first and second capacitors C1 and C2. Accordingly, the voltage of the second node N2 may be expressed as "Vdata[n] - [Ref + |Vth| + {c1/(c1 + c2)}(Vdata[n] - Ref)]" with the voltage "Ref + |Vth|" of the second node N2, a change "Vdata[n] - Ref" in the voltage of the first node N1, and a capacitance ratio "c1/(c1 + c2)" of the first and second capacitors C1 and C2. Therefore, a voltage "VC1" equal to a voltage "Vdata[n] - [Ref + |Vth| + {c1/(c1 + c2)} (Vdata[n] - Ref)]" may be stored in the first capacitor C1. To provide an additional description, the voltage "VC1" stored in the first capacitor C1 may become a voltage "{c2/(c1 + c2)}(Vdata[n] - Ref) - |Vth|".

[0071] Accordingly, since the capacitance ratio of the first and second capacitors C1 and C2 affects a current "Ioled" flowing in the below-described OLED, a case in which the current "Ioled" flowing in the OLED is peaked needs a voltage greater than a case in which the capacitance ratio does not affect the current "Ioled", and thus, the resolving power of the current "Ioled" flowing in the OLED due to a data voltage can be enhanced.

[0072] As a result, during the sampling period t3, the first capacitor C1 may sample a data voltage which is required for the OLED to emit light during the emission period t4.

[0073] According to the comparative example shown in FIG. 3, each OLED included in the OLED display device starts to emit light immediately after sampling of a corresponding scan line is completed in each frame.

[0074] In other words, an operation in which all the scan lines are scanned and immediately all OLEDs emit light will be described below in more detail with reference to FIG. 4.

[0075] FIG. 4 is a timing chart showing in detail the timing chart of FIG. 3. In the OLED display device, when it is assumed that the number of scan lines is m number, scan signals Scan[1], Scan[n] and Scan[m] are respectively applied to a first scan line, an nth scan line, and an mth scan line, and first to mth data voltages Vdata[1] to Vdata[m] are applied to one data line intersecting each scan line.

[0076] Here, a scan period for which a plurality of data voltages are applied to respective sub-pixels may include the initial period t1, the sensing period t2, the sampling period t3, and the emission period t4 for each scan line.

[0077] Thus, the OLED starts to emit light immediately after sampling of a corresponding data voltage is completed for each scan line.

[0078] During the emission period t4, as shown in FIG. 3, the scan signal Scan[n] having a high level and the first and second emission control signals Em[n] and H[n] having a low level may be applied to the sub-pixel.

[0079] Therefore, as illustrated in FIG. 5D, the first transistor T1 may be turned off by the scan signal Scan[n] having a high level, and the second and third transistors T2 and T3 may be respectively turned on by the first and second emission control signals Em[n] and H[n] having a low level, and the reference voltage Ref may be applied to the source of the first transistor T1 through the data line. However, since the first transistor T1 is turned off by the scan signal Scan[n] having a high level, the voltage of the first node N1 may not be changed. Also, since the second transistor T2 is turned on, as the high-level source voltage VDD4 is directly supplied to the third node N3 and the third transistor T3 is turned on, the fourth node N4 may be connected to the fifth node N5, and thus, the OLED may start to emit light.

[0080] Accordingly, the current Ioled flowing in the OLED may be decided with a current flowing in the driving transistor Tdr, and the current flowing in the driving transistor Tdr may be decided with the gate-source voltage (Vgs) of the driving transistor Tdr and the threshold voltage (Vth) of the driving transistor Tdr. The current Ioled may be defined as expressed in Equation (1). Also, the voltage of the first node N1 that is the gate of the driving transistor Tdr may become a voltage "VDD4 + {c2/(c1 + c2)}(Vdata[n] - Ref) - |Vth|" due to the voltage "VC1" which is stored in the first capacitor C1 during the sampling period t3.

$$
\begin{aligned}
Ioled &= K \times (Vgs - Vth)^2 \\
&= K \times (Vsg + Vth)^2 \\
&= K \times [VDD - VDD4 - \{c2/(c1+c2)\}(Vdata[n]-Ref) + |Vth| + Vth]^2 \\
&= K \times [\{c2/(c1+c2)\}(Vdata[n]-Ref) + |Vth| - |Vth|]^2 \\
&= K \times [\{c2/(c1+c2)\}(Vdata[n]-Ref)]^2 \qquad \ldots(1)
\end{aligned}
$$

where K denotes a proportional constant that is decided by the structure and physical properties of the driving transistor Tdr, and may be decided with the mobility of the driving transistor Tdr and the ratio "W/L" of the channel width "W" and length "L" of the driving transistor Tdr. Also, when the transistors included in the OLED are PMOS transistors, the threshold voltage of each of the transistors has a negative value. The threshold voltage "Vth" of the driving transistor Tdr does not always have a constant value, and the deviation of the threshold voltage "Vth" occurs according to the operational state of the driving transistor Tdr.

[0081] Referring to Equation (1), in the OLED display device, the current Ioled flowing in the OLED is not be affected by the threshold voltage "Vth" of the driving transistor Tdr during the emission period t4, and may merely be decided with a difference voltage between the the data voltage Vdata and the reference voltage Ref. The OLED display device is not affected by a high-level source voltage which is changed by IR drop caused by the resistance of a line through which the high-level source voltage is transferred.

[0082] In FIG. 3, it has been described above that an operation of each of the first to third transistors T1 to T3 may be controlled by the control signals such as the scan signal Scan[n] and the first and second emission control signals Em[n] and H[n], and data voltages may be applied to the respective sub-pixels at three horizontal periods (3H). In accordance with embodiments of the present invention, however, the second emission control signal H[n] may be the n+1st first emission control signal Em[n+1] next to the nth first emission control signal Em[n], and data voltages maybe applied to the respective sub-pixels at two horizontal periods (2H).

[0083] Hereinafter, control signals according to an embodiment of the present invention will be described with reference to FIG. 6.

[0084] FIG. 6 is a timing chart of each of control signals supplied to the equivalent circuit of FIG. 2 according to the embodiment of the present invention.

[0085] As shown in FIG. 6, it can be seen that a next data voltage is applied to a sub-pixel at two horizontal periods (2H) unlike the data voltage of FIG. 5, and moreover, the reference voltage Ref is applied to the sub-pixel at two horizontal periods (2H). Also, it can be seen that the second emission control signal "H[n]" is the n+1st first emission control signal "Em[n+1]".

[0086] As shown in FIG. 6, similarly to FIG. 5, the OLED display device according to embodiments of the present invention may fall into an initial period t1, a sensing period t2, a sampling period t3, and an emission period t4, and operate during the respective periods t1 to t4, Here, the sampling period t3 may be one horizontal period (1H), and the sum of the initial period t1 and the sensing period t2 may be one horizontal period (1H).

[0087] Accordingly, by compensating for the threshold voltage deviation caused by the operational state of the driving transistor and the high-level source voltage deviation caused by IR drop, the OLED display device according to the embodiments of the present invention can maintain a constant current flowing in each OLED, thus preventing the degradation of image quality.

[0088] Moreover, since the number of transistors and capacitors included in the compensation circuit is small, the OLED display device according to embodiments of the present invention can be suitable for a large area.

[0089] FIG. 7 is a diagram for describing a change in a current due to a threshold voltage deviation of the OLED display device according to embodiments of the present invention.

[0090] As show in FIG. 7, it can be seen that the level of the current Ioled flowing in the OLED is proportional to the data voltage Vdata, but the level of the current Ioled is not greatly changed according to a threshold voltage deviation "dVth" under the same data voltage Vdata.

[0091] According to the embodiments of the present invention, by compensating for the threshold voltage deviation caused by the operational state of the driving transistor and the high-level source voltage deviation caused by IR drop, a current flowing in each OLED can be maintained without any change, thus preventing the degradation of image quality.

Claims

1. An organic light emitting diode (OLED) display device comprising a plurality of sub-pixels (SP) arranged in an m×n matrix having m rows and n columns, each sub-pixel (SP) comprising:

a first transistor (T1) supplying a data voltage (Vdata) or a reference voltage (Ref) to a first node (N1) according to a scan signal (Scan);
a driving transistor (Tdr), the gate of the driving transistor (Tdr) being connected to the first node (N1), the source of the driving transistor (Tdr) being connected to a second node (N2), and the drain of the driving transistor (Tdr) being connected to a fourth node (N4);
a first capacitor (C1) connected between the first (N1) and second nodes (N2), and storing a threshold voltage of the driving transistor (Tdr);
a second capacitor (C2) connected between the second node (N2) and a third node (N3) that is the source of the second transistor (T2);
said second transistor (T2) supplying a high-level source voltage (VDD), applied to the third node (N3), to the second node (N2) according to a first emission control signal (Em) applied to the second transistor (T2);
an OLED emitting light with a current received from the driving transistor (Tdr) that is a function of the voltage difference between the data voltage (Vdata) and the reference voltage (Ref); and
a third transistor (T3) connecting the fourth node (N4) to a fifth node (N5) according to a second emission control signal (H) applied to the third transistor (T3), the fifth node (T5) being an anode of the OLED, **characterized in that** the OLED display device is configured such that the second emission control signal (H) applied to the third transistors (T3) of the sub-pixels (SP) disposed in the i-th row is at the same time the first emission control signal (Em) applied to the second transistors (T2) of the sub-pixels (SP) disposed in the (i+1)-th row, such that the signal timing of both signals is identical, and wherein $1 \leq i < m$.

2. The OLED display device of claim 1, wherein,

the first transistor (T1) is turned on by the scan signal (Scan) which is applied thereto through a scan line,
the second transistor (T2) is turned on by the first emission control signal (Em) which is applied thereto through a first emission control line, and
the third transistor (T3) is turned on by the second emission control signal (H) which is applied thereto through a second emission control line.

3. The OLED display device of any one of claims 1 to 2, wherein when the first to third transistors (T1, T2, T3) are turned on,
the reference voltage (Ref) is supplied to the first node (N1), the high-level source voltage (VDD) is supplied to the second node (N2), and the fourth node (N4) is connected to the fifth node (N5), such that the voltage of the first node (N1) is initialized to the reference voltage (Ref).

4. The OLED display device of claim 3, wherein when the first and third transistors (T1, T3) are turned on, and the second transistor (T2) is turned off,
the reference voltage (Ref) is supplied to the first node (N1), the fourth node (N4) is connected to the fifth node (N5), and the voltage of the second node (N2) is reduced to less than the high-level source voltage (VDD).

5. The OLED display device of claim 4, wherein the voltage of the second node (N2) is reduced up to a sum of the reference voltage (Ref) and an absolute threshold voltage of the driving transistor (Tdr).

6. The OLED display device of claim 4 or 5, wherein when the first transistor (T1) is turned on, and the second and third transistors (T2, T3) are turned off, the data voltage (Vdata) is supplied to the first node (N1).

7. The OLED display device of claim 6, wherein when the first transistor (T1) is turned off, and the second and third transistors (T2, T3) are turned on, the OLED emits light.

8. A method of driving the organic light emitting diode (OLED) display device according to claim 1, wherein each of the sub-pixels includes the first to third transistors (T1, T2, T3), the driving transistor (Tdr), the first and second capacitors (C1, C2), and the OLED, the method comprising:

initializing a voltage of a first node (N1) to a reference voltage (Ref), when the first to third transistors (T1, T2, T3) are turned on according to a scan signal (Scan) applied to the first transistor (T1), a first emission control signal (Em) applied to the second transistor (T2) and a second emission control signal (H) applied to the third transistor (T3), the first node (N1) being the gate of the driving transistor (Tdr);
storing a threshold voltage of the driving transistor (Tdr) in the first capacitor (C1) connected to a second node (N2) that is the source of the driving transistor (Tdr), when the voltage at the first node (N1) is the reference voltage (Ref) and the first and third transistors (T1, T3) are turned on and the second transistor (T2) is turned off according to the scan signal (Scan) applied to the first transistor (T1), the first emission control signal (Em) applied to the second transistor (T2) and the second emission control signal (H) applied to the third transistor (T3), the other end of the first capacitor (C1) being connected to the first node (N1);
supplying the data voltage (Vdata) to the first node (N1), when the first transistor (T1) is turned on and the second and third transistors (T2, T3) are turned off according to the scan signal (Scan) applied to the first transistor (T1), the first emission control signal (Em) applied to the second transistor (T2) and the second emission control signal (H) applied to the third transistor (T3); and
emitting, by the OLED, light with a current received from the driving transistor (Tdr) that is a function of the voltage difference between the data voltage (Vdata) and the reference voltage (Ref) when the first transistor (T1) is turned off and the second and third transistors (T2, T3) are turned on according to the scan signal (Scan) applied to the first transistor (T1), the first emission control signal (Em) applied to the second transistor (T2) and the second emission control signal (H) applied to the third transistor (T3),
wherein the OLED display device is configured such that the second emission control signal (H) applied to the third transistors (T3) of the sub-pixels (SP) disposed in the i-th row is at the same time the first emission control signal (Em) applied to the second transistors (T2) of the sub-pixels (SP) disposed in the (i+1)-th row, such that the signal timing of both signals is identical, and wherein $1 \leq i < m$.

9. The method of claim 8, wherein the initializing of a voltage comprises:

supplying a high-level source voltage (VDD) to the second node (N2); and
connecting a fourth node (N4) to a fifth node (N5), the fourth node (N4) being a drain of the driving transistor (Tdr), and the fifth node (T5) being an anode of the OLED.

10. The method of claim 8 or 9, wherein the storing of a threshold voltage comprises:

supplying the reference voltage (Ref) to the first node (N1); and
reducing a voltage of the second node (N2) to a sum of the reference voltage (Ref) and an absolute threshold voltage of the driving transistor (Tdr).

11. The method of any one of claims 8 to 10, wherein,
the source of the second transistor (T2) is connected to a third node (N3) receiving a high-level source voltage (VDD),
the drain of the second transistor (T2) is connected to the second node (N2), and
the second capacitor (C2) is connected between the second and third nodes (N2, N3).

12. The method of any one of claims 8 to 11, wherein the supplying of the data voltage (Vdata) comprises disconnecting a fourth node (N4) from a fifth node (N5), the fourth node (N4) being the drain of the driving transistor (Tdr), and the fifth node (N5) being an anode of the OLED.

13. The method of any one of claims 8 to 12, wherein,

the first transistor (T1) is turned on by the scan signal (Scan) which is applied thereto through a scan line (Scan),

the second transistor (T2) is turned on by the first emission control signal (Em) which is applied thereto through a first emission control line, and
the third transistor (T3) is turned on by the second emission control signal (H) which is applied thereto through a second emission control line.

Patentansprüche

1. Eine Organische-Leuchtdioden (OLED)-Anzeigevorrichtung, aufweisend eine Mehrzahl von Subpixeln (SP), die in einer m x n - Matrix angeordnet sind, welche m Reihen und n Spalten hat, wobei jedes Subpixel (SP) aufweist:

   einen ersten Transistor (T1), der eine Datenspannung (Vdata) oder eine Referenzspannung (Ref) an einen ersten Knoten (N1) bereitstellt entsprechend einem Scansignal (Scan);
   einen Treibertransistor (Tdr), wobei das Gate des Treibertransistors (Tdr) mit dem ersten Knoten (N1) verbunden ist, die Source des Treibertransistors (Tdr) mit einem zweiten Knoten (N2) verbunden ist, und der Drain des Treibertransistors (Tdr) mit einem vierten Knoten (N4) verbunden ist;
   einen ersten Kondensator (C1), der zwischen den ersten Knoten (N1) und den zweiten Knoten (N2) geschaltet ist und der eine Schwellenspannung des Treibertransistors (Tdr) speichert;
   einen zweiten Kondensator (C2), der zwischen den zweiten Knoten (N2) und einen dritten Knoten (N3), der die Source des zweiten Transistors (T2) ist, geschaltet ist;
   wobei der zweite Transistor (T2) eine Hochpegel-Source-Spannung (VDD), die an den dritten Knoten (N3) angelegt wird, an den zweiten Knoten (N2) bereitstellt gemäß einem ersten Emissionssteuersignal (Em), das an den zweiten Transistor (T2) angelegt wird;
   eine OLED, die Licht emittiert mit einem von dem Treibertransistor (Tdr) empfangenen Strom, der abhängig ist von der Spannungsdifferenz zwischen der Datenspannung (Vdata) und der Referenzspannung (Ref); und
   einen dritten Transistor (T3), welcher den vierten Knoten (N4) mit einem fünften Knoten (N5) verbindet entsprechend einem zweiten Emissionssteuersignal (H), welches an den dritten Transistor (T3) angelegt wird, wobei der fünfte Knoten (T5) eine Anode der OLED ist,
   dadurch gekennzeichnet, dass
   die OLED-Anzeigevorrichtung so konfiguriert ist, dass das zweite Emissionssteuersignal (H), das an die dritten Transistoren (T3) der Subpixel (SP), die in der i-ten Reihe angeordnet sind, angelegt wird, gleichzeitig das erste Emissionssteuersignal (Em) ist, das an die zweiten Transistoren (T2) der Subpixel (SP), die in der (i+1)-ten Reihe angeordnet sind, angelegt wird, sodass das Signal-Timing beider Signale identisch ist, und wobei $1 \leq i < m$.

2. Die OLED-Anzeigevorrichtung gemäß Anspruch 1, wobei,

   der erste Transistor (T1) von dem Scansignal (Scan) angeschaltet wird, welches daran über eine Scanleitung angelegt wird,
   der zweite Transistor (T2) von dem ersten Emissionssteuersignal (Em) angeschaltet wird, welches daran über eine erste Emissionssteuerleitung angelegt wird, und
   der dritte Transistor (T3) von dem zweiten Emissionssteuersignal (H) angeschaltet wird, welches daran über eine zweite Emissionssteuerleitung angelegt wird.

3. Die OLED-Anzeigevorrichtung gemäß irgendeinem der Ansprüche 1 bis 2, wobei, wenn der erste bis dritte Transistor (T1, T2, T3) angeschaltet werden,
   die Referenzspannung (Ref) an den ersten Knoten (N1) bereitgestellt wird, die Hochpegel-Source-Spannung (VDD) an den zweiten Knoten (N2) bereitgestellt wird und der vierte Knoten (N4) mit dem fünften Knoten (N5) verbunden wird, sodass die Spannung des ersten Knotens (N1) auf die Referenzspannung (Ref) initialisiert wird.

4. Die OLED-Anzeigevorrichtung gemäß Anspruch 3, wobei, wenn der erste und der dritte Transistor (T1, T3) angeschaltet werden und der zweite Transistor (T2) abgeschaltet wird,
   die Referenzspannung (Ref) an den ersten Knoten (N1) bereitgestellt wird, der vierte Knoten (N4) mit dem fünften Knoten (N5) verbunden wird, und die Spannung des zweiten Knotens (N2) auf weniger als die Hochpegel-Source-Spannung (VDD) reduziert wird.

5. Die OLED-Anzeigevorrichtung gemäß Anspruch 4, wobei die Spannung des zweiten Knotens (N2) reduziert wird bis auf eine Summe der Referenzspannung (Ref) und einer absoluten Schwellenspannung des Treibertransistors (Tdr).

6. Die OLED-Anzeigevorrichtung gemäß Anspruch 4 oder 5, wobei, wenn der erste Transistor (T1) angeschaltet wird und der zweite und der dritte Transistor (T2, T3) abgeschaltet werden,
die Datenspannung (Vdata) an den ersten Knoten (N1) bereitgestellt wird.

7. Die OLED-Anzeigevorrichtung gemäß Anspruch 6, wobei, wenn der erste Transistor (T1) abgeschaltet wird und der zweite und der dritte Transistor (T2, T3) angeschaltet werden,
die OLED Licht emittiert.

8. Ein Verfahren zum Betreiben der Organische-Leuchtdioden (OLED)-Anzeigevorrichtung gemäß Anspruch 1, wobei jedes der Subpixel den ersten bis dritten Transistor (T1, T2, T3), den Treibertransistor (Tdr), den ersten und den zweiten Kondensator (C1, C2) und die OLED aufweist, wobei das Verfahren aufweist:

Initialisieren einer Spannung eines ersten Knotens (N1) auf eine Referenzspannung (Ref), wenn der erste bis dritte Transistor (T1, T2, T3) angeschaltet sind entsprechend einem Scansignal (Scan), welches an den ersten Transistor (T1) angelegt wird, einem ersten Emissionssteuersignal (Em), welches an den zweiten Transistor (T2) angelegt wird, und einem zweiten Emissionssteuersignal (H), welches an den dritten Transistor (T3) angelegt wird, wobei der erste Knoten (N1) das Gate des Treibertransistors (Tdr) ist;
Speichern einer Schwellenspannung des Treibertransistors (Tdr) in dem ersten Kondensator (C1), welcher verbunden ist mit einem zweiten Knoten (N2), der die Source des Treibertransistors (Tdr) ist, wenn die Spannung an dem ersten Knoten (N1) die Referenzspannung (Ref) ist und der erste und der dritte Transistor (T1, T3) angeschaltet sind und der zweite Transistor (T2) abgeschaltet ist entsprechend dem Scansignal (Scan), welches an den ersten Transistor (T1) angelegt wird, dem ersten Emissionssteuersignal (Em), welches an den zweiten Transistor (T2) angelegt wird, und dem zweiten Emissionssteuersignal (H), welches an den dritten Transistor (T3) angelegt wird, wobei das andere Ende des ersten Kondensators (C1) mit dem ersten Knoten (N1) verbunden ist;
Bereitstellen der Datenspannung (Vdata) an den ersten Knoten (N1), wenn der erste Transistor (T1) angeschaltet ist und der zweite und der dritte Transistor (T2, T3) abgeschaltet sind entsprechend dem Scansignal (Scan), welches an den ersten Transistor (T1) angelegt wird, dem ersten Emissionssteuersignal (Em), welches an den zweiten Transistor (T2) angelegt wird, und dem zweiten Emissionssteuersignal (H), welches an den dritten Transistor (T3) angelegt wird, und
Emittieren, durch die OLED, von Licht mit einem von dem Treibertransistor (Tdr) empfangenen Strom, der abhängig ist von der Spannungsdifferenz zwischen der Datenspannung (Vdata) und der Referenzspannung (Ref), wenn der erste Transistor (T1) abgeschaltet ist und der zweite und der dritte Transistor (T2, T3) angeschaltet sind entsprechend dem Scansignal (Scan), welches an den ersten Transistor (T1) angelegt wird, dem ersten Emissionssteuersignal (Em), welches an den zweiten Transistor (T2) angelegt wird, und dem zweiten Emissionssteuersignal (H), welches an den dritten Transistor (T3) angelegt wird,
wobei die OLED-Anzeigevorrichtung so konfiguriert ist, dass das zweite Emissionssteuersignal (H), das an die dritten Transistoren (T3) der Subpixel (SP), die in der i-ten Reihe angeordnet sind, angelegt wird, gleichzeitig das erste Emissionssteuersignal (Em) ist, das an die zweiten Transistoren (T2) der Subpixel (SP), die in der (i+1)-ten Reihe angeordnet sind, angelegt wird, sodass das Signal-Timing beider Signale identisch ist, und wobei $1 \leq i < m$.

9. Das Verfahren gemäß Anspruch 8, wobei das Initialisieren einer Spannung aufweist:

Bereitstellen einer Hochpegel-Source-Spannung (VDD) an den zweiten Knoten (N2); und
Verbinden eines vierten Knotens (N4) mit einem fünften Knoten (N5), wobei der vierte Knoten (N4) ein Drain des Treibertransistors (Tdr) ist und wobei der fünfte Knoten (T5) eine Anode der OLED ist.

10. Das Verfahren gemäß Anspruch 8 oder 9, wobei das Speichern einer Schwellenspannung aufweist:

Bereitstellen der Referenzspannung (Ref) an den ersten Knoten (N1); und
Reduzieren einer Spannung des zweiten Knotens (N2) auf eine Summe der Referenzspannung (Ref) und einer absoluten Schwellenspannung des Treibertransistors (Tdr).

11. Das Verfahren gemäß irgendeinem der Ansprüche 8 bis 10, wobei
die Source des zweiten Transistors (T2) mit einem dritten Knoten (N3) verbunden ist, der eine Hochpegel-Source-Spannung (VDD) empfängt,
der Drain des zweiten Transistors (T2) mit dem zweiten Knoten (N2) verbunden ist, und

der zweite Kondensator (C2) zwischen den zweiten Knoten (N2) und den dritten Knoten (N3) geschaltet ist.

12. Das Verfahren gemäß irgendeinem der Ansprüche 8 bis 11, wobei das Bereitstellen der Datenspannung (Vdata) aufweist ein Trennen eines vierten Knotens (N4) von einem fünften Knoten (N5), wobei der vierte Knoten (N4) der Drain des Treibertransistors (Tdr) ist und der fünfte Knoten (N5) eine Anode der OLED ist.

13. Das Verfahren gemäß irgendeinem der Ansprüche 8 bis 12, wobei

der erste Transistor (T1) angeschaltet wird von dem Scansignal (Scan), das daran über eine Scanleitung (Scan) angelegt wird,
der zweite Transistor (T2) angeschaltet wird von dem ersten Emissionssteuersignal (Em), welches daran über eine erste Emissionssteuerleitung angelegt wird, und
der dritte Transistor (T3) angeschaltet wird durch das zweite Emissionssteuersignal (H), welches daran über eine zweite Emissionssteuerleitung angelegt wird.

Revendications

1. Dispositif d'affichage à diode électroluminescente organique (OLED) comprenant une pluralité de sous-pixels (SP) agencée dans une matrice « m x n » présentant « m » lignes et « n » colonnes, chaque sous-pixel (SP) comprenant :

un premier transistor (T1) fournissant une tension de données (Vdata) ou une tension de référence (Ref) à un premier noeud (N1) selon un signal de balayage (Scan) ;
un transistor de commande (Tdr), dans lequel la grille du transistor de commande (Tdr) est connectée au premier noeud (N1), la source du transistor de commande (Tdr) est connectée à un deuxième noeud (N2) et le drain du transistor de commande (Tdr) est connecté à un quatrième noeud (N4) ;
un premier condensateur (C1) connecté entre les premier (N1) et deuxième noeuds (N2) et stockant une tension de seuil du transistor de commande (Tdr) ;
un second condensateur (C2) connecté entre le deuxième noeud (N2) et un troisième noeud (N3) qui correspond à la source du deuxième transistor (T2) ;
ledit deuxième transistor (T2) fournissant une tension de source de haut niveau (VDD), appliquée au troisième noeud (N3), au deuxième noeud (N2), selon un premier signal de commande d'émission (Em) appliqué au deuxième transistor (T2) ;
une diode OLED émettant de la lumière avec un courant reçu en provenance du transistor de commande (Tdr) qui est en fonction de la différence de tension entre la tension de données (Vdata) et la tension de référence (Ref) ; et
un troisième transistor (T3) connectant le quatrième noeud (N4) à un cinquième noeud (N5) selon un second signal de commande d'émission (H) appliqué au troisième transistor (T3), le cinquième noeud (T5) étant une anode de la diode OLED,
caractérisé en ce que :

le dispositif d'affichage OLED est configuré de sorte que le second signal de commande d'émission (H) appliqué aux troisièmes transistors (T3) des sous-pixels (SP) disposés dans la i-ième ligne est en même temps le premier signal de commande d'émission (Em) appliqué aux deuxièmes transistors (T2) des sous-pixels (SP) disposés dans la (i + 1)-ième ligne, de sorte que la temporisation de signaux des deux signaux est identique, et dans lequel $1 \leq i < m$.

2. Dispositif d'affichage OLED selon la revendication 1, dans lequel,

le premier transistor (T1) est activé par le signal de balayage (Scan) qui est appliqué à celui-ci à travers une ligne de balayage ;
le deuxième transistor (T2) est activé par le premier signal de commande d'émission (Em) qui est appliqué à celui-ci à travers une première ligne de commande d'émission ; et
le troisième transistor (T3) est activé par le second signal de commande d'émission (H) qui est appliqué à celui-ci à travers une seconde ligne de commande d'émission.

3. Dispositif d'affichage OLED selon l'une quelconque des revendications 1 à 2, dans lequel, lorsque les premiers à troisièmes transistors (T1, T2, T3) sont activés, la tension de référence (Ref) est fournie au premier noeud (N1), la tension de source de haut niveau (VDD) est fournie au deuxième noeud (N2), et le quatrième noeud (N4) est connecté au cinquième noeud (N5), de sorte que la tension du premier noeud (N1) est initialisée à la valeur de la tension de référence (Ref).

4. Dispositif d'affichage OLED selon la revendication 3, dans lequel lorsque les premier et troisième transistors (T1, T3) sont activés, et que le deuxième transistor (T2) est désactivé,
la tension de référence (Ref) est fournie au premier noeud (N1), le quatrième noeud (N4) est connecté au cinquième noeud (N5), et la tension du deuxième noeud (N2) est réduite à une valeur inférieure à la tension de source de haut niveau (VDD).

5. Dispositif d'affichage OLED selon la revendication 4, dans lequel la tension du deuxième noeud (N2) est réduite jusqu'à une somme de la tension de référence (Ref) et d'une tension de seuil absolue du transistor de commande (Tdr).

6. Dispositif d'affichage OLED selon la revendication 4 ou 5, dans lequel lorsque le premier transistor (T1) est activé, et que les deuxième et troisième transistors (T2, T3) sont désactivés,
la tension de données (Vdata) est fournie au premier noeud (N1).

7. Dispositif d'affichage OLED selon la revendication 6, dans lequel, lorsque le premier transistor (T1) est désactivé, et que les deuxième et troisième transistors (T2, T3) sont activés,
la diode OLED émet de la lumière.

8. Procédé de commande du dispositif d'affichage à diode électroluminescente organique (OLED) selon la revendication 1, dans lequel chacun des sous-pixels inclut les premier à troisième transistors (T1, T2, T3), le transistor de commande (Tdr), les premier et second condensateurs (C1, C2), et la diode OLED, le procédé comprenant les étapes ci-dessous consistant à :

initialiser une tension d'un premier noeud (N1) à la valeur d'une tension de référence (Ref), lorsque les premier à troisième transistors (T1, T2, T3) sont activés selon un signal de balayage (Scan) appliqué au premier transistor (T1), un premier signal de commande d'émission (Em) appliqué au deuxième transistor (T2) et un second signal de commande d'émission (H) appliqué au troisième transistor (T3), le premier noeud (N1) correspondant à la grille du transistor de commande (Tdr) ;
stocker une tension de seuil du transistor de commande (Tdr) dans le premier condensateur (C1) connecté à un deuxième noeud (N2) qui correspond à la source du transistor de commande (Tdr), lorsque la tension au niveau du premier noeud (N1) correspond à la tension de référence (Ref), que les premier et troisième transistors (T1, T3) sont activés, et que le deuxième transistor (T2) est désactivé selon le signal de balayage (Scan) appliqué au premier transistor (T1), le premier signal de commande d'émission (Em) appliqué au deuxième transistor (T2) et le second signal de commande d'émission (H) appliqué au troisième transistor (T3), dans lequel l'autre extrémité du premier condensateur (C1) est connectée au premier noeud (N1) ;
fournir la tension de données (Vdata) au premier noeud (N1), lorsque le premier transistor (T1) est activé et que les deuxième et troisième transistors (T2, T3) sont désactivés selon le signal de balayage (Scan) appliqué au premier transistor (T1), le premier signal de commande d'émission (Em) appliqué au deuxième transistor (T2) et le second signal de commande d'émission (H) appliqué au troisième transistor (T3) ; et
émettre, par le biais de la diode OLED, de la lumière avec un courant reçu en provenance du transistor de commande (Tdr) qui est en fonction de la différence de tension entre la tension de données (Vdata) et la tension de référence (Ref) lorsque le premier transistor (T1) est désactivé et que les deuxième et troisième transistors (T2, T3) sont activés selon le signal de balayage (Scan) appliqué au premier transistor (T1), le premier signal de commande d'émission (Em) appliqué au deuxième transistor (T2) et le second signal de commande d'émission (H) appliqué au troisième transistor (T3) ;
dans lequel le dispositif d'affichage OLED est configuré de sorte que le second signal de commande d'émission (H) appliqué aux troisièmes transistors (T3) des sous-pixels (SP) disposés dans la i-ième ligne est en même temps le premier signal de commande d'émission (Em) appliqué aux deuxièmes transistors (T2) des sous-pixels (SP) disposés dans la (i + 1)-ième ligne, de sorte que la temporisation de signaux des deux signaux est identique, et dans lequel $1 \leq i < m$.

9. Procédé selon la revendication 8, dans lequel l'étape d'initialisation d'une tension comprend les étapes ci-dessous consistant à :

fournir une tension de source de haut niveau (VDD) au deuxième noeud (N2) ; et
connecter un quatrième noeud (N4) à un cinquième noeud (N5), le quatrième noeud (N4) correspondant à un drain du transistor de commande (Tdr), et le cinquième noeud (T5) correspondant à une anode de la diode OLED.

10. Procédé selon la revendication 8 ou 9, dans lequel l'étape de stockage d'une tension de seuil comprend les étapes ci-dessous consistant à :

fournir la tension de référence (Ref) au premier noeud (N1) ; et
réduire une tension du deuxième noeud (N2) à une somme de la tension de référence (Ref) et d'une tension de seuil absolue du transistor de commande (Tdr).

11. Procédé selon l'une quelconque des revendications 8 à 10, dans lequel,
la source du deuxième transistor (T2) est connectée à un troisième noeud (N3) recevant une tension de source de haut niveau (VDD) ;
le drain du deuxième transistor (T2) est connecté au deuxième noeud (N2) ; et
le second condensateur (C2) est connecté entre les deuxième et troisième noeuds (N2, N3).

12. Procédé selon l'une quelconque des revendications 8 à 11, dans lequel l'étape de fourniture de la tension de données (Vdata) comporte l'étape consistant à déconnecter un quatrième noeud (N4) d'un cinquième noeud (N5), le quatrième noeud (N4) correspondant au drain du transistor de commande (Tdr) et le cinquième noeud (N5) correspondant à une anode de la diode OLED.

13. Procédé selon l'une quelconque des revendications 8 à 12, dans lequel,

le premier transistor (T1) est activé par le signal de balayage (Scan) qui est appliqué à celui-ci à travers une ligne de balayage (Scan) ;
le deuxième transistor (T2) est activé par le premier signal de commande d'émission (Em) qui est appliqué à celui-ci à travers une première ligne de commande d'émission ; et
le troisième transistor (T3) est activé par le second signal de commande d'émission (H) qui est appliqué à celui-ci à travers une seconde ligne de commande d'émission.

FIG. 1

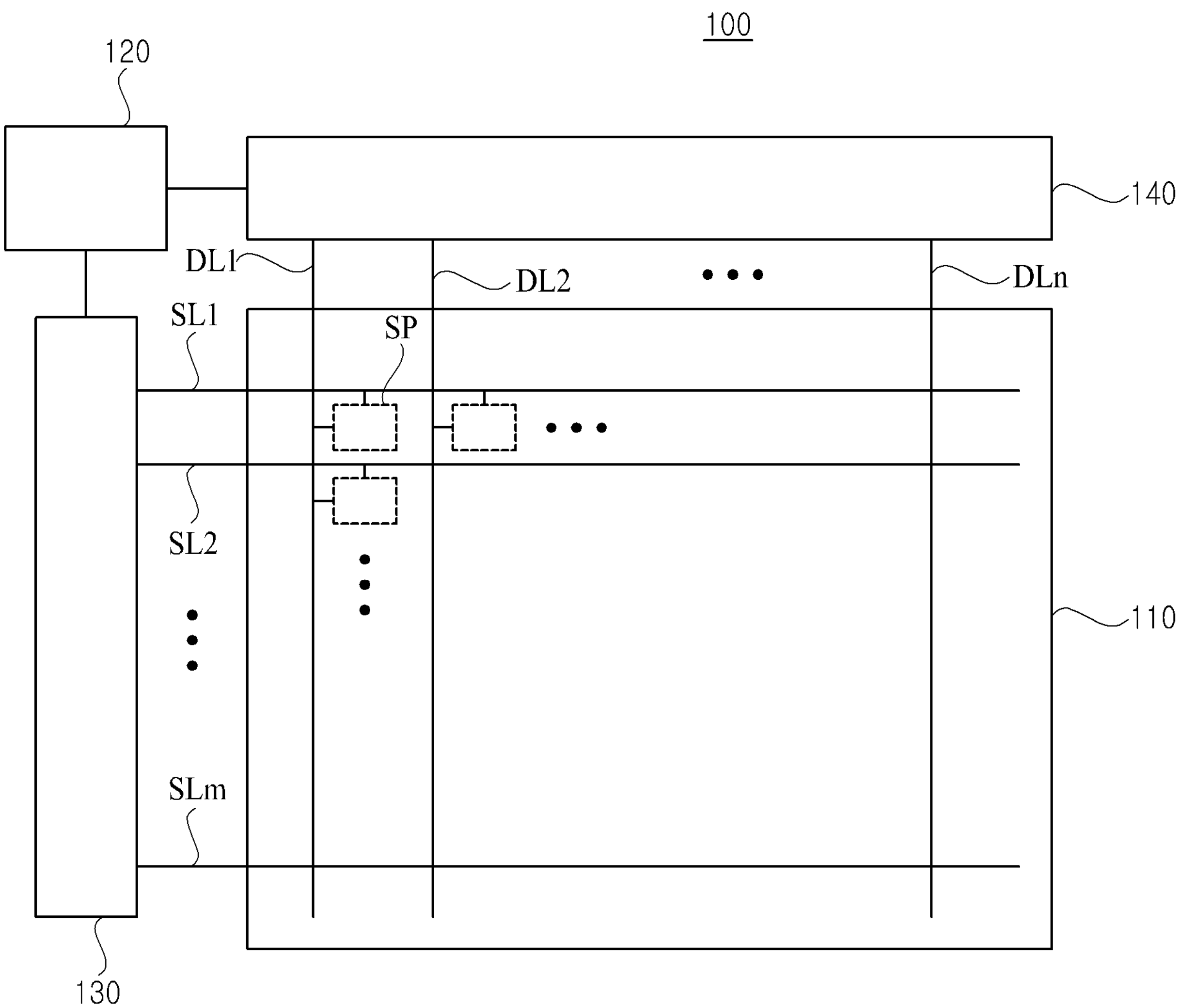


FIG. 2

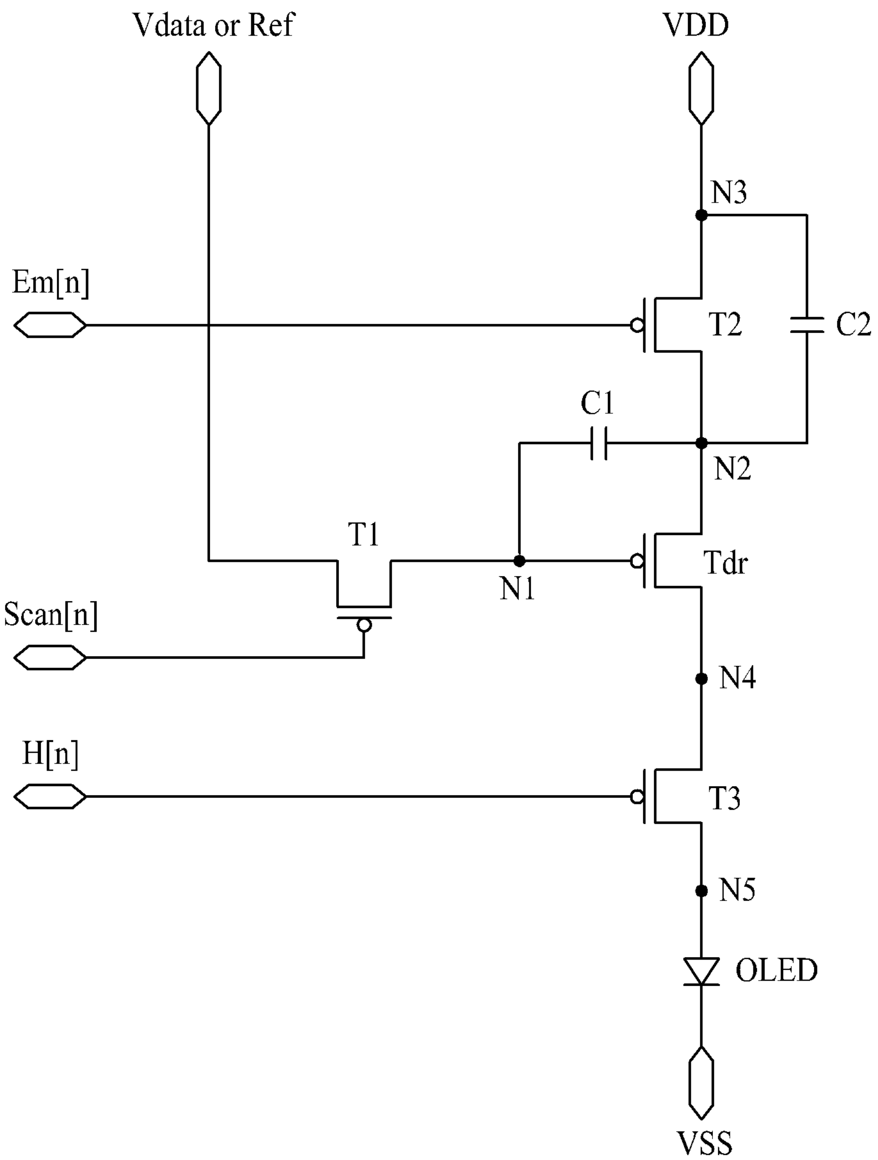

Vdata or Ref
VDD
N3
Em[n]
T2
C2
C1
N2
T1
Tdr
N1
Scan[n]
N4
H[n]
T3
N5
OLED
VSS

FIG. 3

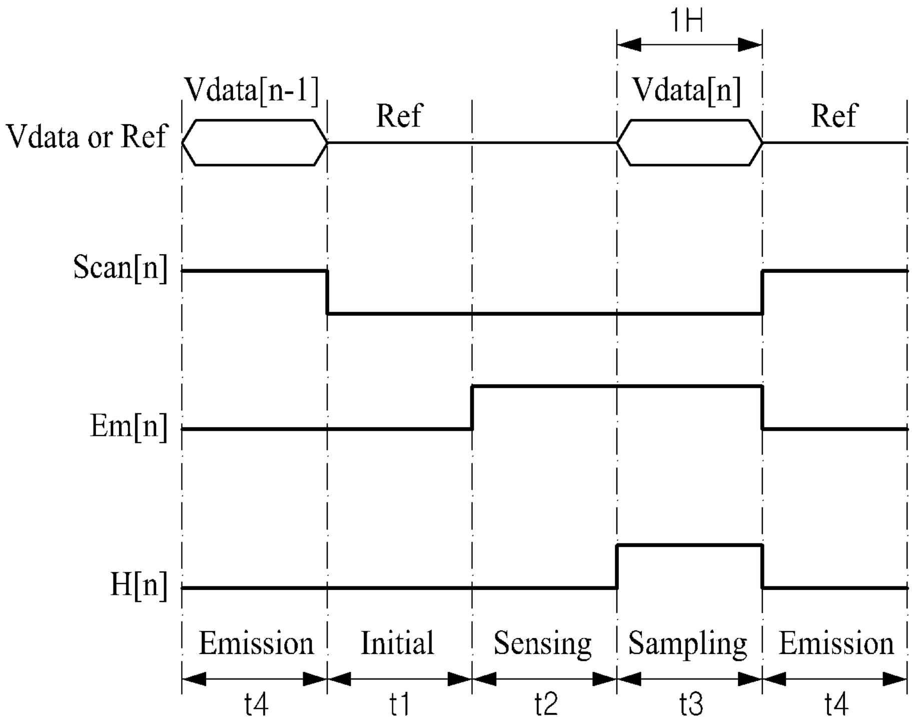

1H
Vdata[n-1]
Ref
Vdata[n]
Ref
Vdata or Ref
Scan[n]
Em[n]
H[n]
Emission
Initial
Sensing
Sampling
Emission
t4
t1
t2
t3
t4

FIG. 4

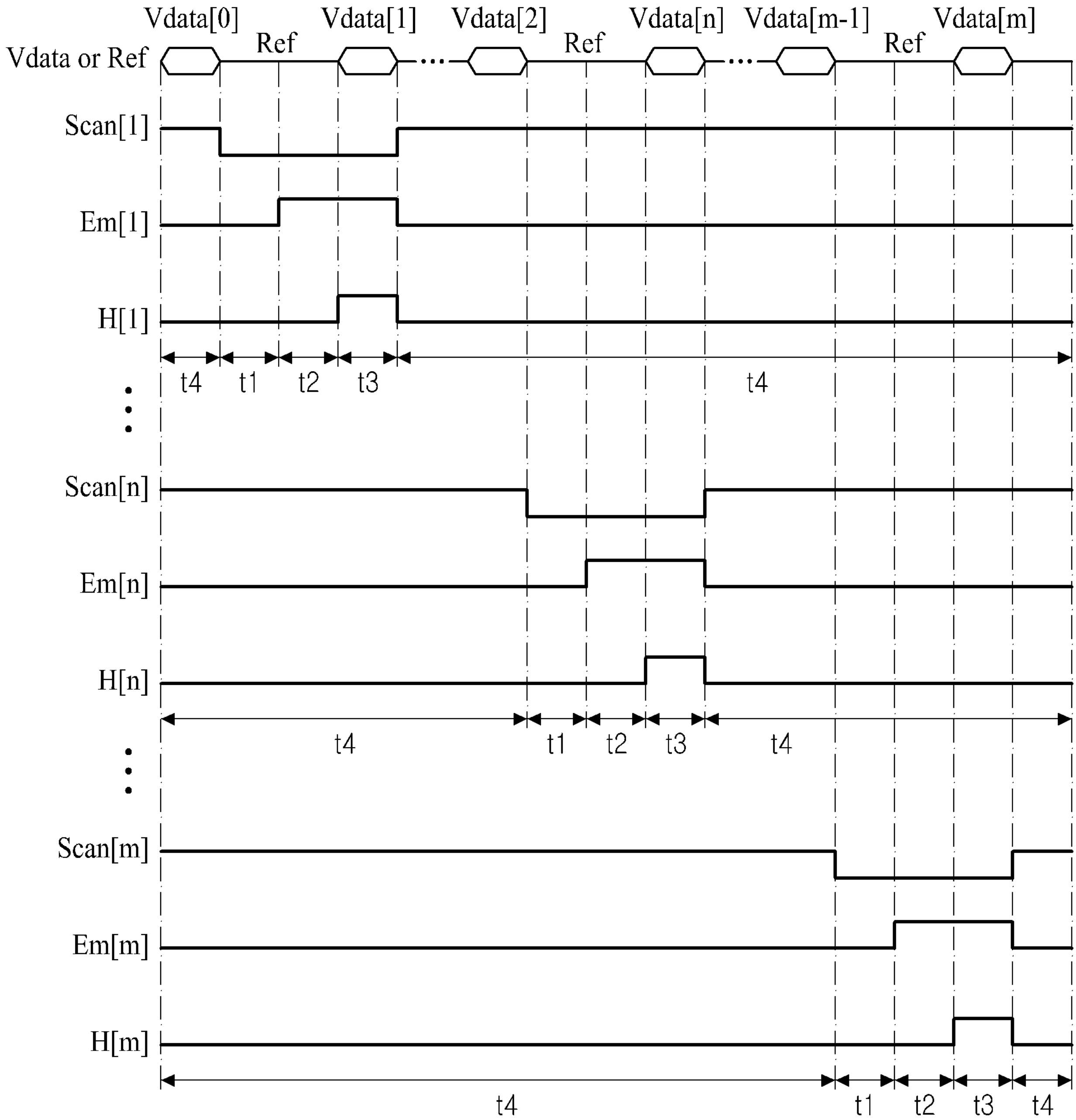

Vdata[0]
Vdata[1]
Vdata[2]
Vdata[n]
Vdata[m-1]
Vdata[m]
Vdata or Ref
Ref
Ref
Ref
Scan[1]
Em[1]
H[1]
t4
t1
t2
t3
t4
Scan[n]
Em[n]
H[n]
t4
t1
t2
t3
t4
Scan[m]
Em[m]
H[m]
t4
t1
t2
t3
t4

FIG. 5A

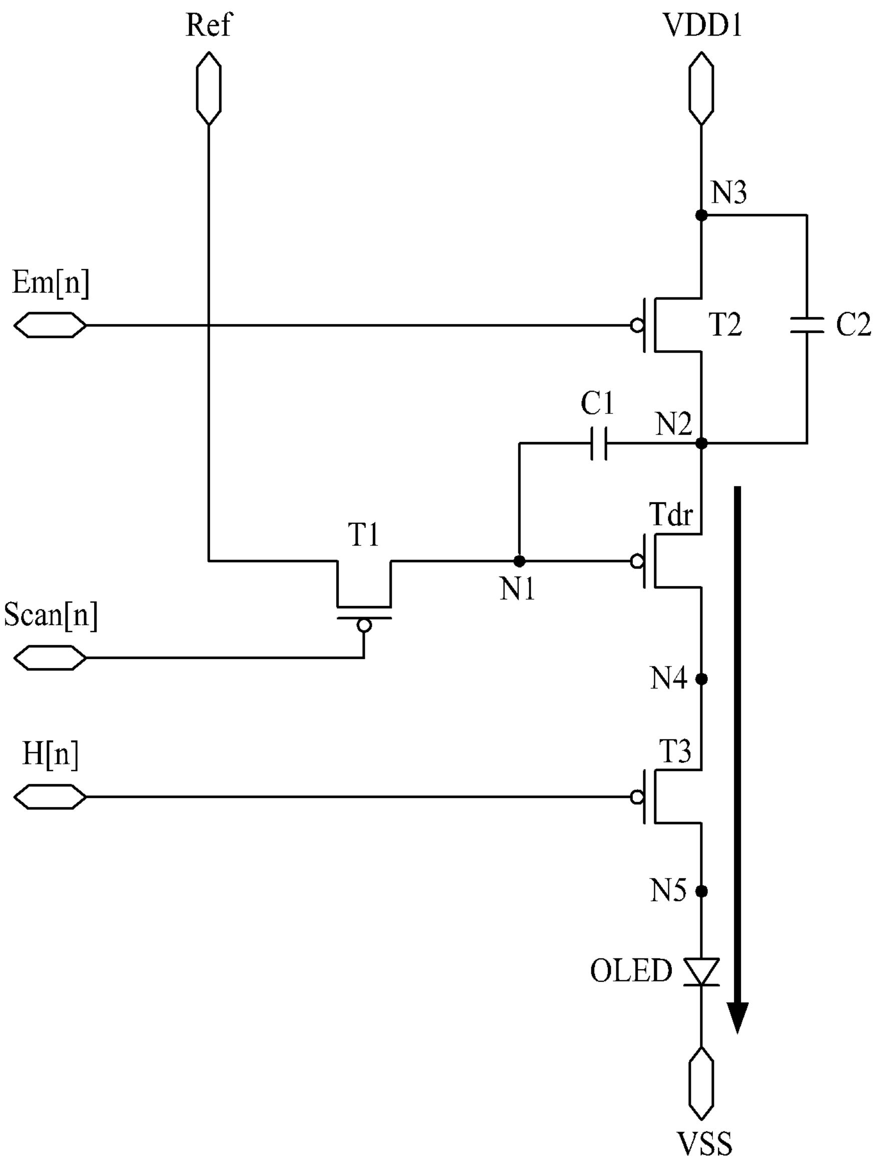


FIG. 5B

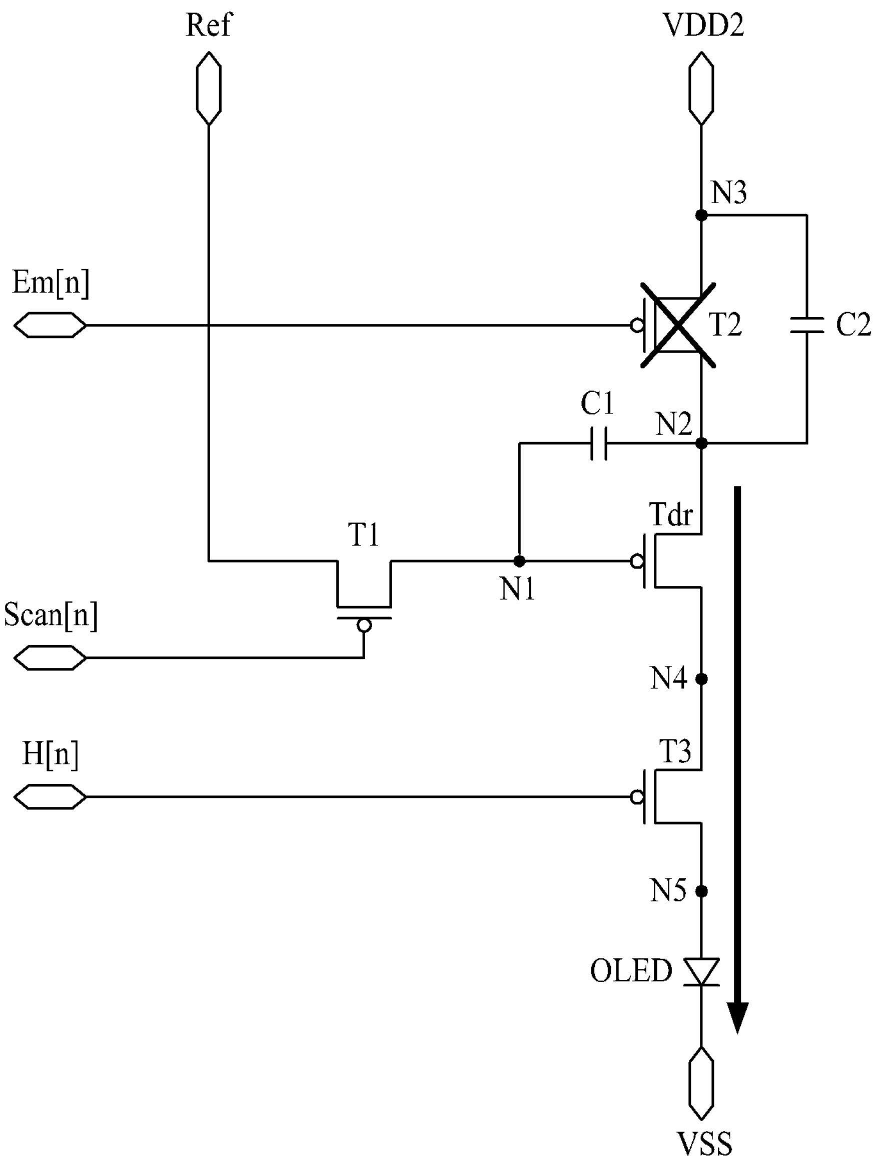


FIG. 5C

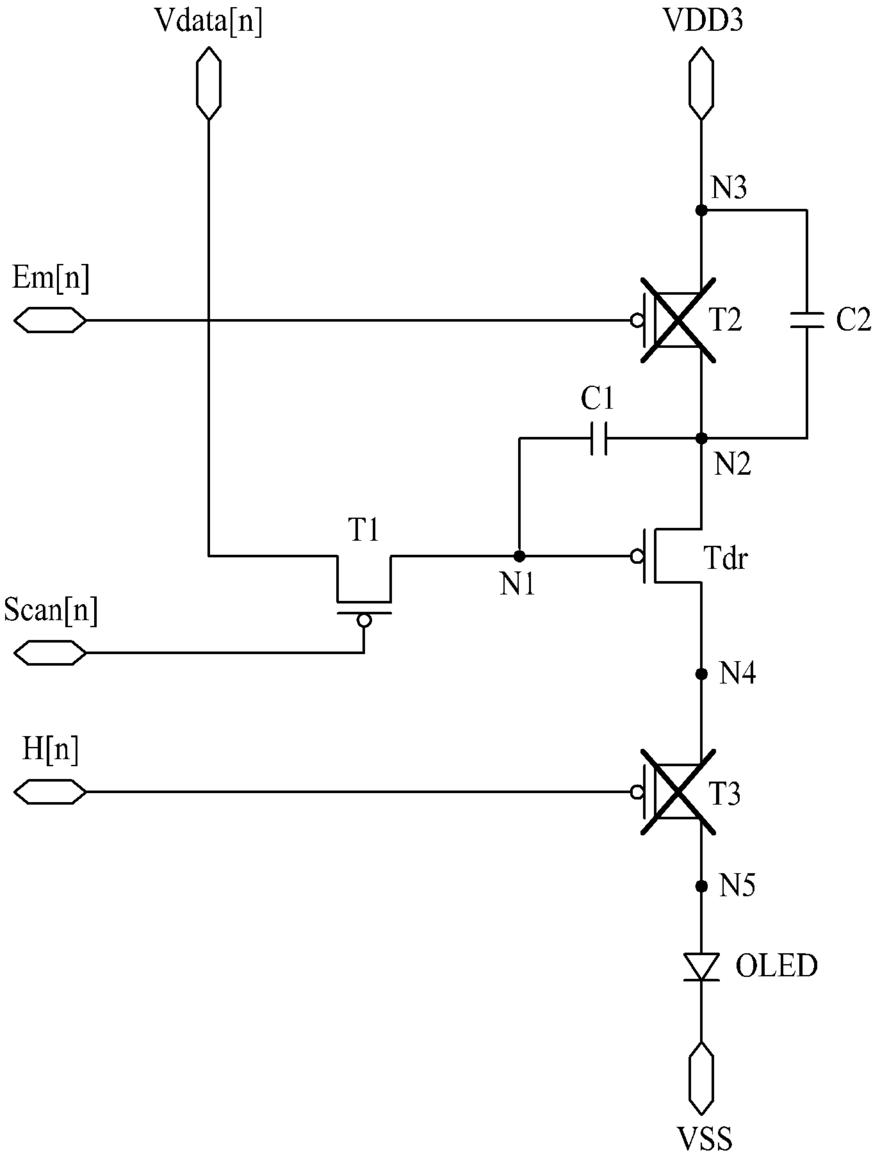

Vdata[n]
VDD3
N3
Em[n]
T2
C2
C1
N2
T1
Tdr
N1
Scan[n]
N4
H[n]
T3
N5
OLED
VSS

FIG. 5D

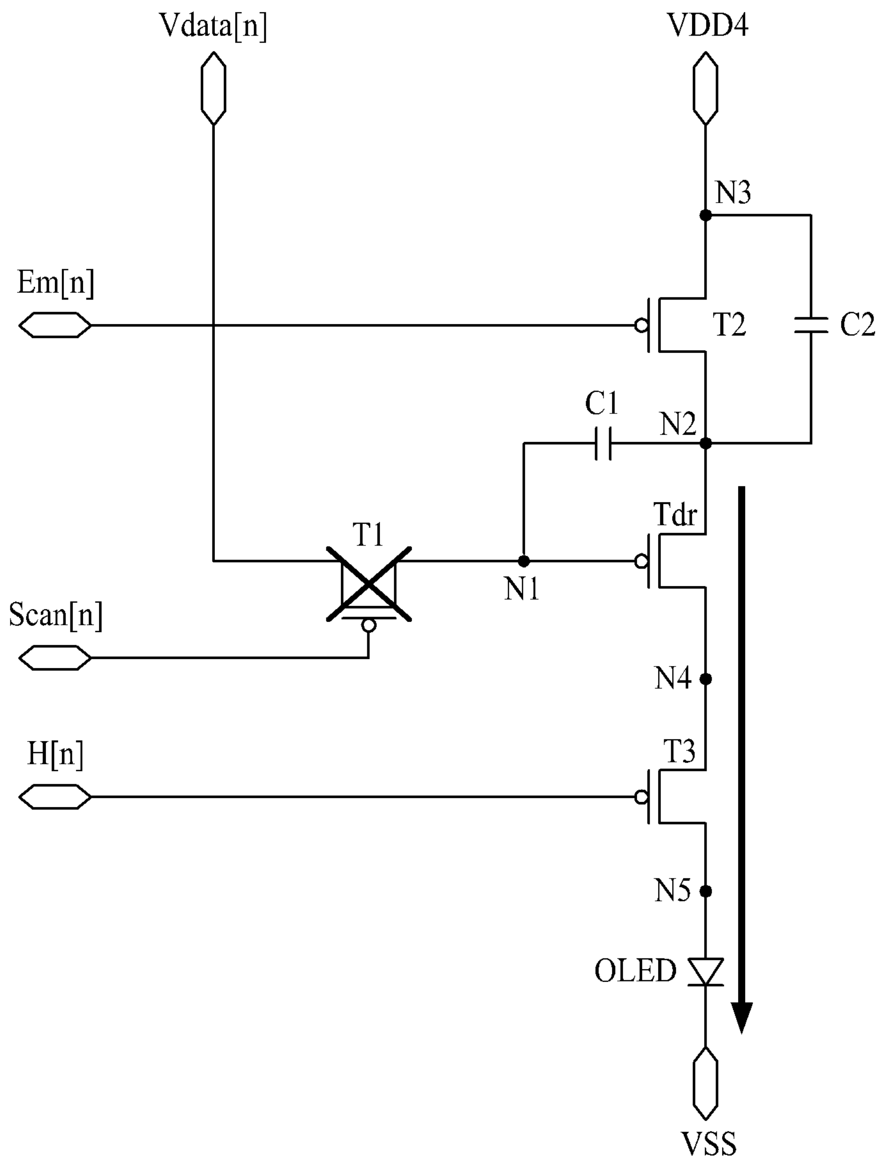

Vdata[n]
VDD4
N3
Em[n]
T2
C2
C1
N2
Tdr
T1
N1
Scan[n]
N4
H[n]
T3
N5
OLED
VSS

FIG. 6

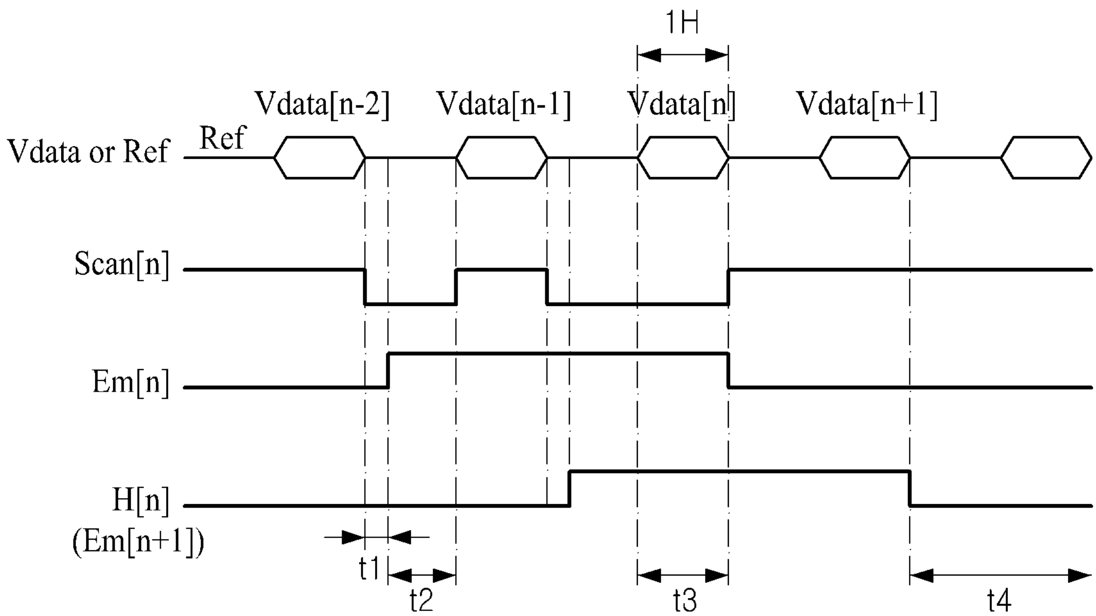
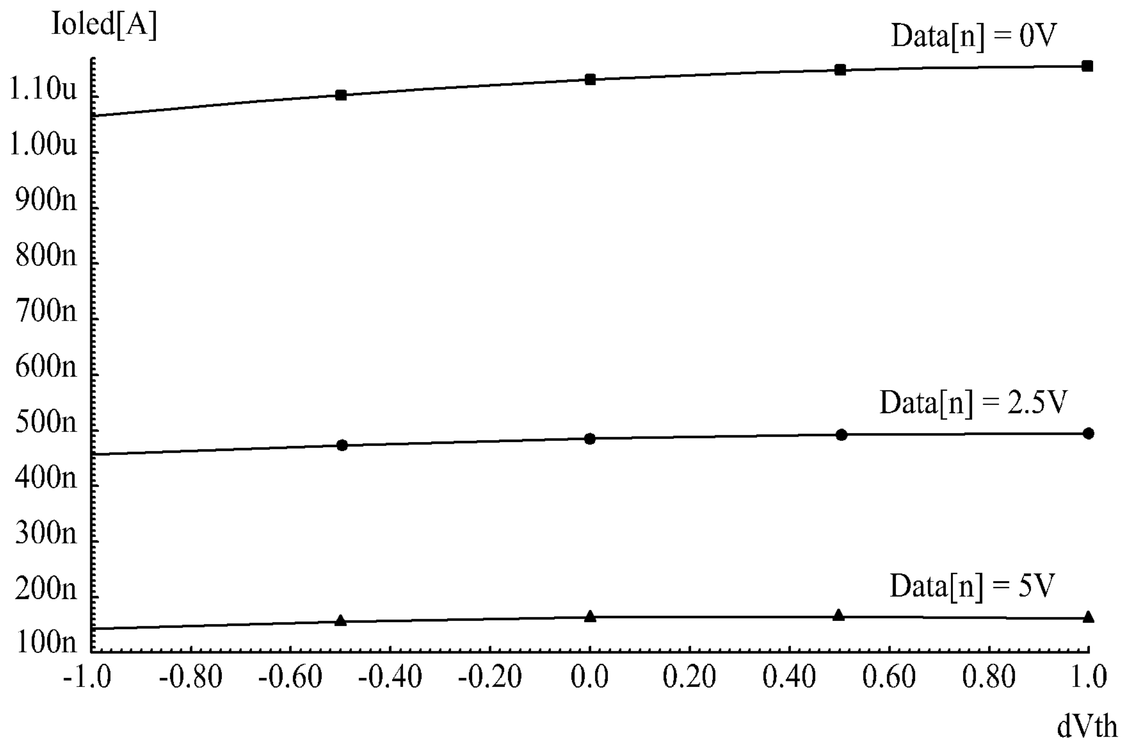

1H
Vdata[n-2]
Vdata[n-1]
Vdata[n]
Vdata[n+1]
Vdata or Ref
Ref
Scan[n]
Em[n]
H[n]
(Em[n+1])
t1
t2
t3
t4

FIG. 7


Ioled[A]
Data[n] = 0V
Data[n] = 2.5V
Data[n] = 5V
1.10u
1.00u
900n
800n
700n
600n
500n
400n
300n
200n
100n
-1.0
-0.80
-0.60
-0.40
-0.20
0.0
0.20
0.40
0.60
0.80
1.0
dVth

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- KR 1020120152218 **[0001]**
- US 20130169611 A1 **[0008]**
- US 20100134388 A1 **[0009]**

专利名称(译)	有机发光二极管显示装置及其驱动方法		
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申请号	EP2013161924	申请日	2013-04-02
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	KWAK SANGHYEON		
发明人	KWAK, SANGHYEON		
IPC分类号	G09G3/32		
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优先权	1020120152218 2012-12-24 KR		
其他公开文献	EP2747064A1		
外部链接	Espacenet		

摘要(译)

公开了一种OLED显示装置。 OLED显示装置包括第一晶体管，驱动晶体管，第一电容器，第二晶体管，OLED和第三晶体管。第一晶体管根据扫描信号向第一节点提供数据电压或参考电压。驱动晶体管的栅极连接到第一节点，驱动晶体管的源极连接到第二节点，驱动晶体管的漏极连接到第四节点。第一电容器连接在第一和第二节点之间。第二晶体管向第二节点提供高电平源电压。 OLED发射具有第一和第二节点的电压之间的差电压的光。第三晶体管根据第二发射控制信号将第四节点连接到第五节点。

$$
\begin{aligned}
Ioled &= K \times (Vgs - Vth)^2 \\
&= K \times (Vsg + Vth)^2 \\
&= K \times [VDD - VDD4 - \{c2/(c1+c2)\}(Vdata[n]-Ref) + |Vth| + Vth]^2 \\
&= K \times [\{c2/(c1+c2)\}(Vdata[n]-Ref) + |Vth| - |Vth|]^2 \\
&= K \times [\{c2/(c1+c2)\}(Vdata[n]-Ref)]^2 \qquad \ldots(1)
\end{aligned}
$$