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(54) **Pixel, display device including the same, and driving method thereof**

Pixel, Anzeigevorrichtung damit und Ansteuerungsverfahren dafür

Pixel, dispositif d'affichage l'utilisant et son procédé de commande

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Description

BACKGROUND

1. Field

[0001] The present invention relates to a pixel, a display device including the same, and a driving method thereof.

2. Description of the Related Art

[0002] Cathode ray tubes (CRTs) have been used to display images. However, CRTs can have the disadvantages of being heavy and large in size. Currently, various flat panel displays are being developed that can reduce the heavy weight and large volume that are drawbacks of CRTs. Examples of flat panel displays include liquid crystal displays (LCDs), field emission displays (FEDs), plasma display panels (PDPs), and organic light emitting diode (OLED) displays.

[0003] OLED displays can display images using OLEDs that generate light by recombination of electrons and holes. An OLED display can have a fast response speed, can be driven with low power consumption, and can have the advantages of improved (or excellent) luminous efficiency, luminance, and viewing angle.

[0004] Generally, OLED displays can be classified into two types according to the driving method of the OLED display: passive matrix OLEDs (PMOLEDs) and active matrix OLEDs (AMOLEDs).

[0005] Of the two types, the active matrix OLED display in which unit pixels are selectively lit is primarily used because of its good resolution, contrast, and operation speed.

[0006] One pixel of an active matrix OLED display may include an OLED, a driving transistor for controlling an amount of current supplied to the OLED, and a switching transistor for transmitting a data signal to the driving transistor to control an amount of light emitted by the OLED.

[0007] Recently, research has been underway on a compensation circuit to compensate for a threshold voltage variation (or deviation) of the driving transistor included in the pixel of the active matrix OLED display. However, when the compensation circuit is used to display an image at a desired luminance, the response speed of the pixel varies according to an increase/decrease in a data voltage applied to the driving transistor, due to hysteresis, such that it is difficult to correctly display gray levels. For example, a delay in response speed may be generated when driving the OLED display to express a luminance from black to white, and this problem may cause sticking when scrolling text on a screen.

[0008] EP1496495 discloses a pixel circuit in an organic light emitting device capable of realizing high gradation representation by self-compensating a threshold voltage, and a method for driving the same. The pixel circuit includes an electroluminescent element for emitting light in response to an applied driving current. A first transistor delivers a data signal voltage in response to a current scan line signal. A second transistor generates a driving current to drive the electroluminescent element in response to the data signal voltage. A third transistor connects the second transistor in the form of a diode in response to a current scan signal to self-compensate the threshold voltage of the second transistor. A capacitor stores the data signal voltage delivered to the second transistor. A fourth transistor delivers a power supply voltage to the second transistor in response to a current light-emitting signal. A fifth transistor provides the driving current, provided from the second transistor, for the electroluminescent element in response to the current light-emitting signal.

[0009] US 2006/055336 discloses an organic light emitting display includes a plurality of pixels, at least one of the pixels having: an organic light emitting diode; a driving transistor adapted to supply a driving current to the organic light emitting diode; a first switching transistor adapted to selectively supply a data signal to the driving transistor; a second switching transistor adapted to selectively supply an initialization signal; a third switching transistor adapted to selectively allow the driving transistor to be connected as a diode and to selectively supply the initialization sought; a storage capacitor adapted to store a first voltage corresponding to the initialization signal received from the third switching transistor and then to store a second voltage corresponding to the data signal applied at a gate electrode of the driving transistor; and an interrupter adapted to selectively supply a pixel power to the driving transistor and to selectively allow the driving current to flow into the organic light emitting diode. In this display, the amount of current leaking out through a switching transistor is decreased, and thus a voltage variance applied to a gate electrode of a driving transistor is decreased, thereby enhancing a contrast of an image.

[0010] EP 1936596 discloses an organic light emitting display including a scan signal line forwarding a scan signal, a data line sending a data signal and a pixel coupled to the scan signal line and the data line, the organic light emitting diode display, wherein the pixel includes a first switching transistor transmitting a data signal from the data line in response to the scan signal of the scan signal line, a driving transistor, coupled to the first switching transistor, controlling driving current from a first power source line, a storage capacitor coupled between the driving transistor and the first power source line, an organic light emitting diode, coupled between the driving transistor and a second power source line, displaying an image with the driving current controlled by the driving transistor, an initial switching transistor, coupled between the storage capacitor and an initial power source line, initializing the storage capacitor, and a switching transistor for applying a reverse bias, coupled between the second power source line and the initial power source line, applying a reverse bias voltage to the organic light emitting diode.

[0011] US 2010/007649 discloses a scan driving circuit includes a shift register unit and a logic circuit unit. The start of a start pulse of an output signal STp+1 of a p+1'th shift register is situated between the start and end of a start pulse of the output signal STp of a p'th shift register, and one each of a first enable signal through a Q'th enable signal exist in sequence between the start of the start pulse of the output signal STp and the start of the start pulse of the output signal STp+1. The operations of a (p', q)'th NAND circuit are restricted based on period identifying signals, such that the NAND circuit generates scanning signals based only on a portion of the output signal STP corresponding to the first start pulse, the signal obtained by inverting the output signal STp+1, and the q'th enable signal ENq.

[0012] The above information disclosed in this Background section is only for enhancement of understanding of the background of the invention and therefore it may contain information that does not form the prior art that is already known in this country to a person of ordinary skill in the art.

SUMMARY

[0013] The present invention sets out to provide a pixel, a display device including the same, and a driving method thereof to reduce (or remove) a delay in response speed and reduce sticking while driving a display.

[0014] The present invention also sets out to provide a pixel circuit that concurrently (e.g., simultaneously) compensates for a threshold voltage variation of a driving transistor while addressing (or solving) the problems of delayed response speed caused by hysteresis and reducing sticking on a screen.

[0015] Also, The present invention sets out to provide a high quality display device producing high image quality that is capable of compensating for a threshold voltage variation (or deviation) of a driving transistor; correctly expressing gray levels by reducing (or solving) a delay in a response speed, for example, in a case of displaying an image according to a data signal having a large luminance variation (or deviation); and a driving method thereof.

[0016] Technical aspects of the present invention are not limited to the above, and other aspects (e.g., non-mentioned aspects) will be clearly understood by a person of ordinary skill in the art by way of the following description.

[0017] A display device according to embodiments of the present invention includes: a display unit including a plurality of pixels respectively coupled to a plurality of scan lines for transmitting a plurality of scan signals, a plurality of data lines for transmitting a plurality of data signals, and a plurality of light emission control lines for transmitting a plurality of light emission control signals; a scan driver for transmitting the plurality of scan signals; a data driver for transmitting the plurality of data signals; and a light emission driver for transmitting the plurality of light emission control signals, wherein each pixel of the plurality of pixels includes: an organic light emitting diode (OLED); a driving transistor configured to transmit a driving current corresponding to a data signal from among the plurality of data signals to the OLED; a first transistor configured to transmit the data signal to the driving transistor according to a first scan signal from among the plurality of scan signals; a second transistor configured to apply a first power source voltage to a first electrode of the driving transistor according to a second scan signal from among the plurality of scan signals, during an initialization period for initializing a gate electrode voltage of the driving transistor; and a capacitor including a first electrode coupled to a gate electrode of the driving transistor and a second electrode coupled to a first power source supply.

[0018] A voltage difference between the gate electrode voltage and a first electrode voltage of the driving transistor during the initialization period may be a voltage for operating the driving transistor.

[0019] The first transistor may be switching-operated according to the first scan signal to transmit the data signal to the first electrode of the driving transistor.

[0020] The second scan signal may be transmitted to a previous scan line from among the plurality of scan lines, and the previous scan line may precede the scan line receiving the first scan signal.

[0021] The scan driver may be configured to transmit the first scan signal and the second scan signal to the plurality of pixels.

[0022] Each pixel of the plurality of pixels may further include: an initialization transistor configured to supply an initialization voltage to the gate electrode of the driving transistor during the initialization period and to initialize the gate electrode voltage of the driving transistor.

[0023] The initialization transistor may be switching-operated according to the second scan signal transmitted to a previous scan line from among the plurality of scan lines, and the previous scan line may precede the scan line receiving the first scan signal transmitted to the first transistor.

[0024] The initialization period may be a period in which the second scan signal is transmitted to the initialization transistor at a gate-on voltage level.

[0025] The initialization period may be before a period in which a threshold voltage of the driving transistor is compensated.

[0026] Each pixel of the plurality of pixels may further include: a threshold voltage compensation transistor configured to be switching-operated according to the first scan signal after the initialization period and to diode-couple the driving transistor and compensate a threshold voltage of the driving transistor.

[0027] Each pixel of the plurality of pixels may further include: at least one light emission control transistor configured to control light emission of the OLED receiving the driving current according to the data signal.

[0028] The at least one light emission control transistor

may be configured to be switching-operated according to a light emission control signal from among the plurality of light emission control signals transmitted at a gate-on voltage level, after the first scan signal and the second scan signal are respectively transmitted at the gate-on voltage level to the first transistor and the second transistor.

[0029] A pixel according to another embodiment of the present invention includes: an organic light emitting diode (OLED); a driving transistor configured to transmit a driving current to the OLED according to a data signal; a first transistor configured to transmit the data signal to the driving transistor according to a first scan signal; a second transistor configured to apply a first power source voltage to a source electrode of the driving transistor according to a second scan signal during an initialization period for initializing a gate electrode voltage of the driving transistor; and a capacitor including a first electrode coupled to a gate electrode of the driving transistor and a second electrode coupled to a first power source supply.

[0030] A voltage difference between the gate electrode voltage and a source electrode voltage of the driving transistor during the initialization period may be a voltage for operating the driving transistor.

[0031] The first transistor may include a gate electrode for receiving the first scan signal, a source electrode for receiving the data signal, and a drain electrode coupled to the source electrode of the driving transistor, and the first transistor may be switching-operated according to the first scan signal and may be configured to transmit the data signal to the source electrode of the driving transistor.

[0032] The second scan signal may be transmitted to a second scan line preceding a first scan line receiving the first scan signal.

[0033] The pixel may further include: an initialization transistor configured to supply an initialization voltage to the gate electrode of the driving transistor during the initialization period and to initialize the gate electrode voltage of the driving transistor.

[0034] The initialization transistor may include: a gate electrode for receiving the second scan signal, a source electrode applied with the initialization voltage, and a drain electrode coupled to the gate electrode of the driving transistor, and the initialization transistor may be configured to be switching-operated according to the second scan signal.

[0035] The initialization period may be a period in which the second scan signal is transmitted to the initialization transistor at a gate-on voltage level.

[0036] The initialization period may be before a period in which a threshold voltage of the driving transistor is compensated.

[0037] The pixel may further include: a threshold voltage compensation transistor configured to be switching-operated according to the first scan signal after the initialization period and to diode-couple the driving transistor and compensate a threshold voltage of the driving transistor.

[0038] The pixel may further include: at least one light emission control transistor coupled between the first power source supply and the OLED and including a gate electrode for receiving a light emission control signal for controlling light emission of the OLED receiving the driving current according to the data signal.

[0039] The at least one light emission control signal may be transmitted at a gate-on voltage level after the first scan signal and the second scan signal are respectively transmitted at the gate-on voltage level to the first transistor and the second transistor in the pixel.

[0040] The at least one light emission control transistor may further include: a source electrode coupled to a drain electrode of the driving transistor, and a drain electrode coupled to an anode of the OLED.

[0041] The at least one light emission control transistor may further include: a source electrode coupled to the first power source supply, and a drain electrode coupled to the source electrode of the driving transistor.

[0042] According to another embodiment of the present invention, a method is provided for driving a display device including a plurality of pixels, wherein each pixel of the plurality of pixels includes: an organic light emitting diode (OLED); a driving transistor for transmitting a driving current to the OLED according to a data signal; a first transistor for transmitting the data signal to the driving transistor according to a first scan signal; a second transistor for applying a first power source voltage to the driving transistor according to a second scan signal; and a capacitor coupled between the driving transistor and a first power source supply, the method including: initializing a gate electrode voltage of the driving transistor; compensating for a threshold voltage of the driving transistor and transmitting the data signal to the driving transistor; and providing the driving current to the OLED according to the data signal to produce light emission, wherein the second scan signal is transmitted at a gate-on voltage level during the initializing the gate electrode voltage of the driving transistor.

[0043] A voltage between a gate electrode and a source electrode of the driving transistor may be a voltage for operating the driving transistor during the initializing the gate electrode voltage of the driving transistor.

[0044] The second scan signal may be transmitted to a second scan line preceding a first scan line receiving the first scan signal.

[0045] The initializing the gate electrode voltage of the driving transistor may include applying an initialization voltage to a gate electrode of the driving transistor via an initialization transistor configured to be switching-operated according to the second scan signal.

[0046] The compensating for the threshold voltage of the driving transistor may include diode-coupling the driving transistor via a threshold voltage compensation transistor configured to be switching-operated according to the first scan signal. The providing the driving current to the OLED according to the data signal to produce light

emission may include controlling the light emission of the OLED via at least one light emission control transistor coupled between the first power source supply and the OLED, and the at least one light emission control transistor may be configured to be switching-operated by a light emission control signal.

[0047] The light emission control signal may be transmitted at the gate-on voltage level after the first scan signal and the second scan signal are respectively transmitted at the gate-on voltage level to the first transistor and the second transistor.

[0048] According to the pixel and the display device including the same of embodiments of the present invention, the problem of the delay in response speed caused by hysteresis may be reduced (or solved) and the sticking on the screen may be reduced such that a grayscale may be correctly expressed.

[0049] Also, according to embodiments of the present invention, a delay in response speed may be concurrently (e.g., simultaneously) reduced (or prevented) when displaying an image according to a data signal having a large luminance variation (or deviation), while concurrently compensating for a threshold voltage variation (or deviation) of a driving transistor such that a high quality display producing high image quality may be realized.

[0050] At least some of the above and other features of the invention are set out in the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0051]

FIG. 1 is a block diagram of a display device according to an embodiment of the present invention.

FIG. 2 is a waveform diagram of a delay in response speed due to hysteresis during expression of gray levels in a conventional pixel circuit.

FIG. 3 is a circuit diagram of a pixel circuit of the display device shown in FIG. 1.

FIG. 4 is a timing diagram showing a driving operation of the pixel circuit shown in FIG. 3.

FIG. 5 is a waveform diagram showing an improved response speed in a display device according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0052] In the following detailed description, only certain embodiments of the present invention have been shown and described, simply by way of illustration. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the scope of the present invention.

[0053] Further, constituent elements having the same configurations in the embodiments are described in a first embodiment using like reference numerals, and only configurations different from those in the first embodiment will be described in other embodiments.

[0054] In addition, some of the parts that are not essential to the description are omitted for clarity, and like reference numerals designate like elements and similar constituent elements throughout the application.

[0055] Throughout this specification and the claims that follow, when it is described that an element is "coupled" to another element, the element may be "directly coupled" to the other element or "electrically coupled" to the other element through a third element. In addition, unless explicitly described to the contrary, the word "comprise" and variations such as "comprises" or "comprising" will be understood to imply the inclusion of the stated elements but not the exclusion of any other elements.

[0056] FIG. 1 is a block diagram of a display device 100 according to an embodiment of the present invention. The display device 100 includes a display unit 10 including a plurality of pixels, a scan driver 20, a data driver 30, a light emission driver 40, a controller 50, and a power source supply unit 60 supplying an external voltage to the display device.

[0057] A plurality of pixels are respectively coupled to two scan lines among a plurality of scan lines S0 to Sn for transmitting scan signals to the display unit 10. In FIG. 1, each pixel is coupled to a scan line that corresponds to a corresponding pixel row, and each pixel is also coupled to the scan line of the previous row thereof. However, embodiments of the present invention are not limited thereto.

[0058] Also, each pixel of a plurality of pixels is respectively coupled to one data line among a plurality of data lines D1 to Dm for transmitting data signals to the display unit 10, and one light emission control line among a plurality of light emission control lines EM1 to EMn for transmitting emission control signals to the display unit 10.

[0059] In this embodiment, the scan driver 20 generates and transmits two corresponding scan signals to the pixels through a plurality of scan lines SO to Sn. That is, the scan driver 20 transmits the first scan signal through the scan line corresponding to the pixel row including the pixels, and the second scan signal through the scan line corresponding to the previous pixel row.

[0060] By way of example, one pixel 70 among a plurality of pixels included in the nth pixel row is respectively coupled to the scan line Sn corresponding to the corresponding nth pixel row and the scan line Sn-1 corresponding to the previous (n-1)th pixel row.

[0061] The pixel 70 receives the first scan signal through the scan line Sn, and concurrently (e.g., simultaneously) receives the second scan signal through the scan line Sn-1.

[0062] The data driver 30 transmits a data signal to each pixel through a plurality of data lines D1 to Dm.

[0063] The light emission driver 40 generates and transmits a light emission control signal to each pixel through a plurality of light emission control lines EM1 to EMn.

[0064] The controller 50 converts (or changes) a plurality of video signals R, G, and B transmitted from an

external source into a plurality of image data signals DR, DG, and DB, and transmits them to the data driver 30. Also, the controller 50 receives a vertical synchronization signal Vsync, a horizontal synchronization signal Hsync, and a clock signal MCLK to generate control signals to control the driving of the scan driver 20, the data driver 30, and the light emission driver 40. That is, the controller 50 generates and transmits the scan driving control signal SCS controlling the scan driver 20, the data driving control signal DCS controlling the data driver 30, and the light emitting driving control signal ECS controlling the light emission driver 40.

[0065] The display unit 10 includes a plurality of pixels positioned at crossing regions of a plurality of scan lines S0 to Sn, a plurality of data lines D1 to Dm, and a plurality of light emission control lines EM1 to EMn.

[0066] The plurality of pixels are supplied with external voltages such as a first power source voltage ELVDD, a second power source voltage ELVSS, and an initialization voltage VINT from the power source supply unit 60. The first power source voltage ELVDD may have a higher voltage level than the second power source voltage ELVSS.

[0067] The display unit 10 includes a plurality of pixels arranged in an approximate matrix format. The plurality of scan lines SO to Sn extend substantially in a row in a first direction so as to be parallel to each other, and the plurality of data lines extend substantially in a column, in a second direction crossing the first direction, so as to be parallel to each other in the arrangement of the pixels. However, embodiments of the present invention are not limited thereto.

[0068] A plurality of pixels respectively emit light having a luminance (e.g., a predetermined luminance), by way of a driving current supplied to an OLED in each pixel, according to a data signal transmitted through a plurality of data lines D1 to Dm.

[0069] FIG. 2 is a waveform diagram of a delay in a response speed due to hysteresis during expression of gray levels in a conventional pixel circuit.

[0070] In a general (or conventional) pixel circuit for compensating for a threshold voltage of a driving transistor, pixels of the display unit are scanned for one frame. The vertical synchronization signal Vsync is transmitted to the scanned pixels and the scanned pixels receive the data signal Data[t] to display the images.

[0071] When the plurality of pixels of the display unit that are displayed with a black image or a white image corresponding to the data signal are driven for a long time, the voltage level applied to the driving transistor in each pixel may be maintained such that hysteresis according thereto is generated. In this case, when displaying the image of a current frame, the gray level may be shifted to the left side or the right side of a TFT characteristic curve by an influence of the gray voltage of the previous frame.

[0072] For example, when the pixels are driven with the black image for a long time, the voltage level applied to the driving transistor is an off-bias voltage that is less than an operation reference voltage of the driving transistor. Accordingly, the gray level according to the video signal of the next frame is shifted to the right side of the TFT characteristic curve. In contrast, when the pixels are driven with the white image for a long time, the voltage level applied to the driving transistor is an on-bias voltage that is more than the operation reference voltage of the driving transistor, and thereby the gray level according to the video signal of the next frame is shifted to the left side of the TFT characteristic curve.

[0073] Accordingly, the response speeds may be different according to the change in the amount of the luminance between the previous frame and the current frame, due to the hysteresis of the driving transistor of the pixel when displaying the same luminance. These response speeds may vary (e.g., deteriorate) according to the application time of the off-bias voltage or the on-bias voltage applied to the driving transistor.

[0074] Accordingly, improvement of the pixel circuit to concurrently (e.g., simultaneously) address (or solve) the response speed problem due to hysteresis while compensating for a threshold voltage variation (or deviation) of a transistor in the pixel is needed.

[0075] In the waveform diagram of FIG. 2, a pixel that is displayed with a black luminance for a long time according to a black data signal Data[t] receives a white data signal emitting light with a white luminance, at the time a1. As shown in FIG. 2, the pixel does not immediately emit light having luminance target values corresponding to the white data signal at the time a1, when the white data signal is first transmitted, but emits light having the luminance target values at the time a2 after one frame has passed.

[0076] When driving the pixel to display images from black to white, in one frame the light may not reach (or may not be increased to) the target value of the white luminance, and may only arrive at a middle luminance. Therefore, the response speed may be delayed compared with the case where the pixel is driven to display the image from white to white. The delay in the response speed due to this hysteresis is manifest (or represented) as sticking during text scrolling of the display screen.

[0077] A pixel circuit structure and a driving method according to an embodiment of the present invention address (or solve) the problem of the delay in response speed caused by hysteresis.

[0078] FIG. 3 is a circuit diagram showing a circuit structure of a pixel 70 of the display device 100 shown in FIG. 1.

[0079] Each pixel in this embodiment of the present invention is coupled to a first scan line and a second scan line. The second scan line applies an initialization voltage VINT to a driving transistor Md in the pixel during an initialization period and transmits a second scan signal controlling the driving transistor Md to maintain it with the operation voltage (on-bias voltage). The first scan line transmits a first scan signal to activate the pixel to trans-

mit the data signal.

[0080] The pixel 70 shown in FIG. 3 is respectively coupled to the nth scan line Sn and the (n-1)th scan line Sn-1 among a plurality of pixels included in the display unit 10 of the display device 100 of FIG. 1. Also, the pixel 70 is coupled to the mth data line Dm and the nth light emission control line EMn.

[0081] The pixel 70 shown in FIG. 3 includes an OLED; a driving transistor Md coupled to an anode of the OLED; a first transistor M1 coupled to the source electrode of the driving transistor Md; a second transistor M2, which has one electrode coupled to a node N2 that is coupled to the driving transistor Md and the first transistor M1, and another electrode that is coupled to the first power source voltage ELVDD; and a capacitor C1 between the driving transistor Md and the first power source voltage ELVDD.

[0082] The pixel 70 further includes an initialization transistor M3 for transmitting the initialization voltage VINT during the initialization period.

[0083] The pixel 70 further includes a threshold voltage compensation transistor M4 diode-coupling the driving transistor Md to compensate for the threshold voltage of the driving transistor Md.

[0084] Also, the pixel 70 further includes light emission control transistor coupled to the anode of the OLED and controlling light emission according to the driving current of the OLED. The light emission control transistors included in the pixel 70 of FIG. 3 include a first light emission control transistor M5 coupled between the anode of the OLED and the driving transistor Md, and a second light emission control transistor M6 coupled between the driving transistor Md and the first power source voltage ELVDD.

[0085] The OLED of the pixel 70 has an anode and a cathode, and emits light as a result of the driving current corresponding to a corresponding data signal. The driving current corresponding to the data signal is compensated for, so as not to be affected by the variations in threshold voltage of the driving transistor included in each of the pixels of the display unit 10.

[0086] The driving transistor Md includes a source electrode coupled to the second node N2 to which the first power source voltage ELVDD is coupled, a drain electrode coupled to a third node N3, and a gate electrode coupled to the first node N1. The driving transistor Md receives the data signal through the first transistor M1 coupled to the second node N2.

[0087] The driving transistor Md transmits the driving current corresponding to the voltage difference between its source electrode and its gate electrode to the OLED for light emission.

[0088] The first transistor M1 includes a source electrode coupled to the data line Dm and transmitting the data signal, a drain electrode coupled to the second node N2, and a gate electrode coupled to the scan line Sn corresponding to the pixel row including the pixel 70 and transmitting the scan signal S[n]. Here, the pixel 70 is included in the nth pixel row such that the corresponding scan line is the nth scan line.

[0089] If the scan signal S[n] is transmitted through the nth scan line such that the first transistor M1 is turned on, the data signal is transmitted to the second node N2, and the data voltage Vdata corresponding to the data signal is transmitted to the source electrode of the driving transistor Md.

[0090] The scan signal S[n] is also concurrently (e.g., simultaneously) transmitted to the gate electrode of the threshold voltage compensation transistor M4.

[0091] The threshold voltage compensation transistor M4 is coupled between the gate electrode and the drain electrode of the driving transistor Md, and is turned on during the time that the scan signal S[n] is transmitted as the gate-on voltage level to diode-couple the driving transistor Md. Thus, a data voltage Vdata applied to the source electrode of the driving transistor Md is reduced by the threshold voltage of the driving transistor Md such that a voltage Vdata-Vth is applied to the gate electrode of the driving transistor Md. The gate electrode of the driving transistor Md is coupled to one terminal of the capacitor C1 such that the voltage Vdata-Vth is maintained by the capacitor C1. The voltage Vdata-Vth reflecting the threshold voltage Vth of the driving transistor Md is applied to the gate electrode of the driving transistor Md and is maintained such that the driving current flowing in the driving transistor Md is not affected by variations in the threshold voltage of the driving transistor Md.

[0092] The second transistor M2 includes a gate electrode coupled to the (n-1)th scan line and receiving the scan signal S[n-1], a source electrode coupled to the first power source voltage ELVDD, and a drain electrode coupled to the second node N2.

[0093] The second transistor M2 is turned on by the scan signal S[n-1], which is transmitted at a gate-on voltage level through the (n-1)th scan line before the scan signal S[n] is transmitted to the pixel 70 through the nth scan line at the gate-on voltage level. Thus, the first power source voltage ELVDD is applied to the source electrode of the driving transistor Md during the period in which the driving transistor Md is switched on by the scan signal S[n-1].

[0094] The initialization transistor M3 transmitting the initialization voltage VINT to the gate electrode of the driving transistor Md is switching-operated by the scan signal S[n-1].

[0095] The initialization transistor M3 includes a gate electrode coupled to the (n-1)th scan line, a source electrode coupled to the voltage source transmitting the initialization voltage VINT, and a drain electrode coupled to the gate electrode of the driving transistor Md.

[0096] The initialization voltage VINT is applied to the gate electrode of the driving transistor Md during the time that the scan signal S[n-1] is transmitted to the initialization transistor M3 as the gate-on voltage level. The gate electrode of the driving transistor Md is initialized at the initialization voltage VINT during a period in which the

scan signal S[n-1] is transmitted at the gate-on voltage level.

[0097] During the initialization period in which the scan signal S[n-1] is transmitted at the gate-on voltage level, the source electrode of the driving transistor Md is applied with the first power source voltage ELVDD, and concurrently (e.g., simultaneously) the gate electrode of the driving transistor Md is applied with the initialization voltage VINT, and thereby the voltage difference Vgs between the gate and the source of the driving transistor Md during the initialization period becomes ELVDD-VINT. This is a voltage value that is greater than the reference voltage at which the driving transistor Md is operated.

[0098] The voltage difference Vgs between the gate and the source of the driving transistor Md during the initialization period is more than the reference voltage such that the driving transistor Md is on-biased.

[0099] The data voltage is written to the driving transistor Md during the state in which the driving transistors Md of all of the pixels are on-biased, and thereby the hysteresis characteristic may be improved.

[0100] When a plurality of driving transistors are applied with the data voltage of the previous frame, the gate-source voltage of each driving transistor may be at a different level than the gate-source voltage of each driving transistor in the current frame, before the data voltage of the current frame is written.

[0101] If there is no initialization period, the hysteresis characteristic of the gate-source voltage of each driving transistor may be different depending on whether the data voltage of the current frame is a higher or lower voltage than the data voltage of the previous frame. In this embodiment of the present invention, the gate-source voltage of each driving transistor during the initialization period becomes ELVDD-VINT such that all of the driving transistors are on-biased with the same condition (e.g., all of the driving transistors have the same gate-source voltage).

[0102] Accordingly, the gate-source voltage of the driving transistors of all pixels is determined according to the data voltage of the current frame in the same conditions without the effect of the hysteresis characteristic.

[0103] In this embodiment of the present invention, the signal controlling the switching operation of the second transistor M2 and the initialization transistor M3 uses the scan signal transmitted through the previous scan line of the scan line coupled to the corresponding pixel row, however it is not limited thereto and an additional control signal may be transmitted.

[0104] On the other hand, in the case of the pixel included in the first pixel row, the scan signal transmitted to the second transistor M2 and the initialization transistor M3 may be a dummy scan signal that is generated and transmitted from the scan driver 20.

[0105] For example, the capacitor C1 includes a first electrode coupled to the first node N1 and a second electrode coupled to the first power source voltage ELVDD.

[0106] The capacitor C1 is coupled to the first node N1 to which the gate electrode of the driving transistor Md is coupled, thereby storing the voltage value of the gate electrode of the driving transistor Md according to the driving process of the pixel.

[0107] Also, the first light emission control transistor M5 of the pixel 70 includes a gate electrode coupled to the nth light emission control line and receiving the light emission control signal EM[n], a source electrode coupled to the third node N3, and a drain electrode organic coupled to the anode of the light emitting diode OLED.

[0108] The pixel 70 includes the second light emission control transistor M6, and the second light emission control transistor M6 has a gate electrode coupled to the nth light emission control line and receiving the light emission control signal EM[n], a source electrode coupled to the first power source voltage ELVDD, and a drain electrode coupled to the second node N2.

[0109] The light emission control transistor of this embodiment of the present invention is only one example and the pixel circuit configuration is not limited thereto.

[0110] If the light emission control signal EM[n] is transmitted at the gate-on voltage level, the first light emission control transistor M5 and the second light emission control transistor M6 are turned on. The driving current corresponding to the data voltage stored in the capacitor C1 is transmitted to the OLED according to the data signal and during the data writing period, such that light is emitted. As described above, the data voltage stored to the capacitor C1 is the voltage value Vdata-Vth reflecting the threshold voltage Vth such that the effect of variations in the threshold voltage is reduced when light emission occurs due to the corresponding driving current.

[0111] Although the transistors included in the driving circuit of the pixel shown in FIG. 3 are PMOS transistors, embodiments of the present invention are not limited thereto, and the transistors may be realized as NMOS transistors.

[0112] A driving timing diagram is shown in FIG. 4 for comprehension of the driving of the pixel 70 shown in FIG. 3.

[0113] The pixel 70 is coupled to two scan lines to receive the scan signals and be operated.

[0114] First, the scan signal S[n-1] is transmitted through the (n-1)th scan line and is transitioned (or changed) to a low level at the time t1 and maintains the low level during the period T1.

[0115] Accordingly, the second transistor M2 and the initialization transistor M3 receiving the scan signal S[n-1] in the pixel are concurrently (e.g., simultaneously) turned on.

[0116] The first power source voltage ELVDD having a high level voltage is applied to the source electrode of the driving transistor Md through the second transistor M2 during the period T1, and the initialization voltage VINT is applied to the gate electrode of the driving transistor Md through the initialization transistor M3.

[0117] The gate-source voltage difference Vgs of the driving transistor Md is maintained as ELVDD-VINT dur-

ing the period T1. At this time, the initialization voltage VINT is at a low level such that the voltage difference Vgs may be more than a minimum reference voltage for operating the driving transistor Md. Accordingly, the driving transistors Md included in all of the pixels are on-biased before the period in which the threshold voltage of the driving transistor Md is compensated for and the data is written in each frame. Accordingly, an image that is displayed with the desired gray level may be realized regardless of the hysteresis characteristic of the driving transistor Md.

[0118] Next, the scan signal S[n-1] is transitioned to a high level at the time t2, and the scan signal S[n] transmitted through the nth scan line is transitioned (or changed) to a low level at the time t3 and maintains the low level during the period T2.

[0119] The scan signal S[n-1] is transmitted at the high level (or maintains the high state) during the period T2 such that the second transistor M2 and the initialization transistor M3 are turned off, and the first node N1 is floating.

[0120] Concurrently (e.g., simultaneously), the first transistor M1 and the threshold voltage compensation transistor M4 receiving the scan signal S[n] in the pixel during period T2 are turned on. Thus, the data voltage Vdata according to the data signal DATA is transmitted to the source electrode of the driving transistor Md through the first transistor M1 during the period T2, and the driving transistor Md is diode-coupled with the threshold voltage compensation transistor M4.

[0121] Accordingly, the voltage maintained at the first node N1 coupled to one terminal of the capacitor C1 during the period T2 is the voltage Vgs. The voltage Vgs corresponds to the voltage difference between gate and source electrodes of the driving transistor Md, and is represented by the voltage value Vdata-Vth, which is the data voltage Vdata reduced by the threshold voltage Vth of the driving transistor Md.

[0122] The driving transistor Md is on-biased during the initialization period of the period T1 such that the hysteresis characteristic may be reduced (or improved), and thereby the delay problem of the response speed may be improved (or solved) during the expression of gray levels according to the data voltage Vdata.

[0123] When the scan signal S[n] is transitioned to a high level at the time t4, the first transistor M1 and the threshold voltage compensation transistor M4 are turned off. Thus, the first node N1 is again floating.

[0124] The light emission control signal EM[n] transmitted to the pixel 70 included in the nth pixel row is transitioned (or changed) to the low level at the time t5.

[0125] Thus, the first light emission control transistor M5 and the second light emission control transistor M6 receiving the light emission control signal EM[n] of the pixel 70 are turned on, and the driving current stored to the capacitor C1 and corresponding to the data voltage according to the data signal is transmitted to the OLED for light emission.

[0126] The voltage value for calculating the driving current is the corresponding voltage ELVDD-Vdata, excluding the effect of the threshold voltage Vth of the driving transistor Md.

[0127] The pixel and the display device including the same according to an embodiment of the present invention may concurrently (e.g., simultaneously) reduce (or solve the problem of) the delay in the response speed due to hysteresis while reducing (or excluding) the effect of variations in the threshold voltage of the driving transistor when displaying the image according to the data signal, such that the response speed is not delayed and light is emitted with the desired luminance in the corresponding frame as shown in the waveform diagram in FIG. 5. As a result, a clear and high quality image may be provided.

[0128] Referring to the waveform diagram of FIG. 5, if the display device is driven using a conventional pixel, the light is not emitted with the desired luminance due to hysteresis, but is displayed with a luminance of a middle degree, and then the light is emitted with a normal luminance in the next frame. However, if the display device is driven through a pixel according to embodiments of the present invention, an improved waveform displaying an improved luminance (e.g., a desired luminance) in the corresponding frame may be obtained.

[0129] Although the present invention is described with reference to detailed embodiments of the present invention, this is by way of example only and the present invention is not limited thereto. A person of ordinary skill in the art may change or modify the described embodiments without departing from the scope of the present invention, and the changes or modifications are also included in the scope of the present invention. Further, materials of each of the components described in the present specification may be selected from or replaced by various materials known to a person of ordinary skill in the art. In addition, a person of ordinary skill in the art may omit some of the components described in the present application without deteriorating the performance, or may add components in order to improve the performance. Further, a person of ordinary skill in the art may change a sequence of processes described in the present application, according to the process environments or equipment. Therefore, while the present invention has been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the scope of the appended claims, and equivalents thereof.

Claims

1. A display panel comprising a plurality of pixels arranged in rows, each row of pixels having a corresponding scan line,

each pixel comprising:

an organic light emitting diode (OLED);
a driving transistor (Md) comprising a drain electrode directly coupled to the OLED;
a first transistor (M1) comprising a gate electrode directly coupled to a first scan line (Sn), a source electrode for receiving a data signal, and a drain electrode directly coupled to the source electrode of the driving transistor;
a second transistor (M2) comprising a gate electrode directly coupled to a second scan line (Sn-1) corresponding to the scan line preceding the first scan line, a source electrode directly coupled to a first power source supply (ELVDD), and a drain electrode directly coupled to the source electrode of the driving transistor;
a capacitor
(C1) comprising a first electrode directly coupled to a gate electrode of the driving transistor and a second electrode directly coupled to the first power source supply (ELVDD);
an initialization transistor (M3) comprising a gate electrode directly coupled to the second scan line (Sn-1), a source electrode for receiving an initialization voltage (VINT), and a drain electrode directly coupled to the gate electrode of the driving transistor, and
a threshold voltage compensation transistor (M4) comprising a gate electrode directly coupled to the first scan line (Sn), a source electrode directly coupled to the drain electrode of the driving transistor (Md), and a drain electrode directly coupled to the gate electrode of the driving transistor (Md);

wherein rows of pixels sequentially receive scan signals in each frame, and wherein within each frame a second scan signal is transmitted to the second scan line preceding a first scan signal being transmitted to the first scan line.

2. The pixel according to claim 1,
wherein the driving transistor is adapted to be operated by a voltage difference between a gate electrode voltage and a source electrode voltage of the driving transistor during an initialization period, and wherein the initialization period is a period in which the second scan signal is transmitted to the second scan line at a gate-on voltage level.

3. The pixel according to claim 1, wherein
the initialization period is before a period in which a threshold voltage of the driving transistor is compensated.

4. The pixel according to claim 1, further comprising:

at least one light emission control transistor (M5, M6) coupled between the first power source supply and the OLED and comprising a gate electrode for receiving a light emission control signal.

5. The pixel according to claim 4, wherein
the at least one light emission control transistor is configured to be operated according to the light emission control signal transmitted at a gate-on voltage level after the first scan signal and the second scan signal are respectively transmitted at the gate-on voltage level to the first transistor and the second transistor in the pixel.

6. The pixel according to claim 5, wherein
the at least one light emission control transistor (M5) further comprises: a source electrode electrically connected to a drain electrode of the driving transistor, and a drain electrode electrically connected to an anode of the OLED.

7. The pixel according to claim 5, wherein
the at least one light emission control transistor (M6) further comprises: a source electrode electrically connected to the first power source supply, and a drain electrode electrically connected to the source electrode of the driving transistor.

8. A display device comprising:

a display unit comprising a plurality of pixels respectively coupled to a plurality of scan lines for transmitting a plurality of scan signals, a plurality of data lines for transmitting a plurality of data signals, and a plurality of light emission control lines for transmitting a plurality of light emission control signals;
a scan driver for transmitting the plurality of scan signals;
a data driver for transmitting the plurality of data signals; and
a light emission driver for transmitting the plurality of light emission control signals,

wherein at least one of the pixels is as set out in one of Claims 1 to 7.

9. The display device according to claim 8, wherein
the scan driver is configured to transmit the first scan signal and the second scan signal to the plurality of pixels.

10. A method of driving a display device comprising a plurality of pixels arranged in rows, each row of pixels having a corresponding scan line, wherein each pixel of the plurality of pixels comprises: an organic light emitting diode (OLED); a driving transistor (Md) comprising a drain electrode directly coupled to the

OLED; a first transistor (M1) comprising a gate electrode directly coupled to a first scan line (Sn), a source electrode for receiving a data signal, and a drain electrode directly coupled to a source electrode of the driving transistor (Md); a second transistor (M2) comprising a gate electrode directly coupled to a second scan line (Sn-1) corresponding to the scan line preceding the first scan line (Sn), a source electrode directly coupled to a first power source supply (ELVDD), and a drain electrode directly coupled to the source electrode of the driving transistor (Md); a capacitor (C1) comprising a first electrode directly coupled to a gate electrode of the driving transistor (Md) and a second electrode directly coupled to the first power source supply (ELVDD); an initialization transistor (M3) comprising a gate electrode directly coupled to the second scan line (Sn-1), a source electrode for receiving an initialization voltage (VINT), and a drain electrode directly coupled to the gate electrode of the driving transistor, and a threshold voltage compensation transistor (M4) comprising a gate electrode directly coupled to the first scan line (Sn), a source electrode directly coupled to the drain electrode of the driving transistor (Md), and a drain electrode directly coupled to the gate electrode of the driving transistor (Md); wherein rows of pixels sequentially receive scan signals in each frame, the method comprising:

transmitting a second scan signal to the second scan line (Sn-1) within each frame; and
transmitting a first scan signal to the first scan line (Sn) after transmitting the second scan signal within each frame.

11. The method according to claim 10, wherein the driving transistor is adapted to be operated by a voltage difference between a gate electrode voltage and a source electrode voltage of the driving transistor during an initialization period, and wherein the initialization period is a period in which the second scan signal is transmitted to the second scan line at a gate-on voltage level.

12. The method according to claim 11, wherein the initialization period is before a period in which a threshold voltage of the driving transistor is compensated.

13. The method according to claim 10, wherein the each pixel of the plurality of pixels further comprising at least one light emission control transistor (M5, M6) coupled between the first power source supply and the OLED and comprising a gate electrode for receiving a light emission control signal, the method further comprising:

transmitting the light emission control signal after transmitting the first scan signal.

Patentansprüche

1. Anzeigetafel umfassend eine Anzahl von in Spalten angeordneten Pixeln, wobei jeder Pixelspalte eine entsprechende Scanleitung zugeordnet ist, und wobei jedes Pixel umfasst:

eine organische Leuchtdiode (OLED);
einen Treibertransistor (Md) mit einer Drain-Elektrode, die direkt mit der OLED gekoppelt ist;
einen ersten Transistor (M1) mit einer Gate-Elektrode, die direkt mit einer ersten Scanleitung (Sn) gekoppelt ist, eine Source-Elektrode zum Empfangen von Datensignalen, und eine Drain-Elektrode, die direkt mit der Source-Elektrode des Treibertransistors gekoppelt ist;
einem zweiten Transistor (M2) umfassend eine Gate-Elektrode, die direkt mit einer zweiten Scanleitung (Sn-1) gekoppelt ist, welche der der ersten Scanleitung vorausgehenden Scanleitung entspricht, eine Source-Elektrode, die direkt mit einer ersten Stromversorgungsquelle (ELVDD) gekoppelt ist, und eine Drain-Elektrode, die direkt mit der Source-Elektrode des Treibertransistors gekoppelt ist;
einen Kondensator (C1) umfassend eine erste Elektrode, die direkt mit einer Gate-Elektrode des Treibertransistors gekoppelt ist und eine zweite Elektrode, die direkt mit der ersten Stromversorgungsquelle (ELVDD) gekoppelt ist;
einem Initialisierungstransistor (M3) umfassend eine Gate-Elektrode, die direkt mit der zweiten Scanleitung (Sn-1) gekoppelt ist, eine Source-Elektrode zur Aufnahme einer Initialisierungsspannung (VINT) und eine Drain-Elektrode, die direkt mit der Gate-Elektrode des Treibertransistors gekoppelt ist, und
einen Transistor zur Spannungsschwellwert-Kompensation (M4) umfassend eine Gate-Elektrode, die direkt mit der ersten Scanleitung (Sn) gekoppelt ist, eine Source-Elektrode, die direkt mit der Drain-Elektrode des Treibertransistors (Md) gekoppelt ist, und eine Drain-Elektrode, die direkt mit dem Gate-Elektrode des Treibertransistors (Md) gekoppelt ist;

wobei die Pixelspalten in jedem Frame Scansignale sequentiell empfangen, und wobei innerhalb eines Frames an die zweite Scanleitung ein zweites Scansignal übertragen wird, dass einem ersten, an die erste Scanleitung übertragenen Scansignal vorausgeht.

2. Pixel nach Anspruch 1, wobei der Treibertransistor so eingestellt ist, dass dieser in Abhängigkeit von

einer Spannungsdifferenz zwischen Gate-Elektroden-Spannung und Source-Elektroden-Spannung des Treibertransistors während einer Initialisierungszeit betrieben wird, und
wobei die Initialisierungszeit eine Zeitspanne darstellt, in der die Übertragung des zweiten Scansignals auf die zweite Scanleitung mit einem Gate-On-Spannungspegel erfolgt.

3. Pixel nach Anspruch 1, wobei die Initialisierungszeit vor einer Zeitspanne liegt, in der eine Spannungsschwellwert des Treibertransistors kompensiert wird.

4. Pixel nach Anspruch 1, ferner umfassend:

mindestens einen Lichtemissionssteuertransistor (M5, M6), der zwischen die erste Stromversorgungsquelle und die OLED gekoppelt ist, sowie eine Gate-Elektrode zum Empfangen eines Lichtemissions-Steuersignals.

5. Pixel nach Anspruch 4, wobei mindestens ein Lichtemissionssteuertransistor so ausgelegt ist, dass dieser über das Lichtemissionssteuersignal mit einem Gate-On-Spannungspegel angesteuert wird, nachdem das erste Scansignal und das zweite Scansignal jeweils mit dem Gate-On-Spannungspegel an den ersten Transistor und den zweiten Transistor in dem Pixel übertragen wurden.

6. Pixel nach Anspruch 5, wobei mindestens ein Lichtemissionssteuertransistor (M5) ferner umfasst:

eine Source-Elektrode, die elektrisch mit einer Drain-Elektrode des Treibertransistors verbunden ist, und wobei eine Drain-Elektrode elektrisch mit einer Anode der OLED verbunden ist.

7. Pixel nach Anspruch 5, wobei der mindestens eine Lichtemissionssteuertransistor (M6) ferner umfasst:

eine Source-Elektrode, die elektrisch mit der ersten Stromversorgungsquelle Leistungsspannungsquelle verbunden ist, und eine Drain-Elektrode, die mit der Source-Elektrode des Treibertransistors elektrisch verbunden ist.

8. Anzeigevorrichtung umfassend:

eine Anzeigeeinheit umfassend eine Anzahl von Pixeln, die jeweils mit einer Anzahl von Scanleitungen zur Übertragung einer Anzahl von Scansignalen gekoppelt sind, eine Anzahl von Datenleitungen zur Übertragung einer Anzahl von Datensignalen, sowie eine Anzahl von Lichtübertragungsleitungen zur Übertragung einer Anzahl von Lichtemissionssteuersignalen;

einen Scantreiber zur Übertragung der Anzahl von Scansignalen;
einen Datentreiber zur Übertragung der Anzahl von Datensignalen; und
einen Lichtemissionstreiber zur Übertragung der Anzahl von Lichtemissionssteuersignalen,

wobei mindestens eines der Pixel so beschaffen ist, wie in einem der Ansprüche 1 bis 7 ausgeführt.

9. Anzeigevorrichtung nach Anspruch 8, wobei der Scantreiber so konfiguriert ist, dass das erste Scansignal und das zweite Scansignal zu der Anzahl von Pixeln übertragen werden.

10. Verfahren zur Ansteuerung einer Anzeigevorrichtung umfassend eine Anzahl von in Spalten angeordneten Pixeln, wobei jeder Pixelspalte eine entsprechende Scanleitung zugeordnet ist, und wobei jedes Pixel der Anzahl von Pixeln folgendes umfasst: eine organische Leuchtdiode (OLED); einen Treibertransistor (Md), der eine Drain-Elektrode umfasst, die direkt mit der OLED gekoppelt ist; einen ersten Transistor (M1), der eine Gate-Elektrode umfasst, die direkt mit der ersten Scanleitung (Sn) gekoppelt ist, eine Source-Elektrode zum Empfangen eines Datensignals und eine Drain-Elektrode, die mit der Source-Elektrode des Treibertransistors (Md) direkt gekoppelt ist; einen zweiten Transistor (M2), der eine Gate-Elektrode umfasst, die direkt mit einer zweiten Scanleitung (Sn-1) gekoppelt ist, die der der ersten Scanleitung vorausgehenden Scanleitung entspricht, eine Source-Elektrode, die direkt mit einer ersten Stromversorgungsquelle (ELVDD) direkt gekoppelt ist, und eine Drain-Elektrode, die mit dem Source-Elektrode des Treibertransistors direkt gekoppelt ist; einen Kondensator (C1), der eine erste Elektrode umfasst, die direkt mit der Gate-Elektrode des Treibertransistors (Md) gekoppelt ist, und eine zweite Elektrode, die mit der ersten Stromversorgungsquelle (ELVDD) direkt gekoppelt ist; einen Initialisierungstransistor (M3), der eine Gate-Elektrode umfasst, die direkt mit der zweiten Scanleitung (Sn-1) gekoppelt ist, eine Source-Elektrode zur Aufnahme einer Initialisierungsspannung (VINT) und eine Drain-Elektrode, die direkt mit der Gate-Elektrode des Treibertransistors gekoppelt ist, und einen Transistor (M4) zur Spannungsschwellwert-Kompensation, der eine Gate-Elektrode umfasst, die direkt mit der ersten Scanleitung (Sn) gekoppelt ist, eine Source-Elektrode, die direkt mit der Drain-Elektrode des Treibertransistors (Md) gekoppelt ist, und eine Drain-Elektrode, der mit dem Gate-Elektrode des Treibertransistors (Md) direkt gekoppelt ist; wobei die Pixelspalten die Scansignale in jedem Frame sequentiell empfangen, wobei das Verfahren Folgendes umfasst:

Übertragen eines zweiten Scansignals zur zweiten Scanleitung (Sn-1) innerhalb jedes Frames; und
Übertragen eines ersten Scansignals zur ersten Scanleitung (Sn) nach erfolgter Übertragung des zweiten Scansignals innerhalb jedes Frames.

11. Verfahren nach Anspruch 10, wobei der Treibertransistor so ausgestaltet ist, dass dieser in Abhängigkeit von einer Spannungsdifferenz zwischen Gate-Elektroden-Spannung und Source-Elektroden-Spannung des Treibertransistors während einer Initialisierungszeit betrieben wird, und
wobei die Initialisierungszeit eine Zeitspanne darstellt, in der die Übertragung des zweiten Scansignals auf die zweite Scanleitung mit einem Gate-On-Spannungspegel erfolgt.

12. Verfahren nach Anspruch 11,
wobei die Initialisierungszeit vor einer Zeitspanne liegt, in der eine Schwellspannung des Treibertransistors kompensiert wird

13. Verfahren nach Anspruch 10, wobei jedes der Pixel der Anzahl von Pixeln ferner mindestens einen Lichtemissionssteuertransistor (M5, M6), der zwischen die erste Leistungsspannungsquelle und die OLED gekoppelt ist, und eine Gate-Elektrode zum Empfangen eines Lichtemissions-Steuersignals umfasst, wobei das Verfahren ferner umfasst:

Übertragen des Lichtemissionssteuersignals nach Übertragung des ersten Scansignals.

Revendications

1. Panneau d'affichage comprenant une pluralité de pixels agencés en rangées, chaque rangée de pixels ayant une ligne de balayage correspondante, chaque pixel comprenant :

une diode électroluminescente organique (OLED) ;
un transistor d'attaque (Md) comprenant une électrode de drain directement couplée à la diode OLED ;
un premier transistor (M1) comprenant une électrode de grille directement couplée à une première ligne de balayage (Sn), une électrode de source pour recevoir un signal de données et une électrode de drain directement couplée à l'électrode de source du transistor d'attaque ;
un deuxième transistor (M2) comprenant une électrode de grille directement couplée à une deuxième ligne de balayage (Sn-1) correspondant à la ligne de balayage précédant la première ligne de balayage, une électrode de source directement couplée à une première alimentation de source électrique (ELVDD), et une électrode de drain directement couplée à l'électrode de source du transistor d'attaque ;
un condensateur (C1) comprenant une première électrode directement couplée à une électrode de grille du transistor d'attaque et une deuxième électrode directement couplée à la première alimentation de source de puissance (ELVDD) ;
un transistor d'initialisation (M3) comprenant une électrode de grille directement couplée à la deuxième ligne de balayage (Sn-1), une électrode de source pour recevoir une tension d'initialisation (VINT), et une électrode de drain directement couplée à l'électrode de grille du transistor d'attaque, et
un transistor de compensation de tension de seuil (M4) comprenant une électrode de grille directement couplée à la première ligne de balayage (Sn), une électrode de source directement couplée à l'électrode de drain du transistor d'attaque (Md), et une électrode de drain directement couplée à l'électrode de grille du transistor d'attaque (Md) ;

dans lequel des rangées de pixels reçoivent séquentiellement des signaux de balayage dans chaque trame, et
dans lequel, dans chaque trame, un deuxième signal de balayage est transmis à la deuxième ligne de balayage précédant un premier signal de balayage étant transmis à la première ligne de balayage.

2. Pixel selon la revendication 1,
dans lequel le transistor d'attaque est adapté à être actionné par une différence de tension entre une tension d'électrode de grille et une tension d'électrode de source du transistor d'attaque pendant une période d'initialisation, et
dans lequel la période d'initialisation est une période pendant laquelle le deuxième signal de balayage est transmis à la deuxième ligne de balayage à un niveau de tension d'activation de grille.

3. Pixel selon la revendication 1, dans lequel :

la période d'initialisation est antérieure à une période pendant laquelle une tension de seuil du transistor d'attaque est compensée.

4. Pixel selon la revendication 1, comprenant en outre :

au moins un transistor de commande d'émission de lumière (M5, M6) couplé entre la première alimentation de source de puissance et la diode OLED et comprenant une électrode de grille pour recevoir un signal de commande d'émis-

sion de lumière.

5. Pixel selon la revendication 4, dans lequel :

l'au moins un transistor de commande d'émission de lumière est configuré pour être actionné en fonction du signal de commande d'émission de lumière transmis à un niveau de tension d'activation de grille après la transmission respective du premier signal de balayage et du deuxième signal de balayage au niveau de tension d'activation de grille au premier transistor et au deuxième transistor dans le pixel.

6. Pixel selon la revendication 5, dans lequel l'au moins un transistor de commande d'émission de lumière (M5) comprend en outre :

une électrode de source reliée électriquement à une électrode de drain du transistor d'attaque, et une électrode de drain reliée électriquement à une anode de la diode OLED.

7. Pixel selon la revendication 5, dans lequel l'au moins un transistor de commande d'émission de lumière (M6) comprend en outre :

une électrode de source reliée électriquement à la première alimentation de source de puissance, et une électrode de drain reliée électriquement à l'électrode de source du transistor d'attaque.

8. Dispositif d'affichage comprenant :

une unité d'affichage comprenant une pluralité de pixels couplés respectivement à une pluralité de lignes de balayage pour transmettre une pluralité de signaux de balayage, une pluralité de lignes de données pour transmettre une pluralité de signaux de données, et une pluralité de lignes de commande d'émission de lumière pour transmettre une pluralité de signaux de commande d'émission de lumière ;
un pilote de balayage pour transmettre la pluralité de signaux de balayage ;
un pilote de données pour transmettre la pluralité de signaux de données ; et
un pilote d'émission de lumière pour transmettre la pluralité de signaux de commande d'émission de lumière,

dans lequel au moins l'un des pixels est tel que défini dans l'une des revendications 1 à 7.

9. Dispositif d'affichage selon la revendication 8, dans lequel :

le pilote de balayage est configuré pour transmettre le premier signal de balayage et le deuxième signal de balayage à la pluralité de pixels.

10. Procédé de commande d'un dispositif d'affichage comprenant une pluralité de pixels agencés en rangées, chaque rangée de pixels ayant une ligne de balayage correspondante, dans lequel chaque pixel de la pluralité de pixels comprend :

une diode électroluminescente organique (OLED) ; un transistor d'attaque (Md) comprenant une électrode de drain directement couplée à la diode OLED ; un premier transistor (M1) comprenant une électrode de grille directement couplée à une première ligne de balayage (Sn), une électrode de source pour recevoir un signal de données, et une électrode de drain directement couplée à une électrode de source du transistor d'attaque (Md) ; un deuxième transistor (M2) comprenant une électrode de grille directement couplée à une deuxième ligne de balayage (Sn-1) correspondant à la ligne de balayage précédant la première ligne de balayage (Sn), une électrode de source directement couplée à une première alimentation de source de puissance (ELVDD), et une électrode de drain directement couplée à l'électrode de source du transistor d'attaque (Md) ; un condensateur (C1) comprenant une première électrode directement couplée à une électrode de grille du transistor d'attaque (Md) et une deuxième électrode directement couplée à la première alimentation de source de puissance (ELVDD) ; un transistor d'initialisation (M3) comprenant une électrode de grille directement couplée à la deuxième ligne de balayage (Sn-1), une électrode de source pour recevoir une tension d'initialisation (VINT), et une électrode de drain directement couplée à l'électrode de grille du transistor d'attaque, et un transistor de compensation de tension de seuil (M4) comprenant une électrode de grille directement couplée à la première ligne de balayage (Sn), une électrode de source directement couplée à l'électrode de drain du transistor d'attaque (Md), et une électrode de drain directement couplée à l'électrode de grille du transistor d'attaque (Md) ; où des rangées de pixels reçoivent séquentiellement des signaux de balayage dans chaque trame, le procédé consistant à :

transmettre un deuxième signal de balayage à la deuxième ligne de balayage (Sn-1) dans chaque trame ; et
transmettre un premier signal de balayage à la première ligne de balayage (Sn) après

avoir transmis le deuxième signal de balayage dans chaque trame.

11. Procédé selon la revendication 10, dans lequel le transistor d'attaque est adapté pour être actionné par une différence de tension entre une tension d'électrode de grille et une tension d'électrode de source du transistor d'attaque pendant une période d'initialisation, et
dans lequel la période d'initialisation est une période pendant laquelle le deuxième signal de balayage est transmis à la deuxième ligne de balayage à un niveau de tension d'activation de grille.

12. Procédé selon la revendication 11, dans lequel la période d'initialisation est antérieure à une période pendant laquelle une tension de seuil du transistor d'attaque est compensée.

13. Procédé selon la revendication 10, dans lequel chaque pixel de la pluralité de pixels comprenant en outre au moins un transistor de commande d'émission de lumière (M5, M6) couplé entre la première alimentation de source de puissance et la diode OLED et comprenant une électrode de grille pour recevoir un signal de commande d'émission de lumière, le procédé consistant en outre à :

transmettre le signal de commande d'émission de lumière après la transmission du premier signal de balayage.

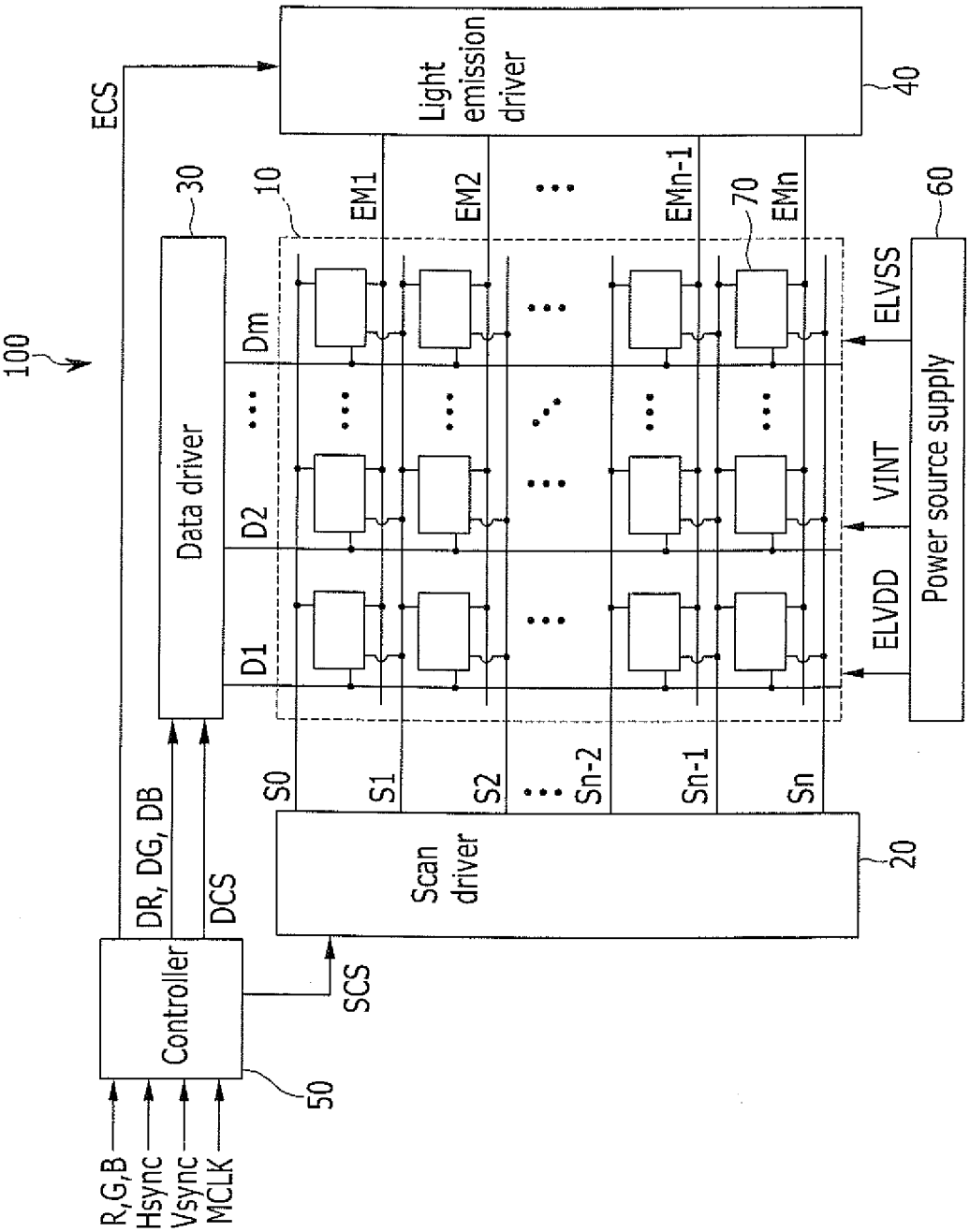

100
ECS
Light emission driver
40
30
10
EM1
EM2
EMn-1
70
EMn
60
Data driver
Dm
D2
D1
ELVSS
VINT
ELVDD
Power source supply
S0
S1
S2
Sn-2
Sn-1
Sn
Scan driver
20
DR, DG, DB
DCS
SCS
Controller
50
R,G,B
Hsync
Vsync
MCLK

FIG.1

FIG. 2

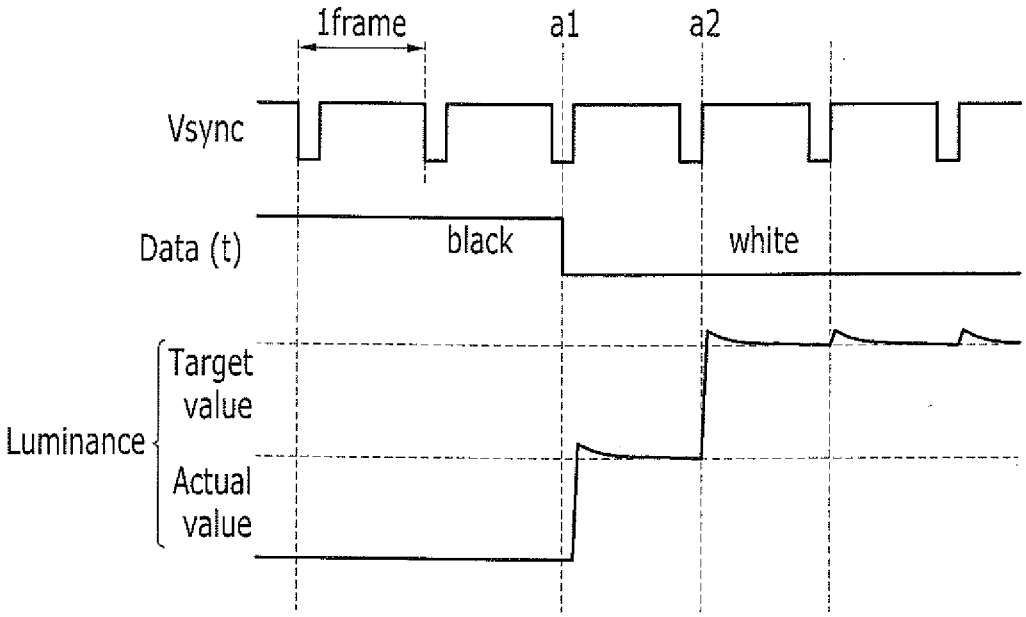

1frame
a1
a2
Vsync
Data (t)
black
white
Luminance
Target value
Actual value

FIG. 3

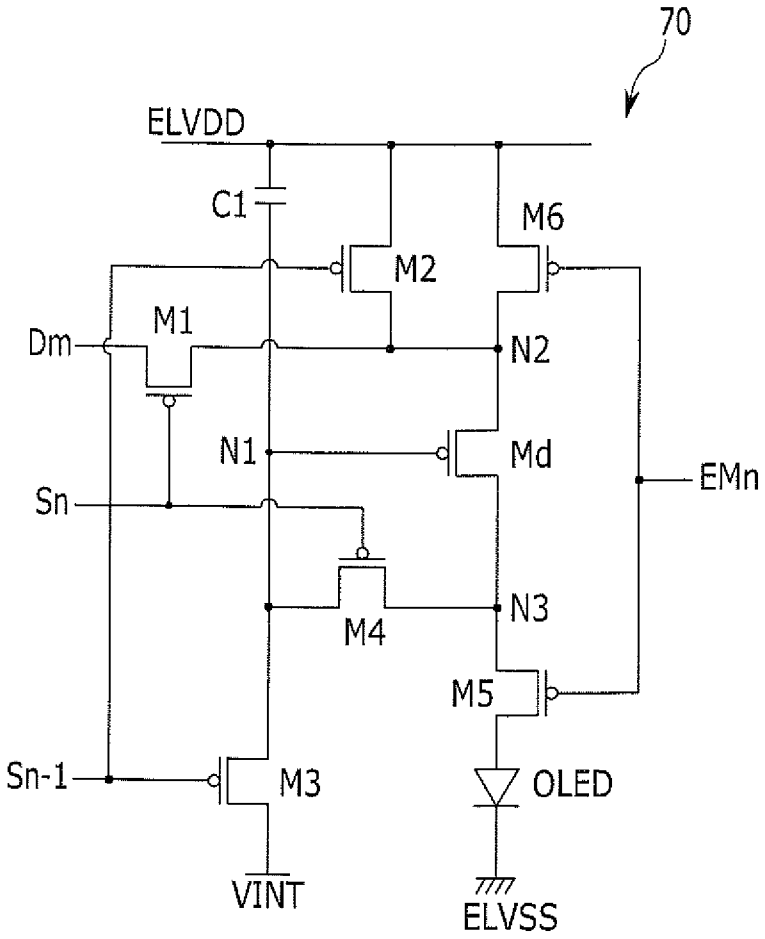

70
ELVDD
C1
M6
M2
M1
Dm
N2
N1
Md
EMn
Sn
M4
N3
M5
Sn-1
M3
OLED
VINT
ELVSS

FIG. 4

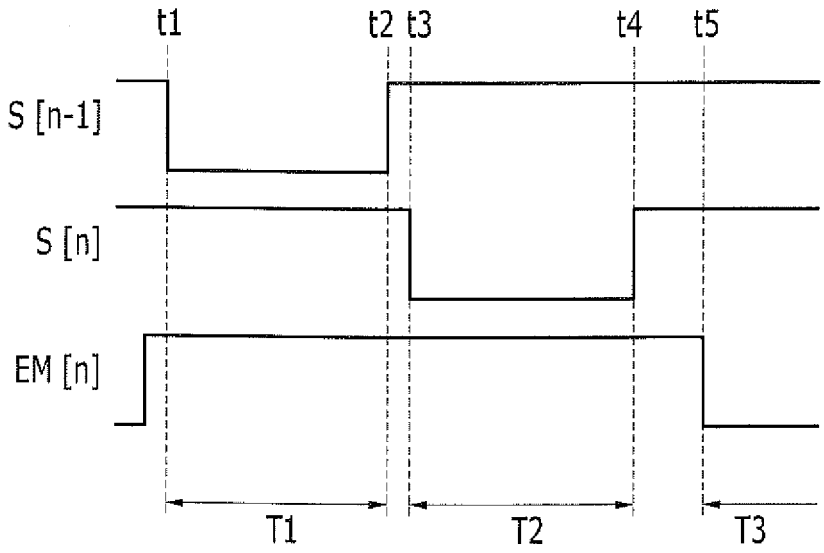
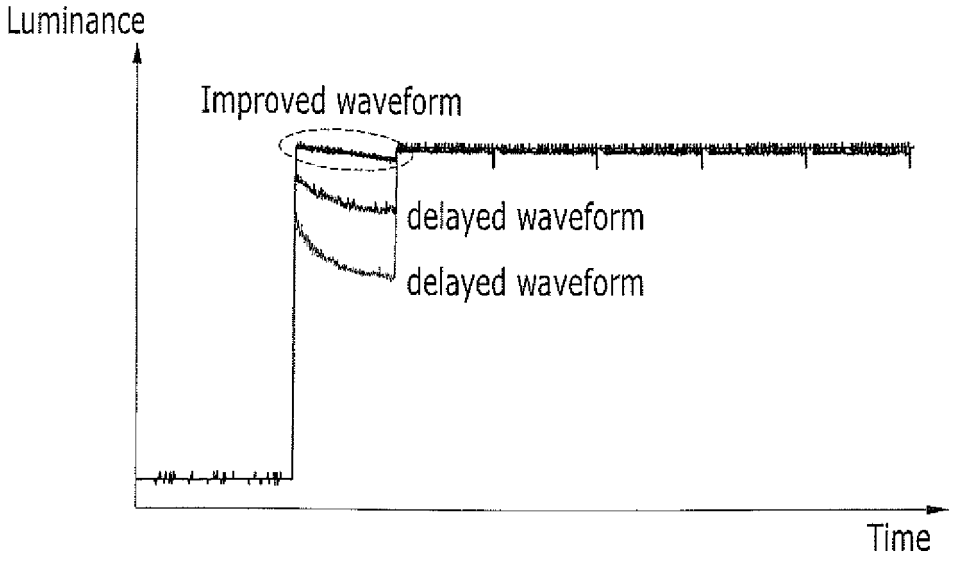


FIG. 5


Luminance
Improved waveform
delayed waveform
delayed waveform
Time

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1496495 A **[0008]**
- US 2006055336 A **[0009]**
- EP 1936596 A **[0010]**
- US 2010007649 A **[0011]**

专利名称(译)	像素，包括其的显示装置及其驱动方法		
公开(公告)号	EP2463849B1	公开(公告)日	2019-03-06
申请号	EP2011178920	申请日	2011-08-25
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星移动显示器有限公司.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
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发明人	JEONG, JIN-TAE		
IPC分类号	G09G3/32		
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优先权	1020100126489 2010-12-10 KR		
其他公开文献	EP2463849A1		
外部链接	Espacenet		

摘要(译)

一种显示装置，包括：显示单元，包括耦合到用于传输扫描信号的扫描线的像素，用于传输数据信号的数据线，以及用于传输光发射控制信号的光发射控制线;扫描驱动程序;数据驱动程序;和一个发光驱动器。每个像素包括：OLED;驱动晶体管，用于将对应于数据信号的驱动电流传输到OLED;第一晶体管，用于根据第一扫描信号将数据信号传输至驱动晶体管;第二晶体管，用于在初始化时段期间根据第二扫描信号将第一电源电压施加到驱动晶体管的第一电极，用于初始化驱动晶体管的栅电极电压;电容器包括耦合到驱动晶体管的栅电极的第一电极和耦合到第一电源的第二电极。

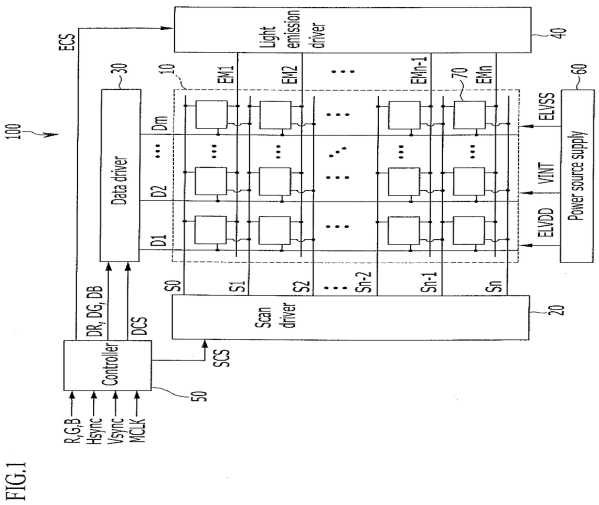

FIG.1