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(54) **Method and System for Programming and Driving Active Matrix Light Emitting Device Pixel**

Verfahren und System zur Programmierung und Ansteuerung der Pixel einer lichtemittierenden Aktivmatrix-Vorrichtung

Procédé et système pour programmer et commander un affichage de dispositif électroluminescent à matrice active

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Description

FIELD OF INVENTION

[0001] The present invention relates to a light emitting device displays, and more specifically to a driving technique for the light emitting device displays.

BACKGROUND OF THE INVENTION

[0002] Recently active-matrix organic light-emitting diode (AMOLED) displays with amorphous silicon (a-Si), poly-silicon, organic, or other driving backplane have become more attractive due to advantages over active matrix liquid crystal displays. An AMOLED display using a-Si backplanes, for example, has the advantages which include low temperature fabrication that broadens the use of different substrates and makes flexible displays feasible, and its low cost fabrication that yields high resolution displays with a wide viewing angle.

[0003] The AMOLED display includes an array of rows and columns of pixels, each having an organic light-emitting diode (OLED) and backplane electronics arranged in the array of rows and columns. Since the OLED is a current driven device, the pixel circuit of the AMOLED should be capable of providing an accurate and constant drive current.

[0004] Figure 1 shows a pixel circuit as disclosed in U.S. Patent. No. 5,748,160. The pixel circuit of Figure 1 includes an OLED 10, a driving thin film transistor (TFT) 11, a switch TFT 13, and a storage capacitor 14. The drain terminal of the driving TFT 11 is connected to the OLED 10. The gate terminal of the driving TFT 11 is connected to a column line 12 through the switch TFT 13. The storage capacitor 14, which is connected between the gate terminal of the driving TFT 11 and the ground, is used to maintain the voltage at the gate terminal of the driving TFT 11 when the pixel circuit is disconnected from the column line 12. The current through the OLED 10 strongly depends on the characteristic parameters of the driving TFT 11. Since the characteristic parameters of the driving TFT 11, in particular the threshold voltage under bias stress, vary by time, and such changes may differ from pixel to pixel, the induced image distortion may be unacceptably high.

[0005] U.S. Patent No. 6,229,508 discloses a voltage-programmed pixel circuit which provides, to an OLED, a current independent of the threshold voltage of a driving TFT. In this pixel, the gate-source voltage of the driving TFT is composed of a programming voltage and the threshold voltage of the driving TFT. A drawback of U.S. Patent No. 6,229,508 is that the pixel circuit requires extra transistors, and is complex, which results in a reduced yield, reduced pixel aperture, and reduced lifetime for the display.

[0006] Another method to make a pixel circuit less sensitive to a shift in the threshold voltage of the driving transistor is to use current programmed pixel circuits, such as pixel circuits disclosed in U.S. Patent No. 6,734,636. In the conventional current programmed pixel circuits, the gate-source voltage of the driving TFT is self-adjusted based on the current that flows through it in the next frame, so that the OLED current is less dependent on the current- voltage characteristics of the driving TFT. A drawback of the current-programmed pixel circuit is that an overhead associated with low programming current levels arises from the column line charging time due to the large line capacitance.

[0007] Document US 2003/095087 A1 describes a circuit for driving an organic light emitting diode (OLED). The circuit includes a current source for providing current to a first terminal of the OLED, and a generator for providing a variable voltage signal to a second terminal of the OLED to facilitate control of the current.

[0008] Document US 2004/0174349 A1 describes a pixel circuit that includes a light emitting device, a storage device configured to represent a level of illumination, and a driving device used to drive the light emitting device. Configuring the storage device includes changing a voltage difference across the storage device to a level larger than a threshold voltage of the driving device. The driving device reduces driving of the light emitting device while the storage device is being configured. After the storage device has been configured, the driving device is permitted to drive the light emitting device to emit light having a luminance level corresponding to the level of illumination represented by the storage device.

SUMMARY OF THE INVENTION

[0009] It is an object of the invention to provide a method and system that obviates or mitigates at least one of the disadvantages of existing systems.

This object is achieved by the present invention as claimed in the independent claims. Advantageous embodiments of the present invention are defined by the dependent claims.

[0010] In accordance with an aspect there is provided a method of programming and driving a display system, the display system includes: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a capacitor having a first terminal and a second terminal; a switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the switch transistor being connected to a select line, the first terminal of the switch transistor being connected to a signal line for transferring voltage data, the second terminal of the switch transistor being connected to the first terminal of the capacitor; and a driving transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the driving transistor being connected to the second terminal of the switch transistor and the first terminal of the capacitor at a first node (A), the first

terminal of the driving transistor being connected to the second terminal of the light emitting device and the second terminal of the capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; a driver for driving the select line, the controllable voltage supply line and the signal line to operate the display array; the method including the steps of: at a programming cycle, at a first operating cycle, charging the second node at a first voltage defined by (VREF-VT) or (-VREF+VT), where VREF represents a reference voltage and VT represents a threshold voltage of the driving transistor, at a second operating cycle, charging the first node at a second voltage defined by (VREF+VP) or (-VREF+VP) so that the difference between the first and second node voltages is stored in the storage capacitor, where VP represents a programming voltage; at a driving cycle, applying the voltage stored in the storage capacitor to the gate terminal of the driving transistor.

[0011] In accordance with a further aspect there is provided a method of programming and driving a display system, the display system includes: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a first capacitor and a second capacitor, each having a first terminal and a second terminal; a first switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the first switch transistor being connected to a first select line, the first terminal of the first switch transistor being connected to the second terminal of the light emitting device, the second terminal of the first switch being connected to the first terminal of the first capacitor; a second switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the second switch transistor being connected to a second select line, the first terminal of the second switch transistor being connected to a signal line for transferring voltage data; a driving transistor having a gate terminal, a first terminal and a second terminal, the first terminal of the driving transistor being connected to the second terminal of the light emitting device at a first node (A), the gate terminal of the driving transistor being connected to the second terminal of the first switch transistor and the first terminal of the first capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; the second terminal of the second switch transistor being connected to the second terminal of the first capacitor and the first terminal of the second capacitor at a third node (C); a driver for driving the first and second select line, the controllable voltage supply line and the signal line to operate the display array, the method including the steps of: at a programming cycle, at a first operating cycle, controlling the voltage of each of the first node and the second node so as to store (VT+VP) or -(VT+VP) in the first storage capacitor, where VT represents a threshold voltage of the driving transistor, VP represents a programming voltage; at a second operating cycle, discharging the third node; at a driving cycle, applying the voltage stored in the storage capacitor to the gate terminal of the driving transistor.

[0012] In accordance with a further aspect there is provided a display system including: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a capacitor having a first terminal and a second terminal; a switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the switch transistor being connected to a select line, the first terminal of the switch transistor being connected to a signal line for transferring voltage data, the second terminal of the switch transistor being connected to the first terminal of the capacitor; and a driving transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the driving transistor being connected to the second terminal of the switch transistor and the first terminal of the capacitor at a first node (A), the first terminal of the driving transistor being connected to the second terminal of the light emitting device and the second terminal of the capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; a driver for driving the select line, the controllable voltage supply line and the signal line to operate the display array; and a controller for implementing a programming cycle and a driving cycle on each row of the display array using the driver; wherein the programming cycle includes a first operating cycle and a second operating cycle, wherein at the first operating cycle, the second node is charged at a first voltage defined by (VREF-VT) or (-VREF+VT), where VREF represents a reference voltage and VT represents a threshold voltage of the driving transistor, at the second operating cycle, the first node is charged at a second voltage defined by (VREF+VP) or (-VREF+VP) so that the difference between the first and second node voltages is stored in the storage capacitor, where VP represents a programming voltage; wherein at the driving cycle, the voltage stored in the storage capacitor is applied to the gate terminal of the driving transistor.

[0013] In accordance with a further aspect there is provided a display system including: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a first capacitor and a second capacitor, each having a first terminal and a second terminal; a first switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the first switch transistor being connected to a first select line, the first terminal of the first switch transistor being connected to the second terminal of the light emitting device, the second

terminal of the first switch being connected to the first terminal of the first capacitor; a second switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the second switch transistor being connected to a second select line, the first terminal of the second switch transistor being connected to a signal line for transferring voltage data; a driving transistor having a gate terminal, a first terminal and a second terminal, the first terminal of the driving transistor being connected to the second terminal of the light emitting device at a first node (A), the gate terminal of the driving transistor being connected to the second terminal of the first switch transistor and the first terminal of the first capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; the second terminal of the second switch transistor being connected to the second terminal of the first capacitor and the first terminal of the second capacitor at a third node (C); a driver for driving the first and second select line, the controllable voltage supply line and the signal line to operate the display array; and a controller for implementing a programming cycle and a driving cycle on each row of the display array using the driver; wherein the programming cycle includes a first operating cycle and a second operating cycle, wherein at the first operating cycle, the voltage of each of the first node and the second node is controlled so as to store (VT+VP) or -(VT+VP) in the first storage capacitor, where VT represents a threshold voltage of the driving transistor, VP represents a programming voltage, at the second operating cycle, the third node is discharged, wherein at the driving cycle, the voltage stored in the storage capacitor is applied to the gate terminal of the driving transistor.

[0014] This summary of the invention does not necessarily describe all features of the invention.

[0015] Other aspects and features of the present invention will be readily apparent to those skilled in the art from a review of the following detailed description of preferred embodiments in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

Figure 1 is a diagram showing a conventional 2-TFT voltage programmed pixel circuit;

Figure 2 is a timing diagram showing an example of programming and driving cycles in accordance with an embodiment of the present invention, which is applied to a display array;

Figure 3 is a diagram showing a pixel circuit to which programming and driving technique in accordance with an embodiment of the present invention is applied;

Figure 4 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 3;

Figure 5 is a diagram showing a lifetime test result for the pixel circuit of Figure 3;

Figure 6 is a diagram showing a display system having the pixel circuit of Figure 3;

Figure 7(a) is a diagram showing an example of the array structure having top emission pixels which are applicable to the array of Figure 6;

Figure 7(b) is a diagram showing an example of the array structure having bottom emission pixels which are applicable to the array of Figure 6;

Figure 8 is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

Figure 9 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 8;

Figure 10 is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

Figure 11 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 10;

Figure 12 is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

Figure 13 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 12;

Figure 14 is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

Figure 15 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 14;

Figure 16 is a diagram showing a display system

having the pixel circuit of Figure 14;

Figure 17 is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

Figure 18 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 17;

Figure 19 is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

Figure 20 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 19;

Figure 21 is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied; and

Figure 22 is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of Figure 21;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

[0017] Embodiments of the present invention are described using a pixel having an organic light emitting diode (OLED) and a driving thin film transistor (TFT). However, the pixel may include any light emitting device other than OLED, and the pixel may include any driving transistor other than TFT. It is noted that in the description, "pixel circuit" and "pixel" may be used interchangeably.

[0018] Figure 2 is a diagram showing programming and driving cycles in accordance with an embodiment of the present invention. In Figure 2, each of ROW(j), ROW(j+1), and ROW(j+2) represents a row of the display array where a plurality of pixel circuits are arranged in row and column.

[0019] The programming and driving cycle for a frame occurs after the programming and driving cycle for a next frame. The programming and driving cycles for the frame at a ROW overlaps with the programming and driving cycles for the same frame at a next ROW. As described below, during the programming cycle, the time depending parameter(s) of the pixel circuit is extracted to generate a stable pixel current.

[0020] Figure 3 illustrates a pixel circuit 200 to which programming and driving technique in accordance with an embodiment of the present invention is applied. The pixel circuit 200 includes an OLED 20, a storage capacitor 21, a driving transistor 24, and a switch transistor 26. The pixel circuit 200 is a voltage programmed pixel circuit. Each of the transistors 24 and 26 has a gate terminal, a first terminal and a second terminal. In the description, the first terminal (second terminal) may be, but not limited to, a drain terminal or a source terminal (a source terminal or a drain terminal).

[0021] The transistors 24 and 26 are n-type TFTs. However, the transistors 24 and 26 may be p-type transistors. As described below, the driving technique applied to the pixel circuit 200 is also applicable to a complementary pixel circuit having p-type transistors as shown in Figure 14. The transistors 24 and 26 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0022] The first terminal of the driving transistor 24 is connected to a controllable voltage supply line VDD. The second terminal of the driving transistor 24 is connected to the anode electrode of the OLED 20. The gate terminal of the driving transistor 24 is connected to a signal line VDATA through the switch transistor 26. The storage capacitor 21 is connected between the source and gate terminals of the driving transistor 24.

[0023] The gate terminal of the switch transistor 26 is connected to a select line SEL. The first terminal of the switch transistor 26 is connected to the signal line VDATA. The second terminal of the switch transistor 26 is connected to the gate terminal of the driving transistor 24. The cathode electrode of the OLED 20 is connected to a ground voltage supply electrode.

[0024] The transistors 24 and 26 and the storage capacitor 21 are connected at node A1. The transistor 24, the OLED 20 and the storage capacitor 21 are connected at node B1.

[0025] Figure 4 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 200 of Figure 3. Referring to Figures 3 and 4, the operation of the pixel circuit 200 includes a programming cycle having three operating cycles X11, X12 and X13, and a driving cycle having one operating cycle X14.

[0026] During the programming cycle, node B1 is charged to the negative threshold voltage of the driving transistor 24, and node A1 is charged to a programming voltage VP.

[0027] As a result, the gate-source voltage of the driving transistor 24 goes to:

$$VGS=VP-(-VT)=VP+VT \quad \ldots(1)$$

where VGS represents the gate-source voltage of the driving transistor 24, and VT represents the threshold voltage of the driving transistor 24.

[0028] Since the driving transistor 24 is in saturation regime of operation, its current is defined mainly by its

gate-source voltage. As a result the current of the driving transistor 24 remains constant even if the OLED voltage changes, since its gate-source voltage is stored in the storage capacitor 21.

[0029] In the first operating cycle X11: VDD goes to a compensating voltage VCOMPB, and VDATA goes to a high positive compensating voltage VCOMPA, and SEL is high. As a result, node A1 is charged to VCOMPA and node B1 is charged to VCOMPB.

[0030] In the second operating cycle X12: While VDATA goes to a reference voltage VREF, node B1 is discharged through the driving transistor 24 until the driving transistor 24 turns off. As a result, the voltage of node B1 reaches (VREF-VT). VDD has a positive voltage VH to increase the speed of this cycle X12. For optimal setting time, VH can be set to be equal to the operating voltage which is the voltage on VDD during the driving cycle.

[0031] In the third operating cycle X13: VDD goes to its operating voltage. While SEL is high, node A1 is charged to (VP+VREF). Because the capacitance 22 of the OLED 20 is large, the voltage at node B1 stays at the voltage generated in the previous cycle X12. Thus, the voltage of node B1 is (VREF-VT). Therefore, the gate-source voltage of the driving transistor 24 is (VP+VT), and this gate-source voltage is stored in the storage capacitor 21.

[0032] In the fourth operating cycle X14: SEL and VDATA go to zero. VDD is the same as that of the third operating cycle X13. However, VDD may be higher than that of the third operating cycle X13. The voltage stored in the storage capacitor 21 is applied to the gate terminal of the driving transistor 24. Since the gate-source voltage of the driving transistor 24 include its threshold voltage and also is independent of the OLED voltage, the degradation of the OLED 20 and instability of the driving transistor 24 does not affect the amount of current flowing through the driving transistor 24 and the OLED 20.

[0033] It is noted that the pixel circuit 200 can be operated with different values of VCOMPB, VCOMPA, VP, VREF and VH. VCOMPB, VCOMPA, VP, VREF and VH define the lifetime of the pixel circuit 200. Thus, these voltages can be defined in accordance with the pixel specifications.

[0034] Figure 5 illustrates a lifetime test result for the pixel circuit and waveform shown in Figures 3 and 4. In the test, a fabricated pixel circuit was put under the operation for a long time while the current of the driving transistor (24 of Figure 3) was monitored to investigate the stability of the driving scheme. The result shows that OLED current is stable after 120-hour operation. The VT shift of the driving transistor is 0.7 V.

[0035] Figure 6 illustrates a display system having the pixel circuit 200 of Figure 3. VDD1 and VDD2 of Figure 6 correspond to VDD of Figure 3. SEL1 and SEL2 of Figure 6 correspond to SEL of Figure 3. VDATA1 and VDATA2 of Figure 6 correspond to VDATA of Figure 3. The array of Figure 6 is an active matrix light emitting diode (AMOLED) display having a plurality of the pixel circuits 200 of Figure 3. The pixel circuits are arranged in rows and columns, and interconnections 41, 42 and 43 (VDATA1, SEL1, VDD1). VDATA1 (or VDATA 2) is shared between the common column pixels while SELL (or SEL2) and VDD1 (or VDD2) are shared between common row pixels in the array structure.

[0036] A driver 300 is provided for driving VDATA1 and VDATA2. A driver 302 is provided for driving VDD1, VDD2, SEL1 and SEL 2, however, the driver for VDD and SEL lines can also be implemented separately. A controller 304 controls the drivers 300 and 302 to programming and driving the pixel circuits as described above. The timing diagram for programming and driving the display array of Figure 6 is as shown in Figure 2. Each programming and driving cycle may be the same as that of Figure 4.

[0037] Figure 7(a) illustrates an example of array structure having top emission pixels are arranged. Figure 7(b) illustrates an example of array structure having bottom emission pixels are arranged. The array of Figure 6 may have array structure shown in Figure 7(a) or 7(b). In Figure 7(a), 400 represents a substrate, 402 represents a pixel contact, 403 represents a (top emission) pixel circuit, and 404 represents a transparent top electrode on the OLEDs. In Figure 7(b), 410 represents a transparent substrate, 411 represents a (bottom emission) pixel circuit, and 412 represents a top electrode. All of the pixel circuits including the TFTs, the storage capacitor, the SEL, VDATA, and VDD lines are fabricated together. After that, the OLEDs are fabricated for all pixel circuits. The OLED is connected to the corresponding driving transistor using a via (e.g. B1 of Figure 3) as shown in Figures 7(a) and 7(b). The panel is finished by deposition of the top electrode on the OLEDs which can be a continuous layer, reducing the complexity of the design and can be used to turn the entire display ON/OFF or control the brightness.

[0038] Figure 8 illustrates a pixel circuit 202 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 202 includes an OLED 50, two storage capacitors 52 and 53, a driving transistor 54, and switch transistors 56 and 58. The pixel circuit 202 is a top emission, voltage programmed pixel circuit. This embodiment principally works in the same manner as that of Figure 3. However, in the pixel circuit 202, the OLED 50 is connected to the drain terminal of the driving transistor 54. As a result, the circuit can be connected to the cathode of the OLED 50. Thus, the OLED deposition can be started with the cathode.

[0039] The transistors 54, 56 and 58 are n-type TFTs. However, the transistors 54, 56 and 58 may be p-type transistors The driving technique applied to the pixel circuit 202 is also applicable to a complementary pixel circuit having p-type transistors as shown in Figure 17. The transistors 54, 56 and 58 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organ-

ic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0040] The first terminal of the driving transistor 54 is connected to the cathode electrode of the OLED 50. The second terminal of the driving transistor 54 is connected to a controllable voltage supply line VSS. The gate terminal of the driving transistor 54 is connected to its first line (terminal) through the switch transistor 56. The storage capacitors 52 and 53 are in series, and are connected between the gate terminal of the driving transistor 54 and a common ground. The voltage on the voltage supply line VSS is controllable. The common ground may be connected to VSS.

[0041] The gate terminal of the switch transistor 56 is connected to a first select line SELL The first terminal of the switch transistor 56 is connected to the drain terminal of the driving transistor 54. The second terminal of the switch transistor 56 is connected to the gate terminal of the driving transistor 54.

[0042] The gate terminal of the switch transistor 58 is connected to a second select line SEL2. The first terminal of the switch transistor 58 is connected to a signal line VDATA. The second terminal of the switch transistor 58 is connected to the shared terminal of the storage capacitors 52 and 53 (i.e. node C2). The anode electrode of the OLED 50 is connected to a voltage supply electrode VDD.

[0043] The OLED 50 and the transistors 54 and 56 are connected at node A2. The storage capacitor 52 and the transistors 54 and 56 are connected at node B2.

[0044] Figure 9 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 202 of Figure 8. Referring to Figures 8 and 9, the operation of the pixel circuit 202 includes a programming cycle having four operating cycles X21, X22, X23 and X24, and a driving cycle having one operating cycle X25.

[0045] During the programming cycle, a programming voltage plus the threshold voltage of the driving transistor 54 is stored in the storage capacitor 52. The source terminal of the driving transistor 54 goes to zero, and the second storage capacitor 53 is charged to zero.

[0046] As a result, the gate-source voltage of the driving transistor 54 goes to:

$$VGS=VP+VT \qquad \ldots(2)$$

where VGS represents the gate-source voltage of the driving transistor 54, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor 54.

[0047] In the first operating cycle X21: VSS goes to a high positive voltage, and VDATA is zero. SEL1 and SEL2 are high. Therefore, nodes A2 and B2 are charged to a positive voltage.

[0048] In the second operating cycle X22: While SEL1 is low and the switch transistor 56 is off, VDATA goes to a high positive voltage. As a result, the voltage at node B2 increases (i.e. bootstrapping) and node A2 is charged to the voltage of VSS. At this voltage, the OLED 50 is off.

[0049] In the third operating cycle X23: VSS goes to a reference voltage VREF. VDATA goes to (VREF-VP). At the beginning of this cycle, the voltage of node B2 becomes almost equal to the voltage of node A2 because the capacitance 51 of the OLED 50 is bigger than that of the storage capacitor 52. After that, the voltage of node B2 and the voltage of node A2 are discharged through the driving transistor 54 until the driving transistor 54 turns off. As a result, the gate-source voltage of the driving transistor 54 is (VREF+VT), and the voltage stored in storage capacitor 52 is (VP+VT).

[0050] In the fourth operating cycle X24: SEL1 is low. Since SEL2 is high, and VDATA is zero, the voltage at node C2 goes to zero.

[0051] In the fifth operating cycle X25: VSS goes to its operating voltage during the driving cycle. In Figure 5, the operating voltage of VSS is zero. However, it may be any voltage other than zero. SEL2 is low. The voltage stored in the storage capacitor 52 is applied to the gate terminal of the driving transistor 54. Accordingly, a current independent of the threshold voltage VT of the driving transistor 54 and the voltage of the OLED 50 flows through the driving transistor 54 and the OLED 50. Thus, the degradation of the OLED 50 and instability of the driving transistor 54 does not affect the amount of the current flowing through the driving transistor 54 and the OLED 50.

[0052] Figure 10 illustrates a pixel circuit 204 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 204 includes an OLED 60, two storage capacitors 62 and 63, a driving transistor 64, and switch transistors 66 and 68. The pixel circuit 204 is a top emission, voltage programmed pixel circuit. The pixel circuit 204 principally works similar to that of in Figure 8. However, one common select line is used to operate the pixel circuit 204, which can increase the available pixel area and aperture ratio.

[0053] The transistors 64, 66 and 68 are n-type TFTs. However, The transistors 64, 66 and 68 may be p-type transistors. The driving technique applied to the pixel circuit 204 is also applicable to a complementary pixel circuit having p-type transistors as shown in Figure 19. The transistors 64, 66 and 68 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0054] The first terminal of the driving transistor 64 is connected to the cathode electrode of the OLED 60. The second terminal of the driving transistor 64 is connected to a controllable voltage supply line VSS. The gate terminal of the driving transistor 64 is connected to its first

line (terminal) through the switch transistor 66. The storage capacitors 62 and 63 are in series, and are connected between the gate terminal of the driving transistor 64 and the common ground. The voltage of the voltage supply line VSS is controllable. The common ground may be connected to VSS.

[0055] The gate terminal of the switch transistor 66 is connected to a select line SEL. The first terminal of the switch transistor 66 is connected to the first terminal of the driving transistor 64. The second terminal of the switch transistor 66 is connected to the gate terminal of the driving transistor 64.

[0056] The gate terminal of the switch transistor 68 is connected to the select line SEL. The first terminal of the switch transistor 68 is connected to a signal line VDATA. The second terminal is connected to the shared terminal of storage capacitors 62 and 63 (i.e. node C3). The anode electrode of the OLED 60 is connected to a voltage supply electrode VDD.

[0057] The OLED 60 and the transistors 64 and 66 are connected at node A3. The storage capacitor 62 and the transistors 64 and 66 are connected at node B3.

[0058] Figure 11 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 204 of Figure 10. Referring to Figures 10 and 11, the operation of the pixel circuit 204 includes a programming cycle having three operating cycles X31, X32 and X33, and a driving cycle includes one operating cycle X34.

[0059] During the programming cycle, a programming voltage plus the threshold voltage of the driving transistor 64 is stored in the storage capacitor 62. The source terminal of the driving transistor 64 goes to zero and the storage capacitor 63 is charged to zero.

[0060] As a result, the gate-source voltage of the driving transistor 64 goes to:

$$VGS=VP+VT \qquad \ldots(3)$$

where VGS represents the gate-source voltage of the driving transistor 64, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor 64.

[0061] In the first operating cycle X31: VSS goes to a high positive voltage, and VDATA is zero. SEL is high. As a result, nodes A3 and B3 are charged to a positive voltage. The OLED 60 turns off.

[0062] In the second operating cycle X32: While SEL is high, VSS goes to a reference voltage VREF. VDATA goes to (VREF-VP). As a result, the voltage at node B3 and the voltage of node A3 are discharged through the driving transistor 64 until the driving transistor 64 turns off. The voltage of node B3 is (VREF+VT), and the voltage stored in the storage capacitor 62 is (VP+VT).

[0063] In the third operating cycle X33: SEL goes to VM. VM is an intermediate voltage in which the switch transistor 66 is off and the switch transistor 68 is on. VDATA goes to zero. Since SEL is VM and VDATA is zero, the voltage of node C3 goes to zero.

[0064] VM is defined as :

$$VT3 << VM < VREF + VT1 + VT2 \qquad \ldots(a)$$

where VT1 represents the threshold voltage of the driving transistor 64, VT2 represents the threshold voltage of the switch transistor 66, and VT3 represents the threshold voltage of the switch transistor 68.

[0065] The condition (a) forces the switch transistor 66 to be off and the switch transistor 68 to be on. The voltage stored in the storage capacitor 62 remains intact.

[0066] In the fourth operating cycle X34: VSS goes to its operating voltage during the driving cycle. In Figure 11, the operating voltage of VSS is zero. However, the operating voltage of VSS may be any voltage other than zero. SEL is low. The voltage stored in the storage capacitor 62 is applied to the gate of the driving transistor 64. The driving transistor 64 is ON. Accordingly, a current independent of the threshold voltage VT of the driving transistor 64 and the voltage of the OLED 60 flows through the driving transistor 64 and the OLED 60. Thus, the degradation of the OLED 60 and instability of the driving transistor 64 does not affect the amount of the current flowing through the driving transistor 64 and the OLED 60.

[0067] Figure 12 illustrates a pixel circuit 206 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 206 includes an OLED 70, two storage capacitors 72 and 73, a driving transistor 74, and switch transistors 76 and 78. The pixel circuit 206 is a top emission, voltage programmed pixel circuit.

[0068] The transistors 74, 76 and 78 are n-type TFTs. However, the transistors 74, 76 and 78 may be p-type transistors. The driving technique applied to the pixel circuit 206 is also applicable to a complementary pixel circuit having p-type transistors as shown in Figure 21. The transistors 74, 76 and 78 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

[0069] The first terminal of the driving transistor 74 is connected to the cathode electrode of the OLED 70. The second terminal of the driving transistor 74 is connected to a common ground. The gate terminal of the driving transistor 74 is connected to its first line (terminal) through the switch transistor 76. The storage capacitors 72 and 73 are in series, and are connected between the gate terminal of the driving transistor 74 and the common ground.

[0070] The gate terminal of the switch transistor 76 is connected to a select line SEL. The first terminal of the

switch transistor 76 is connected to the first terminal of the driving transistor 74. The second terminal of the switch transistor 76 is connected to the gate terminal of the driving transistor 74.

[0071] The gate terminal of the switch transistor 78 is connected to the select line SEL. The first terminal of the switch transistor 78 is connected to a signal line VDATA. The second terminal is connected to the shared terminal of storage capacitors 72 and 73 (i.e. node C4). The anode electrode of the OLED 70 is connected to a voltage supply electrode VDD. The voltage of the voltage electrode VDD is controllable.

[0072] The OLED 70 and the transistors 74 and 76 are connected at node A4. The storage capacitor 72 and the transistors 74 and 76 are connected at node B4.

[0073] Figure 13 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 206 of Figure 12. Referring to Figures 12 and 13, the operation of the pixel circuit 206 includes a programming cycle having four operating cycles X41, X42, X43 and X44, and a driving cycle having one driving cycle 45.

[0074] During the programming cycle, a programming voltage plus the threshold voltage of the driving transistor 74 is stored in the storage capacitor 72. The source terminal of the driving transistor 74 goes to zero and the storage capacitor 73 is charged to zero.

[0075] As a result, the gate-source voltage of the driving transistor 74 goes to:

$$VGS=VP+VT \qquad \ldots(4)$$

where VGS represents the gate-source voltage of the driving transistor 74, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor 74.

[0076] In the first operating cycle X41: SEL is high. VDATA goes to a low voltage. While VDD is high, node B4 and node A4 are charged to a positive voltage.

[0077] In the second operating cycle X42: SEL is low, and VDD goes to a reference voltage VREF where the OLED 70 is off.

[0078] In the third operating cycle X43: VDATA goes to (VREF2-VP) where VREF2 is a reference voltage. It is assumed that VREF2 is zero. However, VREF2 can be any voltage other than zero. SEL is high. Therefore, the voltage of node B4 and the voltage of node A4 become equal at the beginning of this cycle. It is noted that the first storage capacitor 72 is large enough so that its voltage becomes dominant. After that, node B4 is discharged through the driving transistor 74 until the driving transistor 74 turns off.

[0079] As a result, the voltage of node B4 is VT (i.e. the threshold voltage of the driving transistor 74). The voltage stored in the first storage capacitor 72 is (VP-VREF2+VT)=(VP+VT) where VREF2=O.

[0080] In the fourth operating cycle X44: SEL goes to VM where VM is an intermediate voltage at which the switch transistor 76 is off and the switch transistor 78 is on. VM satisfies the following condition:

$$VT3 << VM < VP+VT \qquad \ldots(b)$$

where VT3 represents the threshold voltage of the switch transistor 78.

[0081] VDATA goes to VREF2 (=0). The voltage of node C4 goes to VREF2 (=0).

[0082] This results in that the gate-source voltage VGS of the driving transistor 74 is (VP+VT). Since VM<VP+VT, the switch transistor 76 is off, and the voltage stored in the storage capacitor 72 stays at VP+VT.

[0083] In the fifth operating cycle X45: VDD goes to the operating voltage. SEL is low. The voltage stored in the storage capacitor 72 is applied to the gate of the driving transistor 74. Accordingly, a current independent of the threshold voltage VT of the driving transistor 74 and the voltage of the OLED 70 flows through the driving transistor 74 and the OLED 70. Thus, the degradation of the OLED 70 and instability of the driving transistor 74 does not affect the amount of the current flowing through the driving transistor 74 and the OLED 70.

[0084] Figure 14 illustrates a pixel circuit 208 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 208 includes an OLED 80, a storage capacitor 81, a driving transistor 84 and a switch transistor 86. The pixel circuit 208 corresponds to the pixel circuit 200 of Figure 3, and a voltage programmed pixel circuit.

[0085] The transistors 84 and 86 are p-type TFTs. The transistors 84 and 86 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

[0086] The first terminal of the driving transistor 84 is connected to a controllable voltage supply line VSS. The second terminal of the driving transistor 84 is connected to the cathode electrode of the OLED 80. The gate terminal of the driving transistor 84 is connected to a signal line VDATA through the switch transistor 86. The storage capacitor 81 is connected between the second terminal and the gate terminal of the driving transistor 84.

[0087] The gate terminal of the switch transistor 86 is connected to a select line SEL. The first terminal of the switch transistor 86 is connected to the signal line VDATA. The second terminal of the switch transistor 86 is connected to the gate terminal of the driving transistor 84. The anode electrode of the OLED 80 is connected to a ground voltage supply electrode.

[0088] The storage capacitor 81 and the transistors 84 and 85 are connected at node A5. The OLED 80, the storage capacitor 81 and the driving transistor 84 are

connected at node B5.

[0089] Figure 15 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 208 of Figure. Figure 15 corresponds to Figure 4. VDATA and VSS are used to programming and compensating for a time dependent parameter of the pixel circuit 208, which are similar to VDATA and VDD of Figure 4. Referring to Figures 14 and 15, the operation of the pixel circuit 208 includes a programming cycle having three operating cycles X51, X52 and X53, and a driving cycle having one operating cycle X54.

[0090] During the programming cycle, node B5 is charged to a positive threshold voltage of the driving transistor 84, and node A5 is charged to a negative programming voltage.

[0091] As a result, the gate-source voltage of the driving transistor 84 goes to:

$$VGS=-VP+(-|VT|)=-VP-|VT| \quad \ldots(5)$$

where VGS represents the gate-source voltage of the driving transistor 84, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor 84.

[0092] In the first operating cycle X51: VSS goes to a positive compensating voltage VCOMPB, and VDATA goes to a negative compensating voltage (-VCOMPA), and SEL is low. As a result, the switch transistor 86 is on. Node A5 is charged to (-VCOMPA). Node B5 is charged to VCOMPB.

[0093] In the second operating cycle X52: VDATA goes to a reference voltage VREF. Node B5 is discharged through the driving transistor 84 until the driving transistor 84 turns off. As a result, the voltage of node B5 reaches VREF+|VT|. VSS goes to a negative voltage VL to increase the speed of this cycle X52. For the optimal setting time, VL is selected to be equal to the operating voltage which is the voltage of VSS during the driving cycle.

[0094] In the third operating cycle X53: While VSS is in the VL level, and SEL is low, node A5 is charged to (VREF-VP). Because the capacitance 82 of the OLED 80 is large, the voltage of node B5 stays at the positive threshold voltage of the driving transistor 84. Therefore, the gate-source voltage of the driving transistor 84 is (-VP-|VT|), which is stored in storage capacitor 81.

[0095] In the fourth operating cycle X54: SEL and VDATA go to zero. VSS goes to a high negative voltage (i.e. its operating voltage). The voltage stored in the storage capacitor 81 is applied to the gate terminal of the driving transistor 84. Accordingly, a current independent of the voltage of the OLED 80 and the threshold voltage of the driving transistor 84 flows through the driving transistor 84 and the OLED 80. Thus, the degradation of the OLED 80 and instability of the driving transistor 84 does not affect the amount of the current flowing through the driving transistor 84 and the OLED 80.

[0096] It is noted that the pixel circuit 208 can be operated with different values of VCOMPB, VCOMPA, VL, VREF and VP. VCOMPB, VCOMPA, VL, VREF and VP define the lifetime of the pixel circuit. Thus, these voltages can be defined in accordance with the pixel specifications.

[0097] Figure 16 illustrates a display system having the pixel circuit 208 of Figure 14. VSS1 and VSS2 of Figure 16 correspond to VSS of Figure 14. SEL1 and SEL2 of Figure 16 correspond to SEL of Figure 14. VDATA1 and VDATA2 of Figure 16 correspond to VDATA of Figure 14. The array of Figure 16 is an active matrix light emitting diode (AMOLED) display having a plurality of the pixel circuits 208 of Figure 14. The pixel circuits 208 are arranged in rows and columns, and interconnections 91, 92 and 93 (VDATA1, SEL2, VSS2). VDATA1 (or VDATA 2) is shared between the common column pixels while SEL1 (or SEL2) and VSS1 (or VSS2) are shared between common row pixels in the array structure.

[0098] A driver 310 is provided for driving VDATA1 and VDATA2. A driver 312 is provided for driving VSS 1, VSS2, SEL1 and SEL2. A controller 314 controls the drivers 310 and 312 to implement the programming and driving cycles described above. The timing diagram for programming and driving the display array of Figure 6 is as shown in Figure 2. Each programming and driving cycle may be the same as that of Figure 15.

[0099] The array of Figure 16 may have array structure shown in Figure 7(a) or 7(b). The array of Figure 16 is produced in a manner similar to that of Figure 6. All of the pixel circuits including the TFTs, the storage capacitor, the SEL, VDATA, and VSS lines are fabricated together. After that, the OLEDs are fabricated for all pixel circuits. The OLED is connected to the corresponding driving transistor using a via (e.g. B5 of Figure 14). The panel is finished by deposition of the top electrode on the OLEDs which can be a continuous layer, reducing the complexity of the design and can be used to turn the entire display ON/OFF or control the brightness.

[0100] Figure 17 illustrates a pixel circuit 210 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 210 includes an OLED 100, two storage capacitors 102 and 103, a driving transistor 104, and switch transistors 106 and 108. The pixel circuit 210 corresponds to the pixel circuit 202 of Figure 8.

[0101] The transistors 104, 106 and 108 are p-type TFTs. The transistors 84 and 86 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

[0102] In Figure 17, one of the terminals of the driving transistor 104 is connected to the anode electrode of the OLED 100, while the other terminal is connected to a controllable voltage supply line VDD. The storage capacitors 102 and 103 are in series, and are connected be-

tween the gate terminal of the driving transistor 104 and a voltage supply electrode V2. Also, V2 may be connected to VDD. The cathode electrode of the OLED 100 is connected to a ground voltage supply electrode.

[0103] The OLED 100 and the transistors 104 and 106 are connected at node A6. The storage capacitor 102 and the transistors 104 and 106 are connected at node B6. The transistor 108 and the storage capacitors 102 and 103 are connected at node C6.

[0104] Figure 18 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 210 of Figure 17. Figure 18 corresponds to Figure 9. VDATA and VDD are used to programming and compensating for a time dependent parameter of the pixel circuit 210, which are similar to VDATA and VSS of Figure 9. Referring to Figures 17 and 18, the operation of the pixel circuit 210 includes a programming cycle having four operating cycles X61, X62, X63 and X64, and a driving cycle having one operating cycle X65.

[0105] During the programming cycle, a negative programming voltage plus the negative threshold voltage of the driving transistor 104 is stored in the storage capacitor 102, and the second storage capacitor 103 is discharged to zero.

[0106] As a result, the gate-source voltage of the driving transistor 104 goes to:

$$VGS=-VP-|VT| \quad \ldots(6)$$

where VGS represents the gate-source voltage of the driving transistor 104, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor 104.

[0107] In the first operating cycle X61: VDD goes to a high negative voltage, and VDATA is set to V2. SEL1 and SEL2 are low. Therefore, nodes A6 and B6 are charged to a negative voltage.

[0108] In the second operating cycle X62: While SEL1 is high and the switch transistor 106 is off, VDATA goes to a negative voltage. As a result, the voltage at node B6 decreases, and the voltage of node A6 is charged to the voltage of VDD. At this voltage, the OLED 100 is off.

[0109] In the third operating cycle X63: VDD goes to a reference voltage VREF. VDATA goes to (V2-VREF+VP) where VREF is a reference voltage. It is assumed that VREF is zero. However, VREF may be any voltage other than zero. At the beginning of this cycle, the voltage of node B6 becomes almost equal to the voltage of node A6 because the capacitance 101 of the OLED 100 is bigger than that of the storage capacitor 102. After that, the voltage of node B6 and the voltage of node A6 are charged through the driving transistor 104 until the driving transistor 104 turns off. As a result, the gate-source voltage of the driving transistor 104 is (-VP-|VT|), which is stored in the storage capacitor 102.

[0110] In the fourth operating cycle X64: SEL1 is high. Since SEL2 is low, and VDATA goes to V2, the voltage at node C6 goes to V2.

[0111] In the fifth operating cycle X65: VDD goes to its operating voltage during the driving cycle. In Figure 18, the operating voltage of VDD is zero. However, the operating voltage of VDD may be any voltage. SEL2 is high. The voltage stored in the storage capacitor 102 is applied to the gate terminal of the driving transistor 104. Thus, a current independent of the threshold voltage VT of the driving transistor 104 and the voltage of the OLED 100 flows through the driving transistor 104 and the OLED 100. Accordingly, the degradation of the OLED 100 and instability of the driving transistor 104 do not affect the amount of the current flowing through the driving transistor 54 and the OLED 100.

[0112] Figure 19 illustrates a pixel circuit 212 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 212 includes an OLED 110, two storage capacitors 112 and 113, a driving transistor 114, and switch transistors 116 and 118. The pixel circuit 212 corresponds to the pixel circuit 204 of Figure 10.

[0113] The transistors 114, 116 and 118 are p-type TFTs. The transistors 84 and 86 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

[0114] In Figure 19, one of the terminals of the driving transistor 114 is connected to the anode electrode of the OLED 110, while the other terminal is connected to a controllable voltage supply line VDD. The storage capacitors 112 and 113 are in series, and are connected between the gate terminal of the driving transistor 114 and a voltage supply electrode V2. Also, V2 may be connected to VDD. The cathode electrode of the OLED 100 is connected to a ground voltage supply electrode.

[0115] The OLED 110 and the transistors 114 and 116 are connected at node A7. The storage capacitor 112 and the transistors 114 and 116 are connected at node B7. The transistor 118 and the storage capacitors 112 and 113 are connected at node C7.

[0116] Figure 20 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 212 of Figure 19. Figure 20 corresponds to Figure 11. VDATA and VDD are used to programming and compensating for a time dependent parameter of the pixel circuit 212, which are similar to VDATA and VSS of Figure 11. Referring to Figures 19 and 20, the operation of the pixel circuit 212 includes a programming cycle having four operating cycles X71, X72 and X73, and a driving cycle having one operating cycle X74.

[0117] During the programming cycle, a negative programming voltage plus the negative threshold voltage of the driving transistor 114 is stored in the storage capacitor 112. The storage capacitor 113 is discharged to zero.

[0118] As a result, the gate-source voltage of the driving transistor 114 goes to:

$$VGS = -VP - |VT| \quad \ldots(7)$$

where VGS represents the gate-source voltage of the driving transistor 114, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor 114.

[0119] In the first operating cycle X71: VDD goes to a negative voltage. SEL is low. Node A7 and node B7 are charged to a negative voltage.

[0120] In the second operating cycle X72: VDD goes to a reference voltage VREF. VDATA goes to (V2-VREF+VP). The voltage at node B7 and the voltage of node A7 are changed until the driving transistor 114 turns off. The voltage of B7 is (-VREF-VT), and the voltage stored in the storage capacitor 112 is (-VP-|VT|).

[0121] In the third operating cycle X73: SEL goes to VM. VM is an intermediate voltage in which the switch transistor 106 is off and the switch transistor 118 is on. VDATA goes to V2. The voltage of node C7 goes to V2. The voltage stored in the storage capacitor 112 is the same as that of X72.

[0122] In the fourth operating cycle X74: VDD goes to its operating voltage. SEL is high. The voltage stored in the storage capacitor 112 is applied to the gate of the driving transistor 114. The driving transistor 114 is on. Accordingly, a current independent of the threshold voltage VT of the driving transistor 114 and the voltage of the OLED 110 flows through the driving transistor 114 and the OLED 110.

[0123] Figure 21 illustrates a pixel circuit 214 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 214 includes an OLED 120, two storage capacitors 122 and 123, a driving transistor 124, and switch transistors 126 and 128. The pixel circuit 212 corresponds to the pixel circuit 206 of Figure 12.

[0124] The transistors 124, 126 and 128 are p-type TFTs. The transistors 84 and 86 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

[0125] In Figure 21, one of the terminals of the driving transistor 124 is connected to the anode electrode of the OLED 120, while the other terminal is connected to a voltage supply line VDD. The storage capacitors 122 and 123 are in series, and are connected between the gate terminal of the driving transistor 124 and VDD. The cathode electrode of the OLED 120 is connected to a controllable voltage supply electrode VSS.

[0126] The OLED 120 and the transistors 124 and 126 are connected at node A8. The storage capacitor 122 and the transistors 124 and 126 are connected at node B8. The transistor 128 and the storage capacitors 122 and 123 are connected at node C8.

[0127] Figure 22 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 214 of Figure 21. Figure 22 corresponds to Figure 13. VDATA and VSS are used to programming and compensating for a time dependent parameter of the pixel circuit 214, which are similar to VDATA and VDD of Figure 13. Referring to Figures 21 and 22, the programming of the pixel circuit 214 includes a programming cycle having four operating cycles X81, X82, X83 and X84, and a driving cycle having one driving cycle X85.

[0128] During the programming cycle, a negative programming voltage plus the negative threshold voltage of the driving transistor 124 is stored in the storage capacitor 122. The storage capacitor 123 is discharged to zero.

[0129] As a result, the gate-source voltage of the driving transistor 124 goes to:

$$VGS = -VP - |VT| \quad \ldots(8)$$

where VGS represents the gate-source voltage of the driving transistor 114, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor 124.

[0130] In the first operating cycle X81: VDATA goes to a high voltage. SELis low. Node A8 and node B8 are charged to a positive voltage.

[0131] In the second operating cycle X82: SEL is high. VSS goes to a reference voltage VREF1 where the OLED 60 is off.

[0132] In the third operating cycle X83: VDATA goes to (VREF2+VP) where VREF2 is a reference voltage. SEL is low. Therefore, the voltage of node B8 and the voltage of node A8 become equal at the beginning of this cycle. It is noted that the first storage capacitor 112 is large enough so that its voltage becomes dominant. After that, node B8 is charged through the driving transistor 124 until the driving transistor 124 turns off. As a result, the voltage of node B8 is (VDD-|VT|). The voltage stored in the first storage capacitor 122 is (-VREF2-VP-|VT|).

[0133] In the fourth operating cycle X84: SEL goes to VM where VM is an intermediate voltage at which the switch transistor 126 is off and the switch transistor 128 is on. VDATA goes to VREF2. The voltage of node C8 goes to VREF2.

[0134] This results in that the gate-source voltage VGS of the driving transistor 124 is (-VP-|VT|). Since VM<-VP-VT, the switch transistor 126 is off, and the voltage stored in the storage capacitor 122 stays at (-VP-|VT|).

[0135] In the fifth operating cycle X85: VSS goes to the operating voltage. SEL is low. The voltage stored in the storage capacitor 122 is applied to the gate of the driving transistor 124.

[0136] It is noted that a system for operating an array having the pixel circuit of Figure 8, 10, 12, 17, 19 or 21 may be similar to that of Figure 6 or 16. The array having the pixel circuit of Figure 8, 10, 12, 17, 19 or 21 may have array structure shown in Figure 7(a) or 7(b).

[0137] It is noted that each transistor can be replaced with p-type or n-type transistor based on concept of complementary circuits.

[0138] According to the embodiments of the present invention, the driving transistor is in saturation regime of operation. Thus, its current is defined mainly by its gate-source voltage VGS. As a result, the current of the driving transistor remains constant even if the OLED voltage changes since its gate-source voltage is stored in the storage capacitor.

[0139] According to the embodiments of the present invention, the overdrive voltage providing to a driving transistor is generated by applying a waveform independent of the threshold voltage of the driving transistor and/or the voltage of a light emitting diode voltage.

[0140] According to the embodiments of the present invention, a stable driving technique based on bootstrapping is provided (e.g. Figures 2-12 and 16-20).

[0141] The shift(s) of the characteristic(s) of a pixel element(s) (e.g. the threshold voltage shift of a driving transistor and the degradation of a light emitting device under prolonged display operation) is compensated for by voltage stored in a storage capacitor and applying it to the gate of the driving transistor. Thus, the pixel circuit can provide a stable current though the light emitting device without any effect of the shifts, which improves the display operating lifetime. Moreover, because of the circuit simplicity, it ensures higher product yield, lower fabrication cost and higher resolution than conventional pixel circuits.

[0142] The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

Claims

1. A method of programming a pixel circuit that drives a current-driven organic light emitting device independent of a threshold voltage of a driving transistor (24, 84) connected to the organic light emitting device (20, 80), the pixel circuit including:

a switch transistor (26, 86) operated according to a select line, the switch transistor (26, 86) being adapted to selectively couple a signal line (VDATA) to a gate terminal of the driving transistor (24, 84); and
a storage capacitor (21, 81) coupled across the gate terminal and a first terminal of the driving transistor (24, 84);
the first terminal of the driving transistor (24, 84) being connected to a first terminal of the organic light emitting device (20, 80) at a node (B1, B5), wherein a second terminal of the driving transistor is connected to a controllable voltage supply; the method comprising:

selecting the select line to turn on the switch transistor (26, 86) for applying voltages at the signal line (VDATA) to the gate of the driving transistor (24,86) through the switch transistor (26, 86); and
while the select line is selected:

During a first period (X11, X51), adjusting the controllable voltage supply to a first compensating voltage (VCOMPB) sufficient to turn off the organic light emitting device (20, 80) while applying a second compensating voltage (VCOMPA, -VCOMPA) different from the first compensating voltage (VCOMPB) to the signal line (VDATA), thereby charging the node (B1, B5) at the first compensating voltage (VCOMPB);
During a second period (X12, X52), adjusting the controllable voltage supply to a supply voltage (VH, VL) different from the first compensating voltage (VCOMPB) while applying a reference voltage (VREF) at the signal line (VDATA), thereby charging or discharging the storage capacitor through the driving transistor (24, 84) until the driving transistor (24, 84) turns off, and establishing a voltage defined by the threshold voltage of the driving transistor (24, 84) across the driving transistor (24, 84); and
during a third period (X13, X53), applying a combination of a programming voltage (VP) and the reference voltage (VREF) at the signal line (VDATA) so as to store a fixed voltage according to both the threshold voltage and the applied programming voltage in the storage capacitor (21, 81), thereby establishing said fixed voltage across the driving transistor (24, 84),
wherein the first period (X13, X53), second period (X12, X52), and third period (X13, X53) are performed in this order and are temporally continuous.

2. The method of claim 1, further comprising:

setting the controllable voltage supply to an operating voltage; and
deselecting the select line to complete the programming cycle and initiate a driving cycle while maintaining the fixed voltage across the driving

transistor (24, 84).

3. The method of claim 2, wherein the current of the driving transistor (24, 84) remains constant during the driving cycle even if the turn on voltage of the organic light emitting device (20, 80) changes, due to the fixed voltage being stored in the storage capacitor.

4. The method of claim 2 or 3, wherein the reference voltage is sufficient for preventing the organic light emitting device (20, 80) from being turned on prior to the initiation of the driving cycle.

5. The method of any one of claims 1 to 4, wherein the storage capacitor (21, 81) is coupled across the gate terminal and a source terminal of the driving transistor (24, 84).

6. The method of any one of claims 1 to 5, wherein the reference voltage is a ground voltage and the voltage stored on the node (B1, B5) following the driving transistor (24, 84) turning off is the negative of the threshold voltage.

7. The method of any one of claims 1 to 6, wherein the compensating voltage is also applied to the node (B1, B5) of the pixel circuit, and wherein
adjusting the controllable voltage supply to a supply voltage (VH, VL) comprises
adjusting the controllable voltage to an operating voltage during the charging or discharging of the node (B1, B5) of the pixel circuit.

8. A display system comprising:

a pixel circuit including:

a driving transistor (24, 84) having a gate terminal, a first terminal, and a second terminal, the first terminal being connected to a first terminal of a light-emitting device (20, 80) at a node (B1, B5), the driving transistor (24, 84) having a threshold voltage VT that shifts during operation of the driving transistor (24, 84);
a switch transistor (26, 86) operated according to a select line, the switch transistor (26, 86) being adapted to selectively couple a signal line (VDATA) to the gate terminal of the driving transistor (24, 84); and
a storage capacitor (21, 81) coupled across the gate terminal and the first terminal of the driving transistor (24, 84); and

a controllable power supply connected to the second terminal of the driving transistor (24, 84), wherein the controllable power supply is configured to be adjusted during a first cycle (X11, X51) to a first compensating voltage (VCOMPB) sufficient to turn off the light-emitting device (20, 80) and subsequently adjusted during a second cycle (X12, X52) to a supply voltage (VH, VL) different from the first compensating voltage (VCOMPB);
wherein the pixel circuit is configured to receive during the first cycle (X11, X51) a second compensating voltage (VCOMPA, -VCOMPA) different from the first compensating voltage (VCOMPB) applied at the signal line (VDATA), thereby charging the node (B1, B5) at the first compensating voltage (VCOMPB),
wherein the pixel circuit is configured to receive during the second cycle (X12, X52) a reference voltage (VREF) applied at the signal line (VDATA) thereby charging or discharging the storage capacitor (21, 81) through the driving transistor (24, 84) until the driving transistor (24, 84) turns off, thereby establishing a voltage defined by the threshold voltage of the driving transistor (24, 84) across the driving the transistor (24, 84);
wherein the pixel circuit is further adapted to receive during a third cycle (X13, X53) subsequent to the second cycle (X12, X52) a combination of a programming voltage (VP) and the reference voltage (VREF) at the signal line (VDATA) and to apply the combination of the programming voltage (VP) and the reference voltage (VREF), via the switch transistor (26, 86), to the gate terminal of the driving transistor (24, 84) so as to store a fixed voltage according to both the threshold voltage and the programming voltage in the storage capacitor (21, 81), thereby establishing the fixed voltage across the driving transistor (24, 84);
wherein the select line, during each of the first cycle (X11, X51), the second cycle (X12, X52), and the third cycle (X13, X53) is set at a voltage level for which the switch transistor (26, 86) is turned on for applying voltages at the signal line (VDATA) to the gate of the driving transistor (24,86) through the switch transistor (26, 86),
wherein the first cycle (X11, X51), the second cycle (X12, X52) and the third cycle (X13, X53) are temporally continuous.

9. The display system of claim 8, wherein the pixel circuit includes an organic light emitting diode supplied with the stable pixel current from the driving transistor, and the stable pixel current maintains a substantially constant brightness of the light emitted by the organic light emitting diode.

10. The display system of any one of claims 8 to 9, wherein
the storage capacitor (21, 81) is adapted to maintain

the fixed voltage across the driving transistor (24, 84) during a driving cycle of the pixel circuit.

11. The display system of any one of claims 8 to 10, wherein the light-emitting device (20, 80) is an organic light emitting diode and the driving transistor is an n-type or p-type thin film transistor.

Patentansprüche

1. Verfahren zum Programmieren einer Pixelschaltung, die eine stromgetriebene organische Lichtemissionseinrichtung unabhängig von einer Schwellwertspannung eines mit der organischen Lichtemissionseinrichtung (20, 80) verbundenen Treibertransistors (24, 84) treibt, wobei die Pixelschaltung umfasst:

einen Schalttransistor (26, 86), der gemäß einer Auswahlleitung betrieben wird, wobei der Schalttransistor (26, 86) ausgebildet ist, um wahlweise eine Signalleitung (VDATA) mit einem Gate-Anschluss des Treibertransistors (24, 84) zu koppeln, und
einen Speicherkondensator (21, 81), der über den Gate-Anschluss und einen ersten Anschluss des Treibertransistors (24, 84) gekoppelt ist,
wobei der erste Anschluss des Treibertransistors (24, 84) mit einem ersten Anschluss der organischen Lichtemissionseinrichtung (20, 80) an einem Knoten (B1, B5) verbunden ist, wobei ein zweiter Anschluss des Treibertransistors mit einer steuerbaren Spannungsversorgung verbunden ist,
wobei das Verfahren umfasst:

Auswählen der Auswahlleitung zum Einschalten des Schalttransistors (26, 86) für das Anlegen von Spannungen der Signalleitung (VDATA) an dem Gate des Treibertransistors (24, 86) über den Schalttransistor (26, 86), und
während die Auswahlleitung ausgewählt ist:

während einer ersten Periode (X11, X51), Einstellen der steuerbaren Spannungsversorgung zu einer ersten Kompensationsspannung (VCOMPB), die ausreicht, um die organische Lichtemissionseinrichtung (20, 80) auszuschalten, während eine zweite Kompensationsspannung (VCOMPA, -VCOMPA), die sich von der ersten Kompensationsspannung (VCOMPB) unterscheidet, an der Signalleitung (VDATA) angelegt wird, um dadurch den Knoten (B1, B5) mit der ersten Kompensationsspannung (VCOMPB) zu laden,
während einer zweiten Periode (X12, X52), Einstellen der steuerbaren Spannungsversorgung zu einer Versorgungsspannung (VH, VL), die sich von der ersten Kompensationsspannung (VCOMPB) unterscheidet, während eine Referenzspannung (VREF) an der Signalleitung (VDATA) angelegt wird, um dadurch den Speicherkondensator über den Treibertransistor (24, 84) zu laden oder zu entladen, bis der Treibertransistor (24, 84) ausschaltet, und Herstellen einer Spannung, die durch die Schwellwertspannung des Treibertransistors (24, 84) definiert wird, über den Treibertransistor (24, 84), und
während einer dritten Periode (X13, X53), Anlegen einer Kombination aus einer Programmierspannung (VP) und der Referenzspannung (VREF) an der Signalleitung (VDATA), um eine fixe Spannung in Entsprechung zu der Schwellwertspannung und der angelegten Programmierspannung in dem Speicherkondensator (21, 81) zu speichern, um dadurch die fixe Spannung über den Treibertransistor (24, 84) herzustellen,

wobei die erste Periode (X13, X53), die zweite Periode (X12, X52) und die dritte Periode (X13, X53) in dieser Reihenfolge durchgeführt werden und zeitlich aneinander anschließen.

2. Verfahren nach Anspruch 1, das weiterhin umfasst:

Setzen der steuerbaren Spannungsversorgung zu einer Betriebsspannung, und
Aufheben der Auswahl der Auswahlleitung, um den Programmierzyklus abzuschließen und einen Treiberzyklus einzuleiten, während die fixe Spannung über den Treibertransistor (24, 84) aufrechterhalten wird.

3. Verfahren nach Anspruch 2, wobei der Strom des Treibertransistors (24, 84) während des Treiberzyklus auch dann konstant bleibt, wenn sich die Einschaltspannung der organischen Lichtemissionseinrichtung (20, 80) ändert, weil die fixe Spannung in dem Speicherkondensator gespeichert ist.

4. Verfahren nach Anspruch 2 oder 3, wobei die Referenzspannung ausreicht, um zu verhindern, dass die

organische Lichtemissionseinrichtung (20, 80) eingeschaltet wird, bevor der Treiberzyklus eingeleitet wird.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei der Speicherkondensator (21, 81) über den Gate-Anschluss und einen Source-Anschluss des Treibertransistors (24, 84) gekoppelt ist.

6. Verfahren nach einem der Ansprüche 1 bis 5, wobei die Referenzspannung eine Erdungsspannung ist und die an dem Knoten (B1, B5) gespeicherte Spannung auf das Ausschalten des Treibertransistors (24, 84) folgend die Negative der Schwellwertspannung ist.

7. Verfahren nach einem der Ansprüche 1 bis 6, wobei die Kompensationsspannung auch an dem Knoten (B1, B5) der Pixelschaltung angelegt wird, und wobei:

das Einstellen der steuerbaren Spannungsversorgung zu einer Versorgungsspannung (VH, VL) das Einstellen der steuerbaren Spannung zu einer Betriebsspannung während des Ladens oder Entladens des Knotens (B1, B5) der Pixelschaltung umfasst.

8. Anzeigesystem, das umfasst:

eine Pixelschaltung, die enthält:

einen Treibertransistor (24, 84), der einen Gate-Anschluss, einen ersten Anschluss und einen zweiten Anschluss aufweist, wobei der erste Anschluss mit einem ersten Anschluss einer Lichtemissionseinrichtung (20, 80) an einem Knoten (B1, B5) verbunden ist, wobei der Treibertransistor (24, 84) eine Schwellwertspannung VT aufweist, die während des Betriebs des Treibertransistors (24, 84) variiert,
einen Schalttransistor (26, 86), der gemäß einer Auswahlleitung betrieben wird, wobei der Schalttransistor (26, 86) ausgebildet ist, um wahlweise eine Signalleitung (VDATA) mit dem Gate-Anschluss des Treibertransistors (24, 84) zu koppeln, und
einen Speicherkondensator (21, 81), der über den Gate-Anschluss und den ersten Anschluss des Treibertransistors (24, 84) gekoppelt ist, und
eine steuerbare Stromversorgung, die mit dem zweiten Anschluss des Treibertransistors (24, 84) verbunden ist,

wobei die steuerbare Stromversorgung konfiguriert ist, um während eines ersten Zyklus (X11, X51) zu einer ersten Kompensationsspannung (VCOMPB) eingestellt zu werden, die ausreicht, um die Lichtemissionseinrichtung (20, 80) auszuschalten, und anschließend während eines zweiten Zyklus (X12, X52) zu einer Versorgungsspannung (VH, VL), die sich von der ersten Kompensationsspannung (VCOMPB) unterscheidet, eingestellt zu werden,
wobei die Pixelschaltung konfiguriert ist, um während des ersten Zyklus (X11, X51) eine zweite Kompensationsspannung (VCOMPA, -VCOMPA), die sich von der an der Signalleitung (VDATA) angelegten ersten Kompensationsspannung (VCOMPB) unterscheidet, zu empfangen, um dadurch den Knoten (B1, B5) mit der ersten Kompensationsspannung (VCOMPB) zu laden,
wobei die Pixelschaltung konfiguriert ist, um während des zweiten Zyklus (X12, X52) eine an der Signalleitung (VDATA) angelegte Referenzspannung (VREF) zu empfangen, um dadurch den Speicherkondensator (21, 81) über den Treibertransistor (24, 84) zu laden oder zu entladen, bis der Treibertransistor (24, 84) ausschaltet, um dadurch eine durch die Schwellwertspannung des Treibertransistors (24, 84) definierte Spannung über den Treibertransistor (24, 84) herzustellen,
wobei die Pixelschaltung weiterhin ausgebildet ist, um während eines dritten Zyklus (X13, X53), der auf den zweiten Zyklus (X12, X52) folgt, eine Kombination aus einer Programmierspannung (VP) und der Referenzspannung (VREF) an der Signalleitung (VDATA) zu empfangen und die Kombination aus der Programmierspannung (VP) und der Referenzspannung (VREF) über den Schalttransistor (26, 86) an dem Gate-Anschluss des Treibertransistors (24, 84) anzulegen, um eine fixe Spannung in Entsprechung zu der Schwellwertspannung und der Programmierspannung in dem Speicherkondensator (21, 81) zu speichern, um dadurch die fixe Spannung über den Treibertransistor (24, 84) herzustellen,
wobei die Auswahlleitung während des ersten Zyklus (X11, X51), des zweiten Zyklus (X12, X52) und des dritten Zyklus (X13, X53) auf einen Spannungspegel gesetzt ist, bei dem der Schalttransistor (26, 86) eingeschaltet ist, um Spannungen der Signalleitung (VDATA) an dem Gate des Treibertransistors (24, 86) über den Schalttransistor (26, 86) anzulegen,
wobei der erste Zyklus (X11, X51), der zweite Zyklus (X12, X52) und der dritte Zyklus (X13, X53) zeitlich aneinander anschließen.

9. Anzeigesystem nach Anspruch 8, wobei die Pixelschaltung eine organische Lichtemissionsdiode um-

fasst, zu welcher der stabile Pixelstrom von dem Treibertransistor zugeführt wird, wobei der stabile Pixelstrom eine im Wesentlichen konstante Helligkeit des durch die organische Lichtemissionsdiode emittierten Lichts aufrechterhält.

10. Anzeigesystem nach Anspruch 8 oder 9, wobei:

der Speicherkondensator (21, 81) ausgebildet ist, um die fixe Spannung über den Treibertransistor (24, 84) während eines Treiberzyklus der Pixelschaltung aufrechtzuerhalten.

11. Anzeigesystem nach einem der Ansprüche 8 bis 10, wobei die Lichtemissionseinrichtung (20, 80) eine organische Lichtemissionsdiode ist und der Treibertransistor ein n-Typ- oder p-Typ-Dünnfilmtransistor ist.

Revendications

1. Procédé de programmation d'un circuit de pixel qui pilote un dispositif électroluminescent organique entraîné par du courant électrique, indépendant d'une tension seuil d'un transistor d'attaque (24, 84) relié au dispositif électroluminescent organique (20, 80), le circuit de pixel comprenant:

un transistor de commutation (26, 86) fonctionnant selon une ligne de sélection, le transistor de commutation (26, 86) étant prévu pour coupler sélectivement une ligne de signal (VDATA) à une borne de grille du transistor d'attaque (24, 84); et
un condensateur de stockage (21, 81) couplé de part et d'autre de la borne de grille et une première borne du transistor d'attaque (24, 84); la première borne du transistor d'attaque (24, 84) étant connectée à une première borne du dispositif électroluminescent organique (20, 80) au niveau d'un noeud (B1, B5), dans lequel une seconde borne du transistor d'attaque est connectée à une alimentation de tension contrôlable;
le procédé consistant à:

sélectionner la ligne de sélection pour activer le transistor de commutation (26, 86) pour appliquer des tensions au niveau de la ligne de signal (VDATA) à la grille du transistor d'attaque (24, 86) à travers le transistor de commutation (26, 86); et
tandis que la ligne de sélection est sélectionnée:

pendant une première période (X11, X51), en ajustant l'alimentation de tension contrôlable à une première tension de compensation (VCOMPB) suffisante pour désactiver le dispositif électroluminescent organique (20, 80) tout en appliquant une seconde tension de compensation (VCOMPA, -VCOMPA) différente de la première tension de compensation (VCOMPB) à la ligne de signal (VDATA), chargeant ainsi le noeud (B1, B5) à la première tension de compensation (VCOMPB);
pendant une deuxième période (X12, X52), le réglage de l'alimentation en tension contrôlable à une tension d'alimentation (VH, VL) différente de la première tension de compensation (VCOMPB) lors de l'application d'une tension de référence (VREF) au niveau de la ligne de signal (VDATA), chargeant ou déchargeant ainsi le condensateur de stockage à travers le transistor d'attaque (24, 84) jusqu'à ce que le transistor d'attaque (24, 84) soit désactivé, et établir une tension définie par la tension seuil du transistor d'attaque (24, 84) de part et d'autre du transistor d'attaque (24, 84); et
au cours d'une troisième période (X13, X53), appliquer une combinaison d'une tension de programmation (VP) et de la tension de référence (VREF) au niveau de la ligne de signal (VDATA) de façon à stocker une tension fixe à la fois selon à la fois la tension seuil et la tension de programmation appliquée dans le condensateur de stockage (21, 81),

en établissant ainsi ladite tension fixe de part et d'autre du transistor d'attaque (24, 84)
dans lequel la première période (X13, X53), la deuxième période (X12, X52) et la troisième période (X13, X53) sont effectuées dans cet ordre et sont temporellement continues.

2. Procédé selon la revendication 1, consistant en outre à:

régler l'alimentation de tension contrôlable sur une tension de fonctionnement; et
désélectionner la ligne de sélection pour compléter le cycle de programmation et lancer un cycle d'attaque tout en maintenant la tension fixe de part et d'autre du transistor d'attaque (24, 84).

3. Procédé selon la revendication 2, dans lequel le courant du transistor d'attaque (24, 84) reste constante

pendant le cycle d'attaque même si la tension d'activation du dispositif électroluminescent organique (20, 80) change, en raison de la tension fixe stockée dans le condensateur de stockage.

4. Procédé selon la revendication 2 ou la revendication 3, dans lequel la tension de référence est suffisante pour empêcher l'activation du dispositif électroluminescent organique (20, 80) avant l'amorçage du cycle d'attaque.

5. Procédé selon l'une quelconque des revendications 1 à 4, dans lequel le condensateur de stockage (21, 81) est couplé de part et d'autre de la borne de grille et d'une borne de source du transistor d'attaque (24, 84).

6. Procédé selon l'une quelconque des revendications 1 à 5, dans lequel la tension de référence est une tension de masse et l'inhibition de la tension stockée sur le noeud (B1, B5) en aval du transistor d'attaque (24, 84) est le négatif de la tension seuil.

7. Procédé selon l'une quelconque des revendications 1 à 6, dans lequel la tension de compensation est également appliquée au noeud (B1, B5) du circuit de pixel, et dans lequel
le réglage de l'alimentation en tension contrôlable à une tension d'alimentation (VH, VL) comprend le réglage de la tension contrôlable à une tension de fonctionnement pendant la charge ou la décharge du noeud (B1, B5) du circuit de pixel.

8. Système d'affichage comprenant:

un circuit de pixel comprenant:

un transistor d'attaque (24, 84) ayant une borne de grille, une première borne et une seconde borne, la première borne étant connectée à une première borne d'un dispositif électroluminescent (20, 80) au niveau d'un noeud (B1, B5), le transistor d'attaque (24, 84) ayant une tension seuil VT qui varie pendant le fonctionnement du transistor d'attaque (24, 84);
un transistor de commutation (26, 86) fonctionnant selon une ligne de sélection, le transistor de commutation (26, 86) étant prévu pour coupler sélectivement une ligne de signal (VDATA) à une borne de grille du transistor d'attaque (24, 84); et
un condensateur de stockage (21, 81) couplé de part et d'autre de la borne de grille et une première borne du transistor d'attaque (24, 84); et

une alimentation électrique contrôlable connectée à la seconde borne du transistor d'attaque (24, 84),
dans lequel l'alimentation électrique contrôlable est configurée pour être ajustée pendant un premier cycle (X11, X51) à une première tension de compensation (VCOMPB) suffisante pour éteindre le dispositif électroluminescent (20, 80) et ensuite ajustée pendant un second cycle (X12, X52) à une tension d'alimentation (VH, VL) différente de la première tension de compensation (VCOMPB);
dans lequel le circuit de pixel est configuré pour recevoir pendant le premier cycle (X11, X51) une seconde tension de compensation (VCOMPA, -VCOMPA) différente de la première tension de compensation (VCOMPB) appliquée à la ligne de signal (VDATA), chargeant ainsi le noeud (B1, B5) à la première tension de compensation (VCOMPB),
dans lequel le circuit de pixel est configuré pour recevoir pendant le second cycle (X12, X52) une tension de référence (VREF) appliquée à la ligne de signal (VDATA), chargeant ou déchargeant ainsi le condensateur de stockage (21, 81) de part et d'autre du transistor d'attaque (24, 84) jusqu'à ce que le transistor d'attaque (24, 84) se désactive, établissant ainsi une tension définie par la tension seuil du transistor d'attaque (24, 84) de part et d'autre de l'attaque du transistor (24, 84);
dans lequel le circuit de pixel est en outre prévu pour recevoir pendant un troisième cycle (X13, X53) après le second cycle (X12, X52) une combinaison d'une tension de programmation (VP) et de la tension de référence (VREF) au niveau de la ligne de signal (VDATA) et pour appliquer la combinaison de la tension de programmation (VP) et de la tension de référence (VREF), par l'intermédiaire du transistor de commutation (26, 86), à la borne de grille du transistor d'attaque (24, 84) de manière à stocker une tension fixe selon à la fois la tension seuil et la tension de programmation dans le condensateur de stockage (21, 81), établissant ainsi la tension fixe de part et d'autre du transistor d'attaque (24, 84);
dans lequel la ligne de sélection, au cours du premier cycle (X11, X51), du deuxième cycle (X12, X52) et du troisième cycle (X13, X53) est réglée à un niveau de tension pour lequel le transistor de commutation (26, 86) est activé pour appliquer des tensions au niveau de la ligne de signal (VDATA) à la grille du transistor d'attaque (24, 86) à travers le transistor de commutation (26, 86) dans lequel le premier cycle (X11, X51), le deuxième cycle (X12, X52) et le troisième cycle (X13, X53) sont temporellement continus.

9. Système d'affichage selon la revendication 8, dans lequel le circuit de pixel comprend une diode électroluminescente organique alimentée par le courant de pixel stable provenant du transistor d'attaque et le courant de pixel stable maintient une luminosité sensiblement constante de la lumière émise par la diode électroluminescente organique.

10. Système d'affichage selon l'une quelconque des revendications 8 à 9, dans lequel:

le condensateur de stockage (21, 81) est prévu pour maintenir la tension fixe de part et d'autre du transistor d'attaque (24, 84) pendant un cycle d'attaque du circuit de pixel.

11. Système d'affichage selon l'une quelconque des revendications 8 à 10, dans lequel le dispositif électroluminescent (20, 80) est une diode électroluminescente organique et le transistor d'attaque est un transistor à couches minces de type n ou de type p.

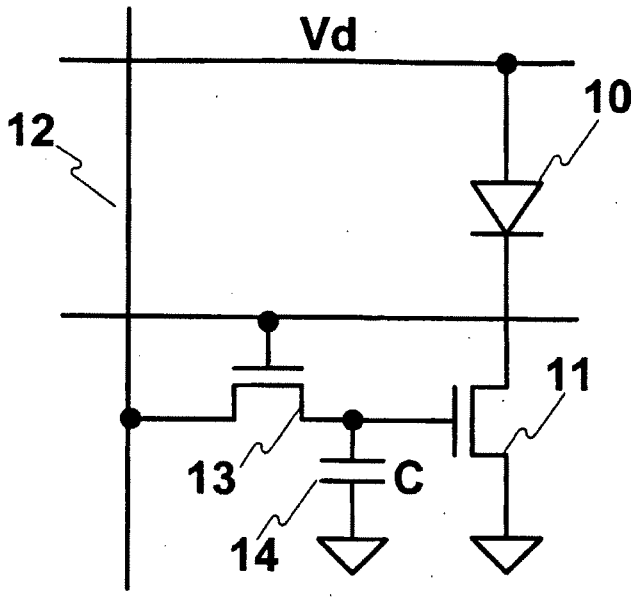
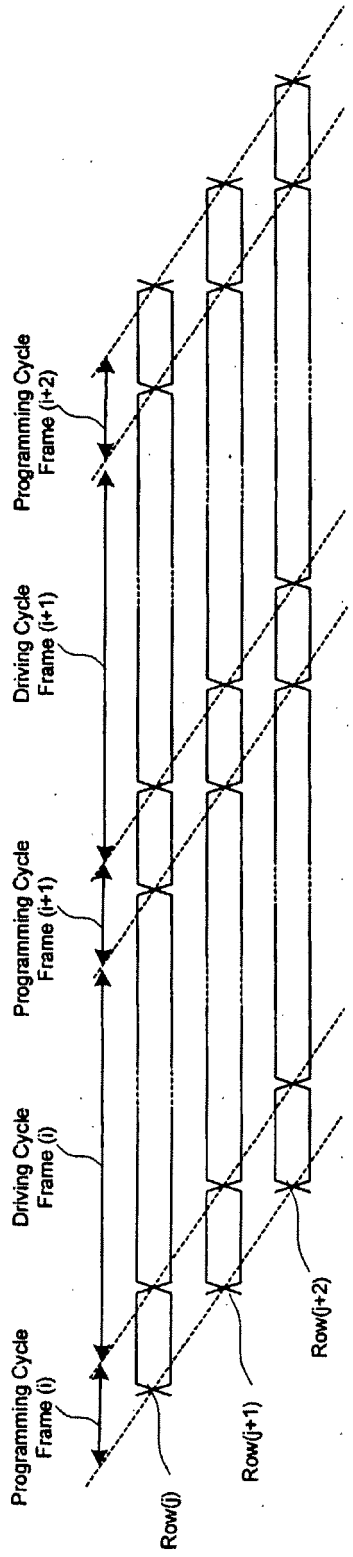


Figure 1

Prior Art


Programming Cycle Frame (i)
Driving Cycle Frame (i)
Programming Cycle Frame (i+1)
Driving Cycle Frame (i+1)
Programming Cycle Frame (i+2)
Row(j)
Row(j+1)
Row(j+2)

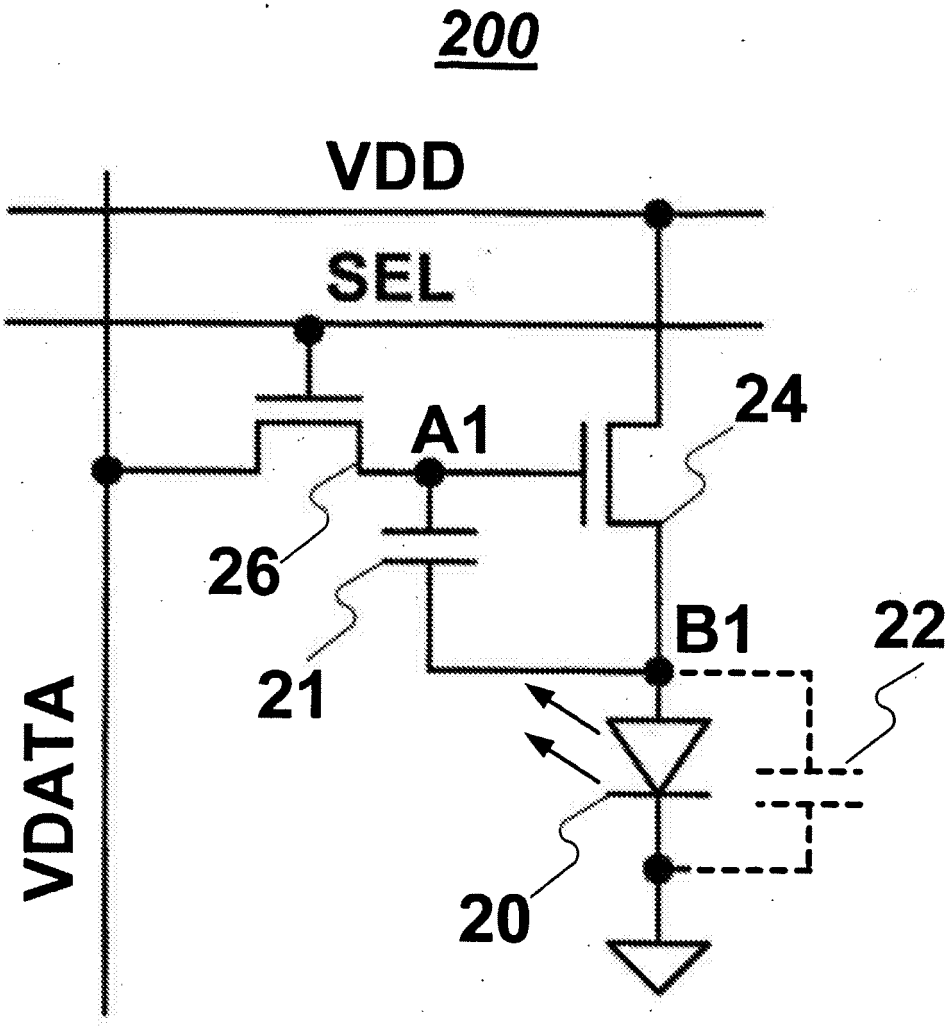


Figure 3

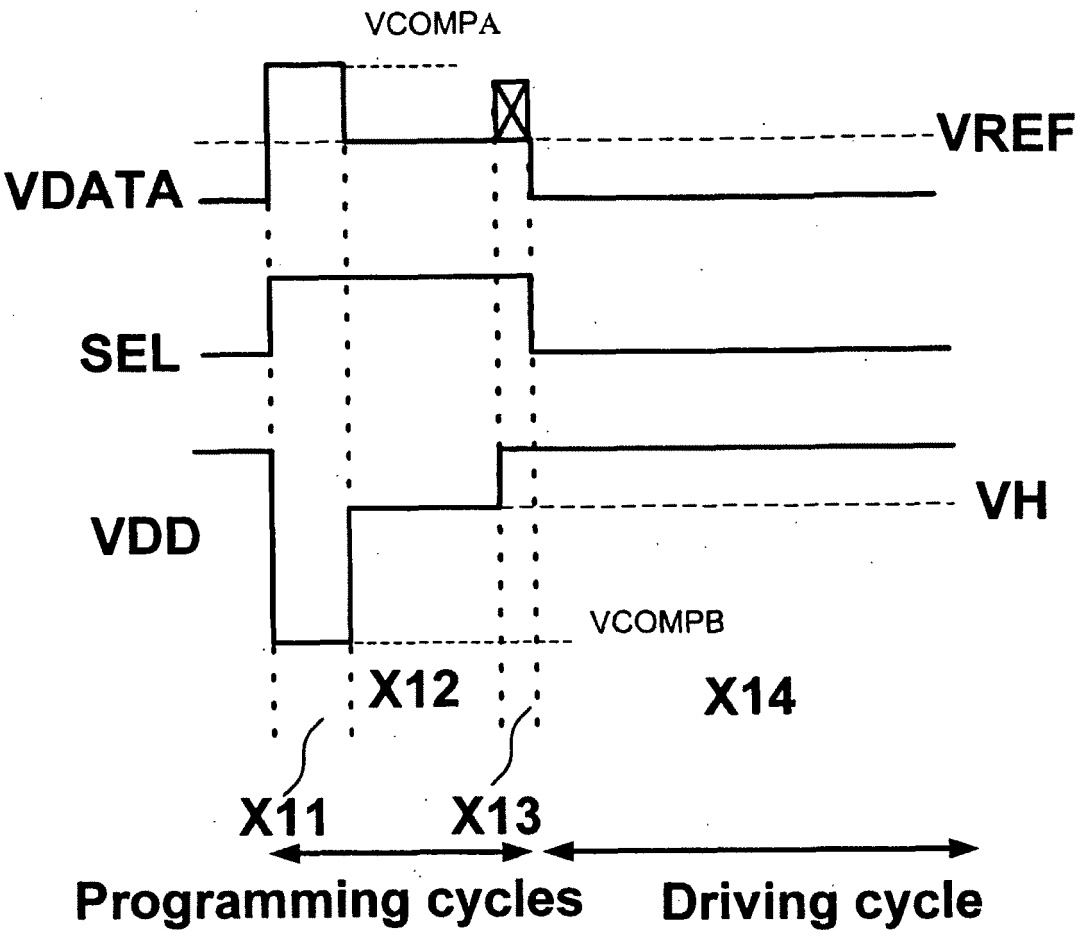

VCOMPA
VREF
VDATA
SEL
VH
VDD
VCOMPB
X12
X14
X11
X13
Programming cycles
Driving cycle

Figure 4

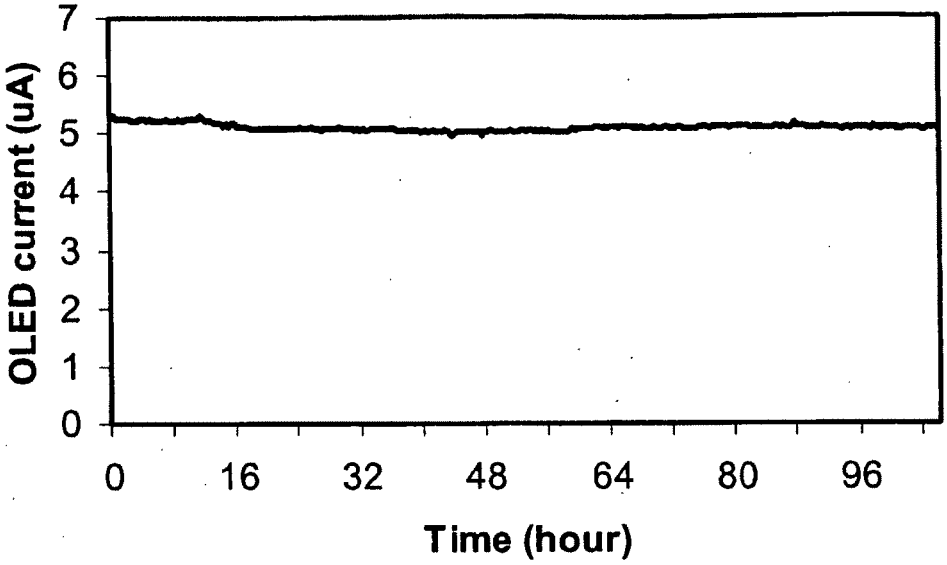


Figure 5

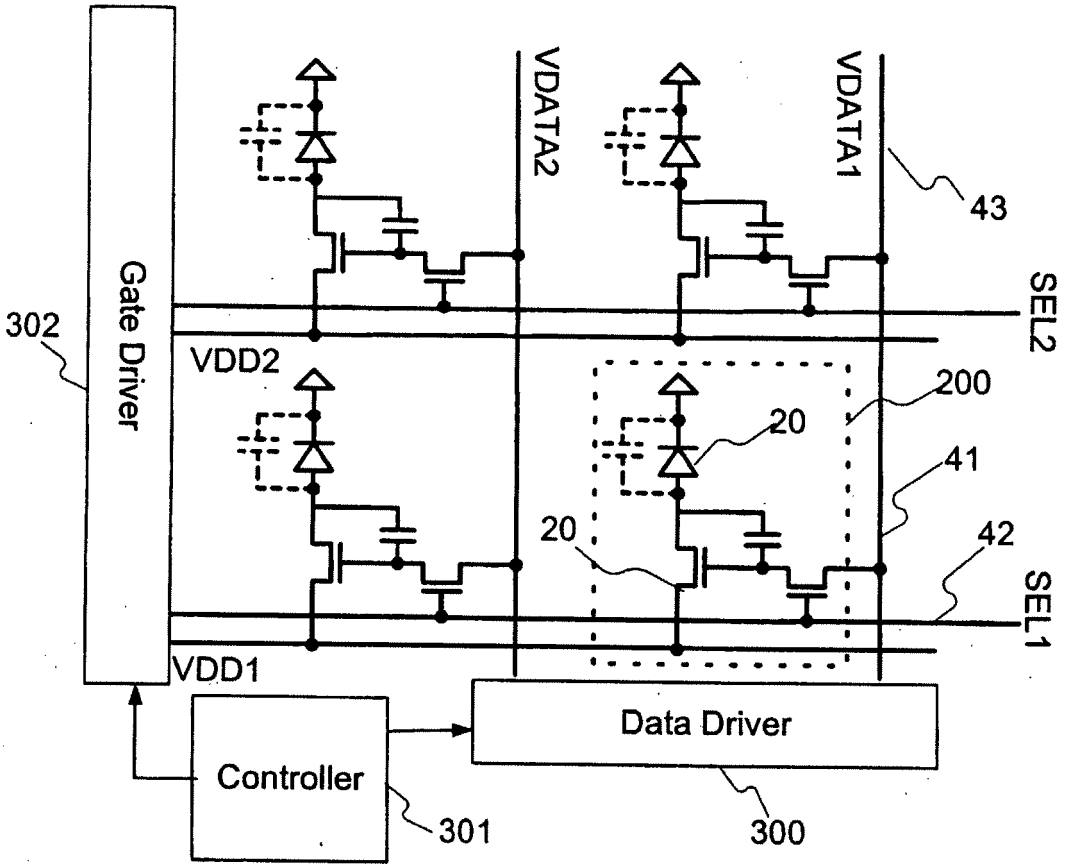
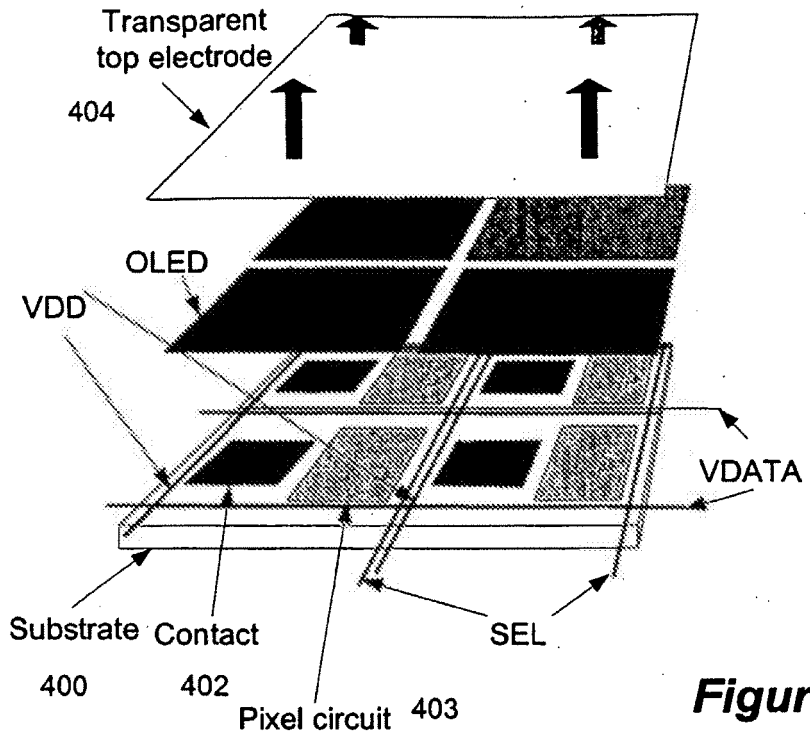
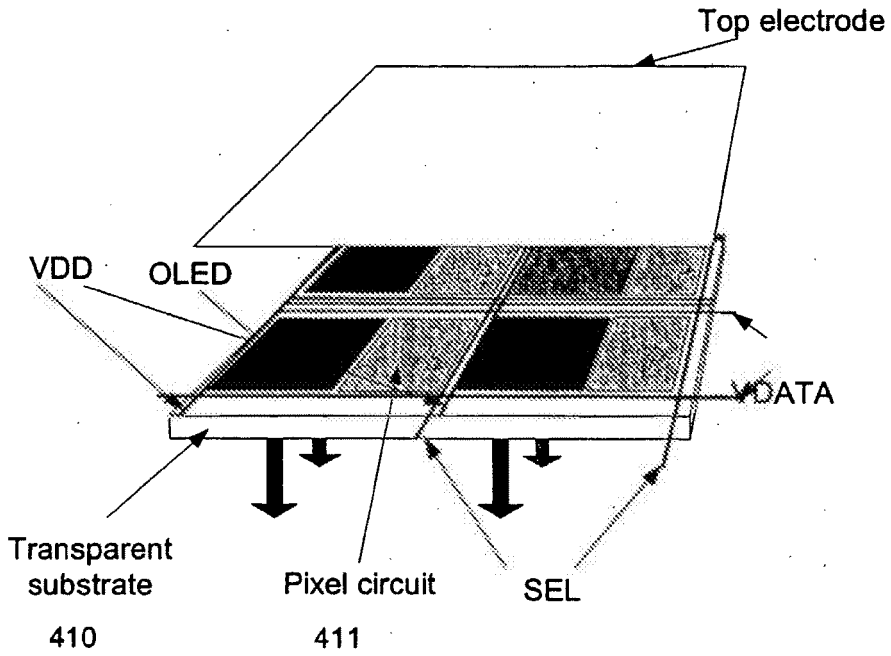

Gate Driver
302
VDATA2
VDATA1
43
SEL2
VDD2
200
20
41
20
42
SEL1
VDD1
Data Driver
Controller
301
300

Figure 6



Top emission pixels

Figure 7(a)



Bottom emission pixels

Figure 7(b)

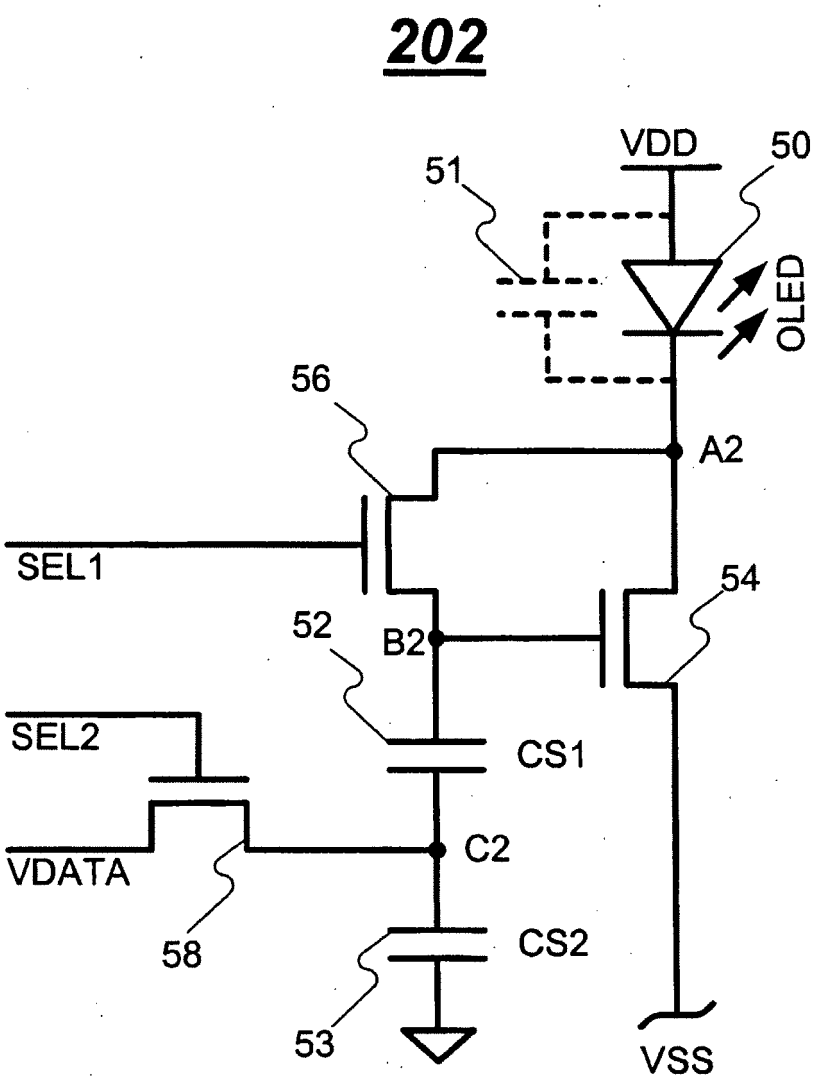

202
VDD
50
51
OLED
56
A2
SEL1
54
52
B2
SEL2
CS1
C2
VDATA
58
CS2
53
VSS

Figure 8

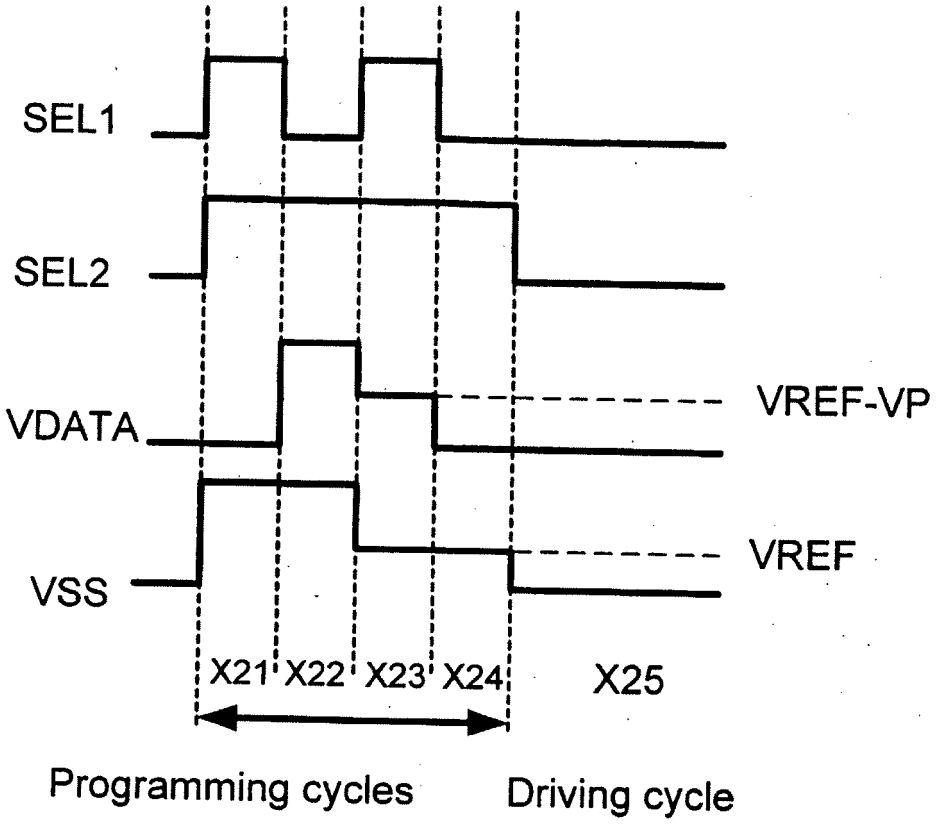

SEL1
SEL2
VDATA
VSS
VREF-VP
VREF
X21
X22
X23
X24
X25
Programming cycles
Driving cycle

Figure 9

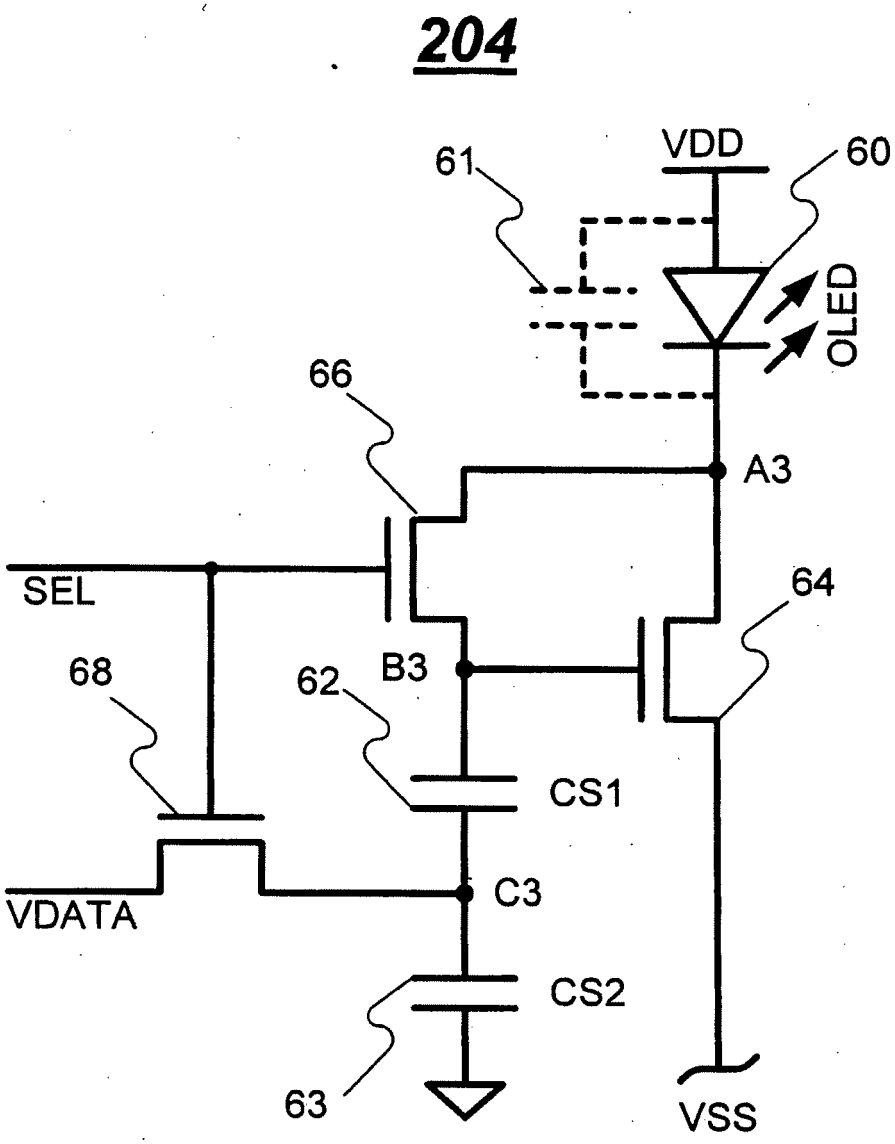


Figure 10

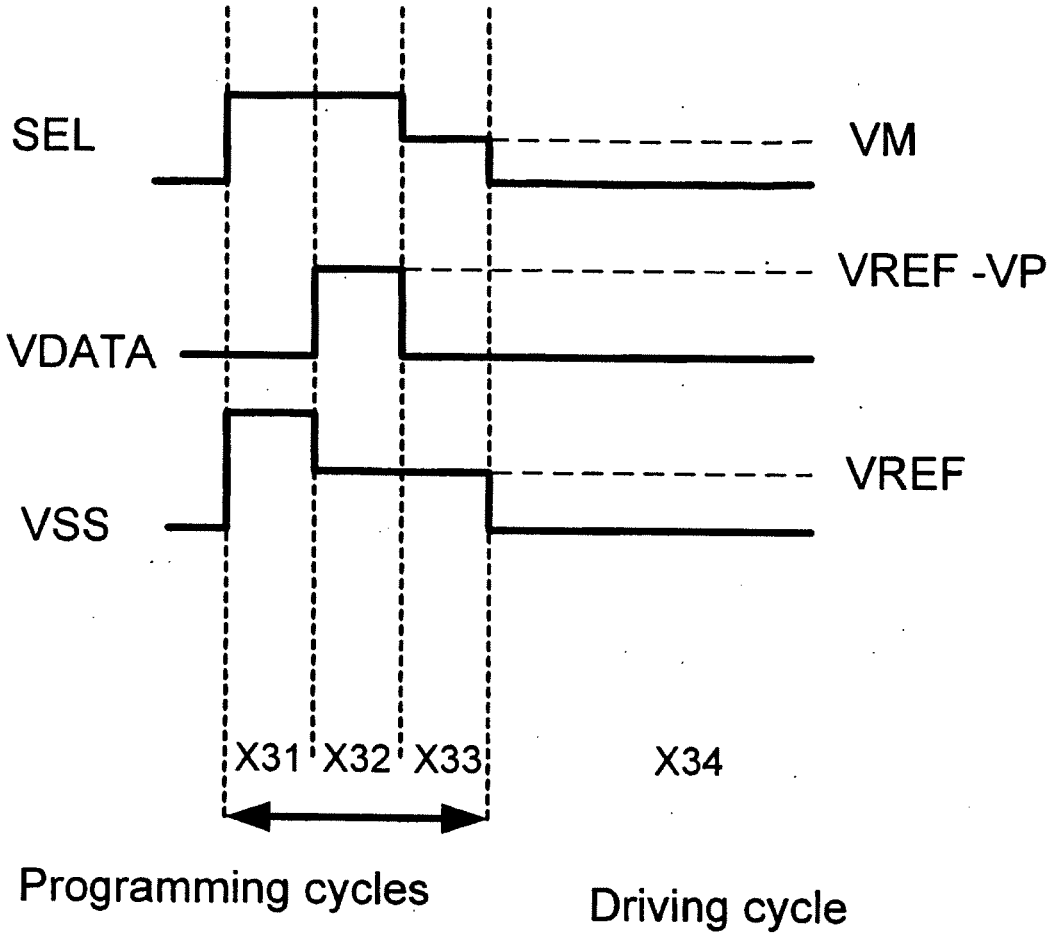

SEL
VM
VREF -VP
VDATA
VREF
VSS
X31
X32
X33
X34
Programming cycles
Driving cycle

Figure 11

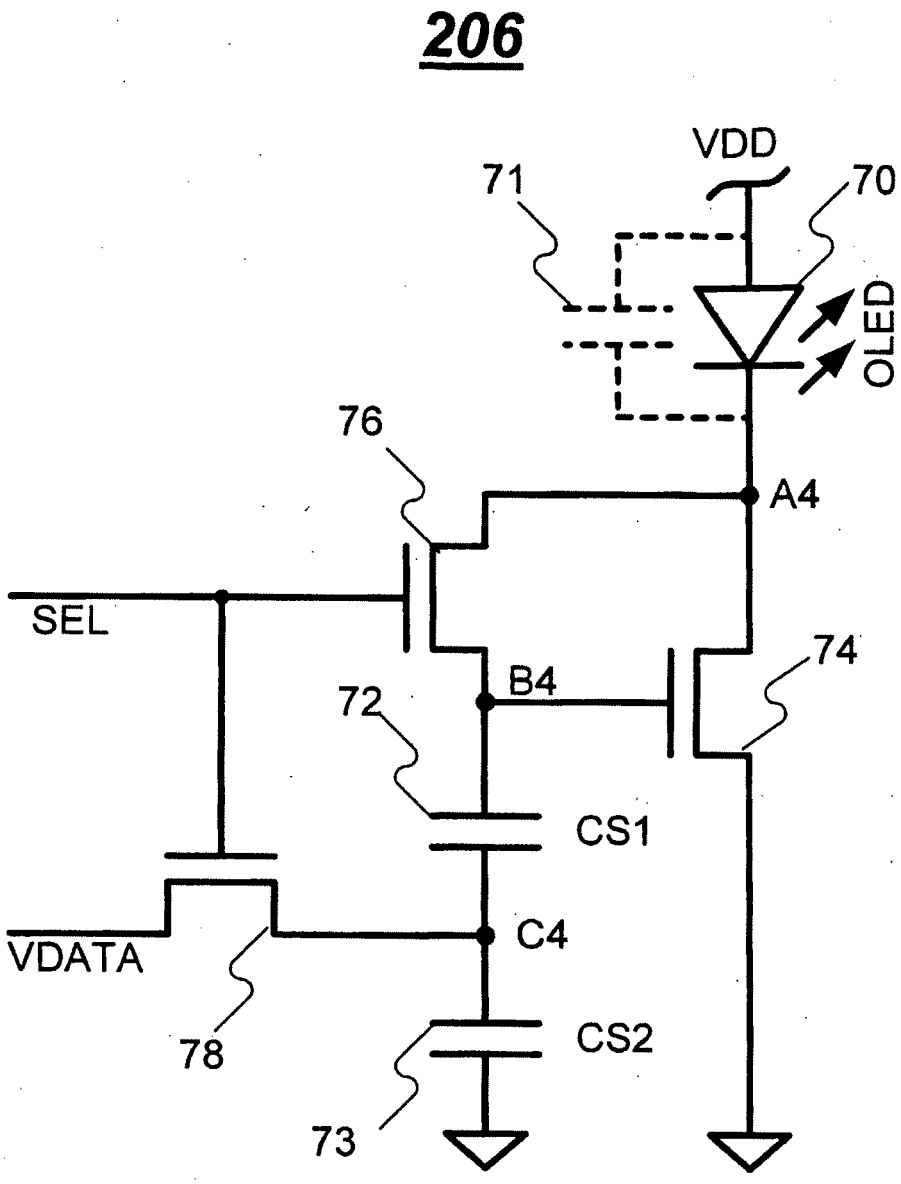


Figure 12

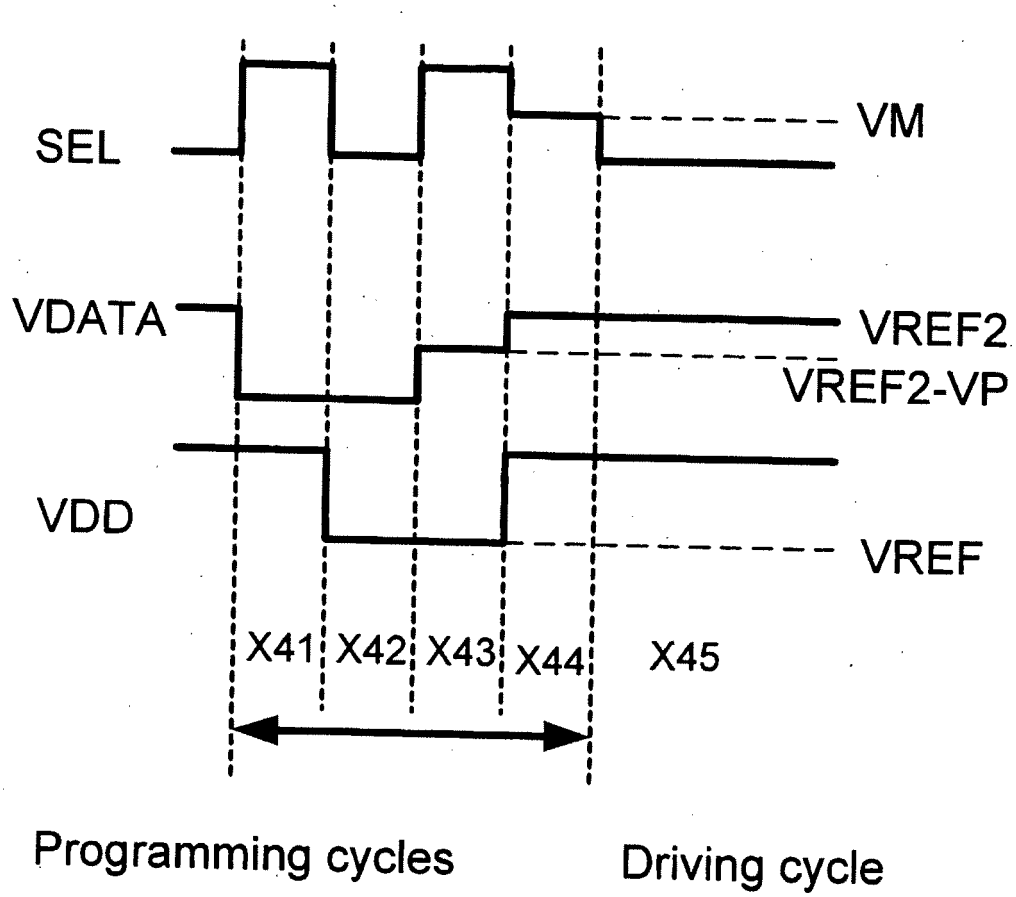

SEL
VM
VDATA
VREF2
VREF2-VP
VDD
VREF
X41
X42
X43
X44
X45
Programming cycles
Driving cycle

Figure 13

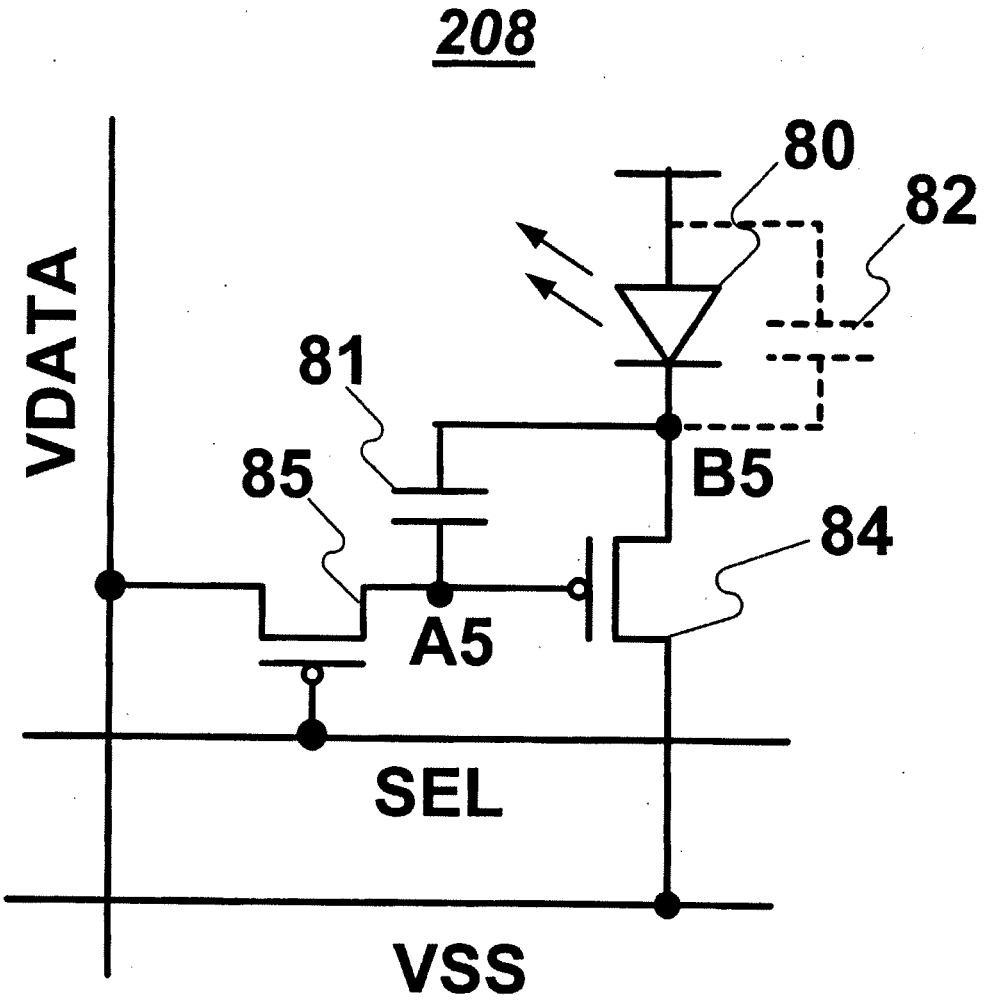


Figure 14

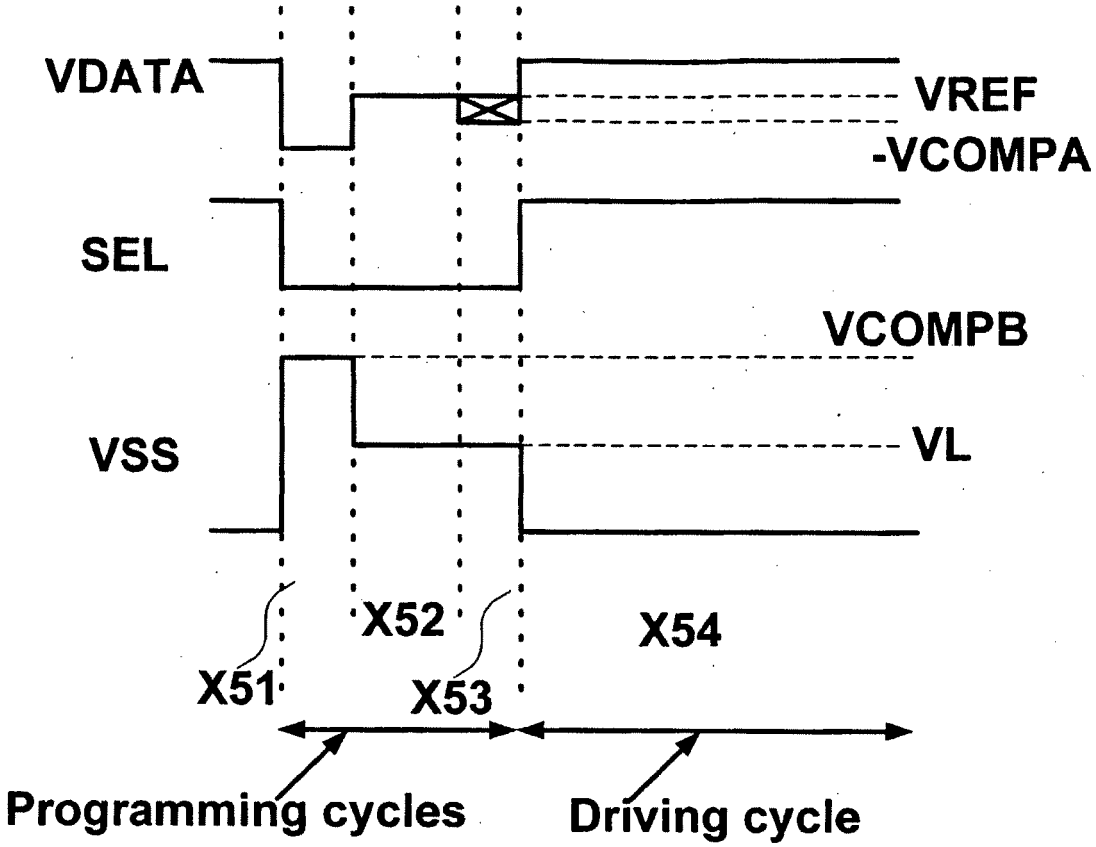

VDATA
VREF
-VCOMPA
SEL
VCOMPB
VSS
VL
X51
X52
X53
X54
Programming cycles
Driving cycle

Figure 15

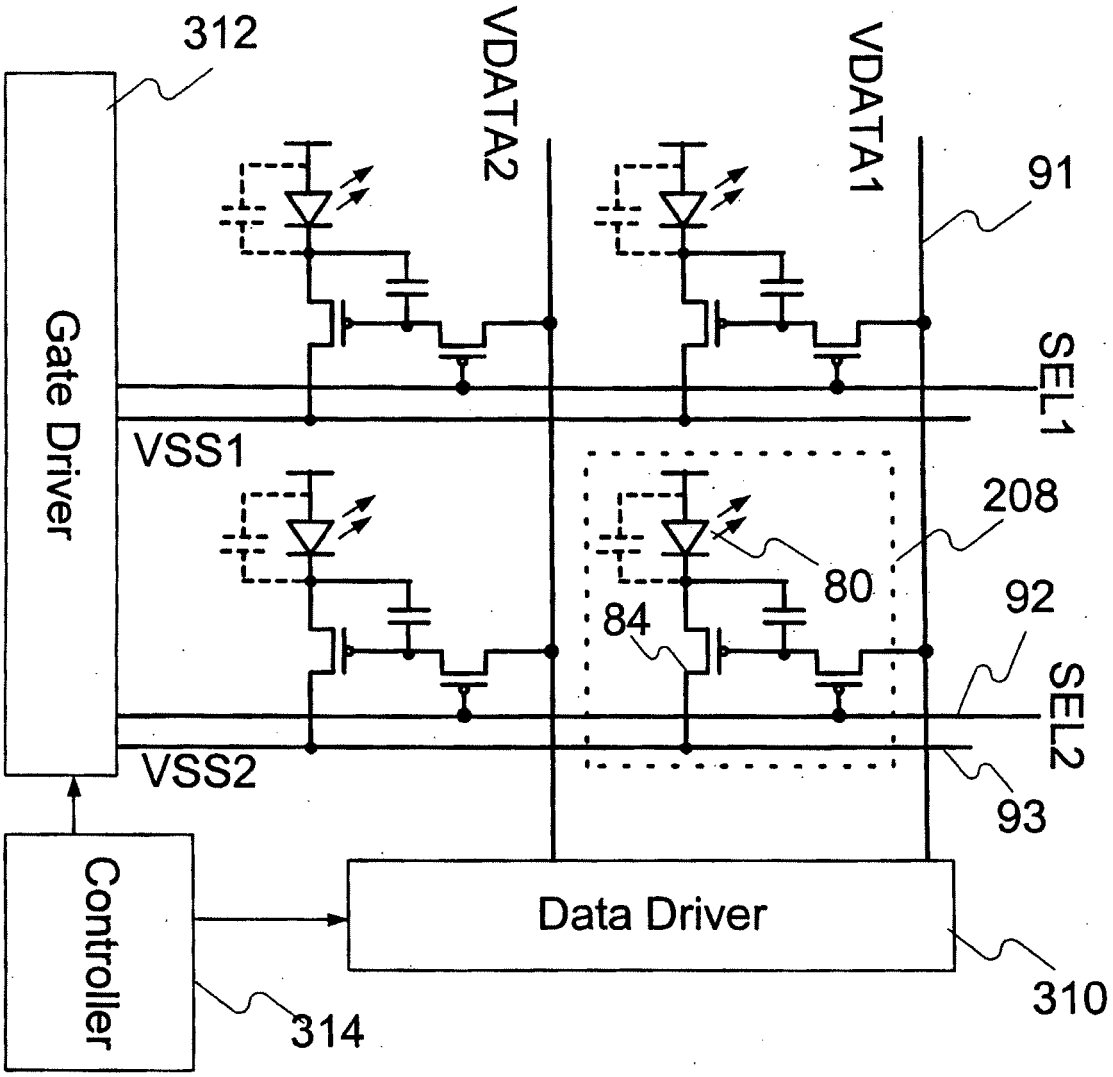

312
VDATA2
VDATA1
91
Gate Driver
SEL1
VSS1
208
80
92
84
SEL2
VSS2
93
Controller
Data Driver
310
314

Figure 16

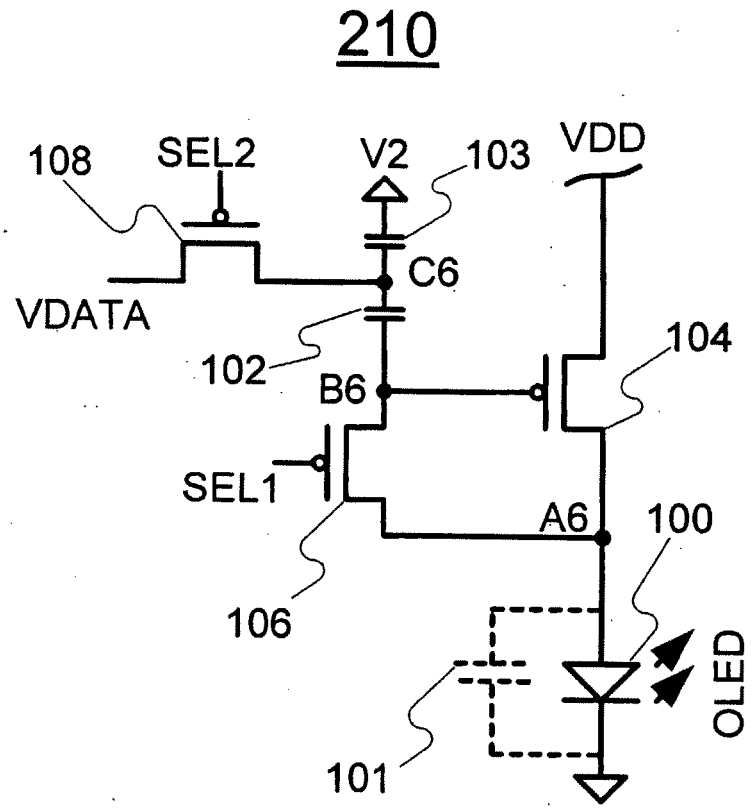

210
108
SEL2
V2
103
VDD
C6
VDATA
102
104
B6
SEL1
A6
100
106
OLED
101

Figure 17

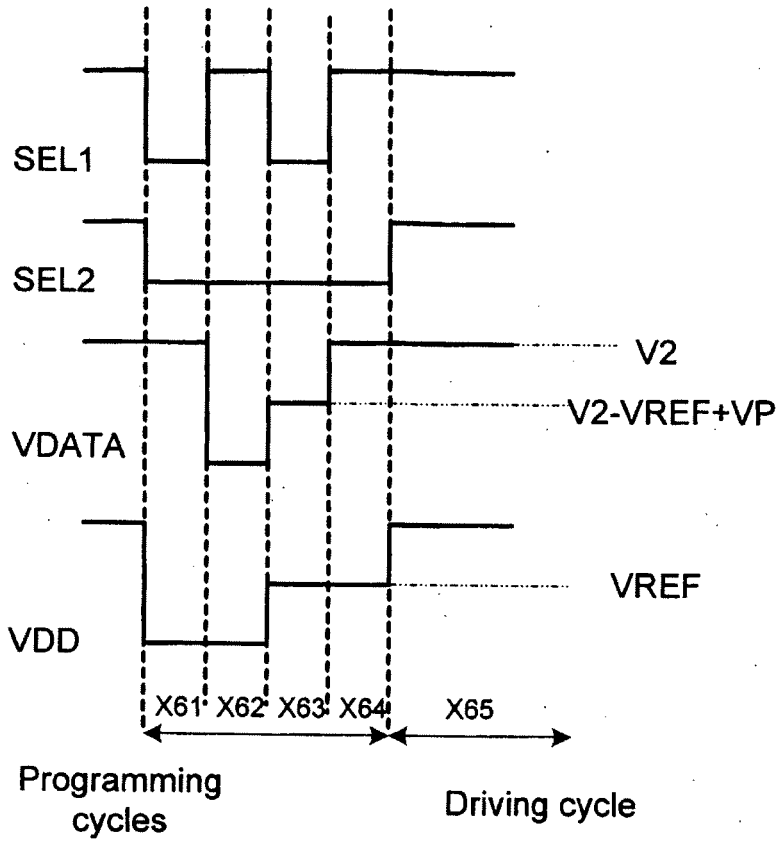

SEL1
SEL2
V2
V2-VREF+VP
VDATA
VREF
VDD
X61
X62
X63
X64
X65
Programming cycles
Driving cycle

Figure 18

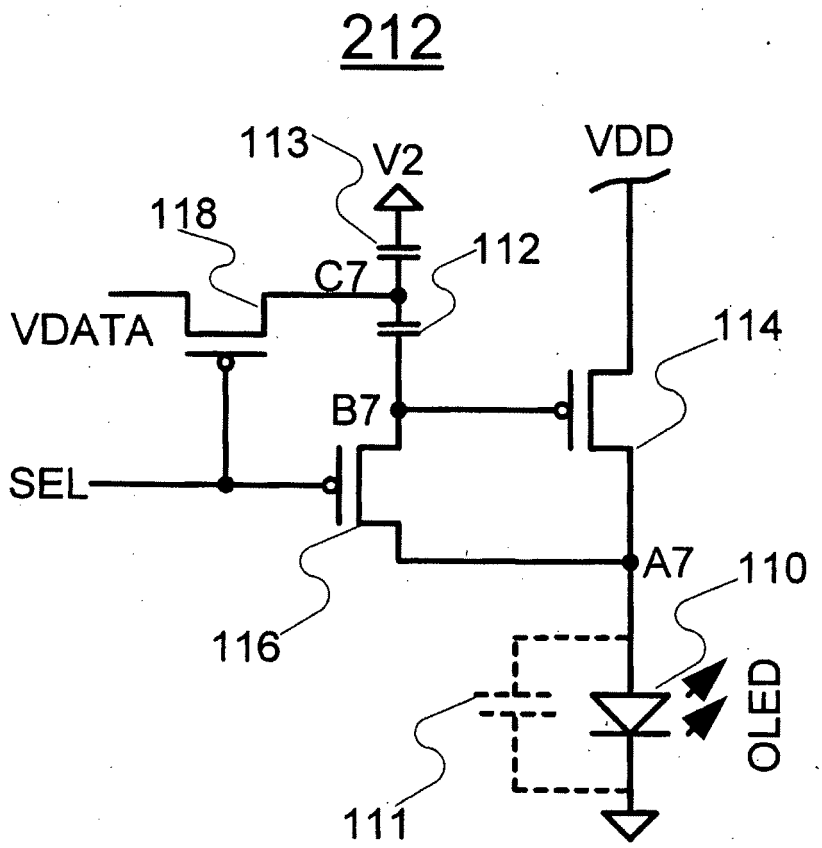


Figure 19

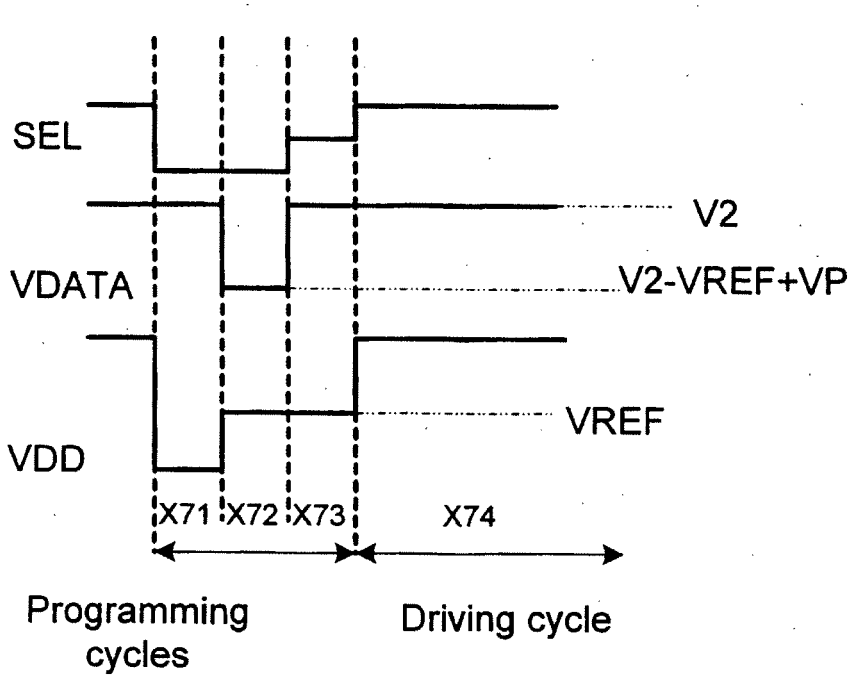

SEL
V2
VDATA
V2-VREF+VP
VREF
VDD
X71
X72
X73
X74
Programming cycles
Driving cycle

Figure 20

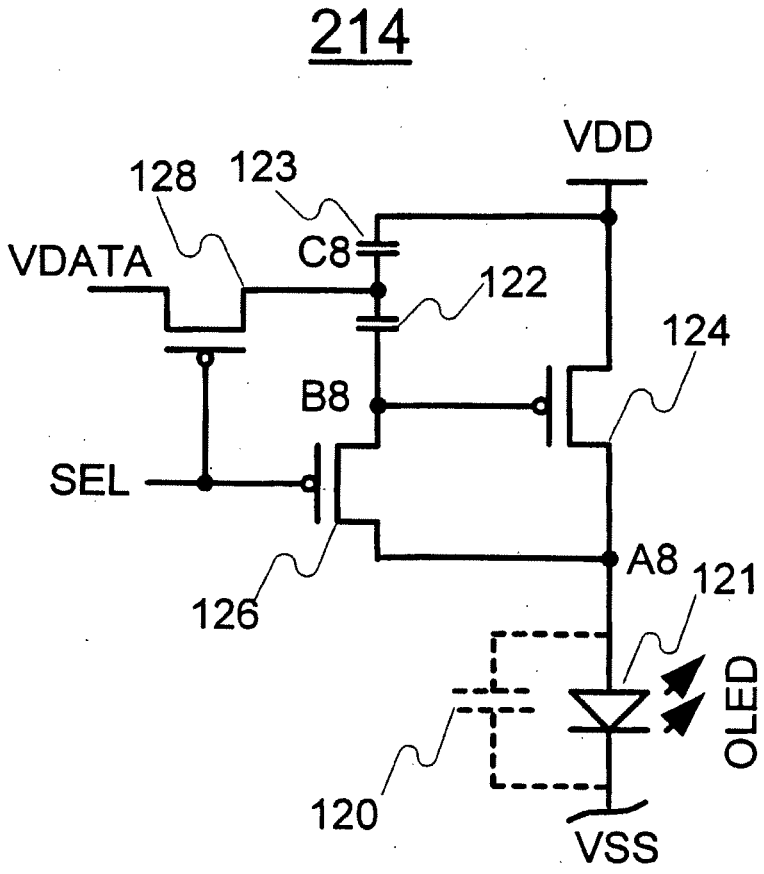


Figure 21

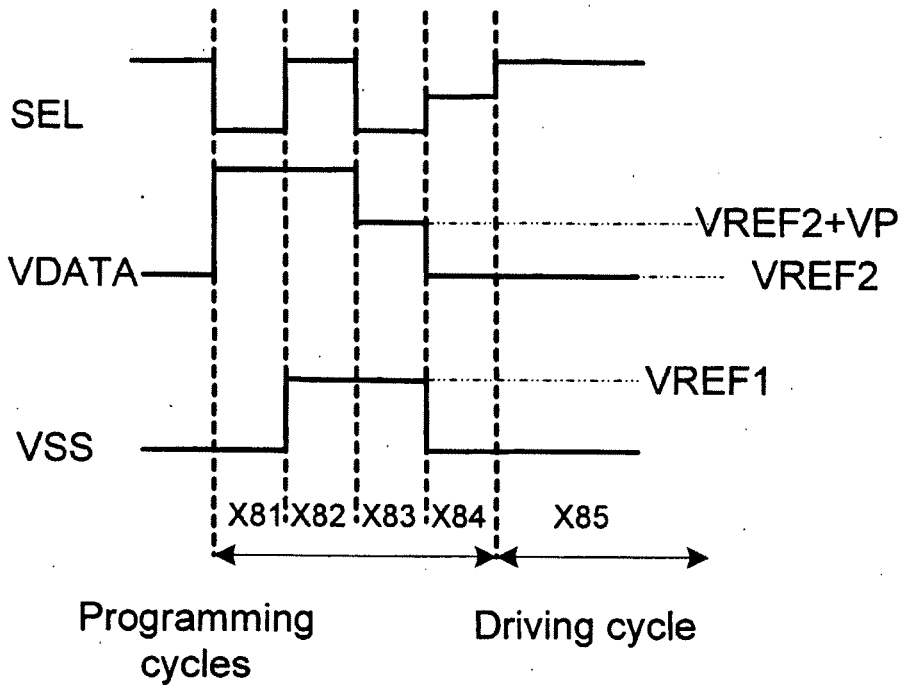

SEL
VDATA
VSS
VREF2+VP
VREF2
VREF1
X81
X82
X83
X84
X85
Programming cycles
Driving cycle

Figure 22

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- US 6229508 B **[0005]**
- US 6734636 B **[0006]**
- US 2003095087 A1 **[0007]**
- US 20040174349 A1 **[0008]**

专利名称(译)	用于编程和驱动有源矩阵发光器件像素的方法和系统		
公开(公告)号	EP2388764B1	公开(公告)日	2017-10-25
申请号	EP2011175223	申请日	2005-12-06
[标]申请(专利权)人(译)	伊格尼斯创新公司		
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IPC分类号	G09G3/32 G09G3/3225		
CPC分类号	G09G3/3258 G09G3/3233 G09G3/3696 G09G2300/0465 G09G2300/0842 G09G2300/0852 G09G2310/0262 G09G2310/06 G09G2310/061 G09G2320/043		
优先权	2490858 2004-12-07 CA		
其他公开文献	EP2388764A3 EP2388764A2		
外部链接	Espacenet		

摘要(译)

提供了用于编程和驱动有源矩阵发光器件像素的方法和系统。像素是电压编程像素电路，并且具有发光器件，驱动晶体管和存储电容器。像素具有编程周期，该编程周期具有多个操作周期和驱动周期。在编程周期期间，控制OLED和驱动晶体管之间的连接电压，使得驱动晶体管的期望栅极 - 源极电压存储在存储电容器中。