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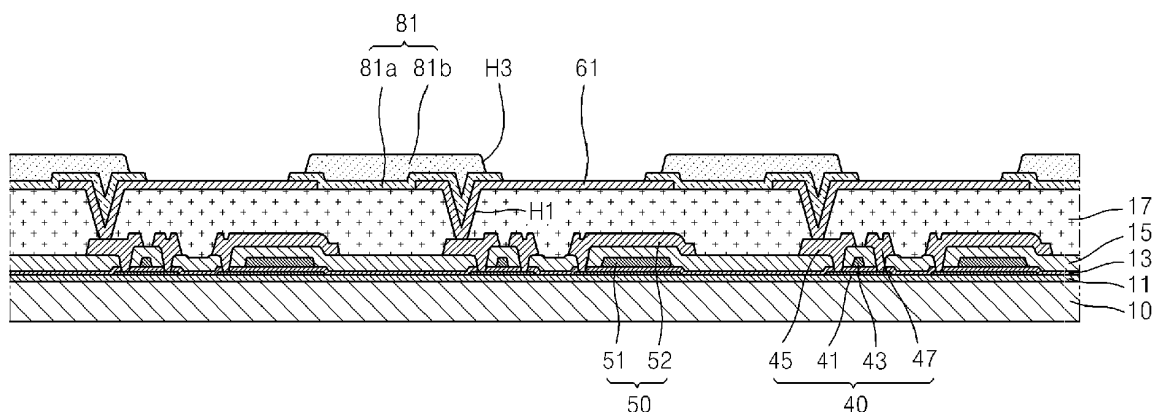
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(54) **Organic light-emitting diode display apparatus and method of manufacturing the same**

(57) Provided are an organic light-emitting diode (OLED) display apparatus and a method of manufacturing the OLED display apparatus. Pixel-defining layers (PDLs) are formed of inorganic and organic insulating

layers to minimize non-uniformities of the thicknesses of organic emission layers (OELs) and planarize lower thin film transistors (TFTs). Therefore, a lifespan of the OLED display apparatus is improved.

FIG. 6



Description

[0001] The invention relates to an organic light-emitting diode (OLED) display apparatus and a method of manufacturing the same, and more particularly, to an OLED display apparatus including pixels having uniform thicknesses and a method of manufacturing the same.

[0002] An organic light-emitting diode (OLED) display apparatus is classified as passive matrix (PM) and active matrix (AM) type OLED display apparatus according to its driving method. In the PM type OLED (PM-OLED) display apparatus, anodes and cathodes are arrayed in a plurality of columns and a plurality of rows. Thus, the cathodes are supplied with scanning signals from a row driving circuit. Here, only one of the plurality of rows is selected. Also, a data signal is input into each pixel from a column driving circuit. The AM type OLED (AM-OLED) display apparatus controls a signal input into each pixel using a thin film transistor (TFT) and is appropriate for processing a large number of signals. Thus, the AM-OLED display apparatus is mainly used as a display apparatus for realizing a moving picture.

[0003] A passivation layer is formed on the TFT of the AM-OLED display apparatus to passivate the TFT and as a planarizing layer for planarizing an upper surface of the TFT. Pixel-defining layers (PDLs) are formed on the passivation layer.

[0004] If the PDLs are formed to be thick to prevent colour mixtures among pixels, the thicknesses of emission parts formed among the PDLs vary. If thin PDLs are formed to solve these colour mixtures, an upper surface of the TFT area underneath the thin PDLs is not planarized. The present embodiments aim to overcome the above problems as well as providing additional advantages.

[0005] The present embodiments provide an organic light-emitting diode (OLED) display apparatus in which a thickness of an emission area is uniform and an upper surface of thin film transistor (TFT) area is planarized and a method of manufacturing the OLED display apparatus.

[0006] According to an aspect of the present embodiments, there is provided an organic light-emitting diode (OLED) display apparatus including: thin film transistor (TFT) which is formed on a substrate; first electrode which is formed on a planarizing layer in each pixel, wherein the planarizing layer covers the TFT; pixel-defining layers (PDLs) which includes first PDL covering an end of the first electrode and second PDL exposing an end of the first PDL and covering the first PDL; intermediate layer which is formed on the first electrode and includes an emission layer (EML); and second electrode which is positioned opposite to the first electrode.

[0007] According to another aspect of the present embodiments, there is provided a method of manufacturing an organic light-emitting diode (OLED) display apparatus, including: forming over a substrate first electrodes in each pixel; forming first PDLs covering ends of the first electrodes; forming second PDLs exposing ends of the

first PDLs and covering the first PDLs; and forming intermediate layers including EMLs on the first electrodes; and forming second electrodes opposite to the first electrodes.

[0008] The second PDL may be formed on the first PDL to bury uneven parts formed on a planarizing layer.

[0009] The first PDLs may be formed of inorganic layers. The first PDLs may be formed of at least one of SiO_2 , SiN_x , Al_2O_3 , CuO_x , Tb_4O_7 , Y_2O_3 , Nb_2O_5 , and Pr_2O_3 , for example.

[0010] Each of the first PDLs may be formed to a thickness of from about $0.1\mu\text{m}$ to about $1\mu\text{m}$.

[0011] The second PDLs may include organic layers. The second PDLs may be formed of one selected from the group consisting of polyacryl, polyimide, polyamide (PA), benzocyclobutene (BCB), and phenolic resin.

[0012] Each of the second PDLs may have a thickness from about $0.1\mu\text{m}$ to about $2\mu\text{m}$ in a direction in which different colour pixels are arrayed, and a thickness between $0.1\mu\text{m}$ and $1\mu\text{m}$ in a direction in which equal colour pixels are arrayed.

[0013] The above and other features and advantages of the present embodiments will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a schematic plan view of a pixel electrode part of an organic light-emitting diode (OLED) display apparatus according to an embodiment;

FIG. 2 is an enlarged plan view of a pixel of OLED display apparatus of FIG. 1;

FIG. 3 is a schematic cross-sectional view of an OLED display apparatus according to another embodiment; and

FIGS. 4 through 6 are schematic cross-sectional views illustrating a method of manufacturing an OLED display apparatus, according to an embodiment.

[0014] Exemplary embodiments will now be described with reference to the accompanying drawings. In the drawings, like reference numerals denote like elements. These embodiments may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the embodiments to those skilled in the art.

[0015] In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. It will be understood that, unless otherwise specified, when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0016] FIG. 1 is a schematic plan view of a pixel electrode part of an organic light-emitting diode (OLED) display apparatus according to an embodiment. FIG. 2 is

an enlarged plan view of a pixel of the OLED display apparatus of FIG. 1.

[0017] Referring to FIGS. 1 and 2, the OLED display apparatus includes a display area in which red (R), green (G), and blue (B) pixels are repeatedly arrayed. In the present embodiment, the R, G, and B pixels are repeatedly arrayed in stripe patterns in columns and rows but the present embodiments are not limited thereto. For example, the R, G, and B pixels may be arrayed in zigzag patterns in which pixels in each row are misaligned, matrix patterns, or the like. In the present embodiment, a part of the display area is illustrated for convenience, the R, G, and B pixels are repeatedly arrayed in direction A-A', and the same colour pixels are repeatedly arrayed in direction B-B'.

[0018] Each of the R, G, and B pixels includes a selective driving circuit, which has thin film transistors (TFTs) 30 and 40, a capacitor 50, and the like, and an OLED 60. Each of the R, G, and B pixels includes a data line 72, a gate line 71, and a power source line 73 that is a driving power source of the OLED 60.

[0019] The TFTs 30 and 40 respectively are a switching TFT and a driving TFT (hereinafter the TFTs 30 and 40 will be respectively referred to as the switching TFT 30 and the driving TFT 40). The switching TFT 30 is driven by a scan signal applied to the gate line 71 to transmit a data signal applied to the data line 72. The driving TFT 40 determines an amount of current flowing into the OLED 60 according to the data signal transmitted through the switching TFT 30 e.g., a voltage difference between a gate and a source. The capacitor 50 stores the data signal transmitted through the switching TFT 30 for a frame.

[0020] A source electrode 31 of the switching TFT 30 is connected to the selective driving circuit through the data line 72, and a gate electrode 32 of the switching TFT 30 is connected to another driving circuit (not shown) through the gate line 71. A drain electrode 33 of the switching TFT 30 is connected to a first capacitor electrode 51 of the capacitor 50 and a gate electrode 43 of the driving TFT 40.

[0021] A second capacitor electrode 52 of the capacitor 50 and a source electrode 47 of the driving TFT 40 are connected to the power source line 73, and a drain electrode 45 of the driving TFT 40 is connected to a first electrode 61 of the OLED 60.

[0022] The number of TFTs and capacitors of the selective driving circuit is not limited thereto, and the selective driving circuit may include a larger number of TFTs and a larger number of capacitors.

[0023] The OLED 60 includes the first electrode 61, which is a pixel electrode, and a second electrode (not shown) which is a common electrode and opposite the first electrode at a predetermined gap from the first electrode 61. An intermediate layer (not shown) including an organic emission layer (OEML) intervenes between the first electrode 61 and the second electrode to emit light by the first electrode 61 and the second electrode.

[0024] A pixel-defining layer (PDL) 81 is formed around an end of the first electrode 61 of the OLED 60. The PDL 81 includes a first PDL 81a, which is an inorganic layer, and a second PDL 81b, which is an organic layer. The first PDL 81a is formed to cover the end of the first electrode 61, and the second PDL 81b is formed on the first PDL 81a to expose an end of the first PDL 81a.

[0025] FIG. 3 is a schematic cross-sectional view of an OLED display apparatus according to another embodiment.

[0026] Referring to FIG. 3, the OLED display apparatus includes a plurality of TFTs 40 and a plurality of OLEDs 60 which are formed on a substrate 10.

[0027] Each TFT 40 includes active layer 41, gate electrode 43, and source and drain electrodes 45 and 47. A gate insulating layer 13 intervenes between the gate electrode 43 and the active layer 41 to insulate the gate electrode 43 from the active layer 41. The active layer 41 includes source and drain regions and a channel region. Here, a high-density dopant has been injected into both ends of each of the source and drain regions, and the channel region is formed between the source and drain regions. The source and drain regions are respectively connected to the source/drain electrodes 45 and 47.

[0028] Each OLED 60 includes a first electrode 61, a second electrode 65, and an intermediate layer 63 intervening between the first and second electrodes 61 and 65. The first electrode 61 is formed on a passivation layer 17 in each pixel and connected to one of the source/drain electrodes 45 and 47 of the TFTs 40 through via holes H1.

[0029] PDLs 81 are formed around ends of the first electrodes 61 to define the pixels. The PDLs 81 include first PDLs 81a and second PDLs 81b. Each of the first PDLs 81a is formed of an inorganic layer. The first PDLs 81a are formed between adjacent two first electrodes 61 and cover the ends of the first electrodes 61. Each of the second PDLs 81b is formed of organic layer on the first PDL 81a to cover steep slope region P in which the end of the first electrode 61 and the via hole H1 is formed. The edge of second PDL 81b is positioned at predetermined distance from edge of the first PDL 81a. Distances between edges of the first and second PDLs 81a and 81b may be about 1 μm or less and may be determined in consideration of aperture ratio and emission effective region of the first electrode 61.

[0030] Thicknesses of the first PDLs 81a may be each set to from about 0.1 μm to about 1 μm .

[0031] Thicknesses of the second PDL 81b may be each set to from about 0.1 μm to about 2 μm in the direction A-A' of FIG. 1 to prevent colour mixtures among adjacent R, G, and B pixels. And thickness of the second PDL 81b may be set to from about 0.1 μm to about 1 μm in the direction B-B' of FIG. 1 to minimize step differences of the OEMLs.

[0032] The first PDLs 81a are formed of an inorganic material having similar surface energy to that of the intermediate layers 63 stacked on the first electrodes 61.

The second PDLs 81b are formed of an organic material having different surface energy from that of the intermediate layers 63.

[0033] The PDL is formed, and a surface of the PDL is processed using a liquid repellent to prevent colour mixtures among pixels in order to form OEML using an ink jet or nozzle printing method. Here, if the PDLs are formed thick, thicknesses of the centre of a pixel and the end of the pixel meeting the PDL are different from each other. If the PDL is formed thin, surface curves of lower TFT area formed by uneven parts such as steep slope regions P or cracks A are not sufficiently planarized, wherein a via hole is formed in the steep slope region P, and the cracks A are formed in an etching process. Thus, moisture, oxygen, or the like penetrates into the PDL, and shorts may occur between the first and second electrodes 61 and 65.

[0034] Accordingly, in the present embodiment, the first PDLs 81a having thin thicknesses are formed around the end of the first electrode 61, and the second PDL 81b is formed at predetermined distance from the edge of the first PDL 81. Thus, non-uniformities of the thicknesses of the OEMLs are minimized. Also, the second PDLs 81b are formed on the first PDLs 81a in which uneven parts such as cracks or the like are formed, to improve step coverage in order to planarize lower TFT area and minimize short between the first and second electrodes 61 and 65.

[0035] In the present embodiment, the second PDLs 81b are formed on the first PDLs 81a, except on the ends of the first PDLs 81a. According to another embodiment, the second PDLs 81b may be additionally formed in the uneven parts such as the steep slope regions P or the cracks A.

[0036] Three TFTs and three capacitors are shown in FIG. 3 but the present embodiment is not limited thereto. Thus, at least one TFT and at least one capacitor may be formed.

[0037] FIGS. 4 through 6 are schematic cross-sectional views illustrating a method of manufacturing an OLED display apparatus, according to an embodiment. The present embodiment exemplifies an OLED display apparatus having a stripe structure in which the same colour pixels are arrayed in column directions, and R, G, and B pixels are repeatedly arrayed in row directions from left to right.

[0038] Referring to FIG. 4, TFTs 40 and first electrodes 61 are formed above a substrate 10.

[0039] The substrate 10 may be formed of a transparent glass material including SiO₂ as a main component but is not limited thereto. That is, the substrate 10 may be formed of a transparent plastic material, a metallic material, or the like.

[0040] If the OLED display apparatus is a bottom-emission type display apparatus which realizes an image toward the substrate 10, the substrate 10 is formed of a transparent material. If the OLED display apparatus is a top-emission type display apparatus which realizes an

image in an opposite direction to the substrate 10, the substrate 10 does not need to be formed of a transparent material. In this case, the substrate 10 may be formed of metal. If the substrate 10 is formed of the metal, the substrate 10 may include at least one or more selected from the group consisting of carbon (C), iron (Fe), chromium (Cr), manganese (Mn), nickel (Ni), titanium (Ti), molybdenum (Mo), stainless steel (SUS), an Invar alloy, an Inconel alloy, and a Kovar alloy. However, the substrate 10 is not limited thereto and may be formed of a metal foil.

[0041] An insulating layer 11 is formed on an upper surface of the substrate 10 to prevent diffusion of dopant ions and penetration of moisture or air and function and for planarizing the upper surface of the substrate 10 as a barrier layer and/or a buffer layer. The insulating layer 11 may be formed of SiO₂ and/or silicon nitride (SiN_x) using a plasma enhanced chemical vapor deposition (PECVD) method, an atmospheric pressure CVD (APCVD) method, a low pressure CVD (LPCVD) method, or the like.

[0042] Active layers 41 of the TFTs 40 are formed on the insulating layer 11. In order to form the active layers 41 of the TFTs 40, amorphous silicon may be deposited and crystallized on the insulating layer 11 to form a polycrystalline silicon layer (not shown), and the polycrystalline silicon layer may be patterned.

[0043] Each active layer 41 of the TFTs 40 includes source and/or drain regions and channel region. Each active layer 41 has the source and drain regions at ends of the active layer 41 corresponding to sides of gate electrode 43 by doped with N-type or p-type dopants. The channel region is formed between the source and drain regions.

[0044] A gate insulating layer 13 is formed on the active layers 41 of the TFTs 40. The gate insulating layer 13 may be formed of an inorganic material such as SiN_x or silicon oxide (SiO_x) using a PECVD method, an APCVD method, an LPCVD method, or the like.

[0045] The gate electrodes 43 are formed partially on the gate insulating layer 13, and an interlayer insulating layer 15 is formed to cover the gate electrodes 43.

[0046] The gate electrodes 43 may be formed of various types of conductive materials such as Al, Mo, tungsten (W), Cr, Ni, or a compound of Al, Mo, W, Cr, and Ni. If light is to pass through the active layers 41 of the TFTs 40 and other elements, the gate electrodes 43 may be formed of various types of transparent conductive materials such as ITO, IZO, or the like.

[0047] Source/drain electrodes 45 and 47 are formed on the interlayer insulating layer 15 and connected to the active layers 41 through contact holes formed in the interlayer insulating layer 15. A planarizing layer 17 is formed on the source/drain electrodes 45 and 47.

[0048] The planarizing layer 17 may be an inorganic insulating layer and/or an organic insulating layer. The inorganic insulating layer may include SiO₂, SiN_x, SiON, Al₂O₃, TiO₂, Ta₂O₅, HfO₂, ZrO₂, BST, PZT, or the like. The organic insulating layer may include commercial pol-

polymer such as polymethyl methacrylate (PMMA), polystyrene (PS), or the like, polymeric derivative having a phenol group, acryl-based polymer, imide-based polymer, allylether-based polymer, amide-based polymer, fluorine-based polymer, p-xylene-based polymer, vinyl alcohol-based polymer, or a blend of commercial polymer, polymeric derivative, acryl-based polymer, imide-based polymer, allylether-based polymer, amide-based polymer, fluorine-based polymer, p-xylene-based polymer, and vinyl alcohol-based polymer. The planarizing layer 17 may have a complex stack structure of an inorganic insulating layer and an organic insulating layer.

[0049] Stack structures of TFTs as described above are not limited thereto, and TFTs having various types of structures may be used. The present embodiment exemplifies top gate type TFTs, but different types of TFTs may be formed.

[0050] The first electrodes 61 are formed on the planarizing layer 17 as pixel electrodes of an OLED and are electrically connected to one of the source/drain electrodes 45 and 47 through via holes H1. The via holes H1 are formed by etching the planarizing layer 17 and exposing the source/drain electrodes 45 and 47.

[0051] The first electrodes 61 may be formed of various types of conductive materials in each pixel. If the OLED display apparatus is a bottom-emission type display apparatus which realizes an image toward the substrate 10, the first electrodes 61 may be transparent electrodes and may be formed of ITO, IZO, ZnO, or In_2O_3 for example, having a high work function. If the OLED display apparatus is a top-emission type display apparatus which realizes an image in an opposite direction to the substrate 10, the first electrodes 61 may be reflective electrodes. A reflective layer may be formed of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, or a compound of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, and Ca, and ITO, IZO, ZnO, or In_2O_3 , for example, having a high work function may be formed on the reflective layer in order to form the first electrodes 61.

[0052] Referring to FIG. 5, first PDLs 81a are formed to cover ends of the first electrodes 61.

[0053] In order to form the first PDLs 81a, an inorganic insulating layer is deposited on a whole surface of the substrate 10 above which the first electrodes 61 have been formed, and patterned using a photolithographic process, to form openings H2 which expose central parts of the first electrodes 61.

[0054] The inorganic insulating layer may be formed of one or more inorganic insulating materials selected from SiO_2 , SiN_x , Al_2O_3 , CuO_x , Tb_4O_7 , Y_2O_3 , Nb_2O_5 , Pr_2O_3 , and the like using a sputtering method, a CVD method, a deposition method, or the like.

[0055] The first PDLs 81a may be each formed to a thickness between about $0.1\mu\text{m}$ and $1\mu\text{m}$ to minimize differences in thicknesses of OEMLs between ends and central parts of the first electrodes 61.

[0056] Referring to FIG. 6, second PDLs 81b are formed on the first PDLs 81a.

[0057] An organic insulating layer is deposited on the whole surface of the substrate 10 above which the first PDLs 81a have been formed, and then patterned using a photolithographic process, to form openings H3 so as to expose central parts of the first electrode 61 and ends of the first PDLs 81a.

[0058] The organic insulating layer may be formed of one or more organic insulating materials selected from the group consisting of polyimide, polyamide, acrylic resin, benzocyclobutene (BCB), and phenolic resin using spin coating, slot coating, or the like.

[0059] Thicknesses of the second PDLs 81b may be each set to a range between about $0.1\mu\text{m}$ and $2\mu\text{m}$ in row directions to prevent colour mixtures among adjacent R, G, and B pixels and a range between about $0.1\mu\text{m}$ and $1\mu\text{m}$ in column directions to minimize step differences in the thicknesses of the OEMLs.

[0060] A gap between edges of the first and second PDLs 81a and 81b around the end of the first electrode 61 may be about $1\mu\text{m}$.

[0061] Cracks may be formed in the first electrodes 61 and the first PDLs 81a due to low step coverage between the ends of the first electrodes 61 and peripheral parts of via holes H. Therefore, the second PDLs 81b are formed on the first PDLs 81a to bury the cracks in order to improve step coverage and prevent penetration of air and shorts between electrodes.

[0062] As shown in FIG. 3, the intermediate layers 63 including the OEMLs and the second electrodes 65 are formed in openings through which first electrodes 61 are exposed.

[0063] The intermediate layers 63 may be formed in a single or complex stack structure of one or more of functional layers including an emissive layer (EML), a hole transport layer (HTL), a hole injection layer (HIL), an electron transport layer (ETL), and an electron injection layer (EIL).

[0064] The intermediate layers 63 may be formed of a low or high molecular weight organic material.

[0065] If the intermediate layers 63 are formed of the low molecular weight organic material, the HTL and the HIL are stacked toward the first electrodes 61 based on the OEMLs, and the ETL and the EIL are stacked toward the second electrodes 65 in order to form the intermediate layers 63. Other types of layers may be stacked in order to form the intermediate layers 63. The low molecular weight organic material may be CuPC, NPB, Alq_3 , or the like.

[0066] If the intermediate layers 63 are formed of the high molecular weight organic material, the intermediate layers 63 may include only the HTL toward the first electrodes 61 with respect to the OEMLs. The HTL may be formed of poly-(2,4)-ethylene-dihydroxy thiophene (PEDOT), polyaniline (PANI), or the like on the first electrodes 61 using ink jet printing, spin coating, or the like. Here, the high molecular weight organic material may be a PPV-based or polyfluorene-based high molecular weight organic material. Colour patterns may be formed

using a normal method such as ink jet printing, spin coating, thermal transfer printing using a laser, or the like, in order to form the intermediate layers 63.

[0067] The second electrodes 65 may be deposited above the whole surface of the substrate 10 and may be formed as common electrodes. In the OLED display apparatus according to the present embodiment, the first electrodes 61 are used as anode electrodes, and the second electrodes 65 are used as cathode electrodes. However, the present embodiments are not limited thereto and the polarities of the first electrodes 61 and the second electrodes 65 may be the opposite.

[0068] If the OLED display apparatus is a bottom-emission type display apparatus which realizes an image toward the substrate 10, the first electrodes 61 are transparent electrodes, and the second electrodes 65 are reflective electrodes. Here, a metal having a low work function, for example, Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, LiF/Ca, LiF/Al, or a compound of Ag, Mg, Al, Pt, Pd, Au, Ni, Nd, Ir, Cr, Li, Ca, LiF/Ca, and LiF/Al, for example, may be thinly deposited to form the reflective electrodes.

[0069] Although not shown in the drawings, a sealing member (not shown) and a moisture absorbent may be further formed on the second electrodes 65 to protect the OEMLs from external moisture or oxygen.

[0070] As described above, an OLED display apparatus according to the present embodiments includes PDLs formed of inorganic and organic insulating layers. Thus, non-uniformities of the thicknesses of OEMLs are minimized, and lower TFTs are planarized, thereby improving a lifespan of the OLED display apparatus.

[0071] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the scope of the invention as defined by the following claims.

Claims

1. An organic light-emitting diode OLED display apparatus comprising:

a plurality of thin film transistors TFT (40) formed on a substrate (10);
 a plurality of pixels including a planarizing layer (17);
 a first electrode (61) formed on the planarizing layer in each pixel, wherein the planarizing layer (17) covers the TFT (40);
 a plurality of pixel-defining layers PDLs (81) which comprise a first PDL (81a) covering an end of the first electrode and a second PDL (81b) exposing an end of the first PDL and covering the first PDL (81a);
 an intermediate layer (63) formed on the first

electrode and comprising an emission layer EML; and
 a second electrode (65) positioned opposite the first electrode (61).

2. The OLED display apparatus of claim 1, wherein the second PDL is formed on the first PDL to bury uneven parts formed on the planarizing layer.
3. The OLED display apparatus of claim 1 or 2, wherein the first PDL comprises inorganic layers.
4. The OLED display apparatus of any one of the preceding claims, wherein the first PDL comprises at least one selected from the group consisting of SiO_2 , SiN_x , Al_2O_3 , CuO_x , Tb_4O_7 , Y_2O_3 , Nb_2O_5 , and Pr_2O_3 .
5. The OLED display apparatus of any one of the preceding claims, wherein the first PDL is formed to a thickness of from about $0.1\text{ }\mu\text{m}$ to about $1\text{ }\mu\text{m}$.
6. The OLED display apparatus of any one of the preceding claims, wherein the second PDL comprises organic layers.
7. The OLED display apparatus of any one of the preceding claims, wherein the second PDL comprises at least one selected from the group consisting of polyacryl, polyimide, polyamide (PA), benzocyclobutene (BCB), and phenolic resin.
8. The OLED display apparatus of any one of the preceding claims, wherein the second PDL has a thickness of about $0.1\text{ }\mu\text{m}$ to about $2\text{ }\mu\text{m}$ in a direction in which different colour pixels are arrayed, and a thickness of about $0.1\text{ }\mu\text{m}$ to about $1\text{ }\mu\text{m}$ in a direction in which equal colour pixels are arrayed.
9. The OLED display apparatus of any one of the preceding claims wherein the planarizing layer comprises at least one of an inorganic insulating layer and an organic insulating layer.
10. The OLED display apparatus of claim 9, wherein the planarizing layer comprises an inorganic layer comprising at least one selected from the group consisting of SiO_2 , SiN_x , SiON , Al_2O_3 , TiO_2 , Ta_2O_5 , HfO_2 , ZrO_2 , BST, and PZT.
11. The OLED display apparatus of claim 9 or 10, wherein the planarizing layer comprises an organic layer comprising at least one of polymethyl methacrylate (PMMA), polystyrene (PS), polymeric derivative having a phenol group, acryl-based polymer, imide-based polymer, allylether-based polymer, amide-based polymer, fluorine-based polymer, p-xylene-based polymer, vinyl alcohol-based polymer.

12. The OLED display apparatus of any one of the preceding claims, wherein the planarizing layer has a complex stack structure of an inorganic insulating layer and an organic insulating layer.

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13. A method of manufacturing an organic light-emitting diode OLED display apparatus, comprising:

forming first electrodes on a planarizing layer in each pixel;

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forming first pixel-defining layers PDLs covering ends of the first electrodes;

forming second PDLs exposing ends of the first PDLs and covering the first PDLs; and

forming intermediate layers comprising emission layers EMLs on the first electrodes; and forming second electrodes opposite the first electrodes.

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14. The method of claim 13, wherein the second PDL is formed on the first PDL to bury uneven parts formed on the planarizing layer.

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FIG. 1

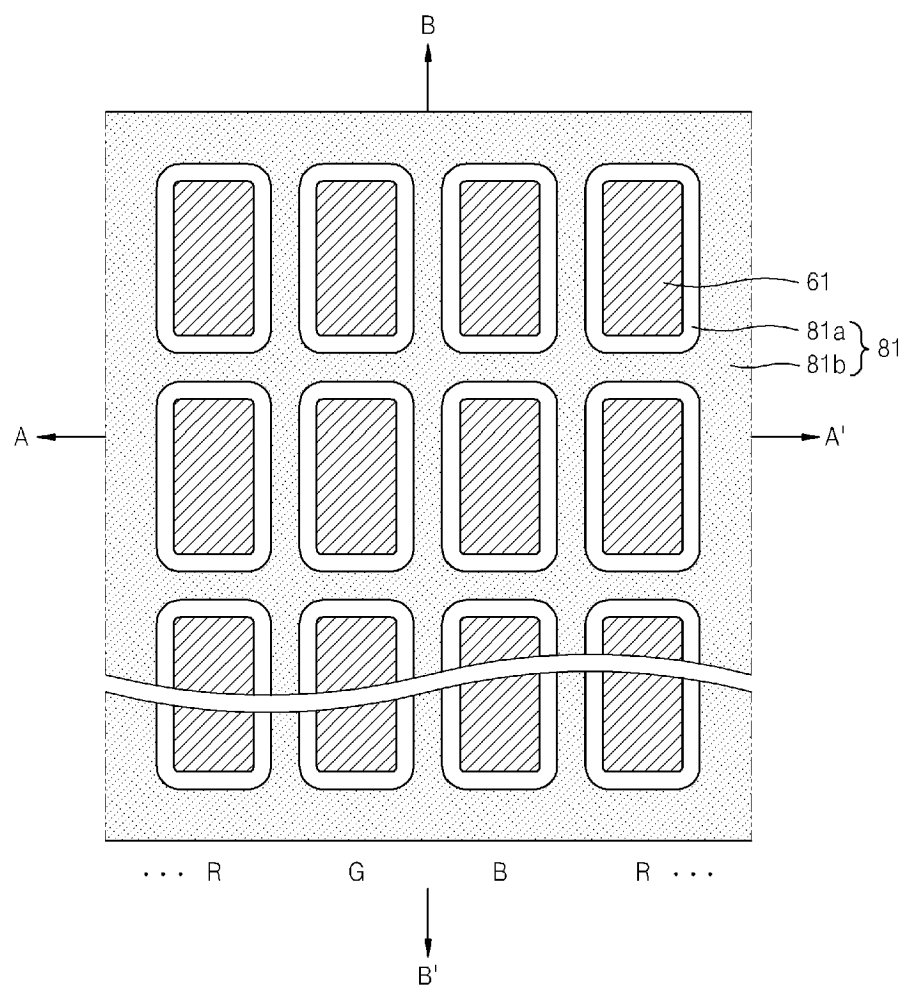


FIG. 2

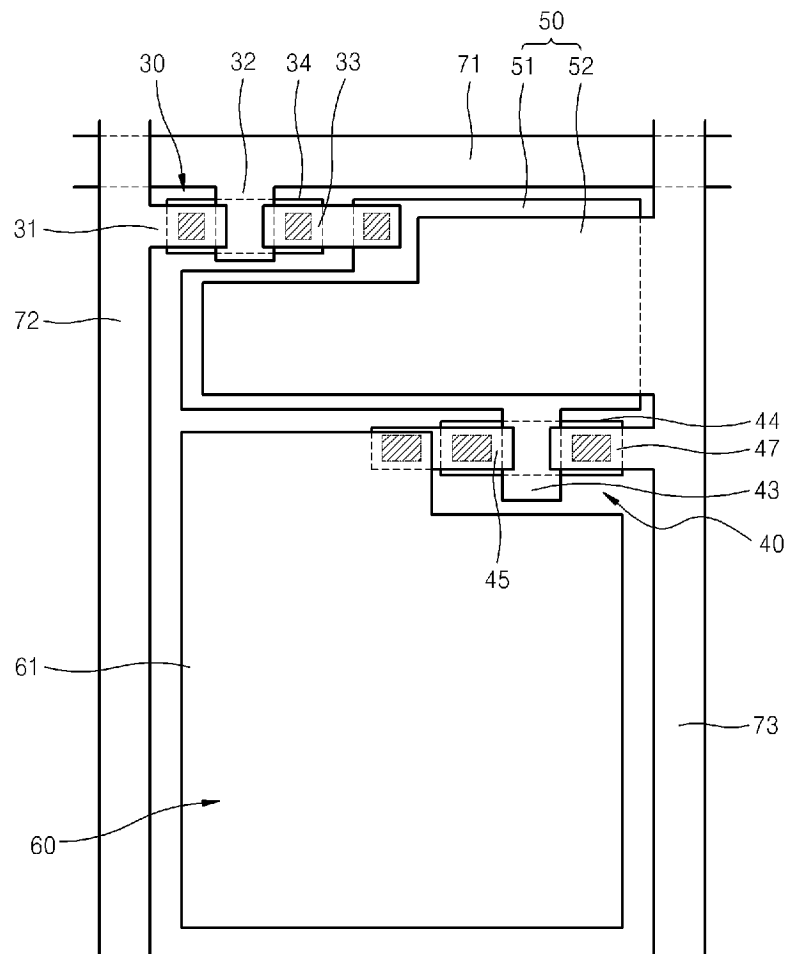


FIG. 3

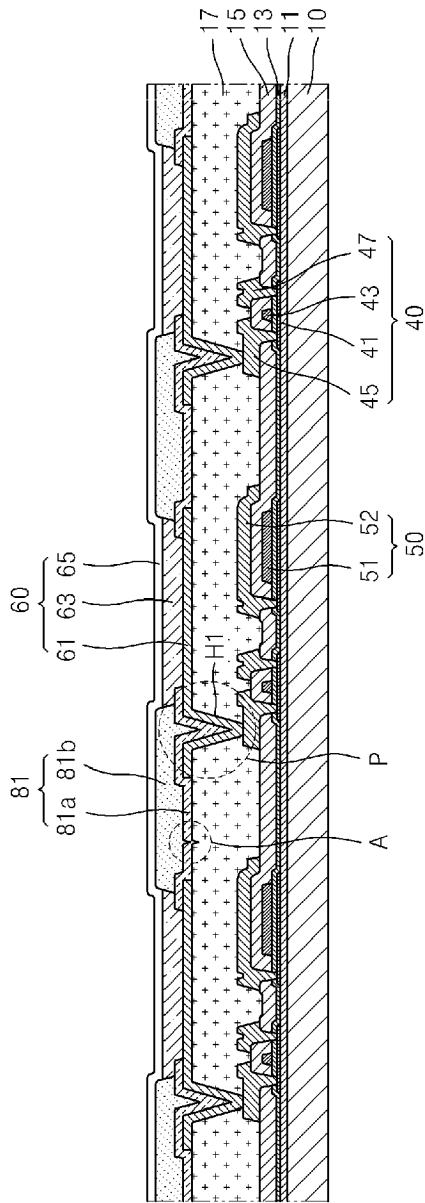


FIG. 4

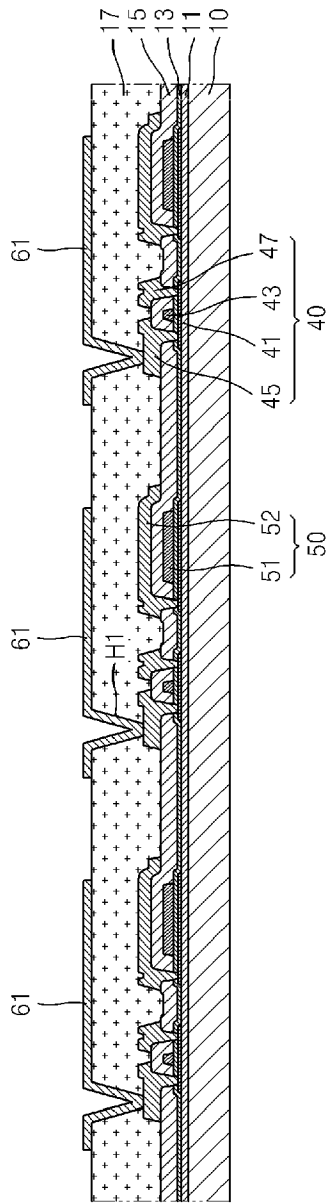


FIG. 5

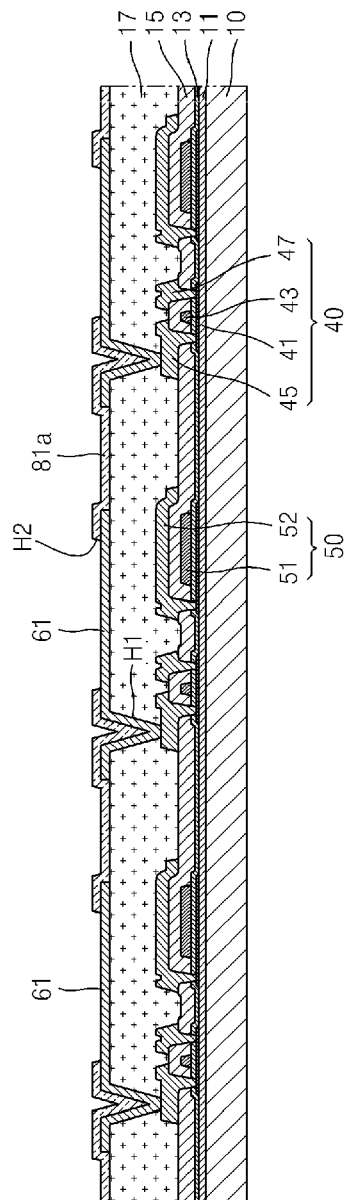
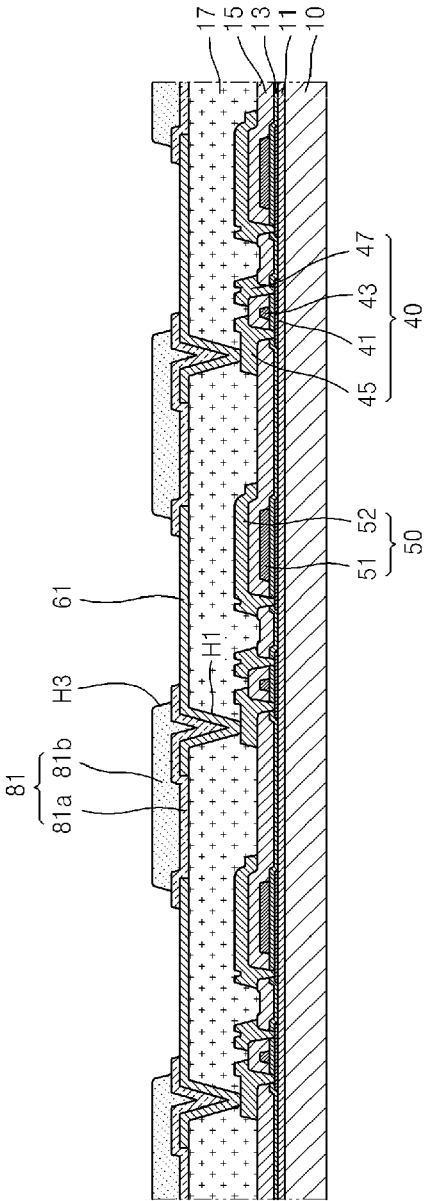


FIG. 6



专利名称(译)	有机发光二极管显示装置及其制造方法		
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摘要(译)

提供了一种有机发光二极管 (OLED) 显示装置和制造该OLED显示装置的方法。像素限定层 (PDL) 由无机和有机绝缘层形成，以最小化有机发光层 (OEML) 的厚度的不均匀性并平坦化下部薄膜晶体管 (TFT) 。因此，改善了OLED显示装置的使用寿命。

FIG. 6

